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A low power Analog Front-end for Bio-signal Monitoring System Application

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A low power Analog Front-end for Bio-signal Monitoring System Application

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THESIS

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應用於生醫訊號偵測系統之低功耗前端電路

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摘要

由於患有慢性疾病的患者越來越多以及老年化社會的來臨，現代社會對於個人化遠距醫療照護的需求也越來越高。幸運的是，隨著半導體產業的快速發展以及積體電路設計產業逐漸的成熟，用來感測及監測生理訊號的生物醫學晶片得以被實現。開發一個無線生醫訊號偵測系統晶片來實現遠距醫療照護的服務是可行的。這不僅能幫助人們預防得到疾病還能促進人們的健康，進而增進生活的品質。根據衛生署所頒佈的資料，心血管疾病是國人的十大死因之一。因此，一個可以應用在遠距醫療照護服務的心電訊號監測系統對於現今社會是有其需要的。為了要實現一個心電訊號監測系統，處理類比生理訊號的類比前端電路在系統裡是扮演關鍵性的電路區塊。本論文提出了兩種低功耗低雜訊的類比前端電路用來降低雜訊的干擾以及提供多種放大倍率的選擇。兩個類比前端電路皆使用 TSMC 0.18μm 的製程技術來完成高性能的生物醫學晶片。

本論文所提出的第一種前端電路是電流回授式儀表放大器以及可程式增益放大器。藉由斬斷技術，電流回授式儀表放大器的輸入相關雜訊為 90nV/$\sqrt{Hz}$，而整個類比前端電路的輸入相關雜訊則是 1uV/$\sqrt{Hz}$ 。為了要符合各種心電訊號大小的偵測，此電路提供了從 36dB 到 54dB 各種不同的增益選擇。此類比前端電路在 1V 的供應電壓下只消耗了 6uW。

第二，本論文提出了一個類比前端電路以及脈衝寬度調變電路。脈衝寬度調變電路是做為類比前端電路及數位訊號處理電路之間的介面電路。此類比前端電路的輸入相關雜訊為 80nV/$\sqrt{Hz}$。此外，本電路不僅提供四種從 30dB 到 50dB 不同的增益選擇，並且具有很高的輸出訊號擺幅。基於 1V 的供應電壓下，此類比前端電路消耗了 8uW 而脈衝寬度調變電路則消耗了 5uW。

A low power Analog Front-End for Bio-signal monitoring system application

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Abstract

With the growing pains suffered from chronic disease and the coming of aging society, there is a highly demand on personal telehealth systems. Fortunately, due to the dramatic development of semiconductor technology and the IC design industries, biomedical chips can be developed for sensing and monitoring bio-signals. It is possible for us to develop a wireless bio-signal monitoring SoC to realize telehealth service. It not only help people prevent illness in advance but also benefit their health that would increase their quality of life. According to the information that announced by the Department of Health, cardiac disease is one of the leading causes of death. Therefore, a wireless ECG monitoring system for personal telehealth service is needed. To realize an ECG monitoring system, the analog front-end is a critical circuit block with the function of signal arrangement in the system. In this thesis, two kinds

of low power and low noise analog front-end are proposed to lower the noise interference and provide a multiple gain selection. Both of the analog front-end based on the TSMC 0.18μm technology are proposed to realize high performance biomedical ICs.

First, a current feedback instrumentation amplifier with a programmable gain amplifier for ECG signal detecting is proposed. By using chopper technique, the input-referred noise of CBIA is 90nV/$\sqrt{Hz}$ and the overall AFE is 1uV/$\sqrt{Hz}$. It provides several gain selections from 36dB to 54dB to meet the requirement for ECG signal detecting. The analog front-end only consumes 6uW based on the 1V voltage supply.

Second, an analog front-end with pulse-width modulation circuit is proposed. The pulse-width modulation circuit acts as an interface between analog front-end and digital signal processing circuit. The input-referred noise of the analog-front end is 80nV/$\sqrt{Hz}$. Besides, it not only provides four gain selections from 30dB to 50dB, but also has high output swing. Based on the 1V voltage supply, the analog front-end consumes 8uW and the pulse-width modulation circuit consumes 5uW.

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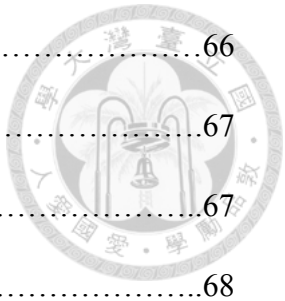

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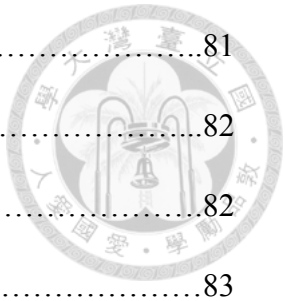

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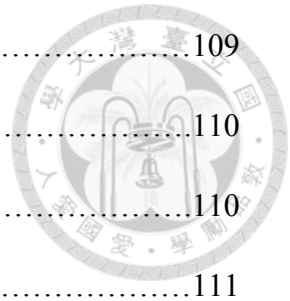

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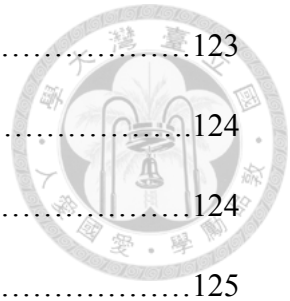

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Chapter 1

Introduction

1.1 Motivation

Due to the urbanization in modern society, the pressure and the fast pace of life may cause growing pains suffered from chronic disease. According to the information that announced by the Department of Health, cardiac disease is one of the leading causes of death. Besides, we are confronting to an aging society. More and more elderly people live alone without receiving a good medical care. All of these lead to a drive towards personal telehealth systems.

Another important reason for the demand on telehealth systems is that people consume more and more medical resource than ever before. Fig1.1-1 shows that healthcare cost has increased in all countries from past till now [12]. It reveals that the healthcare system in modern time needs to be changed.

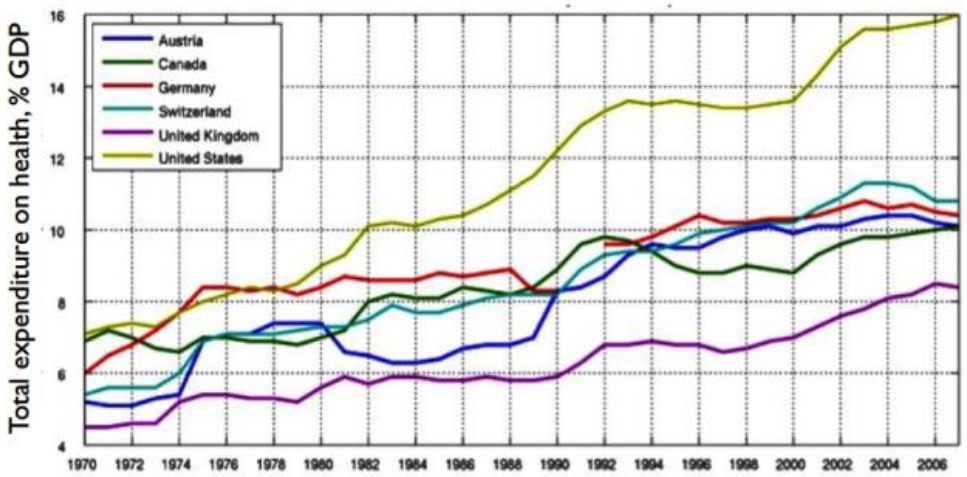


Fig.1.1-1 Healthcare cost from1970 to 2007

Fortunately, with the dramatic development of semiconductor technology and the IC design industries, biomedical chips can be developed for sensing and monitoring bio-signals. It is possible for us to develop a wireless bio-signal monitoring SoC to realize telehealth service. It not only help people prevent illness in advance but also benefit their health that would increase their quality of life. In view of this, we decide to make a wireless ECG monitoring system.

The key requirements from such bio-signal monitoring systems are the extraction, analysis, and wireless transmission of the bio-signals with low-power consumption, and robust operation on removing noise artifact [9]. Fig1.1-2 shows the block diagram of ECG monitoring system, which is composed by an analog front-end, ADC, DSP, and transmitter. ECG signal has characteristics of the low-level and low frequency. Thus, it is easy to be interfered with flicker noise, baseline drift and power line noise (60Hz). In order to lower the effect of such interference, a well-designed analog front-end is added as an analog process block, which is used to amplify and filter the ECG signal. Thus, it compensates some unwanted characteristics such as weak signals

and high noise to insure the purity of the ECG signal. In addition, analog front-end also provides a good driving ability for circuit system such as ADC in biomedical system. Hence, analog front-end is a critical circuit block having the function of signal arrangement in bio-signal monitoring system.

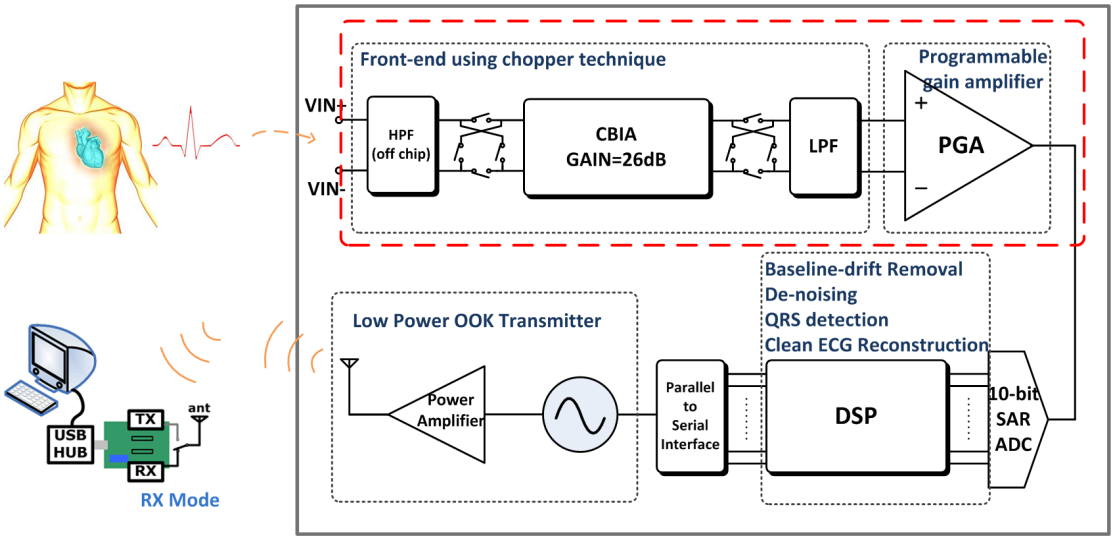


Fig.1.1-2 Block diagram of the ECG monitoring system

In this thesis, two kinds of low-power and low-noise analog front-end are proposed to lower the noise interference and provide a multiple gain selection. Besides, it is common to use ADC circuit to digitalize the analog signal in traditional way. A pulse-width modulation (PWM) circuit is proposed to be another way that uses time-proportioning technique to represent the analog signal in time domain, and the digital circuit can use high-resolution counter to digitalize the signal. The proposed circuits have been implemented in TSMC 0.18μm 1P6M CMOS process and consume low power from a 1V supply.

1.2 Thesis Organization

The thesis is organized into six chapters.

Chapter 1 gives a brief introduction of this thesis.

Chapter 2 begins with a brief introduction of the ECG signal and then the ECG signal monitoring system is introduced. Finally, we focus on the introduction about the analog-front end for ECG signal monitoring application.

Chapter 3 begins with the discussion of noise and offset in CMOS circuits, then the low-noise and low-offset techniques such as auto-zero and chopper technique are introduced. The theory of chopper technique is especially discussed. In addition, sub-threshold conduction is also introduced in this chapter. Finally, some kinds of circuits in analog front-end are presented.

Chapter 4 presents a low-noise and low-power current feedback instrumentation amplifier with programmable gain amplifier. The chopper technique is used to reduce the noise in an amplifier. Some measurement setups for example AC response measurement and noise measurement are presented, and both simulated and measured results confirm the function of analog front-end.

Chapter 5 presents another low-noise and low-power analog front-end with pulse-width modulation circuit. The chopper technique is also used in this circuit. Because of the difficulties to design a high resolution SAR ADC in such a low

voltage supply application and low-power consumption limitation, we proposed a pulse-width modulation circuit to act as an interface between analog front-end and digital signal processing circuit. Both simulation results and measurement results about the analog front-end and pulse-width modulation circuit are provided in this chapter to show that the performance of the circuit is good enough to detect ECG signals.

Eventually, the conclusions of this work are summarized in Chapter 6.

Chapter 2

ECG Signal and System Requirement

2.1 ECG Signal Introduction

Electrocardiogram (ECG/EKG) is a representation of electrical activity of the heart over a period of time, which is used in the analysis of heart disease. As the heart performs its function of bumping blood through the circulatory system, the result of action potentials within the heart would generate a certain sequence of electrical event. A typical ECG signal consists of a P wave, a QRS complex, and a T wave, as Fig. 2.1-1 shows. This display indicates the overall rhythm of the heart and weaknesses in different parts of the heart muscle. By positioning electrodes on a patient's skin in particular location, it is possible to extract useful information about the functionality of the heart. The placement of electrodes can form different ECG leads. There are 10 electrodes used for a 12-lead ECG. Table 2.1-1 shows the electrode label and

placement [31]. The electrode labels of RA, LA, RL, and LL form three limb leads and three augmented limb leads. The others electrode labels form six precordial leads.

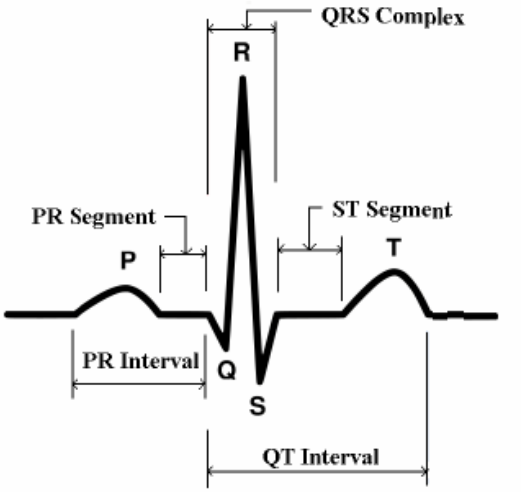


Fig2.1-1 Ideal ECG signal

Table 2.1-1 Electrode label and placement

Electrode label	Electrode placement
RA	On the right arm or right shoulder
LA	On the left arm or left shoulder
RL	On the right leg or right thigh
LL	On the left leg or left thigh
V_1	In the fourth intercostal space just to the right of the sternum.
V_2	In the fourth intercostal space just to the left of the sternum.
V_3	Between leads V_2 and V_4.
V_4	In the fifth intercostal space in the mid-clavicular line.
V_5	Horizontally even with V_4, in the anterior axillary line.
V_6	Horizontally even with V_4 and V_5 in the midaxillary line.

Fig. 2.1-2 shows the electrode placement of the limb leads [32]. Each lead represents a particular vector. These vectors are defined according to the Einthoven's triangle, as Fig. 2.1-3 depicts.

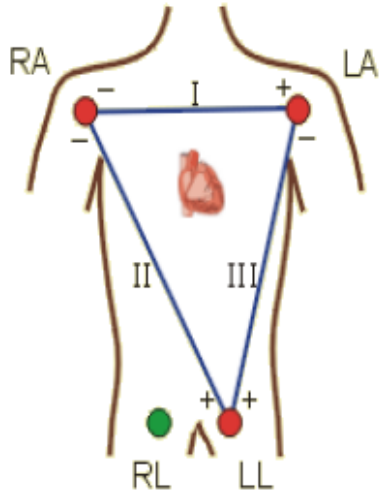


Fig. 2.1-2 Electrode placement of the limb leads

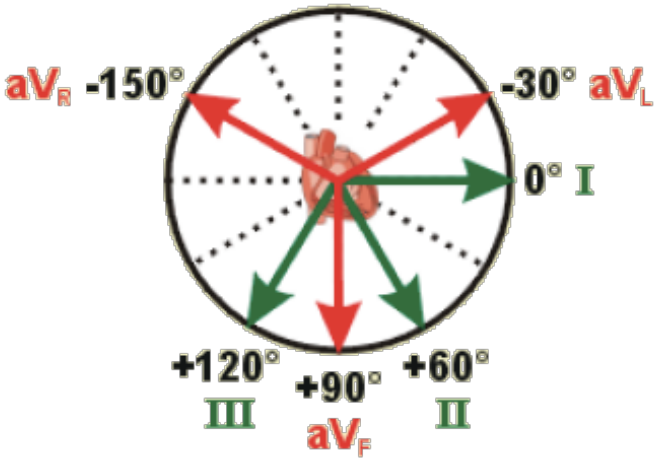


Fig. 2.1-3 Vectors of limb leads and augmented limb leads

Limb leads can be defined as follows:

- Lead I: The voltage between LA (positive) electrode and RA (negative) electrode.

  $Lead\ I = V_{LA} - V_{RA}$

- Lead II: The voltage between LL (positive) electrode and RA (negative) electrode.

  $Lead\ II = V_{LL} - V_{RA}$

- Lead III: The voltage between LL (positive) electrode and LA (negative) electrode.

  $Lead\ III = V_{LL} - V_{LA}$

From the equation above we can know that II = I + III

Augmented limb leads can be defined as follows:

- Lead augmented vector right (aV_R): RA is the positive electrode. The negative electrode is the combination of LA electrode and LL electrode.

  $aV_R = RA - (LA + LL) / 2 = -(Lead\ I + Lead\ II) / 2$

- Lead augmented vector left (aV_L): LA is the positive electrode. The negative electrode is the combination of RA electrode and LL electrode.

  $aV_L = LA - (RA + LL) / 2 = -(Lead\ I - Lead\ III) / 2$

- Lead augmented vector foot (aV_F): LL is the positive electrode. The negative electrode is the combination of RA electrode and LA electrode.

  $aV_F = LL - (RA + LA) / 2 = -(Lead\ II + Lead\ III) / 2$

The rest of the six electrode labels form the six precordial leads. These electrodes are placed directly on the chest. For the reason that these electrodes are close to the heart, they do not need augmented. Fig. 2.1-4 shows the electrode placement of the precordial leads.

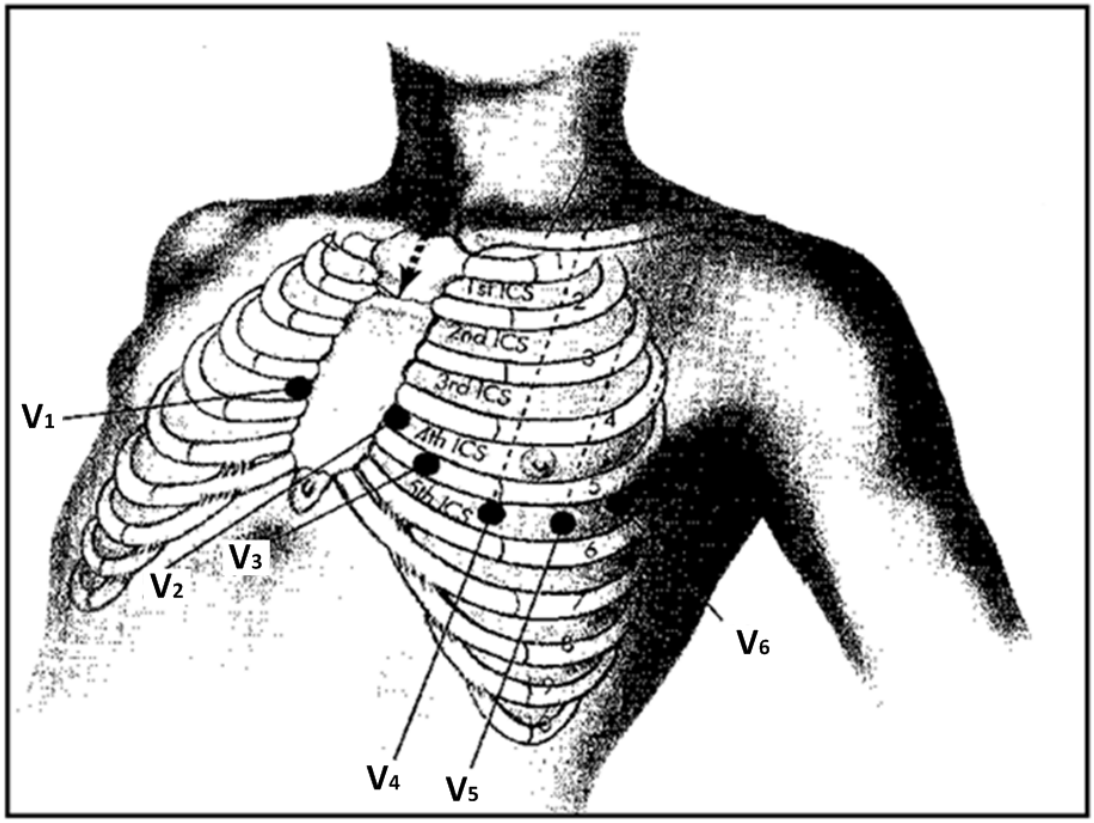


Fig. 2.1-4 Electrode placement of the precordial leads

2.2 A Wireless ECG Monitoring System

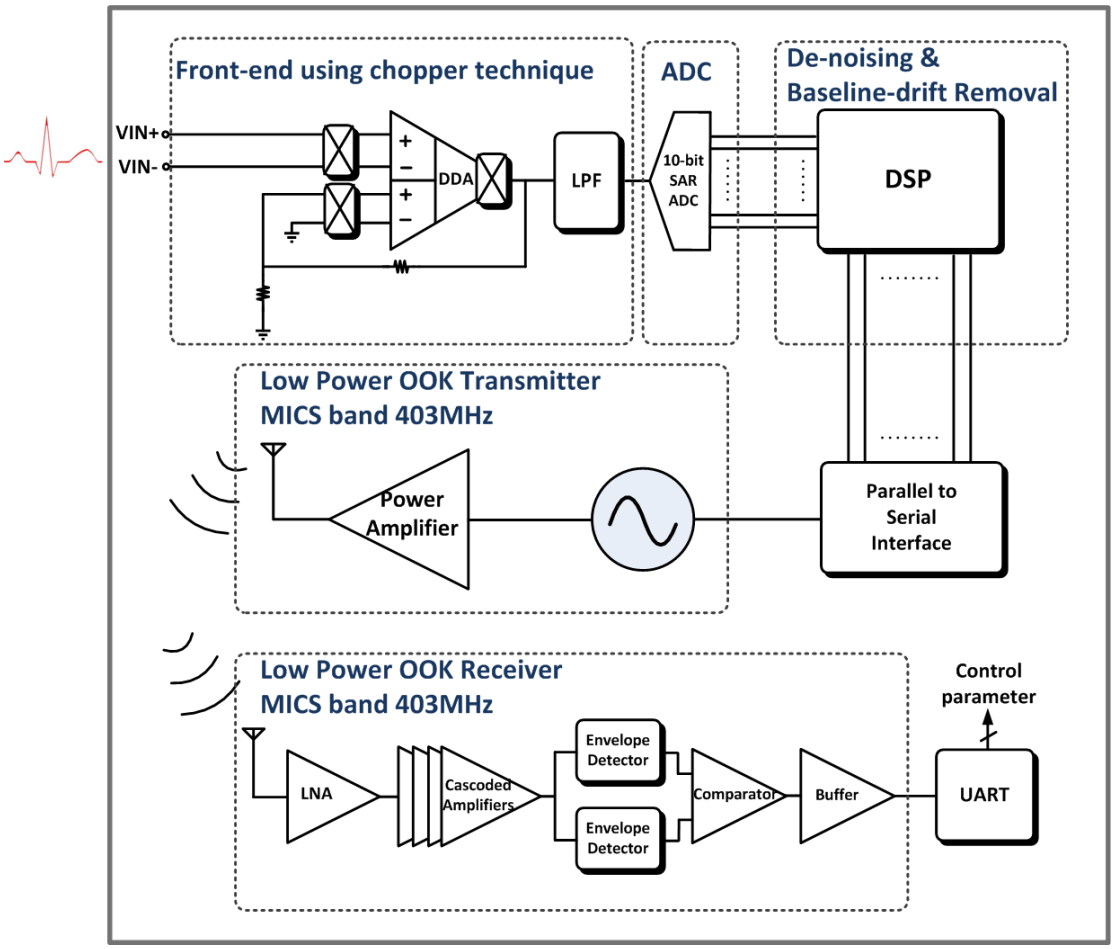


Fig. 2.2-1 Block diagram of the wireless ECG monitoring system

Fig. 2.2-1 shows the block diagram of the wireless ECG monitoring system. This system is composed by an analog front-end (AFE), an analog-to-digital converter (ADC), a digital signal processing circuit (DSP), an OOK transmitter (TX), and an OOK receiver (RX). The brief introduction of these circuits will be introduced below.

2.2.1 Analog front-end (AFE)

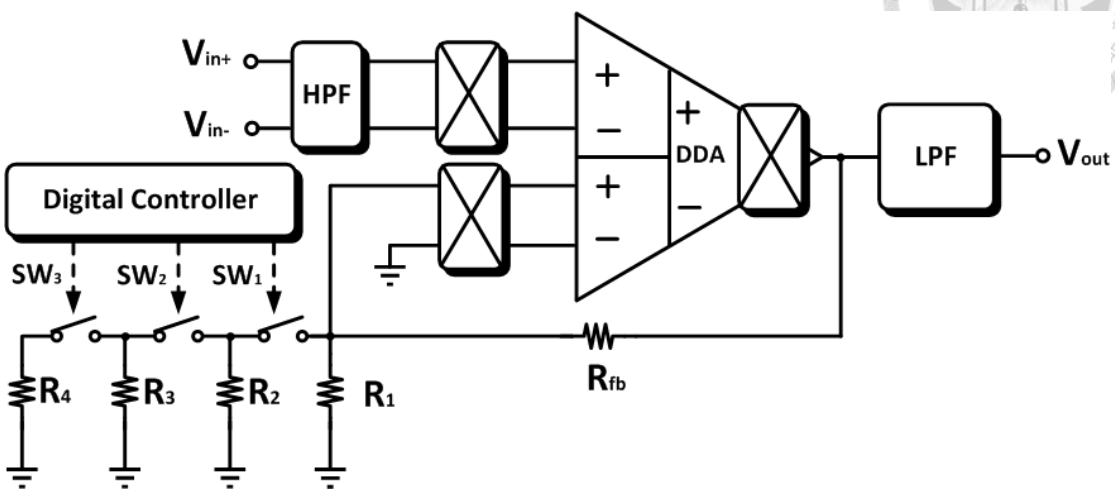


Fig. 2.2.1-1 Architecture of the analog front-end

Analog front-end is the beginning building block of the overall ECG monitoring system. It directly contacts with the ECG signal at the front and acts as an analog signal processor to amplify and filter the bio-signal. Typically, the amplitude of the ECG signal ranges between 100uV and 5mV, and the frequency ranges between 0.5 Hz and 250Hz. It means that the ECG signal has characteristics of low-level and low frequency so that it is easy to be interfered with noise and offset. By implementing analog front-end, we can use low-noise technique to lower the noise effect and amplify the bio-signal at the same time. The amplifier is the most critical building block of the analog front-end in terms of the signal quality and clarity. Hence, it is generally the most power consuming building block of an analog front-end. In view of this, in this thesis, the design effort focuses on implementing a low-power and low-noise amplifier. Fig. 2.2.1-1 shows the architecture of the analog front-end.

2.2.2 Analog-to-digital converter (ADC) [24][34]

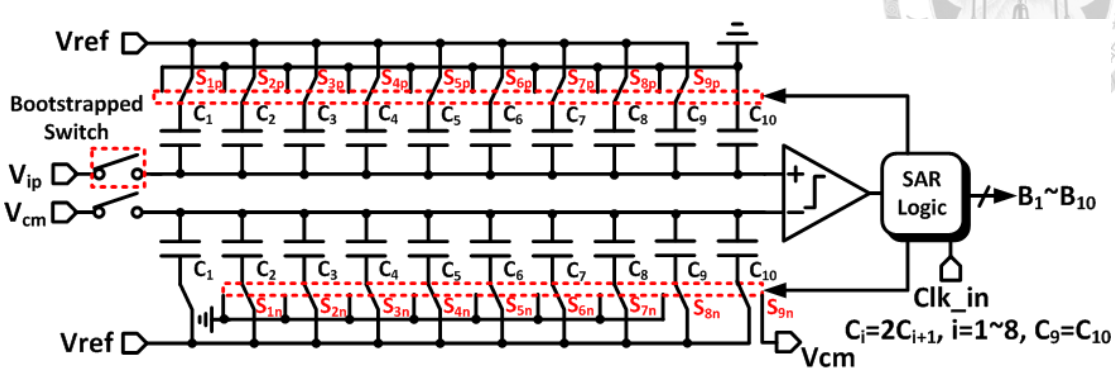


Fig. 2.2.2-1 Architecture of the analog-to-digital converter

Since the limitation of the low voltage supply and low power consumption, we choose the successive approximation register (SAR) ADC as the analog-to-digital converter in this system. ADC is the key to mixed signal SoCs in that it provides the interface between the physical world and digital processing. Speed, resolution, and power consumption are three critical parameters of an ADC. As a result, the SAR ADC is usually preferred in biomedical applications due to its high power efficiency at low and medium data rates. In this design, low power consumption and small chip area are preferred, so the single-ended architecture is employed. The primary sources of power consumption in the SAR ADC are the comparator and charge/discharge of the capacitor array. To reduce power, we use dynamic comparator to avoid the static power dissipation and MOM capacitor to reduce the power consumption in DAC.

In this application, ADCs with a sampling rate 360Hz which is the same as the clock of sensor interface front-end circuits and a resolution of 10 bits or greater are well suited. The fundamental building blocks of a SAR ADC are: a sampling switch,

a digital-to-analog converter (DAC), a dynamic comparator including latch, and a successive approximation logic. Fig. 2.2.2-1 shows our proposed single-ended SAR ADC.

2.2.3 Digital signal processing circuit (DSP) [35]

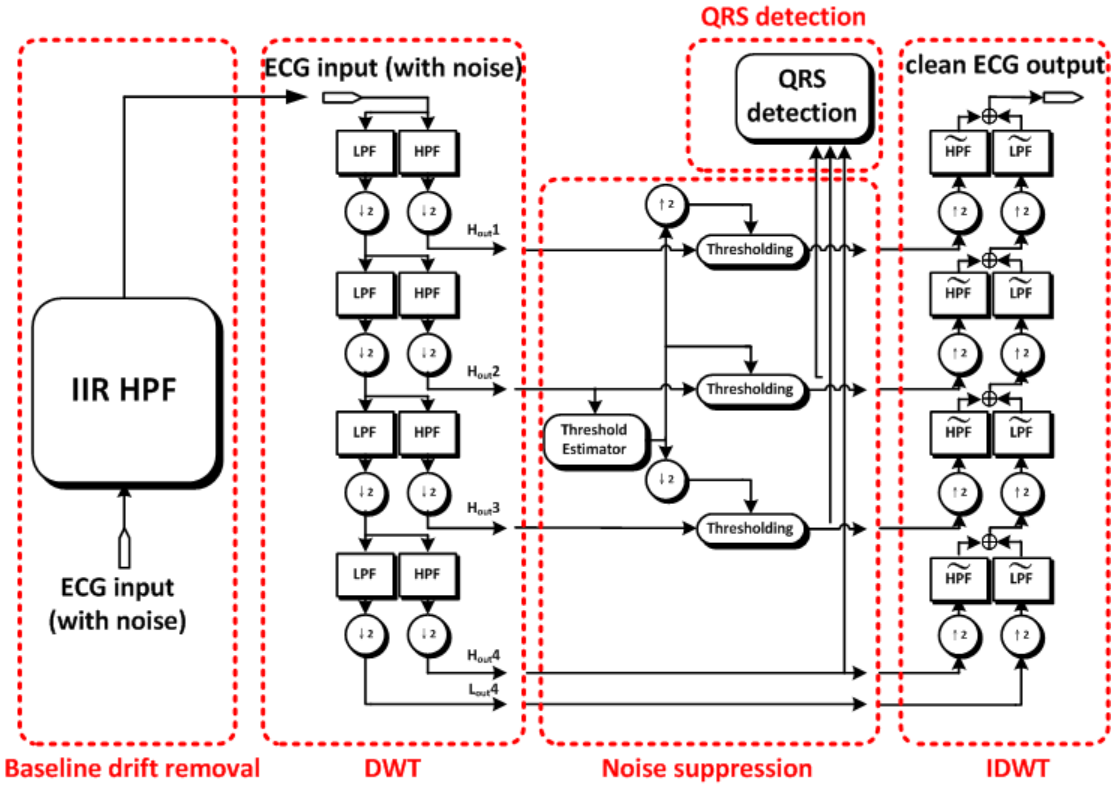


Fig. 2.2.3-1 Architecture of the digital signal processing circuit

Common filtering methods are often affected by ECG waveform variety, and they may lead to signal distortion. Thus, it is necessary to study new ECG signal noise reduction method. “Discrete Wavelet transform” can be thought of as an extension of the classic Fourier transform; instead of working on a single scale, it works on a

multi-scale basis. The main advantage of wavelet transform is that it has a varying window size, which is broad at low frequencies and narrow at high frequencies. It leads to an optimal time-frequency resolution in all frequency ranges, and the signal can be analyzed in different frequency sub-bands. Therefore, it is more suitable than traditional analyzing method for ECG signal processing. Based on the multi-resolution analysis, we can apply soft thresholding for removing various noise and artifacts, and then extract R-wave feature at multi-scale to increase accuracy of detection. Fig. 2.2.3-1 shows the architecture of the digital signal processing circuit.

2.2.4 OOK transmitter (TX) [36][37]

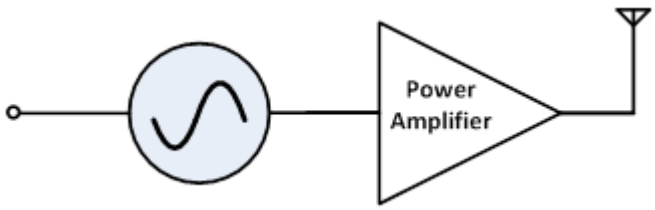


Fig. 2.2.4-1 Architecture of the OOK transmitter

To realize a wireless ECG monitoring system, a transmitter and a receiver are needed. Fig. 2.2.4-1 shows the architecture of the OOK transmitter, which includes a voltage-controlled oscillator (VCO) and a power amplifier (PA). The voltage-controlled oscillator generates 403MHz carrier and OOK modulation is achieved by turning voltage-controlled oscillator on and off. Amplitude-shift keying (ASK) is a form of modulation that represents digital data as variations in

the amplitude of a carrier wave. On-off keying (OOK) modulation is a special case of ASK modulation. Fig. 2.2.4-2 shows the difference between ASK modulation and OOK modulation. In the case of OOK modulation, the RF signal is only transmitted when the logic of data is one and does not transmits RF signal when the logic of data is 0. In this way, we can save half of the power so that it is more suitable for wireless ECG monitoring system application.

According to the Federal Communications Commission (FCC), Medical Implant Communication Service (MICS) is the name of a specification for using a frequency band between 402 and 405 MHz in communication with medical implants. Therefore, in this system, we choose 420~205 MHz as our carrier frequency.

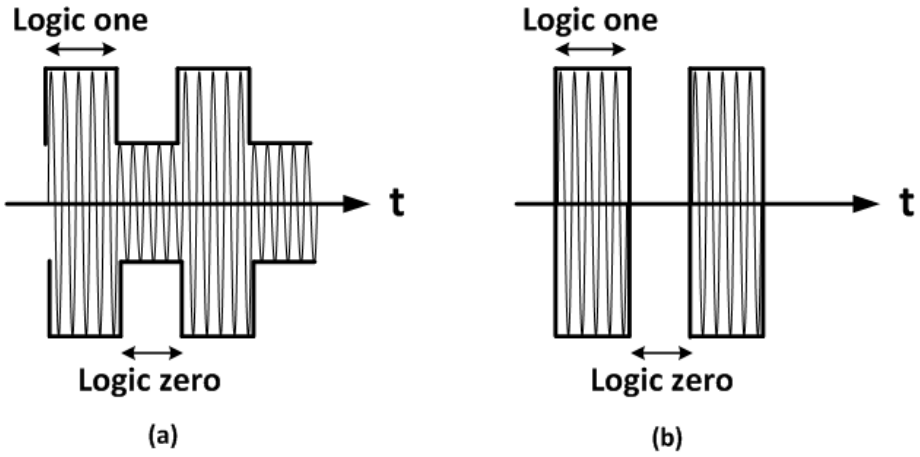


Fig. 2.2.4-2 (a) ASK modulation (b) OOK modulation

2.2.5 OOK receiver (RX) [38]

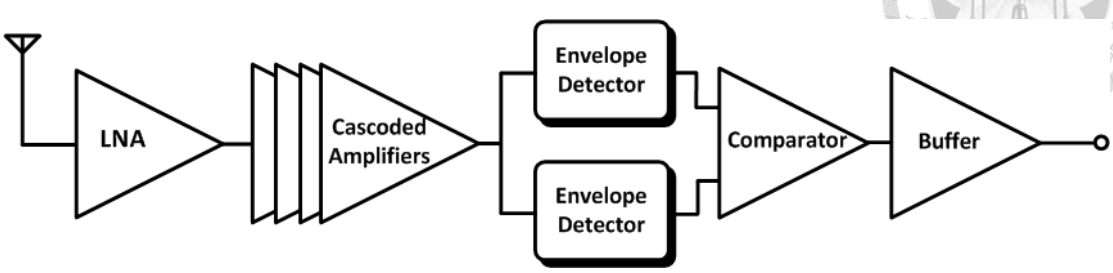


Fig. 2.2.5-1 Architecture of the OOK receiver

In this section, we will introduce an OOK receiver, which is also applied in MICS band system. A highly integrated receiver with low-voltage operation and low-power consumption is important for MICS communication systems. In the past, receivers are usually composed of low-noise amplifiers, down-conversion mixers, voltage-controlled oscillators, and baseband circuits. For low-IF receiver configuration, two mixers and one poly-phase filter with large chip area are necessary. For the homodyne topology, in addition to two mixers, a large amount of analog circuits are required to handle the DC offset. These receiver architectures not only need a large chip area but also consume huge power. Hence, they are not suitable for system integration. In this work, we proposed an OOK (on-off keying) receiver without mixers and VCO, etc. Fig. 2.2.5-1 shows the architecture of the OOK receiver. We adopt a pair of differential envelope detector in this circuit. By using this structure, we do not need additional reference voltage and can obtain a higher sensitivity.

2.3 Principle of Analog Front-End Design

In order to fulfill the ECG monitoring system, we must cooperate with other teammates in laboratory. In this thesis, we will focus on the discussion of the analog front-end. The essential purpose of an analog front-end for biomedical application is to amplify and filter the extremely weak bio-signals, such as ECG, EEG or EMG signal. The frequency and amplitude characteristics of the bio-signals mentioned above are illustrated in Fig. 2.3-1 [2]. This thesis is focusing on the analog front-end design for ECG signal processing. As we can see in Fig. 2.3-1, the amplitude of ECG signal is about 100uV~5mV and the frequency is about 0.5Hz~250Hz. The signal is quite low level and low frequency so that it is easy to be interfered with noise and offset. An analog front-end for biomedical application must cope with various challenges in order to extract the bio-signal.

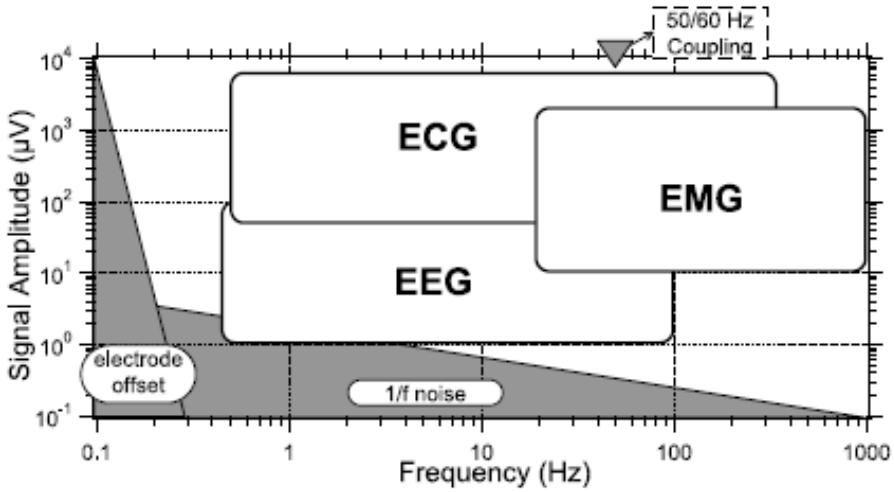


Fig. 2.3-1 Frequency and amplitude characteristics of the bio-signals

The challenges of designing an analog front-end for portable bio-signal acquisition systems can be summarized as follows [2]:

- High CMRR to reject interference from mains.
- HPF characteristics for filtering DC electrode offset.
- Low-noise design for high signal quality.
- Low power design for long-term battery life.
- Configurable gain and filter characteristics that suit the needs of different bio-signals.

Chapter 3

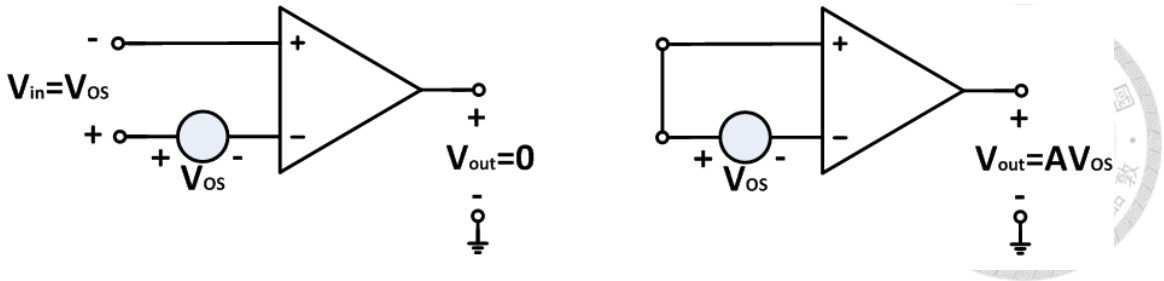
Fundamentals of

Analog Front-End

3.1 Offset and Noise in CMOS Circuits

3.1.1 Offset

Because of the variation of the CMOS process, there are several non-ideal effects would limit the performance of the CMOS operational amplifier, such as offset and noise effect. Input offset in a system is generally defined as the input level that forces the output level to go to zero. For an amplifier, as shown in Fig 3.1.1-1 [3], the input offset is the differential input voltage that forces the output voltage to go to zero, typically in the range 100uV to 10mV. Due to the amplifier's high voltage gain, input offset voltage virtually assures that the amplifier output will go into saturation. This definitely reduces the performance of the CMOS operational amplifier.



(a) (b)

Fig. 3.1.1-1 Amplifiers with offset (a) differential input voltage equal to input offset voltage forces output to zero, (b) output offset of an amplifier with shorted input

3.1.2 Noise

Noise is an unwanted random addition to a signal. It limits the minimum signal level that a circuit can process with acceptable quality. Analog signals processed by integrated circuits are corrupted by interference noise (or man-made noise) and device electronic noise. The former refers to random disturbances that a circuit experiences through the supply or ground lines. The latter refers to thermal noise and flicker noise. Fig. 3.1.2-1 shows the easy concept of the signal interferes by noise [13]. In general, we strive to maximize the signal to noise ratio in a system. Therefore, noise reduction has been an important topic due to the reduced supply voltage.

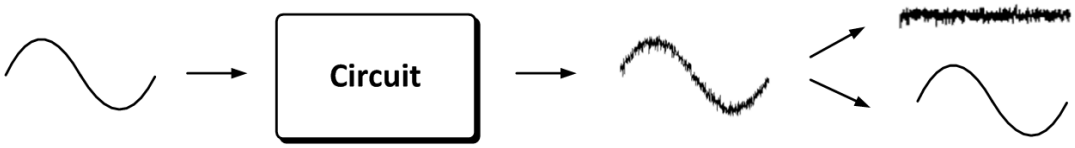


Fig. 3.1.2-1 Concept of signal interferes by noise

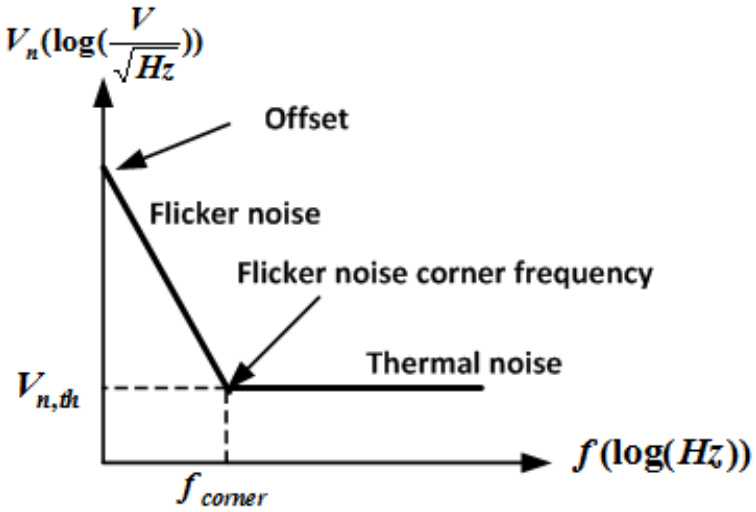
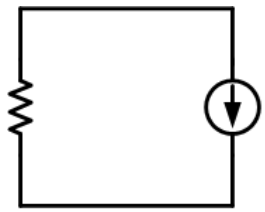


Fig. 3.1.2-2 Noise spectrum of standard CMOS amplifier

A conventional CMOS amplifier has a typical input-referred noise spectrum which as shown in Fig.3.1.2-2. For relative high frequencies, the noise, which spreads widely over the entire frequency band, can be considered as white noise. This is usually called the thermal noise floor. At low frequencies, the noise is increasing almost linearly with decreasing frequency and is generally called flicker noise. The frequency at which the noise becomes dominant over the white noise is called the noise corner frequency. At very low frequencies, offset becomes the dominant error. Although offset is usually modeled as a time-invariant voltage source, it may change due to aging and temperature variations. This implies that it has a certain bandwidth and can be considered as a very low-frequency noise source.

3.1.2.1 Thermal noise [1]

Thermal noise is a wide spectrum of electromagnetic noise appearing in electronic circuits and devices as a result of the temperature-dependent random motions of electrons and other charge carriers.



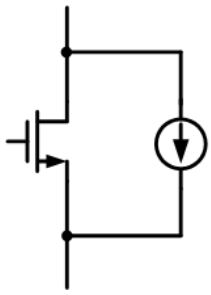
$$\overline{I_n^2} = \frac{4kT}{R} \quad (A^2/Hz)$$

Fig. 3.1.2.1-1 Representation of resistor thermal noise by a current source

As shown in Fig. 3.1.2.1-1, the thermal noise of a resistor R can be modeled by a parallel current source, with the spectral density:

$$\overline{I_n^2} = \frac{4kT}{R} \quad \text{or} \quad \overline{V_n^2} = 4kTR \quad -(3.1)$$

Where k = 1.38×10^{-23} J/K is the Boltzmann constant. Note that $\overline{I_n^2}$ is expressed in A^2/Hz, $\overline{V_n^2}$ is expressed in V^2/Hz.



$$\overline{I_n^2} = 4kT\gamma g_m \quad (A^2/Hz)$$

Fig. 3.1.2.1-2 Representation of MOSFET thermal noise by a current source

MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. For long-channel MOS devices operating in saturation, the channel noise can be modeled by a current source connected between the drain and source terminals. Fig. 3.1.2.1-2 shows the MOSFET thermal noise by a current source with the spectral density:

$$\overline{I_n^2} = 4kT\gamma g_m \quad \text{or} \quad \overline{V_n^2} = \frac{4kT\gamma}{g_m} \quad -(3.2)$$

The coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFET.

3.1.2.2 Flicker noise [1]

As charge carriers move at the interface between the gate oxide and the silicon substrate in a MOSFET, the trap-and-release energy states phenomenon associated with the dangling bonds would introduce flicker noise in the drain current. In electronic devices, it is a low-frequency phenomenon, as the higher frequencies are overshadowed by thermal noise from other sources. In MOSFET, flicker noise can be modeled as a voltage source in series with the gate and roughly given by:

$$\overline{V_n^2} = \frac{K}{C_{OX}WL} \cdot \frac{1}{f} \quad -(3.3)$$

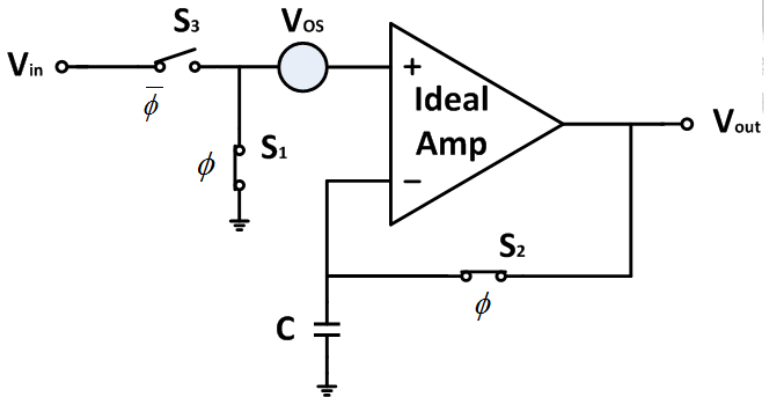
Where K is a process-dependent constant on the order of 10^{-25} V^2F. As this equation shows, flicker noise is proportional to 1/*f*, and therefore, flicker noise is also called 1/*f* noise.

The inverse dependence of (3.3) on WL suggests that to decrease 1/*f* noise the device area must be increased. Besides, PMOS devices exhibit less 1/*f* noise than NMOS devices because the former carry the holes in a buried channel.

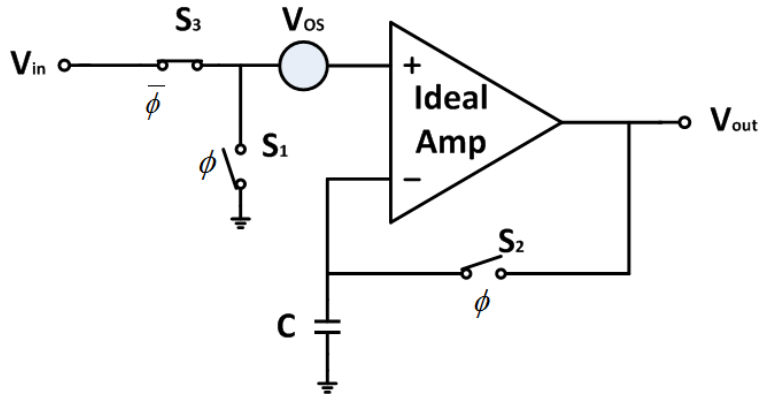
3.2 Low-Offset and Low-noise Technique

Noise reduction has become increasingly important in modern technology with reduced supply voltage. Because the sensitivity of CMOS amplifiers is always limited by offset and noise, some techniques such as auto-zero technique or the chopper technique are presented to decrease them. The fundamental difference between them is offset handing. While the auto-zero principle is time-modulated, chopper technique is frequency-modulated.

3.2.1 Auto-zero technique



(a)



(b)

Fig. 3.2.1-1 Principle of Auto-zero technique (a) Phase 1, ϕ=1 (b) Phase 2, ϕ=0

The principle of auto-zero technique is depicted in Fig. 3.2.1-1 [15]. The offset cancellation is done in two phases. First, as shown in Fig. 3.2.1-1(a), when ϕ=1 (sampling phase), $S_{1,2}$ is closed and S_3 is open. The amplifier is configured in negative feedback structure, and the amplifier's offset is stored on capacitor. The voltage over the auto-zero capacitor C can be expressed as:

$$V_C = \frac{A}{A+1} V_{OS} \quad -(3.4)$$

Second, as shown in Fig. 3.2.1-1(b), during ϕ=0(signal phase), $S_{1,2}$ is open and S_3 is closed. The sampled offset is subtracted from the input signal and amplified. The output voltage can be expressed as:

$$V_C = A(V_{in} + V_{OS} - V_C) = A(V_{in} + V_{OS} - \frac{A}{A+1}V_{OS}) = A(V_{in} + \frac{1}{A+1}V_{OS}) \quad -(3.5)$$

A channel charge of switch S_2 will feed into the auto-zero capacitor. This effect is called charge injection. Therefore, the overall residual offset can be expressed as:

$$V_{offset,residual} = \frac{1}{A+1}V_{OS} + \frac{q_{inj3}}{C} \quad -(3.6)$$

Because input offset voltage can be divided by the voltage gain, the residual offset is then dominated by the charge injection. The influence of the charge injection caused by switch S_2 on the residual offset can be reduced by increasing the size of the capacitor. In addition, the leakage of the capacitor C during the amplification phase can cause residual offset. These two effects cannot be divided by the voltage gain because the auto-zero capacitor is already at the input.

Besides the offset, the auto-zero technique can also minimize the flicker noise of the amplifier if the sampling frequency f_s is chosen higher than the noise corner frequency f_{corner}, as shown in Fig. 3.2.1-2. However, auto-zero technique has the problem of noise-folded at the frequency lower than sampling frequency f_s.

Intuitively, it can be assumed that when the amplifier depicted in Fig. 3.2.1-1 is auto-zeroed, the broadband noise of the amplifier is projected onto the capacitor C. At the end of the sampling phase the input offset and noise voltage are held on the

capacitor, which means that all components of noise above the auto-zeroing frequency will fold back due to aliasing. Fig. 3.2.1-2 shows that the noise at frequency lower than f_s is about $a \bullet V_{n,th}$, which is slightly higher than thermal noise.

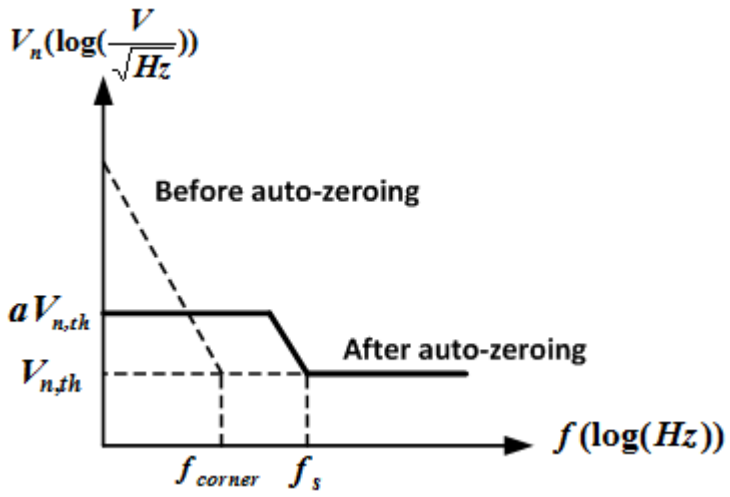


Fig. 3.2.1-2 Noise spectrum of auto-zero technique

3.2.2 Chopper technique

In chopper amplifiers the signal of interest and the offset signal are shifted to different frequencies. In Fig. 3.2.2-1, a chopper amplifier is shown [14]. This amplifier consists of a frequency modulator (or chopper CH1), a voltage amplifier, another chopper CH2, and a low-pass filter (LPF). The chopper switch is driven by a square wave φ with a chopping frequency f_c.

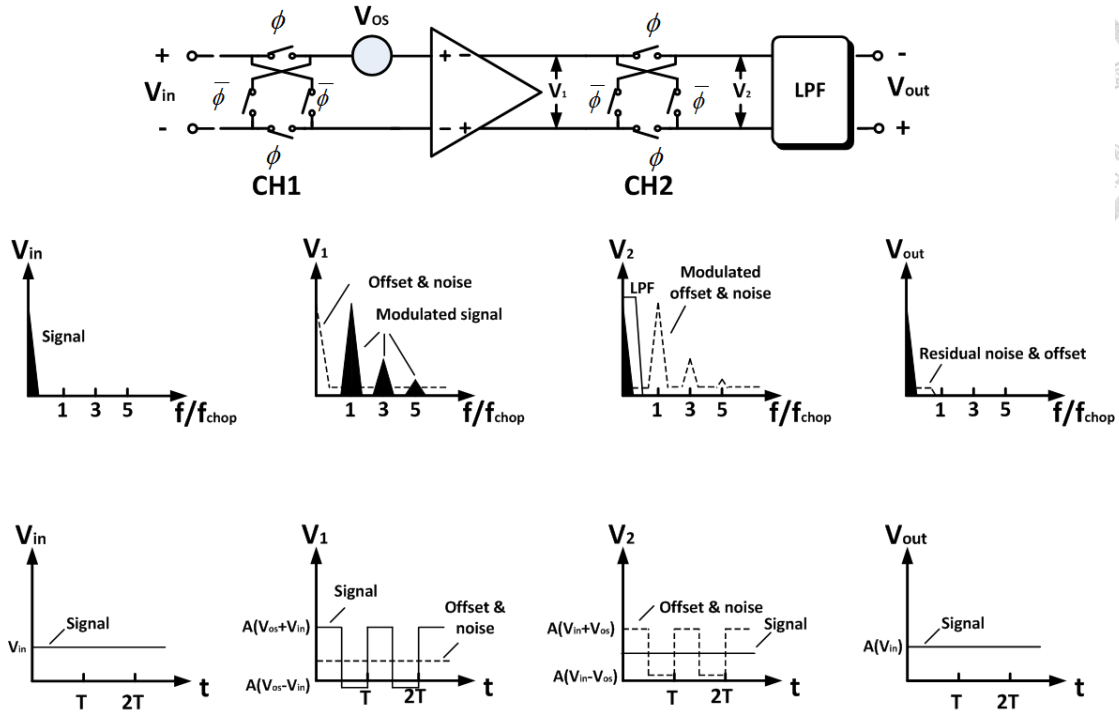


Fig. 3.2.2-1 Principle of Chopper technique and

its operation in Frequency/Time domain

From Fig. 3.2.2-1, we can know the method of operation of chopper technique both in frequency and time domain. The input signal is modulated to the chopping frequency at first. After amplify by an operational amplifier, the signal will be modulated back to the baseband. The offset and flicker noise is modulated only once and appears at the chopping frequency and its odd harmonics. At last, these frequency components can be removed through a low-pass filter.

The effect of chopper modulation can be analyzed from Fig. 3.2.2-2. Where V_{in} is the input signal and m(t) is the carrier signal taking values of +1 and -1 with frequency of chopping frequency f_c. It can be realized by two pairs of switch and complementary square wave ϕ and $\overline{\phi}$.

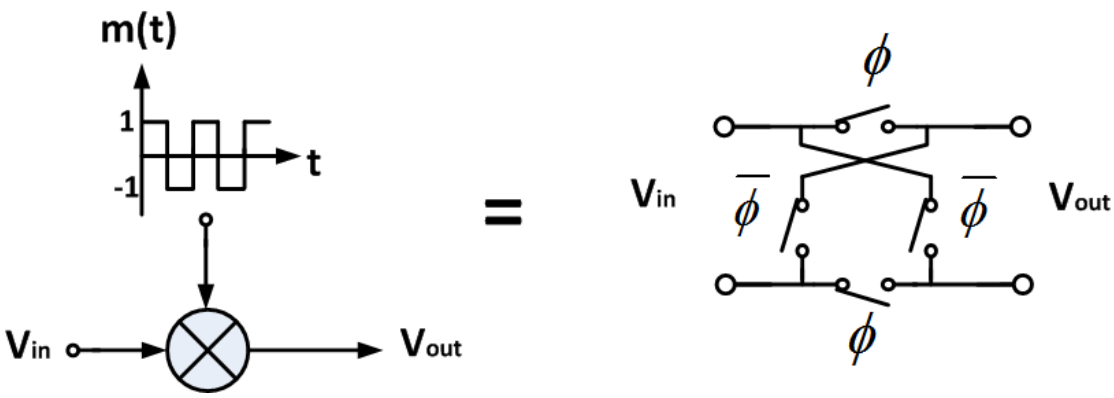


Fig. 3.2.2-2 Chopper modulation

The input signal V_{in} is multiplied by the square wave modulation signal m(t). After this modulation, the output signal V_{out} is transposed around the odd harmonic frequencies of the modulation signal and is given by the following Fourier series:

$$V_{in}(t) = a_0 + \sum_{n=1}^{\infty}\left\{a_n \cos\frac{2\pi}{T}t + b_n \sin\frac{2\pi}{T}t\right\} \quad -(3.5)$$

$$\text{with} \quad V_{in}(t) = 1, 0 < t < \frac{T}{2} \text{ and } V_{in}(t) = 0, \frac{T}{2} < t < T \quad -(3.6)$$

Therefore,

$$V_{in}(t) = \frac{4}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}\sin nwt \quad -(3.7)$$

According to (3.7), we can note that chopper modulation will shift offset and noise to the odd harmonic frequencies.

When a low-pass filter is used after the chopper amplifier, the chopper ripple and low-frequency noise can be filtered. CMOS amplifiers usually have a high DC input offset voltage and flicker noise. To reduce the flicker noise, the chopper frequency chosen should be higher than the $1/f$ corner frequency.

From Fig. 3.2.2-1, this analysis can be concluded that the chopper technique completely reduces the 1/*f* noise when the chopper frequency is higher than the corner frequency of the 1/*f* noise. In practice the noise level of a chopper amplifier is slightly higher than the thermal noise level. Fig. 3.2.2-3 shows the noise spectrum of chopper technique. In contrast to the auto-zero technique, we can observe that the baseband noise of chopper amplifier is almost equal to the wideband thermal noise. Thus chopper technique is adopted to suppress the dc offset and low frequency in this thesis.

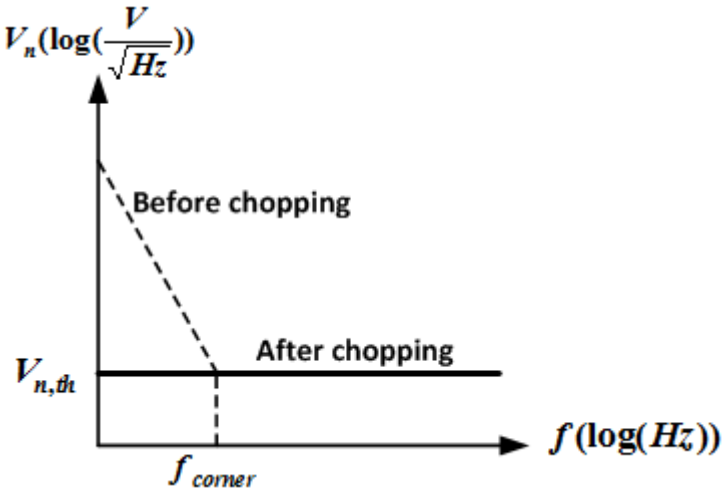


Fig. 3.2.2-3 Noise spectrum of auto-chopper technique

Although chopper technique has better performance on noise suppression than auto-zero technique, it still has some non-ideal effect. The ideal and non-ideal waveforms are depicted in time domain in Fig. 3.2.2-4. The gray line shows the ideal waveform and the black line shows the actual waveform. The limited bandwidth of the amplifier is a fundamental cause of switching glitches, so the square wave at the output of amplifier would not be like a perfect square wave. Therefore after

demodulation the actual waveform would include part of the chopper ripple, just as Fig. 3.2.2-4(b) depicts.

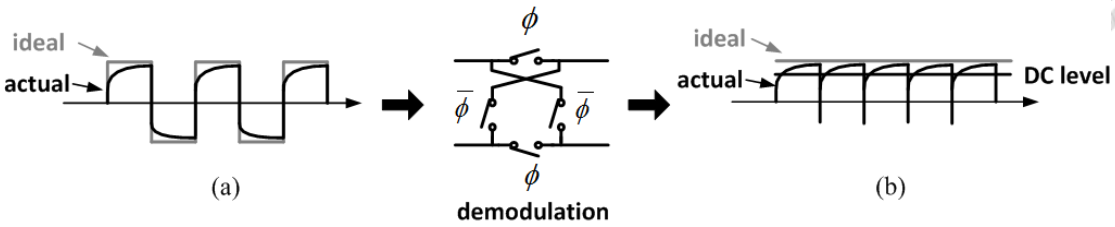


Fig. 3.2.2-4 Ideal and non-ideal waveforms of chopper amplifier in time domain

(a) Amplifier output (b) Demodulated amplifier output

Another non-ideal effect is the residual offset caused by charge injection, which is generated by chopper modulator. Fig. 3.2.2-5 shows the basic concept of charge injection.

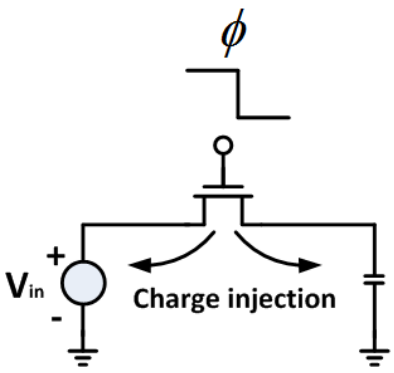


Fig. 3.2.2-5 Basic concept of charge injection

The gate voltage changes from high to low, transitioning the switch from closed to open state. When the gate of the NMOS transistor is high and the transistor is on, the voltage on the voltage source is sampled on the capacitor. When the gate of the NMOS transistor is low and the transistor is off, the voltage on the capacitor should ideally remain unchanged so that it could be processed. However, non-ideal effects

from the MOS switch create an error in the sampled voltage. When the transistor turns off, channel charge is dispersed into the source and drain so that charge injection occurs. This effect will cause channel charge entering the source or drain and introduces an error voltage.

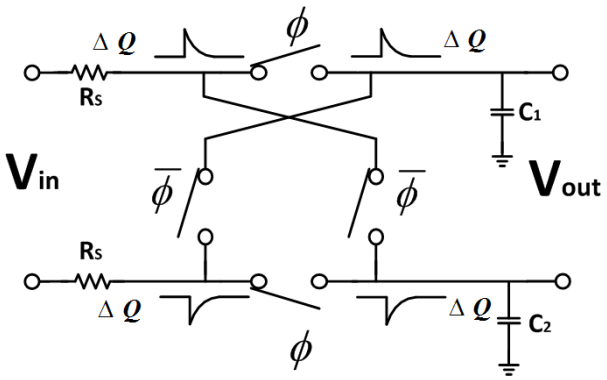


Fig. 3.2.2-6 Charge injection model of a chopper modulator

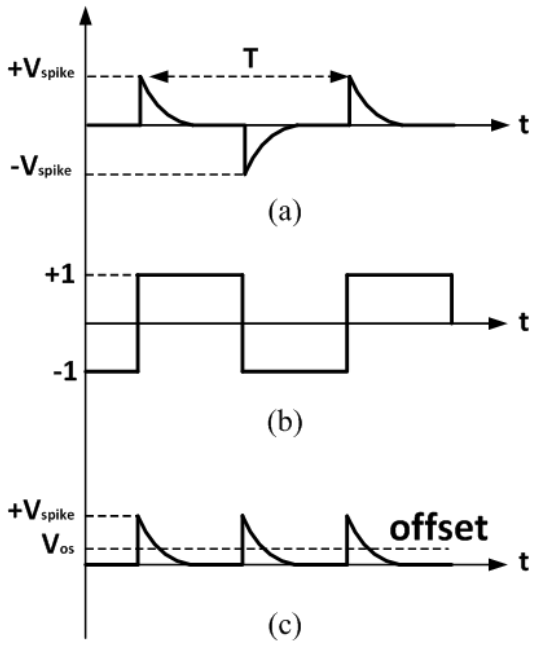


Fig. 3.2.2-7 Residual offset caused by spike (a) Spike signal (b) Demodulation signal (c) Demodulated spike

Fig.3.2.2-6 is the charge injection model of a chopper modulator, where R_S is the input resistor. C_1 and C_2 are the parasitic capacitors [33]. The effect of the mismatch between $C_1$and C_2 will be analyzed. When both lines are loaded with identical capacitors, no residual offset will occur since it will be a common-mode spike. However, if there is a slight mismatch between the two capacitors, a differential component will also appear at V_{out}, which will translate into a residual offset, because these spikes are actually demodulated by the input chopper towards the input.

This effect is illustrated in Fig. 3.2.2-7 [33]. Therefore, each time the chopper clock switches charge is being injected into the input, this differential charge can be expressed by:

$$q_{inj}=(C_1-C_2)V_{spike} \quad -(3.8)$$

Where V_{spike} is the spike voltage generated by chopper modulator. This charge is applied two times the per clock period. This means that a current will run through the resistor R_S. So the residual offset can be expressed by:

$$V_{OS}=2(R_S)(C_1-C_2)V_{spike}f_c \quad -(3.9)$$

Where f_c is the chopping frequency. Since the time constant of these parasitic spikes is generally much smaller than the half chopper period, most of the spike appears at frequencies higher than chopper frequencies [3].

Transmission gate can reduces charge injection effect. As Fig. 3.2.2-8 depict, since the charge carriers in the NMOS and PMOS have inversed polarity. The negative charge from the NMOS cancels the positive charge from the PMOS.

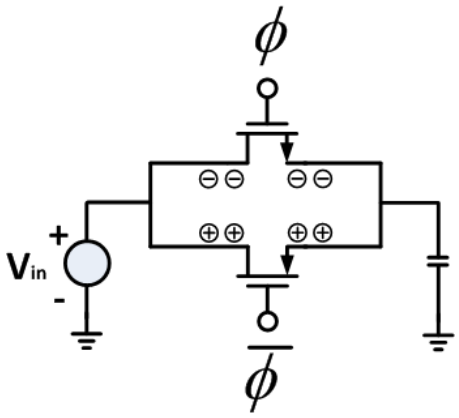


Fig. 3.2.2-8 Reduce charge injection effect by using transmission gate

3.3 Sub-threshold conduction design

Sub-threshold conduction is the current flows between the source and drain of a MOSFET when the transistor is operating in weak inversion region, that is, for gate-to source voltage V_{GS} is below the threshold voltage V_{th}. Traditionally, we assumed that the device turns off immediately when $V_{GS} < V_{th}$. In fact, for $V_{GS} \approx V_{th}$, a weak inversion layer still exists and some current flow between source and drain. Different from the current function when MOS is operating in saturation region, which is formulated as:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \quad -(3.10)$$

Sub-threshold conduction can be formulated as:

$$I_D = I_0 \cdot e^{\frac{V_{GS}}{nV_T}}, \quad V_T = \frac{kT}{q} \quad -(3.11)$$

Where *n* is a non-ideal factor, which is given by the capacitor divider:

$$n = \frac{C_{js} + C_{ox}}{C_{ox}} = 1 + \frac{C_{js}}{C_{ox}} \quad -(3.12)$$

Where C_{js} is the depletion layer capacitance. Typically, n ≈ 1.5~2. To obtain the g_m factor from two modes, we have differentiation to I_D and can get two separate equations:

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} = \mu C_{OX} \frac{W}{L}(V_{GS} - V_{th}) = \frac{2I_D}{V_{GS} - V_{th}} \quad -(3.13)$$

Sub-threshold region:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{I_0 e^{\frac{V_{GS}}{nV_T}}}{nV_T} = \frac{I_D}{nV_T} \quad -(3.14)$$

To compare the pros and cons between these two regions, we introduce g_m/I_D factor, which is also known as transconductance efficiency factor. It means we want a large g_m, for as little current as possible. Therefore, (3.13) and (3.14) can turn into:

Saturation region:

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{th}} = \frac{2}{V_{OV}} \quad -(3.15)$$

Sub-threshold region:

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \quad -(3.16)$$

We can plot these two equations in Fig. 3.3-1.

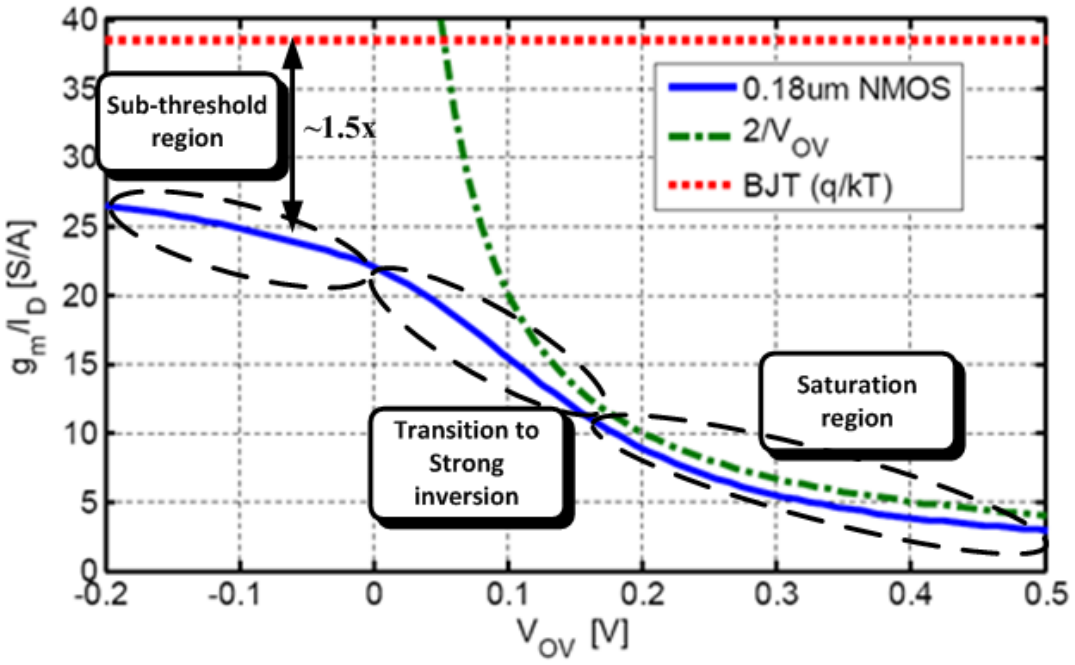


Fig. 3.3-1 g_m/I_D plot

In Fig. 3.3-1, we can see that $\frac{2}{V_{OV}}$ is fairly close for V_{OV} > 150mV [13]. However, g_m/I_D does not approach to infinity for $V_{OV} \rightarrow 0$. It is obviously to observe that MOS operates in sub-threshold region has better transconductance efficiency than operates in saturation region. It means that we can get a larger g_m value at same current condition when MOS operates in sub-threshold region. We can also observe that g_m/I_D is nearly a constant in sub-threshold conduction, which is similar to the behavior of BJT. Compare with the transconductance efficiency of BJT, it seems that we cannot do better than BJT even though the MOS is operating in sub-threshold region because it has a non-ideal factor n in its current function. The g_m/I_D value of sub-threshold conduction is about 1.5 times lower than BJT. However, in MOSFET

application, it is a great choice to have better transconductance efficiency by using sub-threshold conduction technique.

Besides to obtain the benefit of better tansconductance efficiency value, we can also analyze the noise effect when MOS operates in sub-threshold region. From equation (3.2), we already know that thermal noise spectral density of MOSFET is $\overline{V_n^2} = \frac{4kT\gamma}{g_m}$. If g_m is as large as possible, the noise spectral density can be reduced to a small value. Hence we can not only increase transconductance efficiency but also reduce the thermal noise spectral density by using sub-threshold conduction design.

3.4 Instrumentation Amplifier [33]

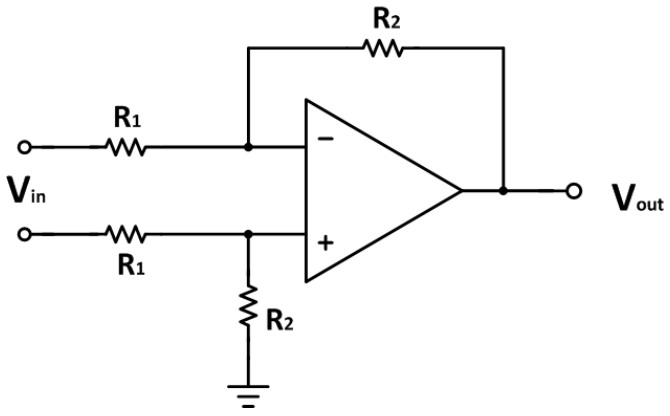


Fig. 3.4-1 Differential amplifier with resistive feedback

Bio-signal is a weak differential signal, which is often accompanies with a strong common-mode signal. Instrumentation amplifiers are the amplifiers that designed to

handle such tasks. Fig. 3.4-1 is a basic differential amplifier with resistive feedback. This amplifier suffers from unequal and low input impedances. Therefore its gain is dependent on the source impedances. To solve this problem, the three operational amplifiers based instrumentation amplifier has been developed, as shown in Fig. 3.4-2. The amplifier can accomplish differential inputs with a voltage gain of:

$$A_d = \frac{V_{out}}{V_{in}} = -\left(1 + \frac{R_2}{R_1}\right)\frac{R_4}{R_3} \quad -(3.17)$$

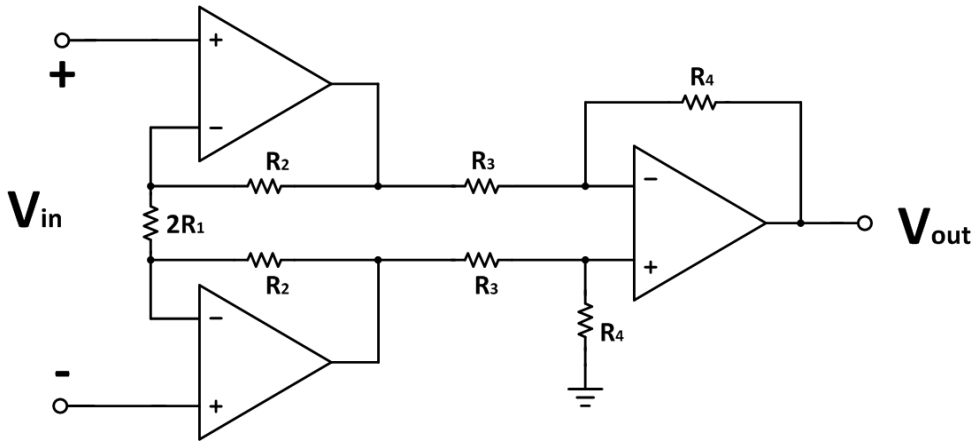


Fig. 3.4-2 A three operational amplifiers based instrumentation amplifier

Compare with differential amplifier in Fig. 3.4-1, instrumentation amplifier has higher input impedance since it uses two amplifiers to isolate feedback resistors from input signal. However, this topology has the problem of resistor mismatch that would reduce the performance of CMRR value. In order to achieve the goal of high CMRR, instrumentation amplifiers are often designed with the help of expensive laser-trimmed resistors. Therefore, we propose two topologies of instrumentation amplifier in this thesis to achieve better performance.

3.5 Proposed Instrumentation Amplifier

The Instrumentation amplifier (IA) is the most critical building block of the analog front-end in terms of the signal quality and clarity. It defines the noise level and the CMRR of the readout front-end, and filters the differential DC electrode offset. Hence, it is generally the most power consuming building block of an analog front-end. Therefore, the design effort focuses on implementing a low-power and low-noise IA.

3.5.1 Current feedback instrumentation amplifier (CBIA)

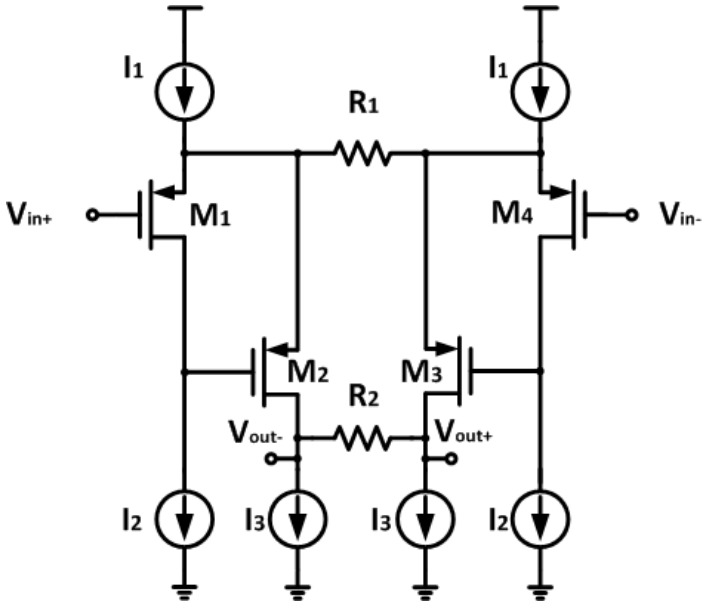


Fig. 3.5.1-1 Schematic of the current feedback instrumentation amplifier (CBIA)

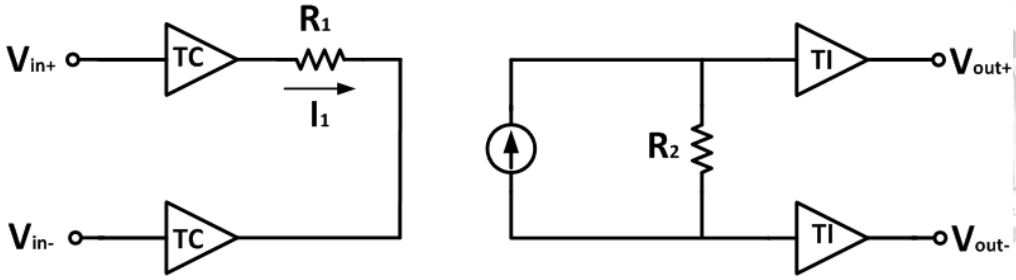


Fig. 3.5.1-2 Simplified schematic of CBIA

Fig. 3.5.1-1 shows schematic of the current feedback instrumentation amplifier (CBIA) [6]. It has only four parallel branches and there is no need for opamps. Fig. 3.5.1-2 shows the simplified schematic of CBIA. The input stage acts as a transconductance amplifier. The current passing through R_1 is copied to the transimpedance stage, and the voltage produced on R_2 is buffered to the output. Therefore, the voltage gain of the CBIA can be written as:

$$\left(V_{out+} - V_{out-}\right) = \frac{R_2}{R_1}\left(V_{in+} - V_{in-}\right) \quad (3.18)$$

Where the ratio of the two resistors defines the voltage gain of the CBIA. Thus, the CBIA topology eliminates not only the need for matched resistors for achieving high CMRR but also the need for low output impedance amplifiers. Besides, there is no need for three opamp, so the power dissipation can be low. Therefore, the CBIA topology is suitable for implementing low-power and low-noise IA. More details about the circuit will be discussed in chapter 4.

3.5.2 Differential difference amplifier with resistive feedback

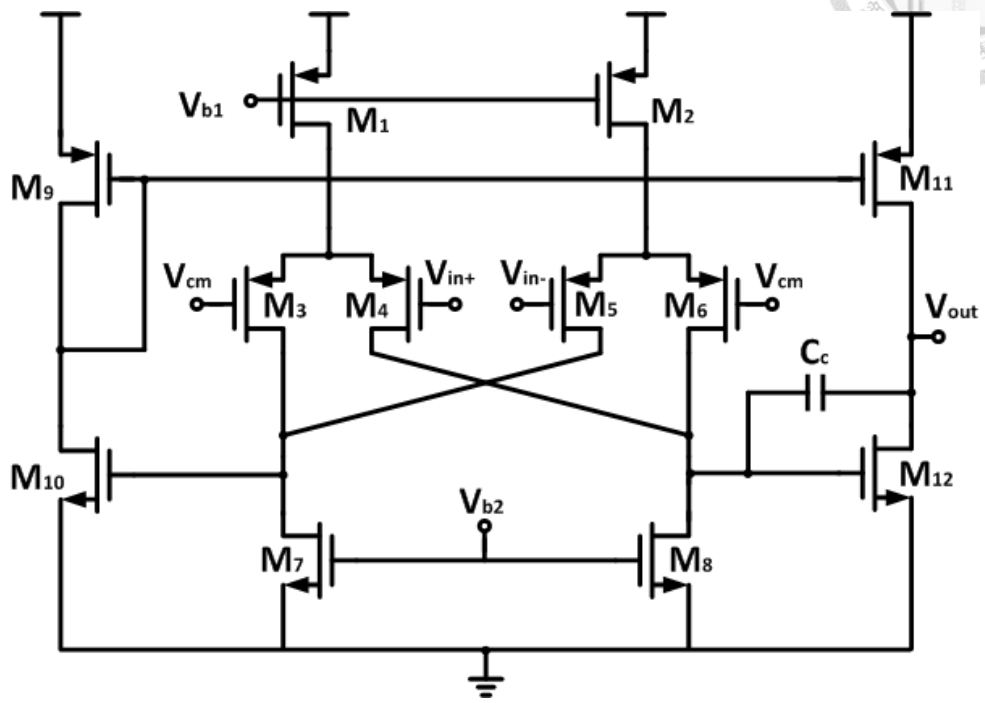


Fig. 3.5.2-1 Schematic of the differential difference amplifier (DDA)

Fig. 3.5.2-1 shows schematic of the differential difference amplifier (DDA). Since the current feedback instrumentation amplifier (CBIA) is a fully differential architecture, it requires common-mode feedback (CMFB) circuit, which means that CBIA needs extra power dissipation to realize CMFB circuit. Besides, CMFB circuit would limit the output swing of the CBIA because the output sees a voltage V_{GS} from the input of CMFB circuit. For low supply voltage, a voltage drop of V_{GS} severely decreases the output swing of the amplifier and reduces the resolution of the signal. By implementing differential difference amplifier, the problems mentioned above can be solved.

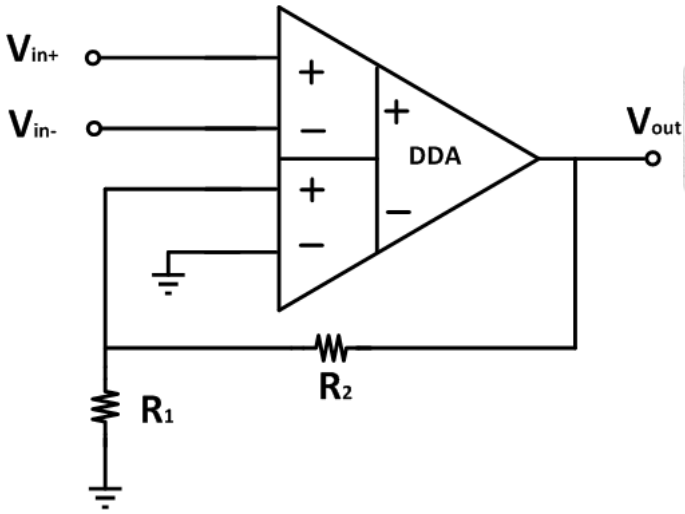


Fig. 3.5.2-2 Differential difference amplifier with resistive feedback

Fig. 3.5.2-2 shows a differential difference amplifier with resistive feedback. The voltage gain of the circuit can be written as:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)\left(V_{in+} - V_{in-}\right) \quad (3.19)$$

The ratio of the two resistors defines the voltage gain of the amplifier. Compare with traditional three opamp instrumentation amplifier, it doesn't need for resistor matching. More details about the circuit will be discussed in chapter 5.

Chapter 4

A Current Feedback IA with a Programmable Gain Amplifier for ECG signal Detecting

4.1 Introduction

Some principles about current feedback instrumentation amplifier (CBIA) has introduced in Chapter 3. To realize a low-power and low-noise analog front-end for ECG signal detecting, we will introduce a complete system based on CBIA in this chapter. The circuit includes a pair of high pass filter (HPF) at the front, a CBIA incorporates with chopper technique and negative feedback resistors R_1 and R_2, a low pass filter, and a programmable gain amplifier. Furthermore, both simulation result and measurement result are provided in this chapter to show that the performance of the circuit is good enough to detect ECG signals.

4.2 Circuits Architecture

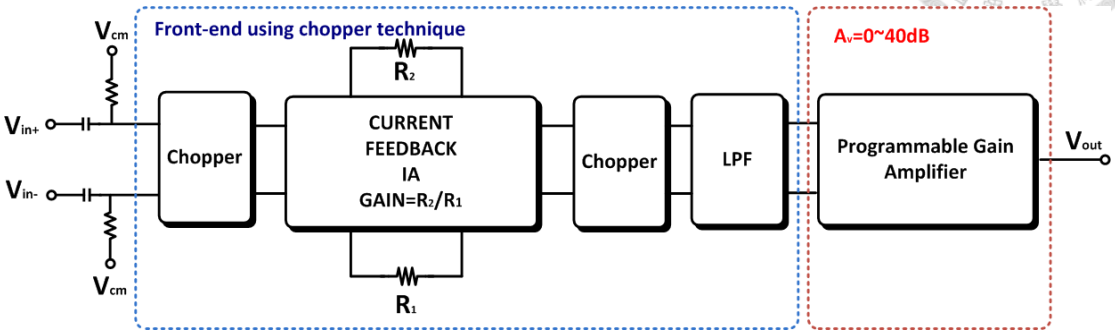


Fig. 4.2-1 Architecture of the CBIA with PGA

Fig. 4.2-1 represents the architecture of the current feedback instrumentation amplifier with programmable gain amplifier [6]. The chopper technique is used in this circuit. In order to benefit from the advantages of the chopper modulation technique for biomedical application, AC coupling must be introduced to prevent the readout circuit saturation. As Fig. 4.2-2 shows, AC coupling acts like a high pass filter and provides the common mode voltage through a large resistor R to insure the input voltage of CBIA is operating at V_{cm}. Besides, high pass filter can lower the input offset voltage so that the bio-signals would not saturate after being amplified by CBIA.

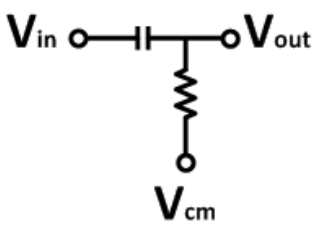


Fig. 4.2-2 AC coupling circuit (HPF)

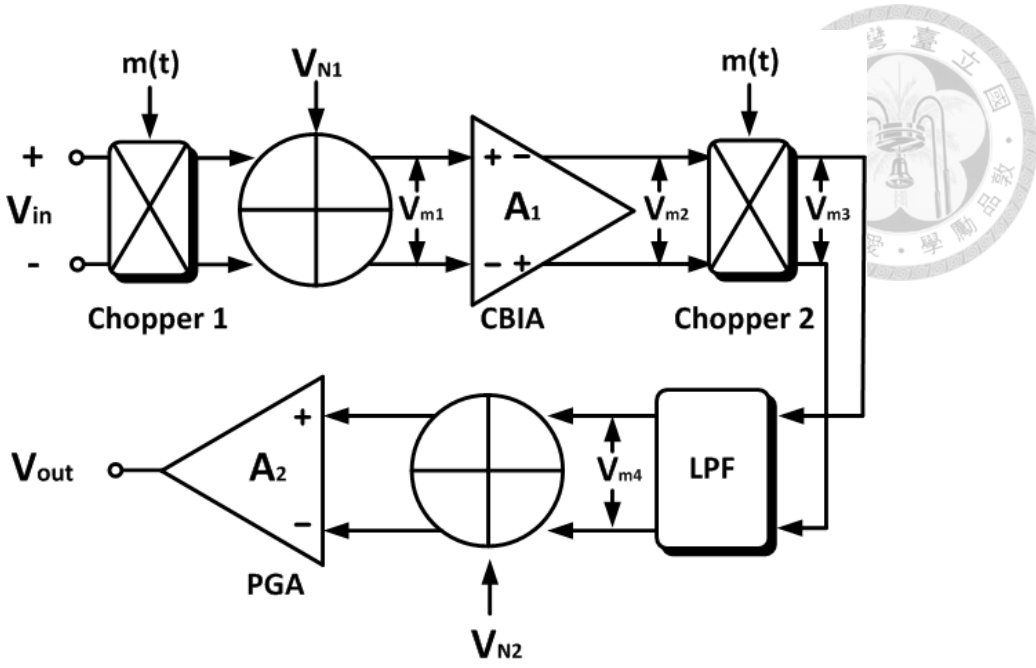


Fig. 4.2-3 Concept of the analog front-end with chopper technique

After AC coupling circuits, the bio-signal enters the analog front-end circuit. We can use Fig. 4.2-3 to analyze the signal and noise of the analog front-end with chopper technique [33]. The differential ECG signal is modulated by chopper switch (Chopper 1) and the modulated signal at the input pair can be written as:

$$V_{m1} = V_{in} \cdot m(t) + V_{N1} \quad -(4.1)$$

Where V_{N1} contributes the DC offset and flicker noise to the input pairs, and m(t) is the chopping signal taking values of +1 and -1 at the chopping frequency f_c. Because of the operation of input chopper modulator, the input signal is modulated to odd harmonics of chopping frequency f_c while the undesired component of V_{N1} resides at the baseband spectrum. After amplifying by CBIA, we obtain the equation below:

$$V_{m2} = A_1[V_{in} \cdot m(t) + V_{N1}] = A_1 \cdot V_{in} \cdot m(t) + A_1 \cdot V_{N1} \quad -(4.2)$$

After the demodulator (Chopper 2), the signal of V_{m2} is demodulated back to the baseband spectrum, and the undesired component V_{N1} is modulated to the odd harmonics of chopping frequency f_c. Now we can obtain this equation:

$$V_{m3} = m(t)[A_1 \cdot V_{in} \cdot m(t) + A_1 \cdot V_{N1}] = A_1 \cdot V_{in} \cdot m(t) \cdot m(t) + A_1 \cdot V_{N1} \cdot m(t) \quad -(4.3)$$

Due to the chopping process, $m(t) \cdot m(t) = 1$. Therefore, equation (4.3) can be simplified like this:

$$V_{m3} = A_1 \cdot V_{in} \cdot m(t) \cdot m(t) + A_1 \cdot V_{N1} \cdot m(t) = A_1 \cdot V_{in} + A_1 \cdot V_{N1} \cdot m(t) \quad -(4.4)$$

As the equation (4.4) shows, the last term signal contains the undesired component V_{N1}, including DC offset and flicker noise, is modulated to the odd harmonics of chopping frequency f_c. While we add a low pass filter after V_{m3}, V_{N1} can be removed. Therefore equation (4.4) can be modified like this:

$$V_{m4} = A_1 \cdot V_{in} \quad -(4.5)$$

When the signal enters to the last stage of the programmable gain amplifier (PGA), having a gain of A_2 and noise of V_{N2}, V_{out} can be expressed as:

$$V_{out} = A_2[A_1 \cdot V_{in} + V_{N2}] = A_1 A_2 \cdot V_{in} + A_2 \cdot V_{N2} \quad -(4.6)$$

According to equation (4.6), the analysis shows that the DC offset and flicker noise of input pairs are removed by using chopper technique. Moreover, in order to suppress the offset and flicker noise of V_{N2}, the gain of $A_1 V_{in} >> V_{N2}$ must be attained.

4.3 Circuits Implementation

In this section, we will introduce about the building blocks of the analog-front end system, including current feedback instrumentation amplifier (CBIA), common mode feedback circuit (CMFB), low pass filter (LPF), programmable gain amplifier (PGA), and clock generator.

4.3.1 Current feedback instrumentation amplifier (CBIA)

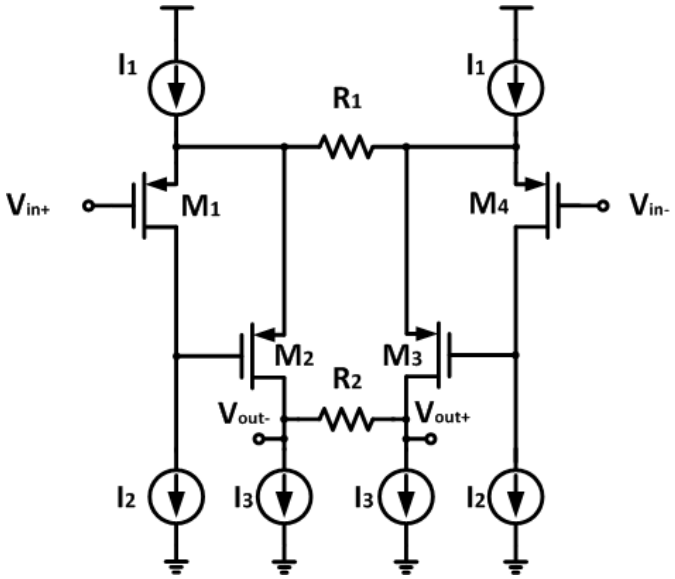


Fig. 4.3.1-1 Simplified schematic of CBIA

The main power-consuming block of the analog front-end is CBIA. Fig.4.3.1-1 shows the simplified schematic of the implemented CBIA structure [6]. It consists of

4 parallel branches and the need for opamp as in the case of traditional three-opamp instrumentation amplifier is eliminated. Thus, the power dissipation can be reduced.

The voltage gain of the CBIA can be calculated from the small signal half-circuit model. Fig. 4.3.1-2 depicts the small signal half-circuit of the simplified CBIA [6].

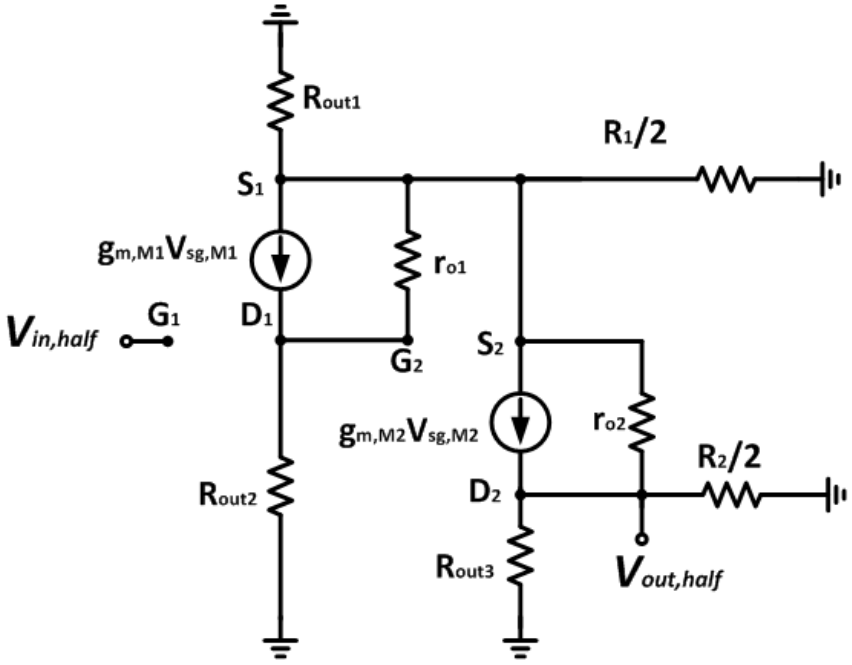


Fig. 4.3.1-2 Small signal half-circuit model of the simplified CBIA

Where g_{m1} is the transconductance value and r_{o1} is the output resistance of transistor M_1. g_{m2} is the transconductance value and r_{o2} is the output resistance of transistor M_2. R_{out1}, R_{out2}, and R_{out3} are the output resistances of the current source I_1, I_2, I_3, respectively.

Assuming that r_{o1} and r_{o2} are much larger than $R_1/2$ and $R_2/2$, the voltage gain of the CBIA structure can be derived as:

$$A_v = \frac{V_{out,half}}{V_{in,half}} = -\frac{R_2}{R_1}\frac{1}{1+\left(\frac{\alpha R_2}{R_{out,eq}}\right)} \quad -(4.7)$$

$$\alpha = \left(1+\frac{1}{g_{m,M_1}R_1}\right)\left(1+\frac{1}{g_{m,M_2}R_2}\right) \quad -(4.8)$$

Where $R_{out,eq}$ equals to $r_{o1}//r_{o2}$. If $\alpha R_2 << R_{out,eq}$, then the differential gain of the CBIA can be written as:

$$A_v = \frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}} = \frac{R_2}{R_1} \quad -(4.9)$$

From equation (4.9), we can know that the differential gain of the CBIA can be defined by only two resistors. Therefore, there's no need for the matched resistors.

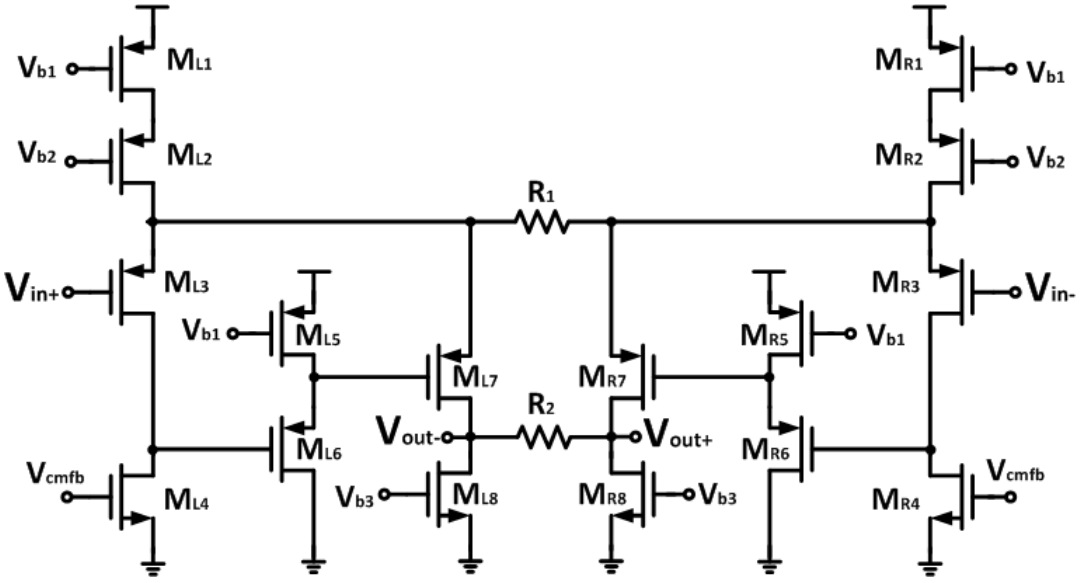


Fig. 4.3.1-3 Complete schematic of CBIA

Fig. 4.3.1-3 shows the complete schematic of CBIA [6]. The transistors M_{L5}, M_{L6} and M_{R5}, M_{R6} serve as a level shifter in order to maximize the input-output voltage swing of the CBIA. For the purpose of increase the CMRR value, we use cascade structure for current source I_1. Besides, due to the fully differential structure of the CBIA, a CMFB circuit is implemented. The CMFB circuit of the CBIA will be introduced in the next section.

4.3.2 Common mode feedback circuit (CMFB)

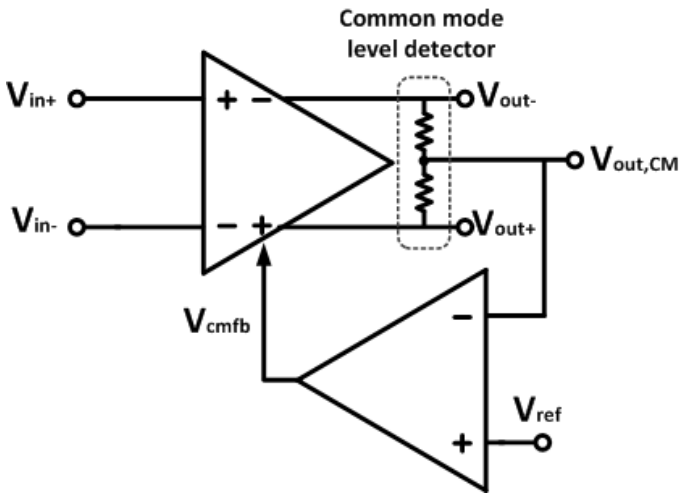


Fig. 4.3.2-1 Concept of CMFB with resistive sensing

As we have mentioned CBIA in the last section, it is a fully differential structure and its output common mode voltage cannot be stabilized by means of differential feedback. It needs a common mode feedback circuit (CMFB) to control the common mode component of the output signal.

Fig. 4.3.2-1 shows the traditional concept of CMFB with resistive sensing. In differential amplifiers, the output common mode level is quite sensitive to the mismatch of the components [25]. Thus, a CMFB network must be added to sense the common mode level of the two outputs and accordingly adjust one of the bias currents in the amplifier. In order to sense the output common mode level, we can employ a resistive divider to serve as a common mode level detector, just as shown in Fig. 4.3.2-1. The common mode level voltage can be written as:

$$V_{out,CM} = \frac{(R_+ V_{out+} + R_- V_{out-})}{R_+ + R_-} \quad -(4.10)$$

If $R_+ = R_-$, the equation can be reduced to:

$$V_{out,CM} = \frac{(V_{out+} + V_{out-})}{2} \quad -(4.11)$$

It seems reasonable to use a resistor divider to sense the common mode level. However, R_+ and R_- must be much greater than the output impedance of the opamp to avoid reducing the open-loop gain. It is difficult for such large resistors to occupy the chip area. Moreover, the mismatch of the two resistors is also a big problem.

In order to avoid such problems mentioned above, a current based CMFB is adopted. Fig. 4.3.2-2 depicts the schematic of current based CMFB. In this case, one of the input terminals of both differential pairs is connected to reference voltage V_{cm} and the outputs of the differential amplifier are connected to the other two input terminals of the pairs. A signal current is generated and gives rise to control voltage V_{cmfb} in the differential amplifier. Therefore, we do not need a resistor divider to serve

as a common mode level detector. Besides, a resistor divider suffers from the poor linearity because of the mismatch problem. Improved linearity is achieved due to the differential structure and operation of the common mode level detector [25].

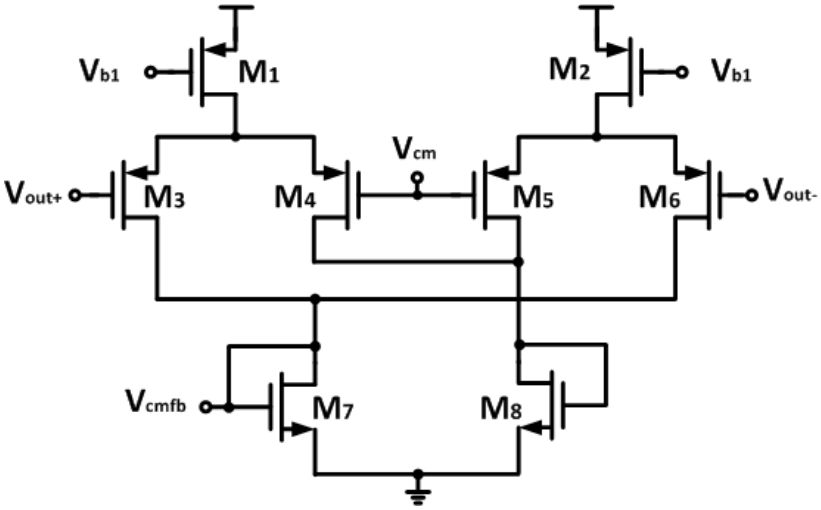


Fig. 4.3.2-2 Schematic of current based CMFB

4.3.3 Low pass filter (LPF) [4]

The main purpose of the low pass filter (LPF) is filtering the noise which is chopped to the chopping frequency f_c in analog front-end. In order to reduce the effect of the noise, we implement second-order low pass filter in the analog front-end.

There are two topologies for second-order low pass filter. They are the Multiple Feedback topology and the Sallen-Key topology. The former topology is commonly used in filters that have high Q_s and require a high gain. The latter is usually applied

in unity gain filter design. In this thesis, we adopt the Sallen-Key topology as our low pass filter. Fig. 4.3.3-1 shows the structure of unity gain Sallen-Key low pass filter

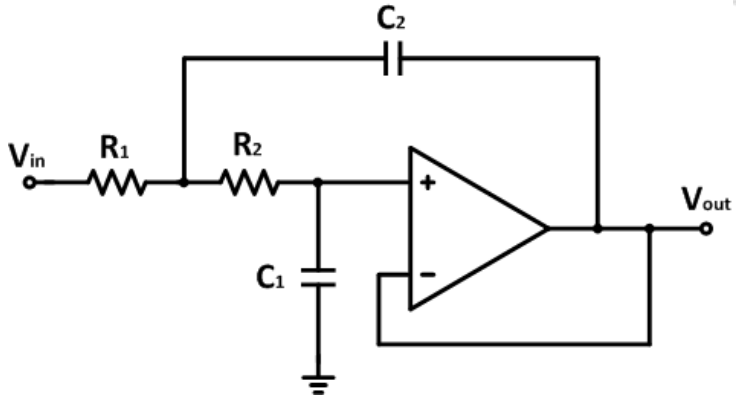


Fig. 4.3.3-1 Unity gain Sallen-Key low pass filter

The basic transfer function of the second-order low pass filter can be written as:

$$A(s) = \frac{A_0}{1 + a_1 s + b_1 s^2} \quad -(4.12)$$

For the unity gain Sallen-Key low pass filter in Fig. 4.3.3-1, the transfer function can be written as:

$$A(s) = \frac{1}{1 + \omega_c C_1 (R_1 + R_2) s + \omega_c{}^2 R_1 R_2 C_1 C_2 s^2} \quad -(4.13)$$

The coefficient comparing between (4.12) and (4.13) yields:

$$\begin{cases} A_0 = 1 \\ a_1 = \omega_c C_1 (R_1 + R_2) \\ b_1 = \omega_c{}^2 R_1 R_2 C_1 C_2 \end{cases} \quad -(4.14)$$

Given C_1 and C_2, the resistor values for R_1 and R_2 are calculated through:

$$R_{1,2} = \frac{a_1 C_2 \mp \sqrt{a_1^{\,2} C_2^{\,2} - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} \quad -(4.15)$$

In order to obtain real values under the square root, C_2 must satisfy the following condition:

$$C_2 \geq C_1 \frac{4 b_1}{a_1^{\,2}} \quad -(4.16)$$

As we know the relationship between C_1, C_2, R_1, R_2, a_1, b_1, and ω_c, we can use these coefficients to design the low pass filter. The following three types of filter are the most commonly used filters:

- Butterworth Low-pass filter:

  This filter provides maximum passband flatness. Therefore, it is usually used when the precise signal levels are required across the entire passband.

- Tschebyscheff Low-pass filter:

  This filter has a steeper roll-off and more passband ripple than Butterworth filter. It minimizes the error between the idealized and the actual filter characteristic, but with ripples in the passband.

- Bessel Low-pass filter:

  The passband gain of a Bessel filter is not as flat as that of the Butterworth filter, and the transition from passband to stopband is by far not as sharp as that of a Tschebyscheff filter.

Comparison of gain responses of the three types low pass filter is shown in Fig. 4.3.3-2. For the reason that Butterworth filter has maximum passband and has a moderate slope of transition from passband to stopband, we choose Butterworth type to realize our low pass filter in this thesis.

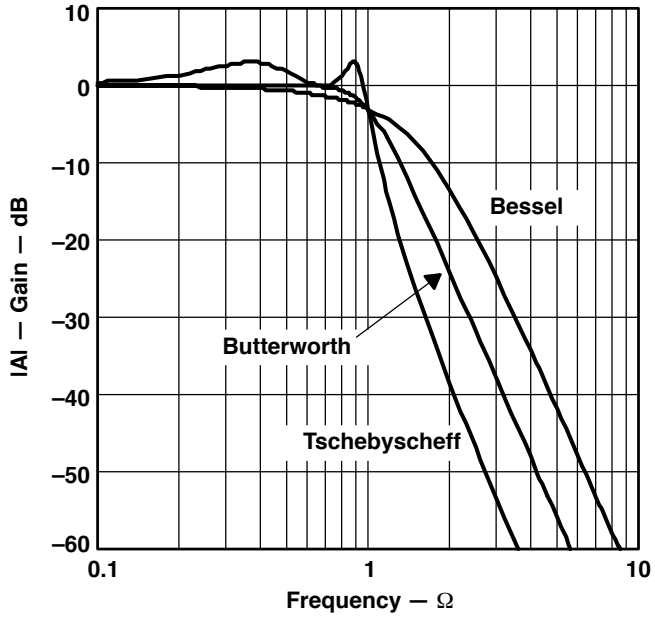


Fig. 4.3.3-2 Comparison of gain responses of the three types low pass filter

Table 4.3.3-1 Second-order filter coefficients

Second-order	Butterworth	Tschebyscheff	Bessel
a_1	1.4142	1.065	1.3617
b_1	1	1.9305	0.618

Table 4.3.3-1 lists the coefficients of a second-order filter type. From this table we can find out that the a_1 and b_1 coefficients of Butterworth filter are 1.4142 and 1, respectively. Assuming C_1 = 15pF, we can calculate equation (4.16):

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} = C_1 \cdot 4 \cdot \frac{1}{1.414^2} = 15 \cdot 10^{-12} pF \cdot 2 = 30 pF \quad -(4.17)$$

Inserting a_1 and b_1 into the resistor equation (4.15) results in:

$$R_{1,2} = \frac{1.414 \cdot C_2 \mp \sqrt{2C_2^2 - 4 \cdot \frac{C_2}{2} \cdot C_2}}{4\pi f_c \cdot \frac{C_2}{2} \cdot C_2} = \frac{1.414 \mp 0}{2\pi f_c \cdot C_2} = \frac{0.707}{\pi f_c \cdot C_2} \quad -(4.18)$$

For ECG signal detecting, we know that the characteristic frequency of ECG signal is about 0.5Hz~250Hz. Therefore, it is reasonable to set 3-dB frequency at 500Hz in low pass filter. Inserting f_c = 500 into equation (4.18) results in:

$$R_{1,2} = \frac{0.707}{\pi f_c \cdot C_2} = \frac{0.707}{\pi \cdot 500 \cdot 30 \cdot 10^{-12}} = 15M\Omega \quad -(4.19)$$

The value of C_1, C_2, R_1, and R_2 of the second-order Butterworth low pass filter can be sum up in Fig. 4.3.3-3.

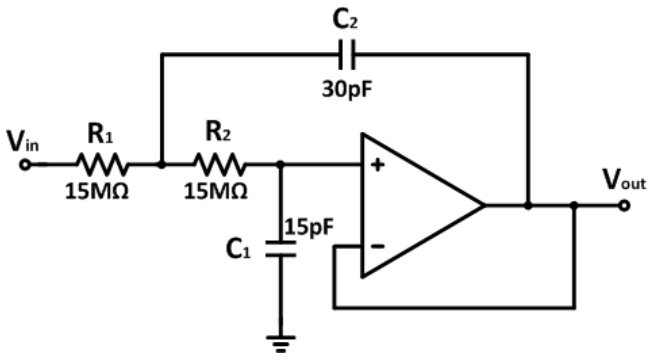


Fig. 4.3.3-3 Butterworth low pass filter

4.3.4 Programmable gain amplifier (PGA)

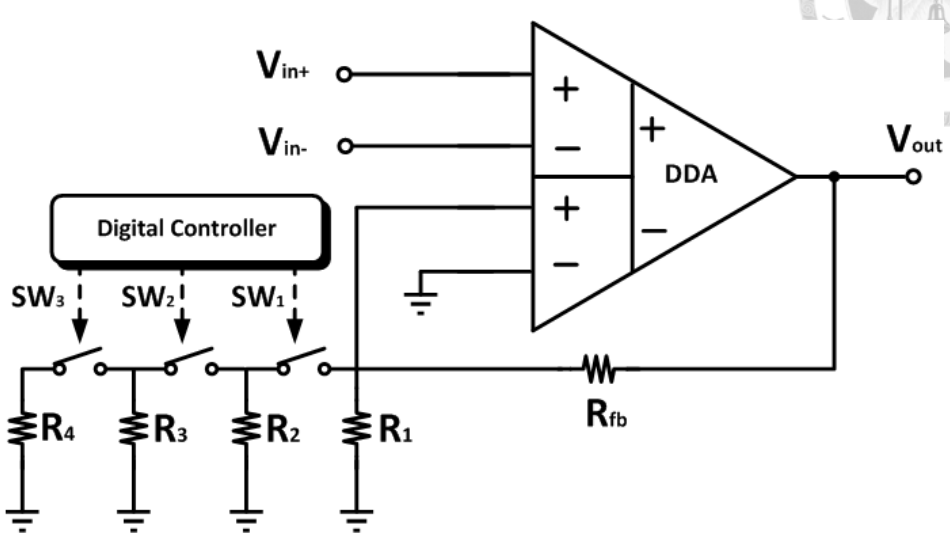


Fig. 4.3.4-1 Programmable gain amplifier

The programmable gain amplifier is depicted in Fig.4.3.4-1. The programmable gain amplifier includes a differential difference amplifier (DDA), a poly resistor string of R_1-R_4, and three transmission gate switches of SW_1-SW_3. The variable gain is obtained by poly resistor string of R_1-R_4 along with three transmission gate switches of SW_1-SW_3 and the gain setting is selected according to the digital controller. Based on the variable resistances controlled by the CMOS switches, programmable gain is defined as:

$$V_{out} = \left(1 + \frac{R_{fb}}{R_i}\right)\left(V_{in+} - V_{in-}\right) \quad -(4.20)$$

$$R_i = R_1,\ or\ R_1 // R_2, or\ R_1 // R_2 // R_3, or\ R_1 // R_2 // R_3 // R_4 \quad -(4.21)$$

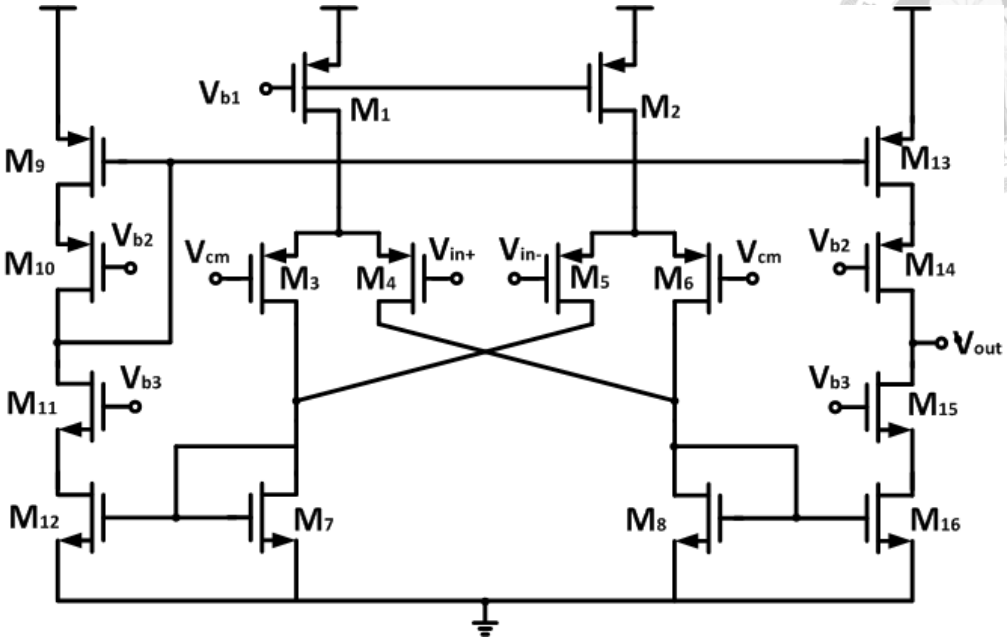


Fig. 4.3.4-2 Differential difference operational transconductance amplifier

Fig. 4.3.4-2 is a differential difference operational transconductance amplifier [18]. By implementing the differential difference structure, the output signal of CBIA would not see the finite feedback resistor but the high input impedance stage so that the signal would not decay. The operational transconductance amplifier (OTA) is a device that converts an input voltage into an output current. It is primarily voltage-to-current amplifiers. The g_m stage of the OTA can be written as:

$$\frac{I_{out}}{V_{in}} = (g_{m4,5} + g_{m3,6})\frac{g_{m16}}{g_{m8}} \quad -(4.22)$$

The open-loop gain of the amplifier in Fig. 4.3.4-2 is:

$$\frac{V_{out}}{V_{out}} = \frac{I_{out}}{V_{in}} \cdot \frac{V_{out}}{I_{out}} = \frac{(g_{m4,5} + g_{m3,6})}{g_{m8}} \cdot g_{m16} \cdot [(g_{m15} r_{o15} r_{o16}) // (g_{m14} r_{o14} r_{o13})] \quad -(4.23)$$

Although the programmable gain can be defined by equation (4.20), there's some intrinsic problems exist in the amplifier. To understand it, we can use the circuit depicted in Fig. 4.3.4-3 (a) and (b) to explain this problem.

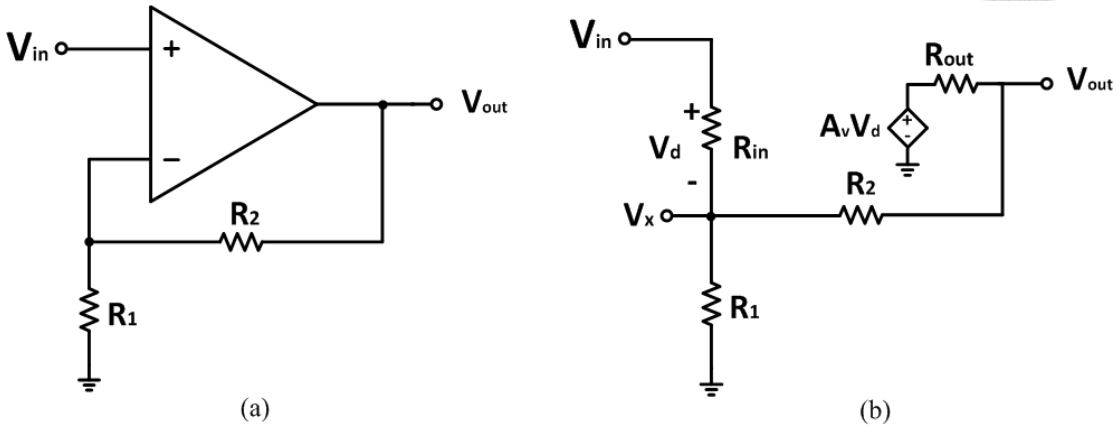


Fig. 4.3.4-3 (a) Non-inverting amplifier (b) Non-inverting amplifier equivalent circuit

Fig. 4.3.4-3 (a) shows a non-inverting amplifier. We all know that the ideal closed-loop gain can be written as $1+(R_2/R_1)$. However, the amplifier is not that ideal in reality. Fig. 4.3.4-3 (b) shows the equivalent circuit of the non-inverting amplifier. The non-zero resistor R_{out} and the infinite resistor R_{in} have non-ideal effect on circuit. Writing a KCL equation at output node yields:

$$\frac{A_V V_d - V_{out}}{R_{out}} = \frac{V_{out}}{R_1 + R_2} \quad -(4.24)$$

$$V_d = V_{in} - V_X \text{ , } V_X = V_{out}\frac{R_1}{R_1 + R_2} \quad -(4.25)$$

Solving the equation (4.24) and (4.25), then we have:

$$\frac{V_{out}}{V_{in}} = \frac{A_V}{1 + \frac{A_V R_1 + R_{out}}{R_1 + R_2}} \quad -(4.26)$$

By multiplying $\frac{R_1 + R_2}{A_V}$, we have:

$$\frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_1 + \frac{R_1 + R_2 + R_{out}}{A_V}} \quad -(4.27)$$

From equation (4.27), we can observe that if the non-inverting amplifier is an ideal amplifier, for A_v = ∞ and R_{out} = 0. The ideal closed-loop gain can be written as $1+(R_2/R_1)$. Since the R_{out} term is not zero in (4.27), it severely affects the closed-loop gain of the amplifier. As we can see in Fig. 4.3.4-2, the output resistance R_{out} can be written as:

$$R_{out} = (g_{m15} r_{o15} r_{o16}) // (g_{m14} r_{o14} r_{o13}) \quad -(4.28)$$

Because the output impedance of the operational transconductance amplifier is high, the OTA must implement a buffer for driving resistive loads. To analyze the output resistance of the buffer, we can use Fig.4.3.4-4 to calculate the value of R_{out}.

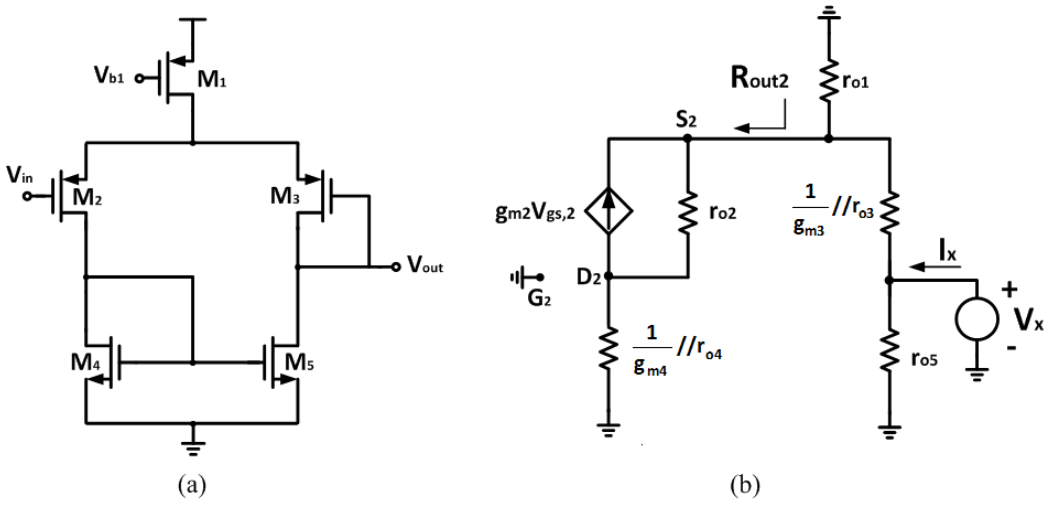


Fig. 4.3.4-4 (a) Buffer (b) Small signal model of the buffer

As Fig. 4.3.4-3(b) illustrates, R_{out} can be expressed by:

$$R_{out} = \frac{V_X}{I_X} = r_{o5} // \left(\frac{1}{g_{m3}} // r_{o3} + r_{o1} // R_{out2} \right) \quad -(4.29)$$

$$R_{out2} = \frac{r_{o2} + \left(\frac{1}{g_{m4}} // r_{o4} \right)}{1 + g_{m2} r_{o2}} \quad -(4.30)$$

In general, r_o is big enough that we can simplify equation (4.29) and (4.30) into:

$$R_{out} = \frac{V_X}{I_X} = r_{o5} // \left(\frac{1}{g_{m3}} // r_{o3} + r_{o1} // \frac{1}{g_{m2}} \right) = r_{o5} // \left(\frac{1}{g_{m3}} + \frac{1}{g_{m2}} \right) = \frac{2}{g_{mp}} \quad -(4.31)$$

$$\text{For} \quad \frac{1}{g_{m2}} = \frac{1}{g_{m3}} = \frac{1}{g_{mp}}$$

Compare the R_{out} value in (4.28) to (4.31), with the implementation of the buffer we can reduce the output resistance to $\frac{2}{g_{mp}}$. Therefore, the resistive feedback can be well defined since R_{out} is small in equation (4.27). Fig. 4.3.4-5 shows the overall programmable gain amplifier that used differential difference operational transconductance amplifier with a buffer stage.

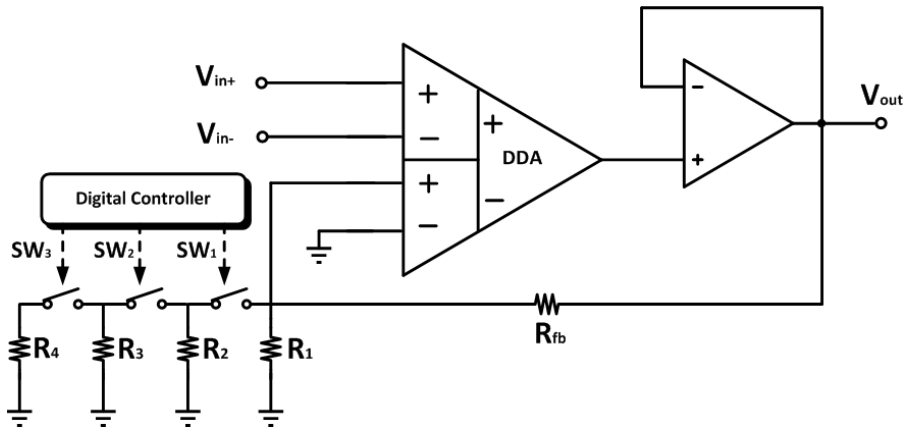


Fig. 4.3.4-5 A differential difference operational transconductance amplifier with a buffer stage to realize a programmable gain amplifier

4.3.5 Clock generator [33]

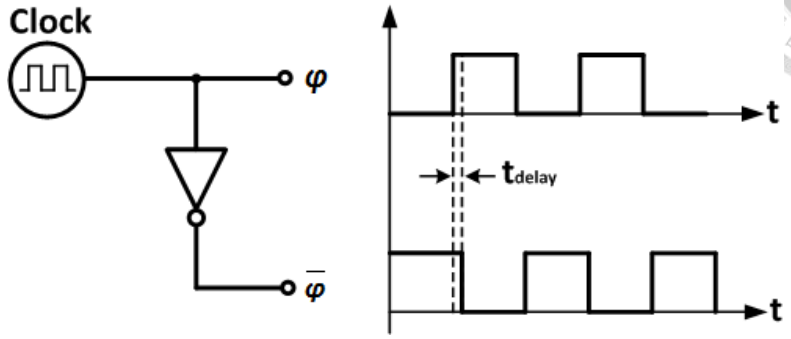


Fig. 4.3.5-1 Problem of clock overlapping

Chopper modulator needs two clock signals that are 180 degree of phase difference. If we just add an inverter to generate another path to obtain ϕ and $\bar{\phi}$, $\bar{\phi}$ may have time delay comparing with the ϕ and results in the problem of clock overlapping, just as Fig. 4.3.5-1 depicts. The problem of clock overlapping may cause chopper modulator malfunction. To prevent it, we use non-overlapping clock generator.

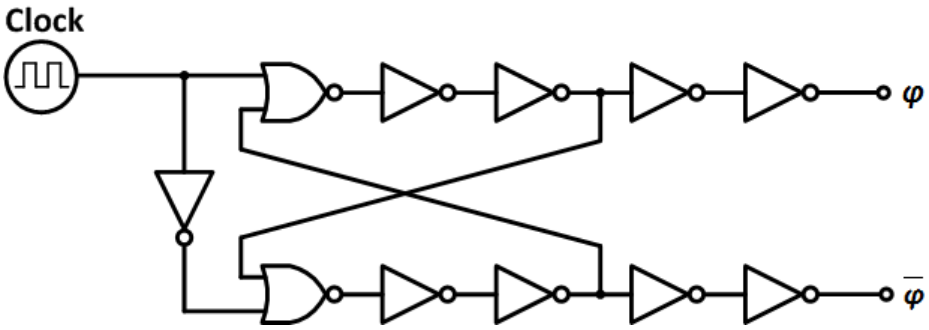


Fig. 4.3.5-2 Non-overlapping clock generator

Fig. 4.3.5-2 shows a non-overlapping clock generator. Non-overlapping clock generator can be used to insure that no signals can propagate through more than one latch at a time. It can synchronize ϕ and $\overline{\phi}$ by latch so that there is no time delay between two clock. Thus, chopper modulator can be correctly operation.

4.4 Simulation

Fig. 4.4-1 shows the AC response simulation result of the CBIA. The f_t is at 70k Hz, the gain is 20dB, and the phase margin is 50°. Fig. 4.4-2 shows the AC response simulation result of the DDA. The f_t is at 50k Hz, the gain is 90dB, and the phase margin is 70°. Fig. 4.4-3 shows the AC response simulation result of the second-order Butterworth low-pass filter. The f_{3dB} is about 650Hz, and the gain is 0. The overall CBIA with PGA simulation result is shown in Fig. 4.4-4 with the gain of 36dB, 42dB, 48dB, and 54dB. The simulation result of the CMRR is about 86dB in this AFE system, as shown in Fig. 4.4-5. The simulation result of the PSRR is about 75dB in this AFE system, as shown in Fig. 4.4-6. The overall AFE system only consumes 6uA with 1V supply voltage (V_{DD}).

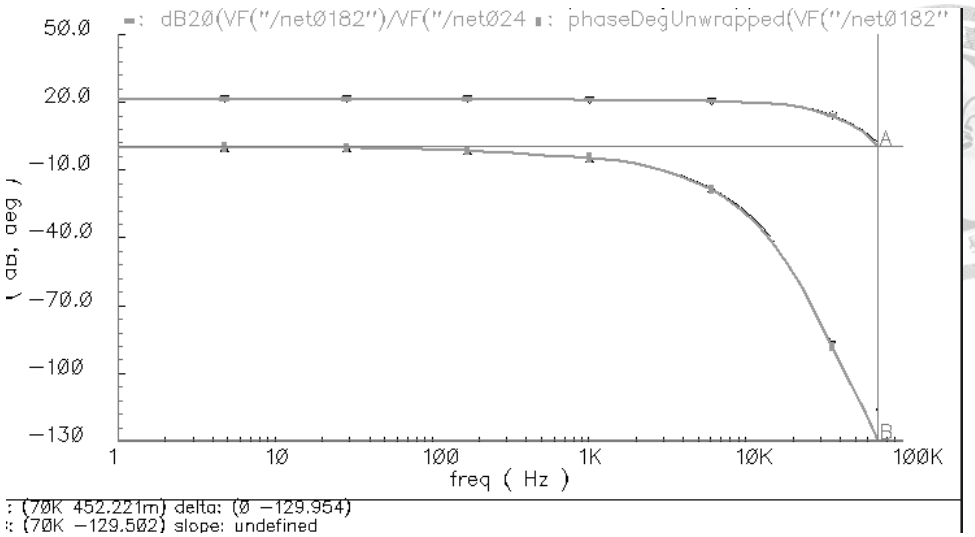


Fig. 4.4-1 AC response simulation of CBIA

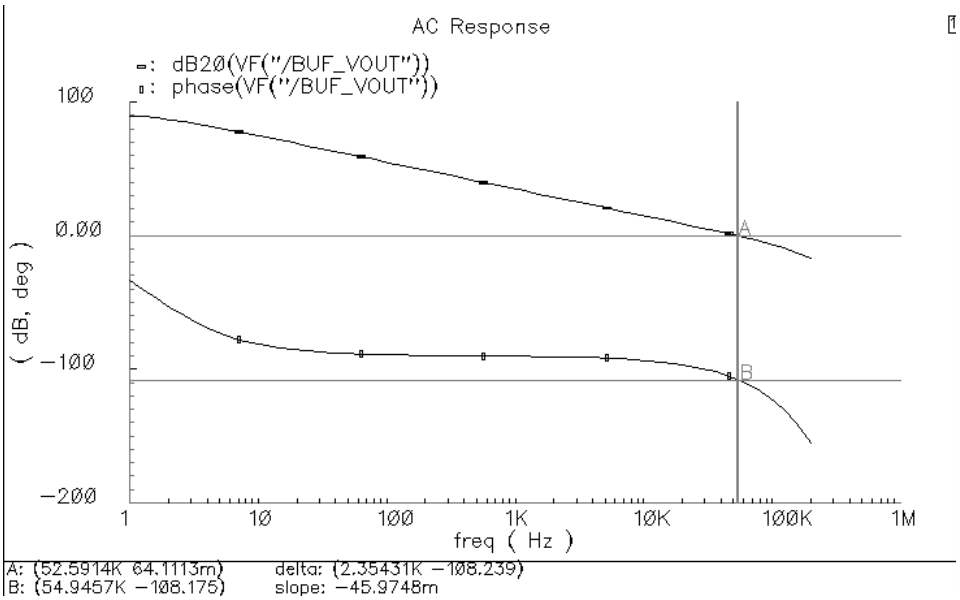


Fig. 4.4-2 AC response simulation of DDA

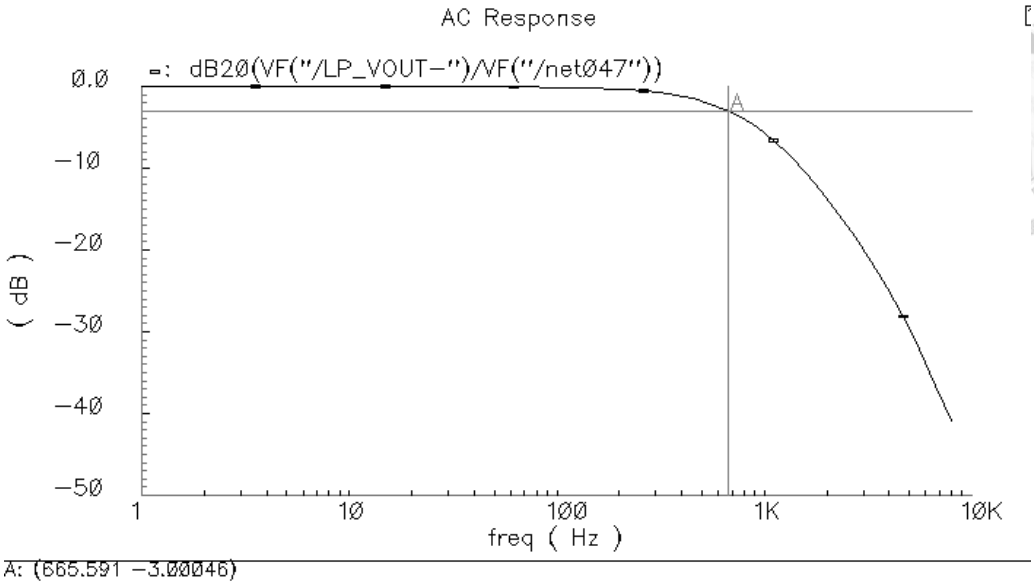


Fig. 4.4-3 AC response simulation of Low-pass filter

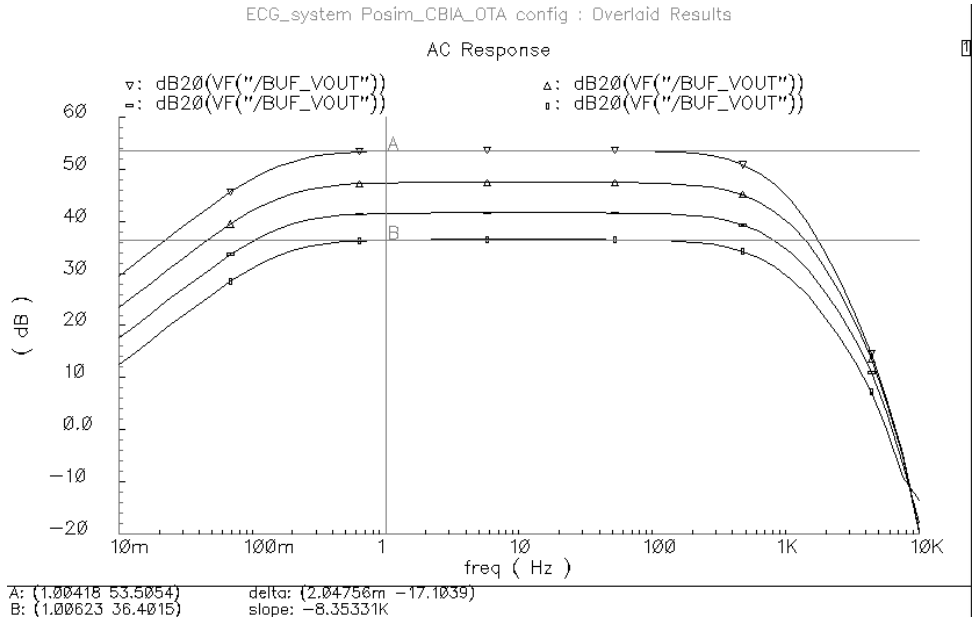


Fig. 4.4-4 AC response simulation of CBIA with PGA

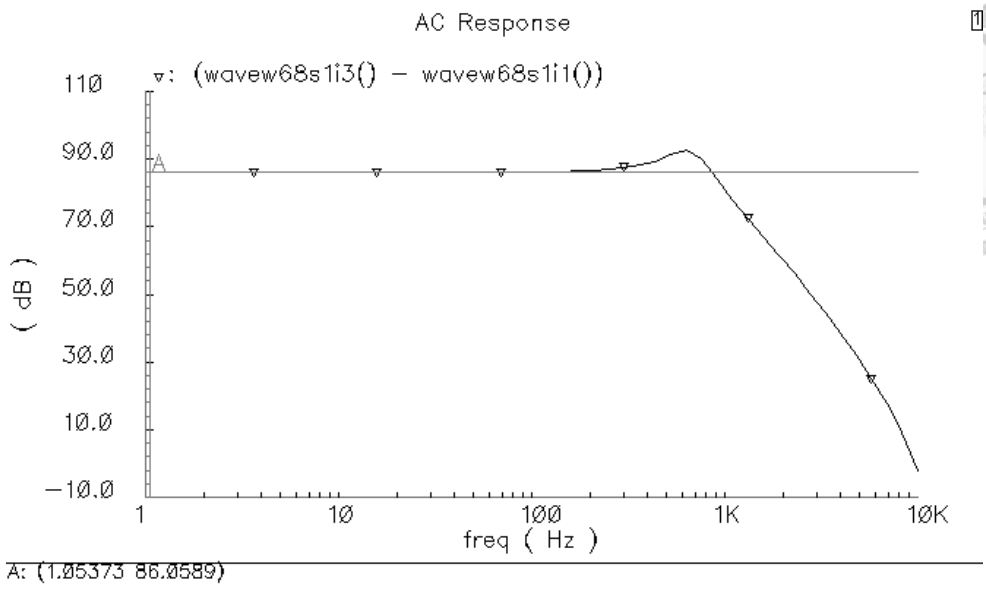


Fig. 4.4-5 CMRR Simulation of CBIA with PGA

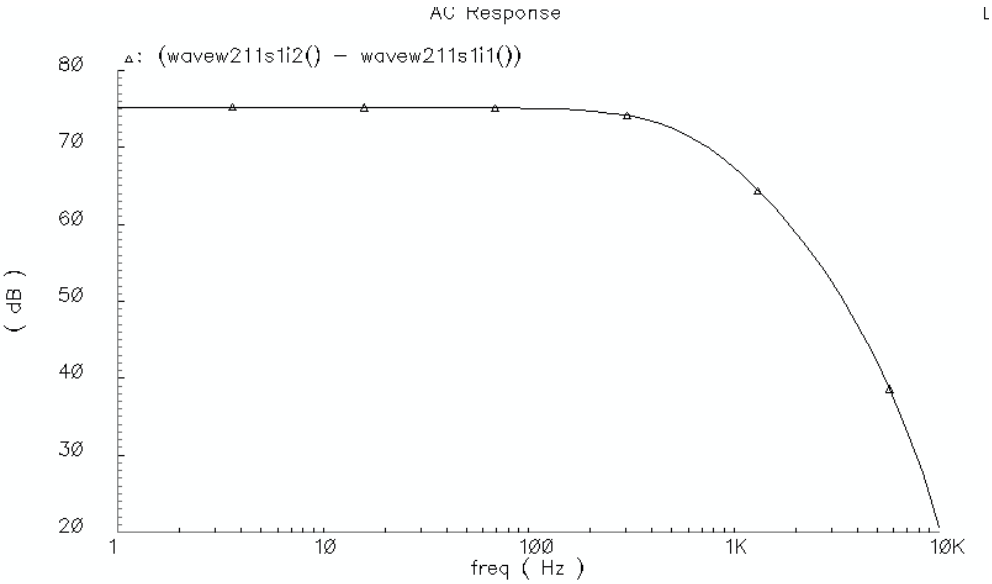


Fig. 4.4-6 PSRR Simulation of CBIA with PGA

Fig. 4.4-7 shows the input-referred-noise simulation result of the CBIA. From this figure we can observe that flicker noise is quite a large non-ideal effect at the baseband. As we know, chopper modulation is a low-noise technique that would modulate the noise to the chopping frequency f_c. In order to efficiently reduce the flicker noise with chopper technique, the chopping frequency should be larger than 1/f noise corner. Here we choose chopping frequency f_c = 10k Hz. Fig. 4.4-8 shows that the noise will be chopped to 10k Hz. Fig. 4.4-9 shows the noise simulation result after the noise is removed by the low-pass filter. Compare with Fig. 4.4-7, the noise at the baseband has been reduced due to the chopper technique.

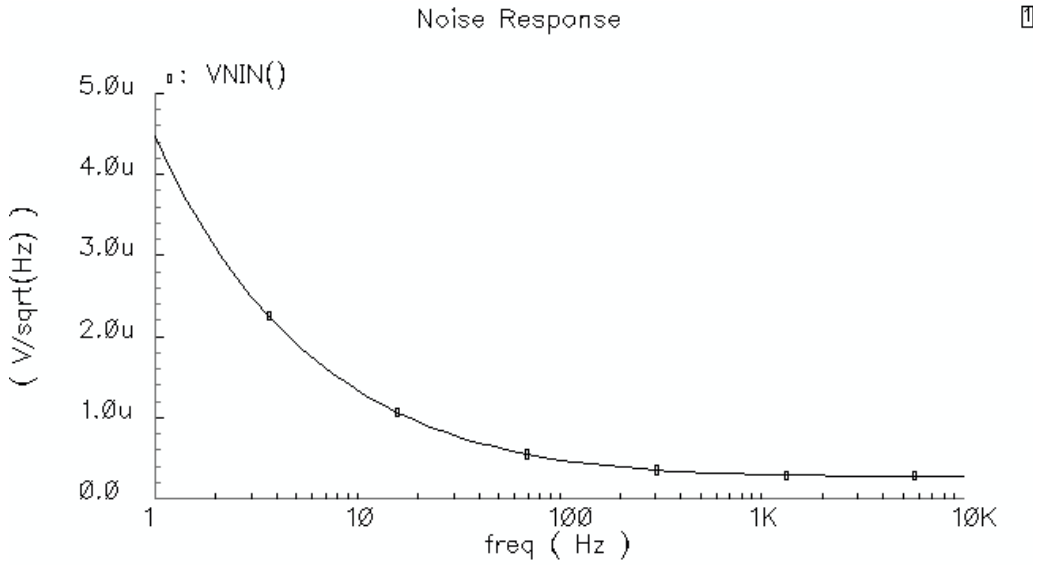


Fig. 4.4-7 Noise response simulation of CBIA

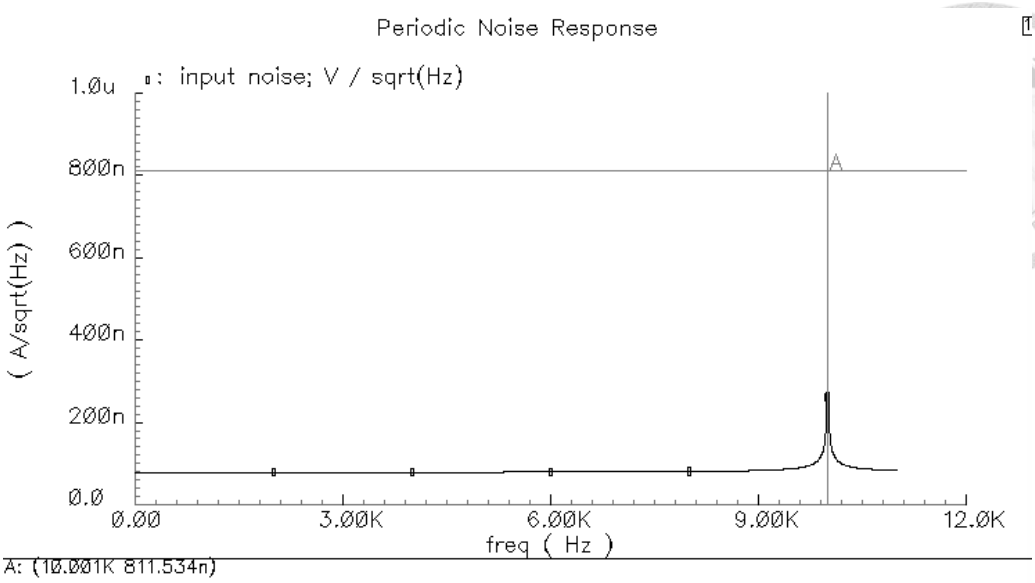


Fig. 4.4-8 Noise response simulation of CBIA with chopper modulation

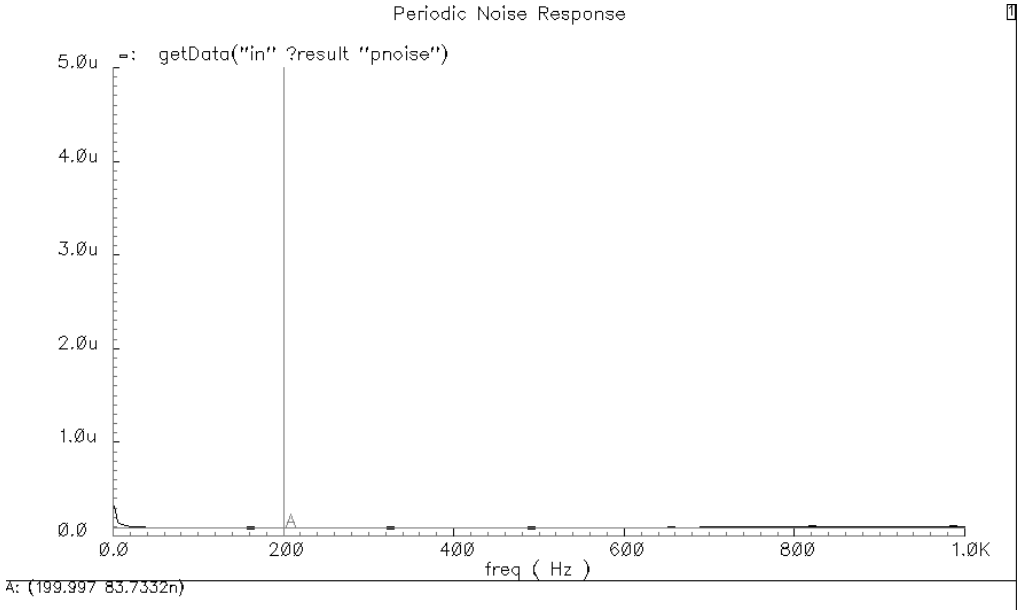


Fig. 4.4-9 Noise response simulation at the output of LPF

Fig. 4.4-10 to Fig. 4.4-13 illustrates the chopper modulation technique in time domain. Fig. 4.4-10 shows the transient response simulation at input modulation. The red line is the input sine wave signal, and the black line is the modulation signal with the chopping frequency 10k Hz. After amplifying by the CBIA, the amplified signal is as the red line that shown in Fig. 4.4-11. Follow with the demodulation, the signal will be modulated back to the baseband. The black line in Fig. 4.4-11 shows the demodulated signal, and its partial enlarged detail is shown in Fig. 4.4-12. We can observe that the waveform includes lots of chopper ripples. With the low-pass filter, the chopper ripples will be removed and the simulation result is shown in Fig. 4.4-13. The red line shows the signal waveform at the output of low-pass filter, and the black line show the signal waveform at the output of PGA.

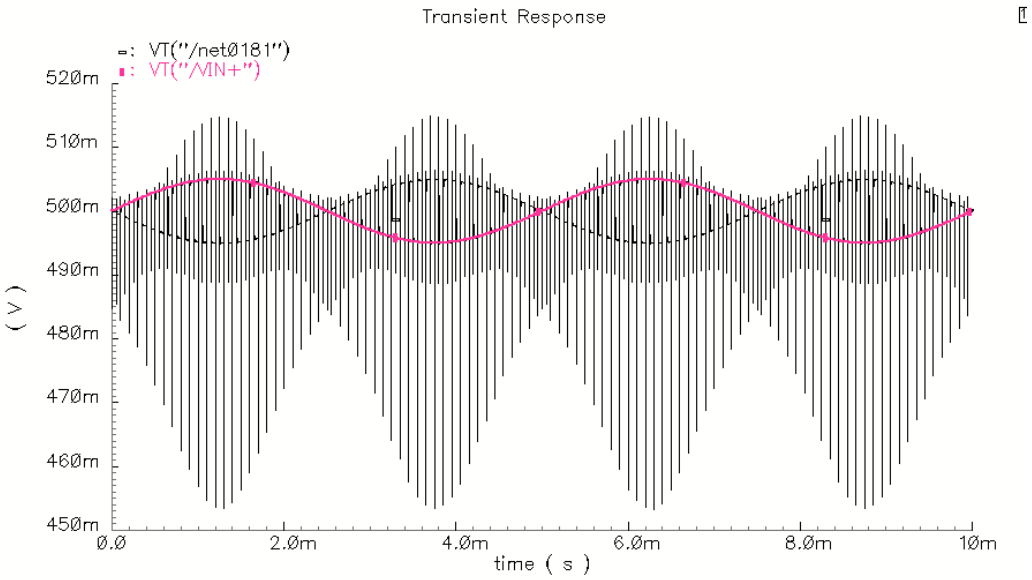


Fig. 4.4-10 Transient response simulation at the input modulation

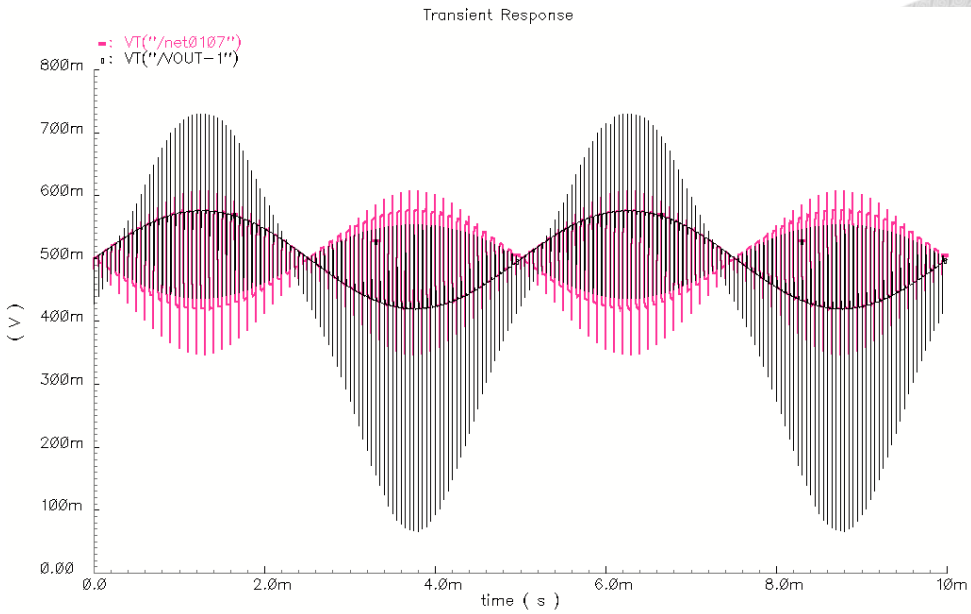


Fig. 4.4-11 Transient response simulation at the output modulation

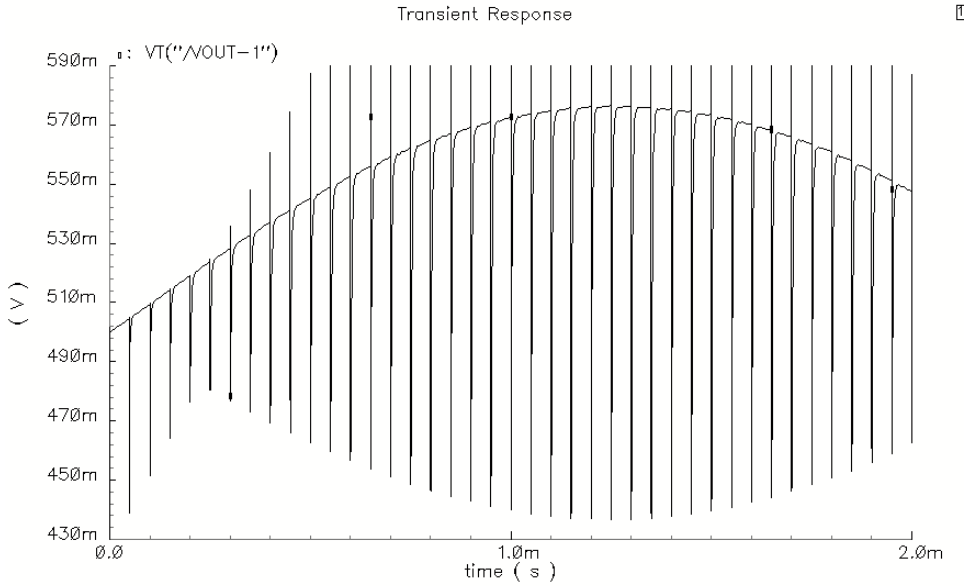


Fig. 4.4-12 Transient response simulation at the output modulation

(Partial enlarged detail)

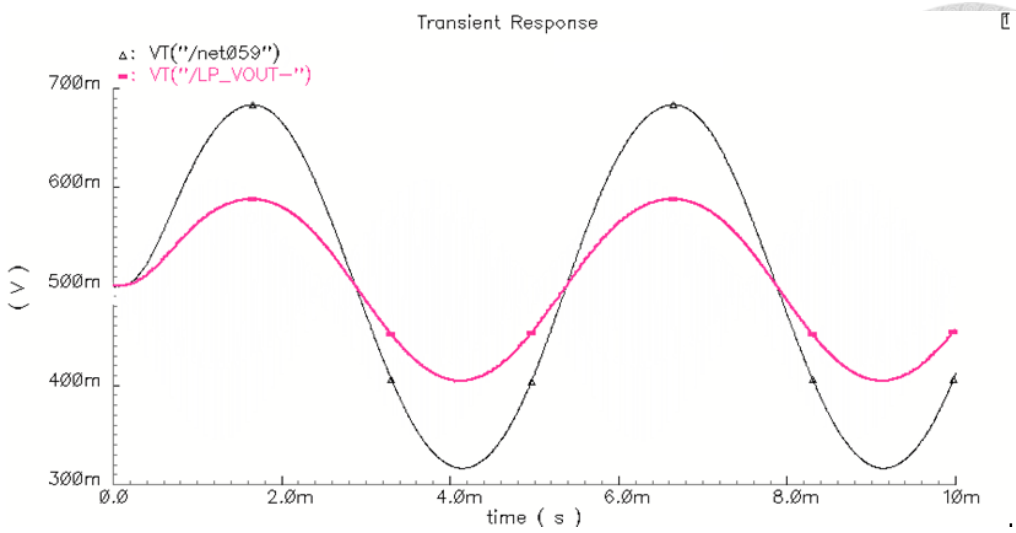


Fig. 4.4-13 Transient response simulation at the output of LPF, and the output of PGA

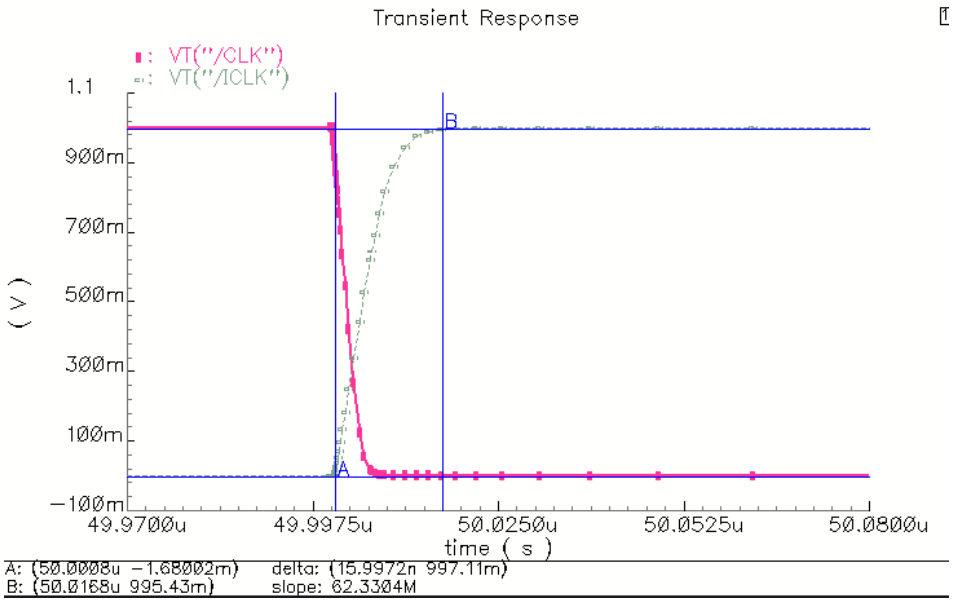


Fig. 4.4-14 Transient response simulation of non-overlapping clock

Fig. 4.4-14 shows the transient response simulation of non-overlapping clock. In this figure we can observe that the transition between two clocks will be synchronized. Table 4.4-1 shows the simulation results of this work.

Table 4.4-1 Summary of simulation result

Features	Performance
Power supply	1V
Power	6uW
Chopper frequency	10k Hz
Programmable gain selection	36dB, 42dB, 48dB, 54dB
3dB frequency	650Hz
Input-referred noise density	83.7nV/$\sqrt{Hz}$
CMRR	86dB
PSRR	75dB

4.5 Layout

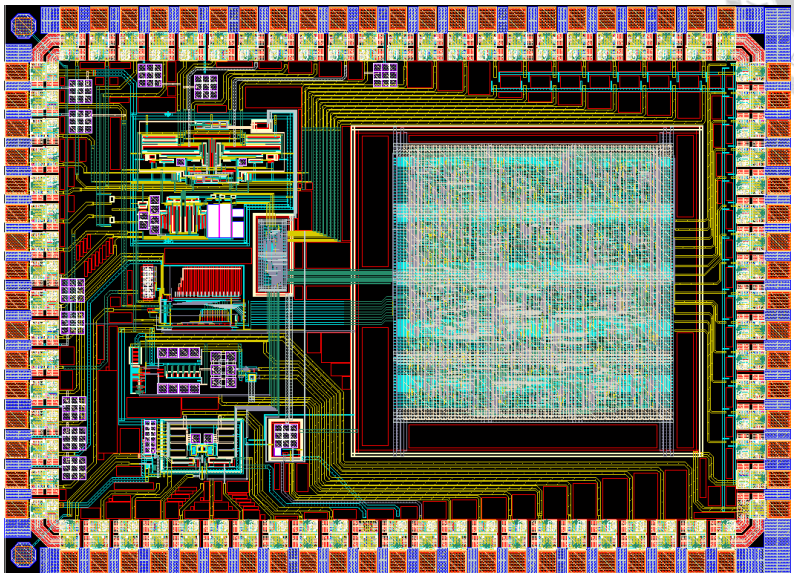


Fig. 4.5-1 Layout of ECG monitoring system (Ver.1)

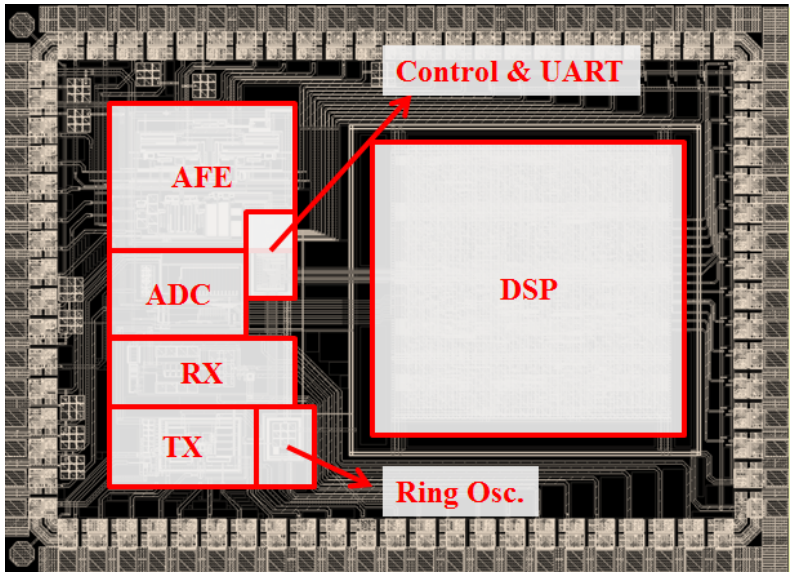


Fig. 4.5-2 Layout floor plain of ECG monitoring system (Ver.1)

Fig. 4.5-1 and Fig. 4.5-2 show the layout and the layout floor plain of the ECG monitoring system. The analog-front end is integrated in this system.

4.6 Measurement

4.6.1 Die photo and PCB design

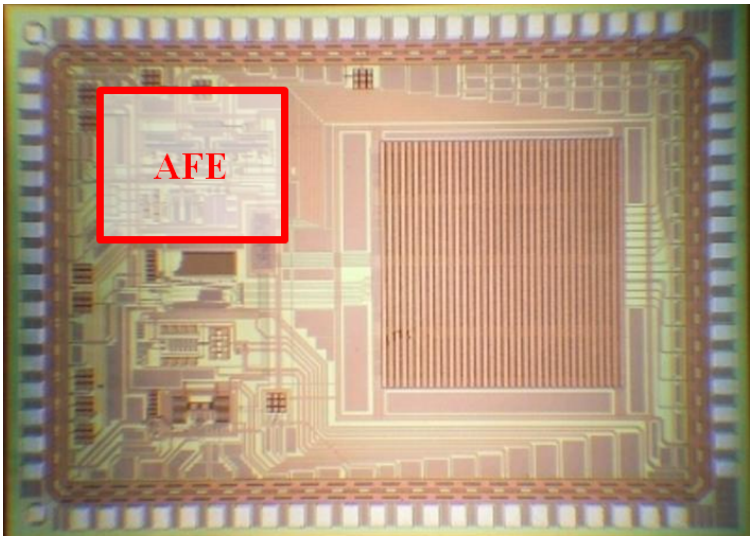


Fig. 4.6.1-1 Die photo of ECG monitoring system (Ver.1)

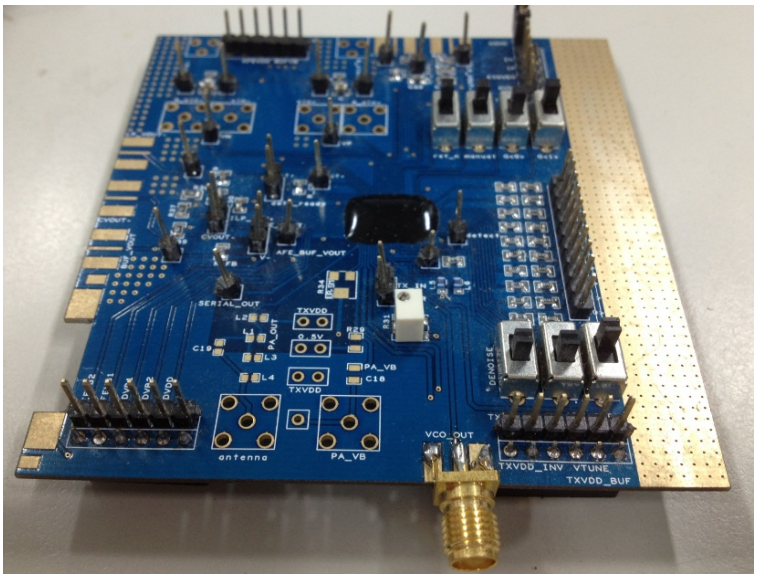


Fig. 4.6.1-2 PCB design of ECG monitoring system (Ver.1)

The die photograph and corresponding PCB design of the ECG monitoring system chip are shown in Fig. 4.6.1-1 and Fig. 4.6.1-2.

4.6.2 Measurement setup

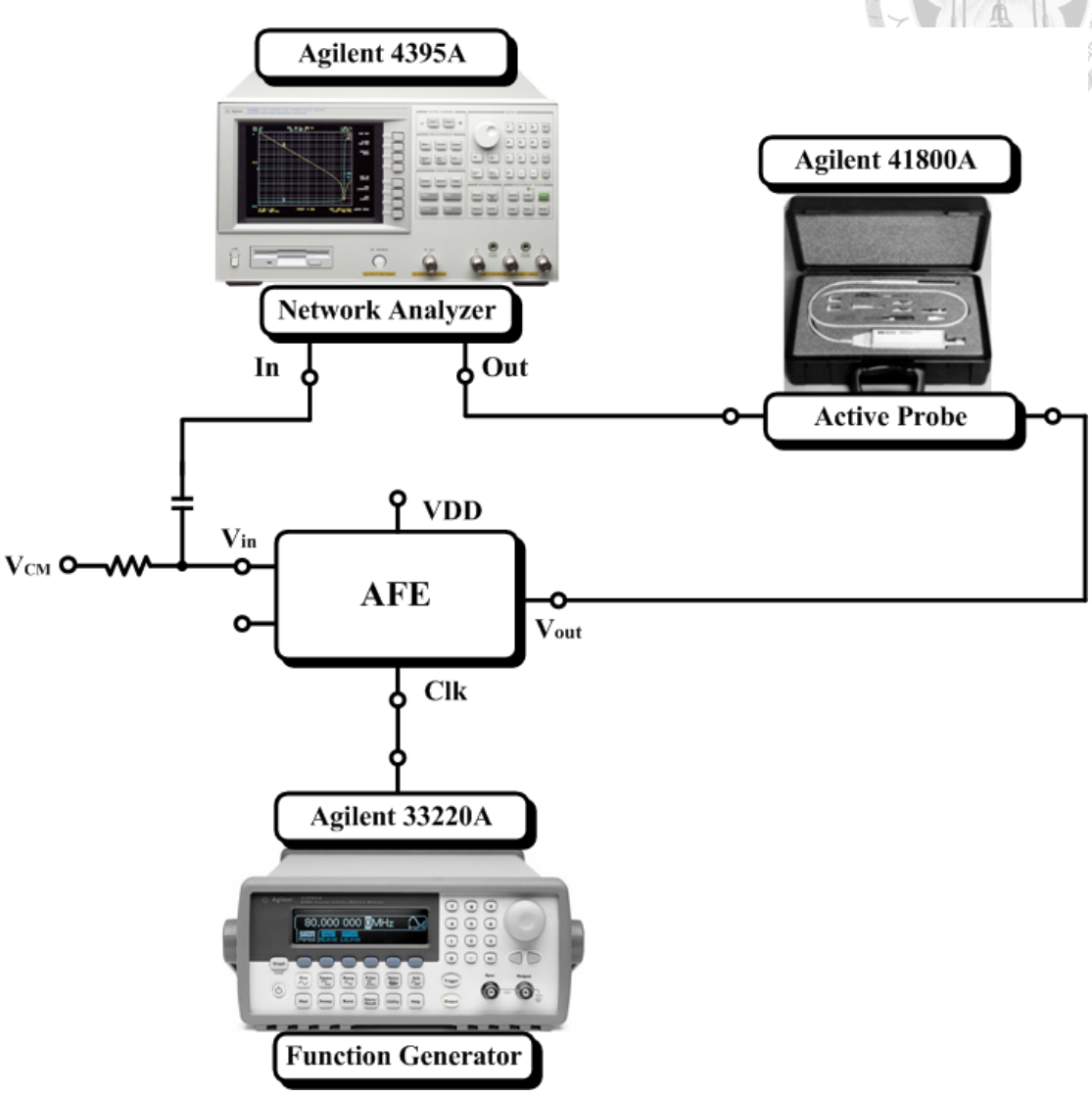


Fig. 4.6.2-1 AC response measurement setup

Fig. 4.6.2-1 shows the AC response measurement setup of AFE. The equipment of Agilent 4395A has three analysis types: network analyzer, spectrum analyzer, and impedance analyzer. In order to measure AC response, network analyzer type is used. At first, Agilent 4395A would export a signal to AFE. Then Agilent 4395A analyzes the output signal of AFE and generates the AC response measurement result of AFE. In addition, the Agilent 41800A-active probe connects the output of AFE and the

analyze probe of Agilent 4395A. It provides high impedance of 1MΩ for preventing the loading effect. Agilent 3320A Function generator provides clock for chopping.

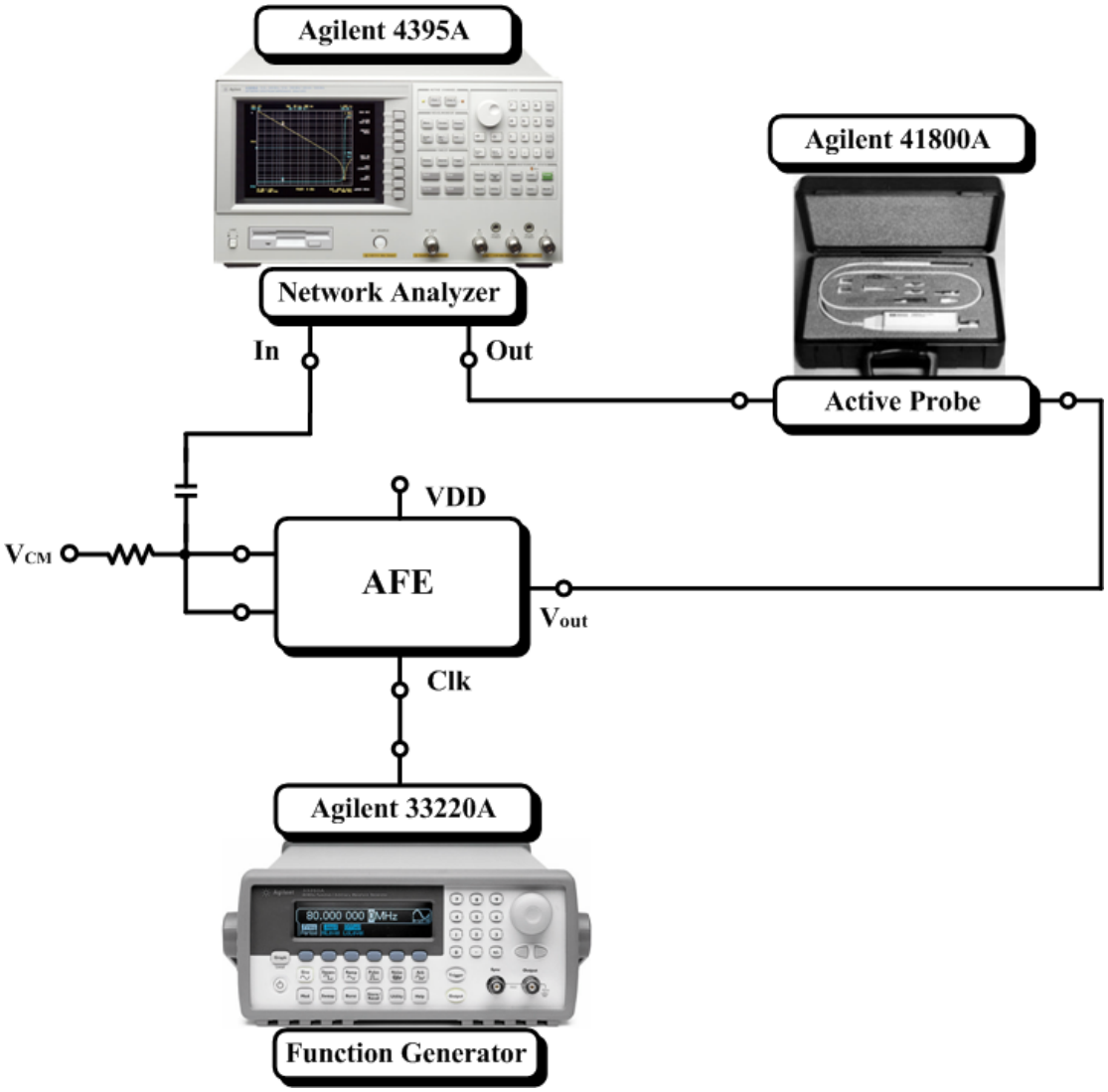


Fig. 4.6.2-2 Noise and A_{cm} measurement setup

Fig. 4.6.2-2 shows the noise and A_{cm} measurement setup of AFE. The equipment of Agilent 4395A has three analysis types: network analyzer, spectrum analyzer, and impedance analyzer. In order to measure noise, spectrum analyzer type is used. At first, power supply provides constant voltages of V_{CM} and VDD. Then Agilent 4395A

would export a signal to AFE and analyzes the output noise of AFE. In addition, the Agilent 41800A-active probe connects the output of AFE and the analyze probe of Agilent 4395A. Agilent 3320A Function generator provides clock for chopping.

The same measurement setup can be used to measure the A_{cm}. However, we should choose network analyzer type this time. After obtaining A_{cm}, we can know the CMRR value by this equation: CMRR= A_d/A_{cm}.

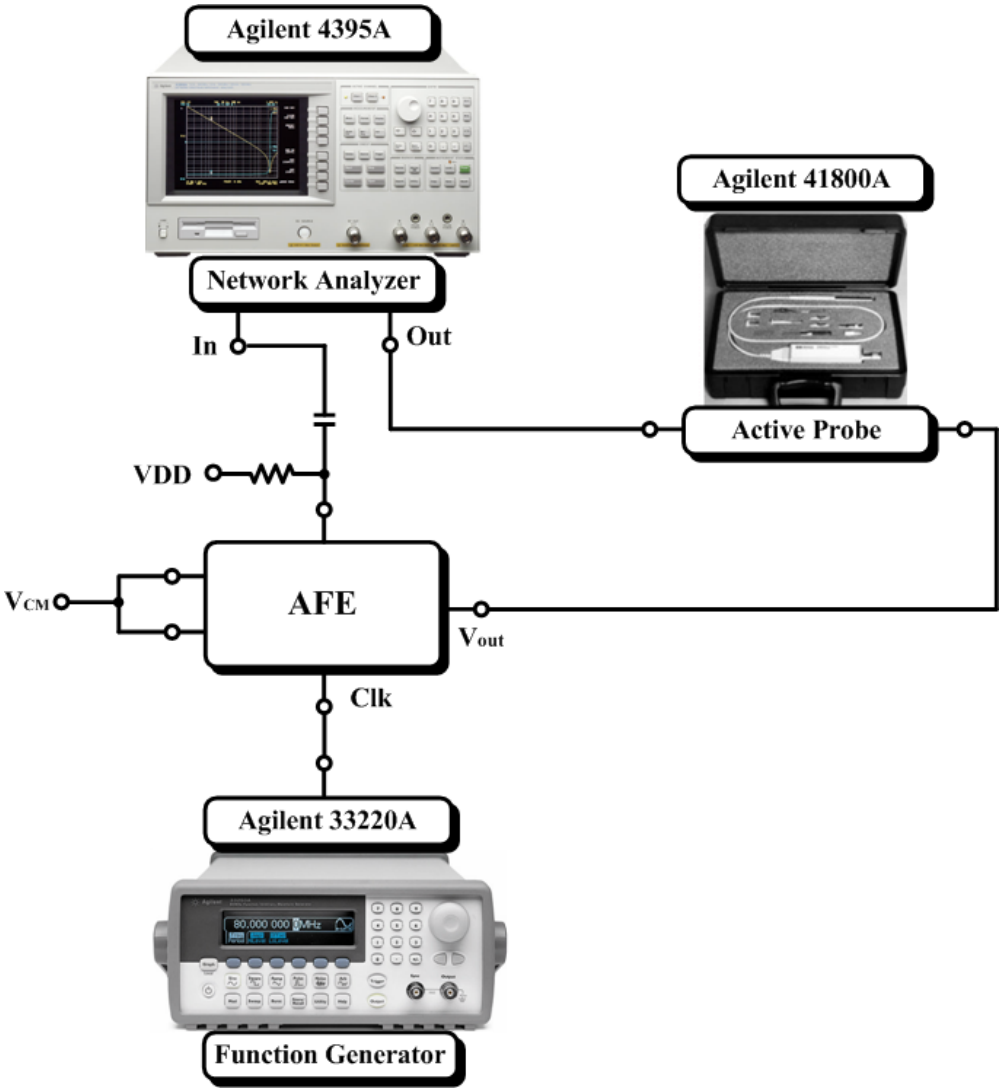


Fig. 4.6.2-3 PSRR measurement setup

Fig. 4.6.2-3 shows the PSRR measurement setup of AFE. The equipment of Agilent 4395A has three analysis types: network analyzer, spectrum analyzer, and impedance analyzer. In order to obtain PSRR, network analyzer type is used. At first, power supply provides constant voltages of V_{CM} and VDD. Then Agilent 4395A would export a signal to the VDD of AFE and analyzes the output of AFE. In addition, the Agilent 41800A-active probe connects the output of AFE and the analyze probe of Agilent 3320A Function generator provides clock for chopping. In this way, we can measure the A_{d-}. Then the PSRR value can be obtained by this equation: PSRR= A_d/A_{d-}.

4.6.3 Measurement result

Fig. 4.6.3-1(a), (b), (c), and (d) depict the AC response measurement result of the AFE, respectively. Fig. 4.6.3-2 depicts all the gain selection measurement result of the AFE in a picture. The gains are 35.3dB, 41.1dB, 47.8dB, and 53.3dB. The bandwidth of the AFE is about 450Hz. The CMRR and PSRR measurement result are depict in Fig. 4.6.3-3 and Fig. 4.6.3-4. It shows that CMRR > 85dB, and PSRR > 70dB. Fig. 4.6.3-5 shows the DC gain of the AFE. We can see that the output swing of the AFE is from 0.15V to 0.75V.

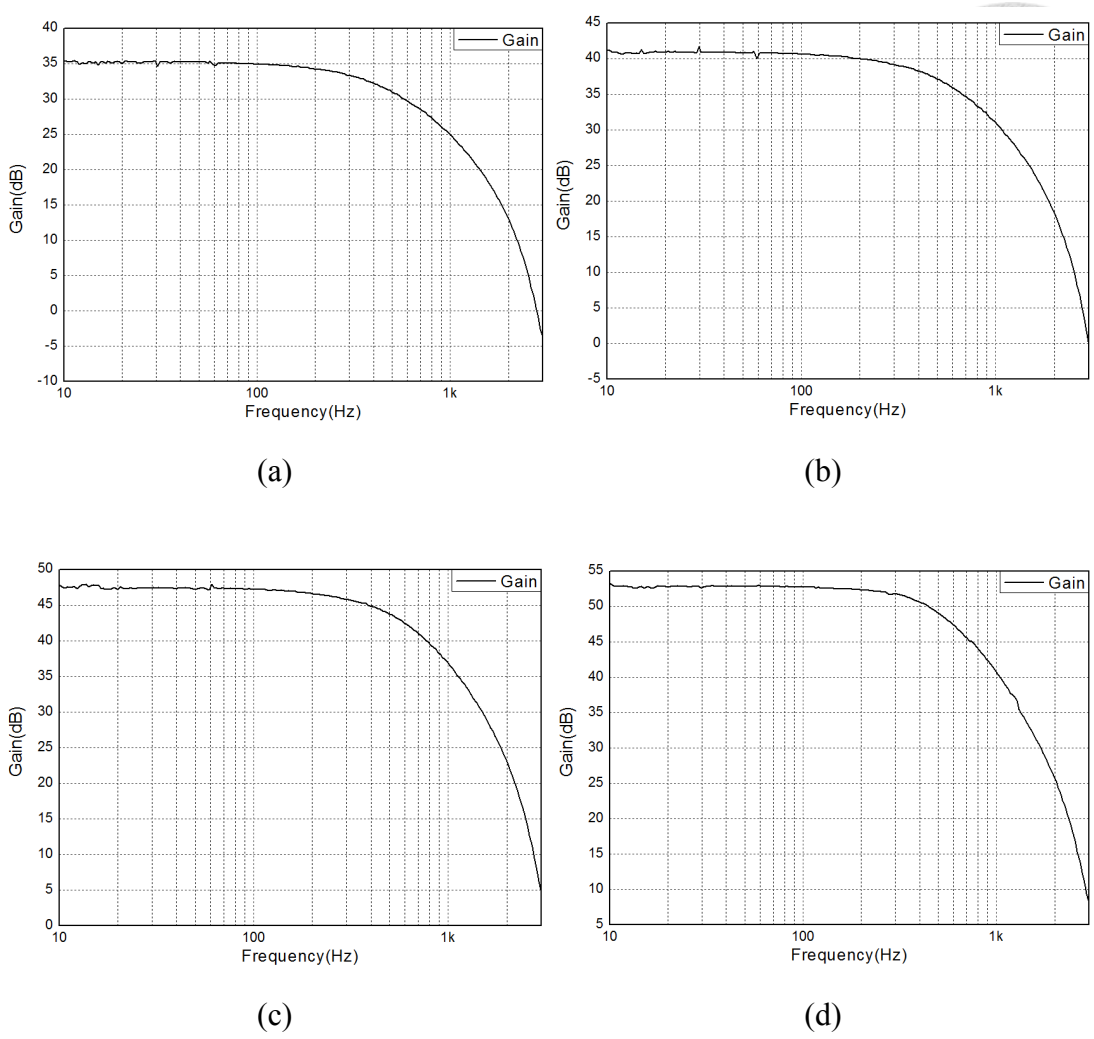


Fig. 4.6.3-1(a)(b)(c)(d) AC response measurement result of the AFE

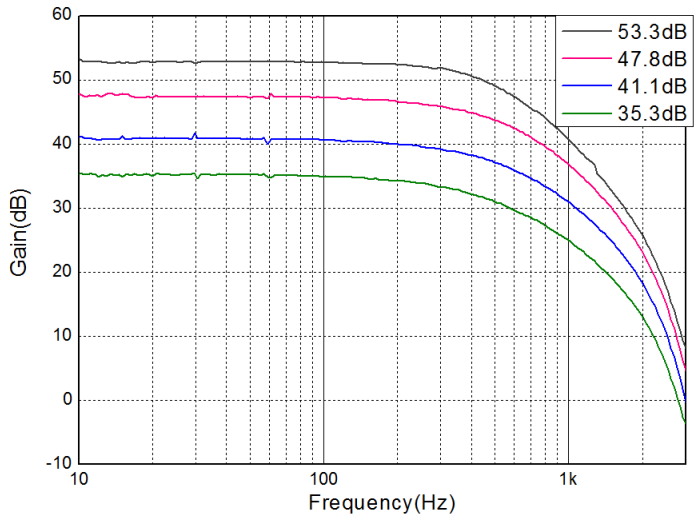


Fig. 4.6.3-2 AC response measurement result of the AFE

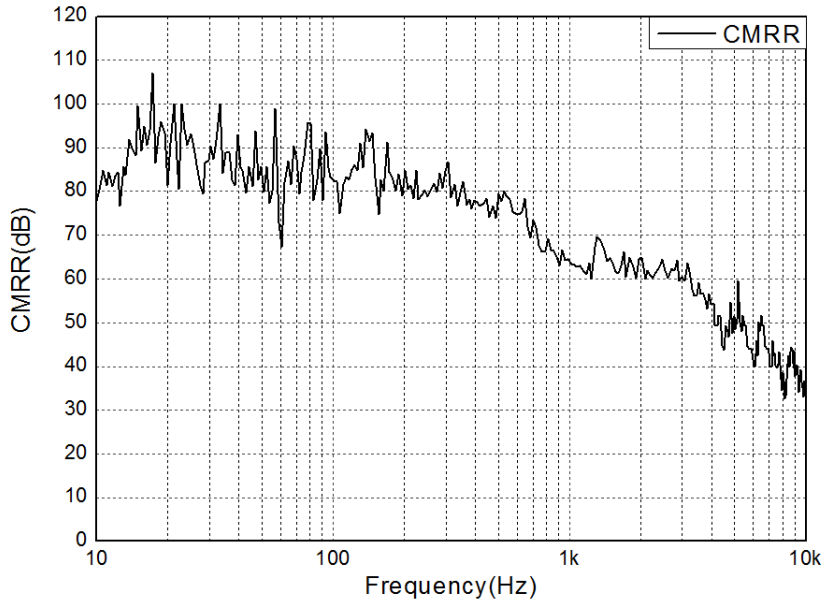


Fig. 4.6.3-3 CMRR measurement result of the AFE

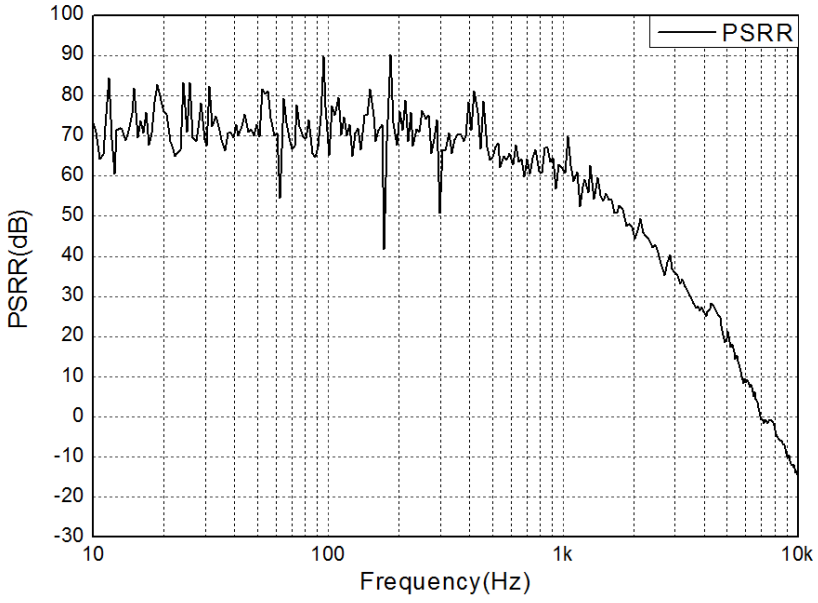


Fig. 4.6.3-4 PSRR measurement result of the AFE

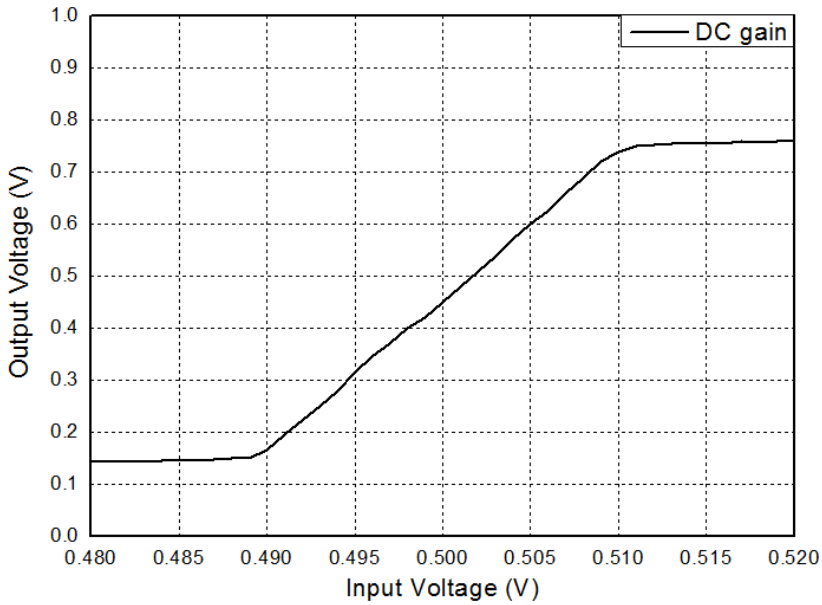


Fig. 4.6.3-5 DC gain of the AFE

The measurement results of the input-referred noise spectrum are shown from Fig.4.6.3-6 to Fig.4.6.3-12. Fig. 4.6.3-6 shows the input-referred noise spectrum of the CBIA in log scale. We can see that with chopper technique, the flicker noise which is close to the baseband has been reduced. To see this figure in detail, we can examine Fig.4.6.3-7 and Fig.4.6.3-8, which depict the input-referred noise in log scale and linear scale, respectively. From these two pictures, it is obvious to know that the input-referred noise has been reduced to about 90 nV/$\sqrt{Hz}$. Fig. 4.6.3-9 shows that before the signal enters the low pass filter, the noise will be chopped to the chopping frequency, which is 9.6 KHz here. Since the critical ECG signal bandwidth is located between 1Hz and 200Hz, we care about the input-referred noise in this bandwidth. Fig. 4.6.3-10 shows the input-referred noise spectrum of the CBIA in this bandwidth. The peak at 60Hz is the power line interference.

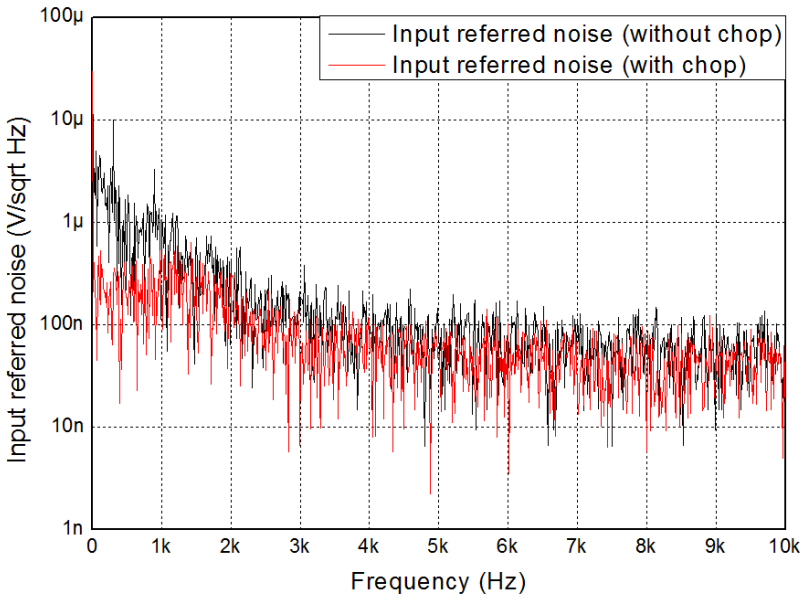


Fig. 4.6.3-6 Input-referred noise spectrum of the CBIA in log scale

(with and without chopper technique)

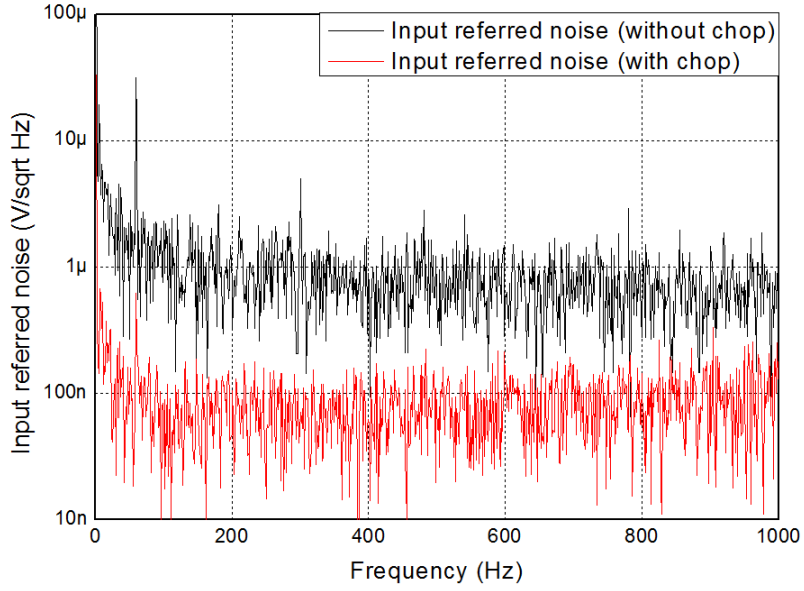


Fig. 4.6.3-7 Input-referred noise spectrum of the CBIA in log scale

(with and without chopper technique)

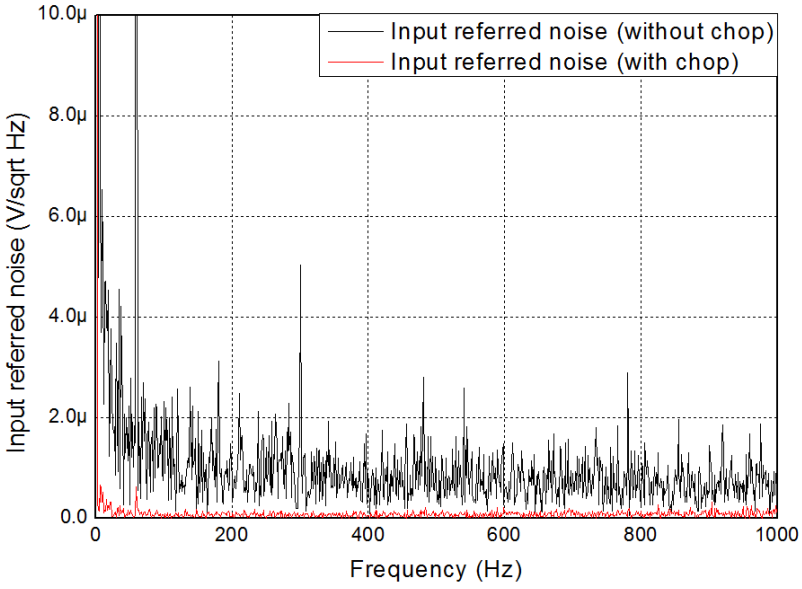


Fig. 4.6.3-8 Input-referred noise spectrum of the CBIA in linear scale

(with and without chopper technique)

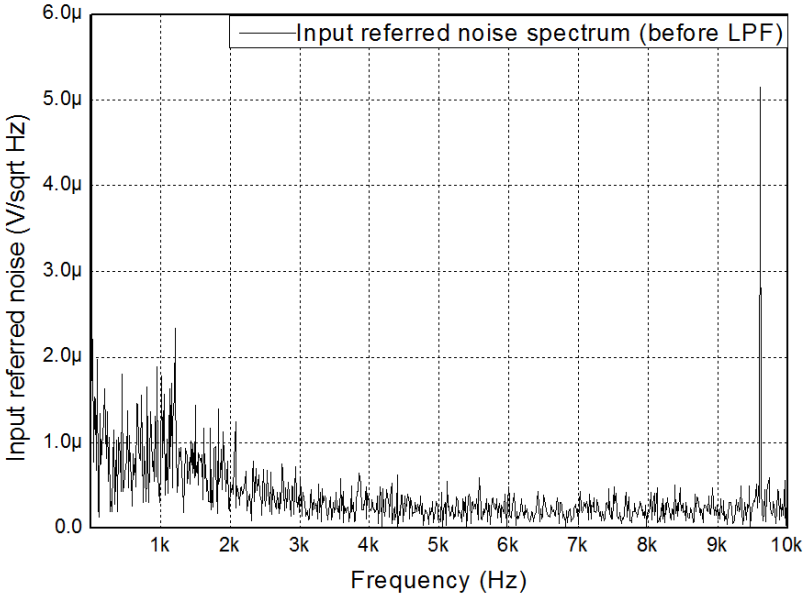


Fig. 4.6.3-9 Input-referred noise spectrum of the CBIA (before LPF)

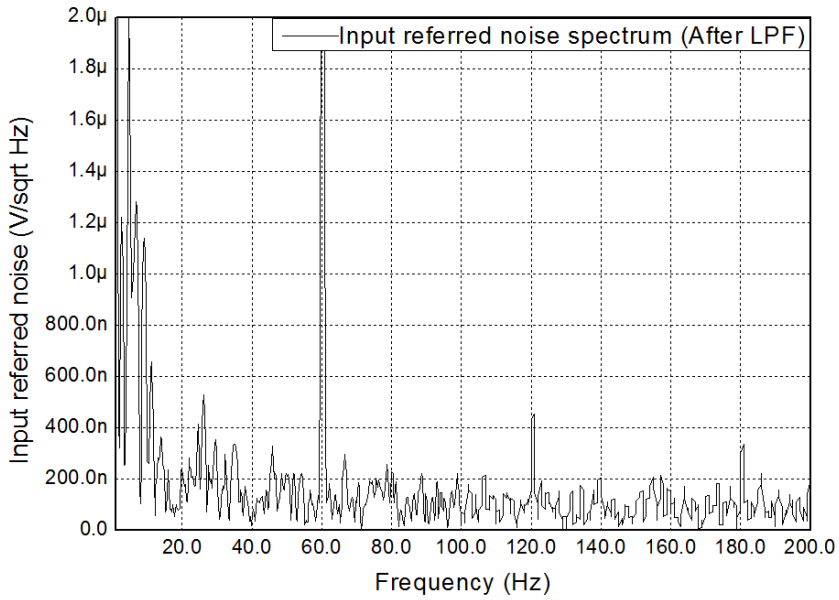


Fig. 4.6.3-10 Input-referred noise spectrum of the CBIA (after LPF)

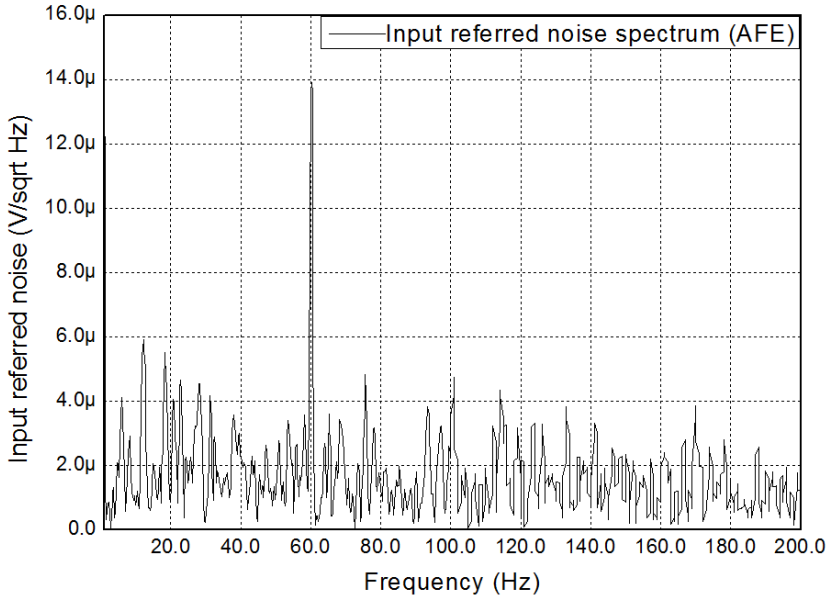


Fig. 4.6.3-11 Input-referred noise spectrum of the AFE (after PGA)

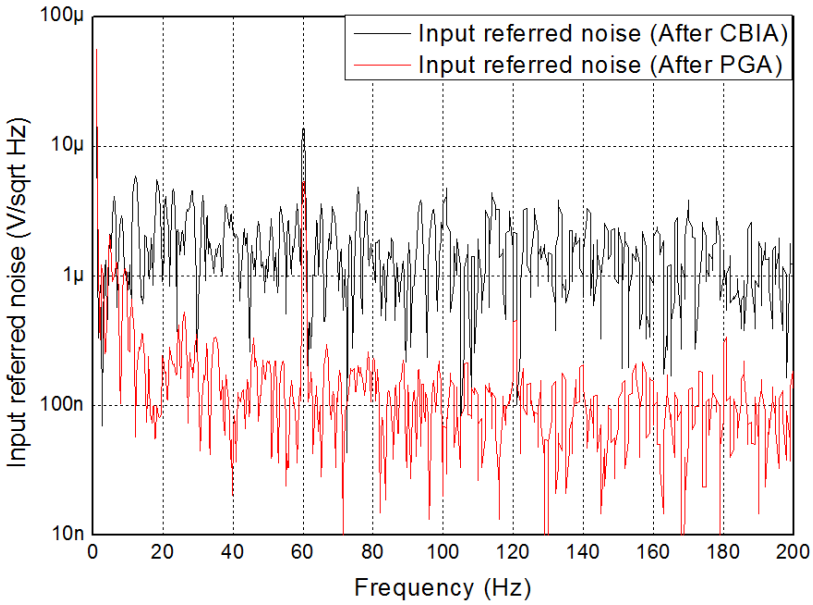


Fig. 4.6.3-12 Input-referred noise spectrum comparison of the AFE (after PGA) and CBIA (after LPF)

The measurement result of the input-referred noise spectrum of the AFE (CBIA with PGA) is shown in Fig.4.6.3-11. The input-referred noise density of the AFE compares with the CBIA is shown in Fig. 4.6.3-12. The input-referred noise density of the AFE is about 1uV/$\sqrt{Hz}$. The ECG signal measurement result is depicted in Fig. 4.6.3-13. The signal source is from a real person's heart and the measurement lead is Lead II.

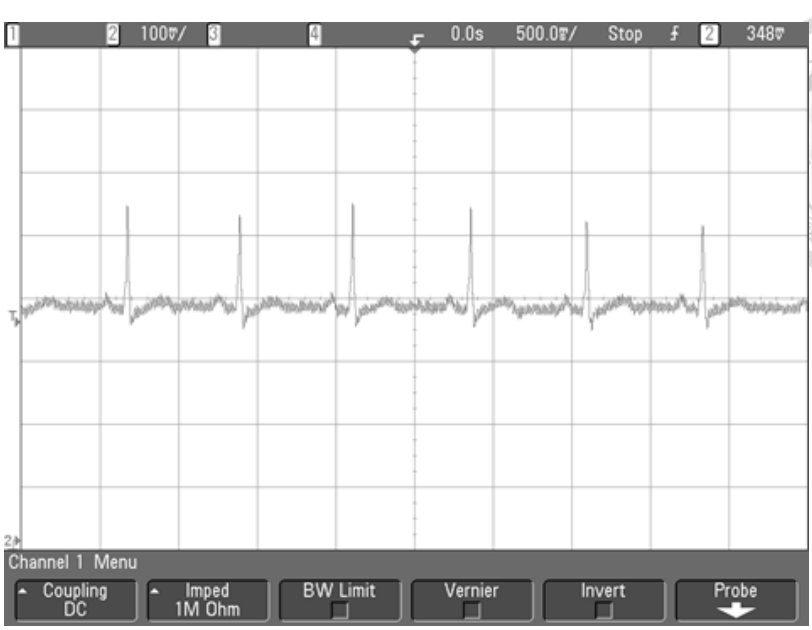


Fig. 4.6.3-13 ECG signal measurement result

4.6 Summary

A biomedical analog front-end is presented and fabricated in TSMC 0.18μm 1P6M CMOS process. With the implementation of chopper techniques, low frequency noise such as flicker noise and dc input-referred noise is dramatic decrease. A second-order low pass filter inserted in the back of current feedback instrumentation amplifier filters the chopping spike. Besides, the programmable gain amplifier provides four different gain selections to meet the requirement for ECG signal detecting. Table 4.6-1 shows the measured results of this work

Table 4.6-1 Summary of measurement result

Features		**Performance**
Power supply		1V
Power		6uW
Chopper frequency		9.6k Hz
Programmable gain selection		35.3dB, 41.1dB, 47.8dB, 53.3dB
Output swing		0.15V~0.75V
3dB frequency		450Hz
Input-referred noise density	CBIA	90nV/$\sqrt{Hz}$
	AFE	1uV/$\sqrt{Hz}$
CMRR		>85dB
PSRR		>70dB

Chapter 5

An ECG Signal Monitoring Analog Front-End with Pulse-Width Modulation Circuit

5.1 Introduction

In the analog front-end for ECG signal monitoring, the amplifier is the core building block. In order to lower the noise effect and the power dissipation, we should avoid using too many transistors in analog front-end design. Thus, in this chapter, we combine the instrumentation amplifier with chopper technique and programmable gain amplifier together so that the ECG signal would not pass through many stages of the amplifier. Besides, in order to improve the output swing of the analog front-end, we abandon the fully differential structure so that the amplifier does not need CMFB circuit, which may limits the output swing since the output of the amplifier would see

a voltage V_{GS} from the input of the CMFB circuit. Moreover, a rail-to-rail input structure is also adopted in the unity gain low pass filter to increase the input common-mode range of the filter. The analog front-end includes a pair of high pass filter (HPF) at the front, a differential difference amplifier corporates with chopper technique and programmable gain, and a low pass filter.

After the analog front-end, we implement a pulse-width modulation (PWM) circuit as an interface between analog front-end (AFE) and digital signal processing circuit (DSP). Both simulation result and measurement result about the AFE and PWM circuit are provided in this chapter to show that the performance of the circuit is good enough to detect ECG signals.

5.2 Circuits Architecture

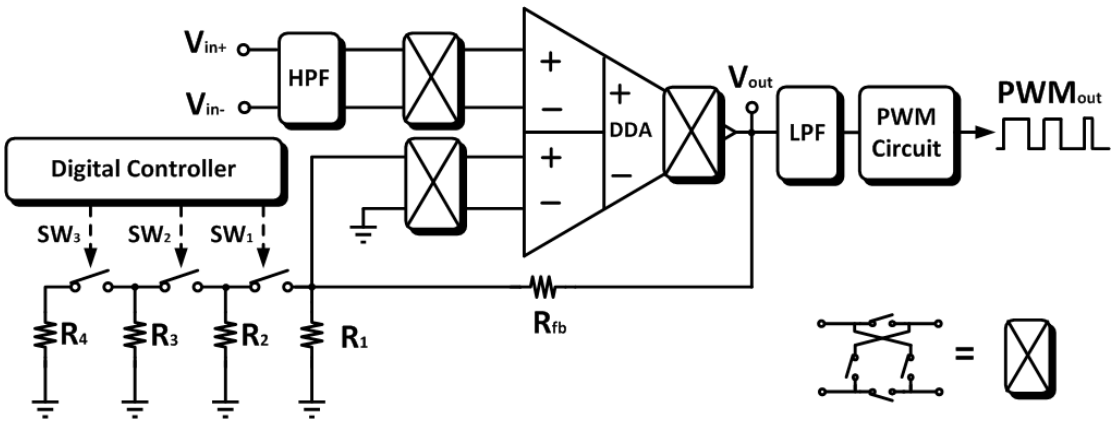


Fig. 5.2-1 Architecture of the AFE with PWM circuit

Fig. 5.2-1 represents the architecture of the analog front-end (AFE) with pulse-width modulation (PWM) circuit. The proposed analog front-end consists of a pair of high pass filter, a programmable gain differential difference amplifier with chopper technique, and a low pass filter. A digital controller is also inserted to support flexible configuration for various magnitude of ECG signals. The programmable gain of analog front-end ranges from 30dB to 50dB. The proposed analog front-end utilizes a simple architecture that capable of dealing with the ECG signals only by an amplifier and a low pass filter.

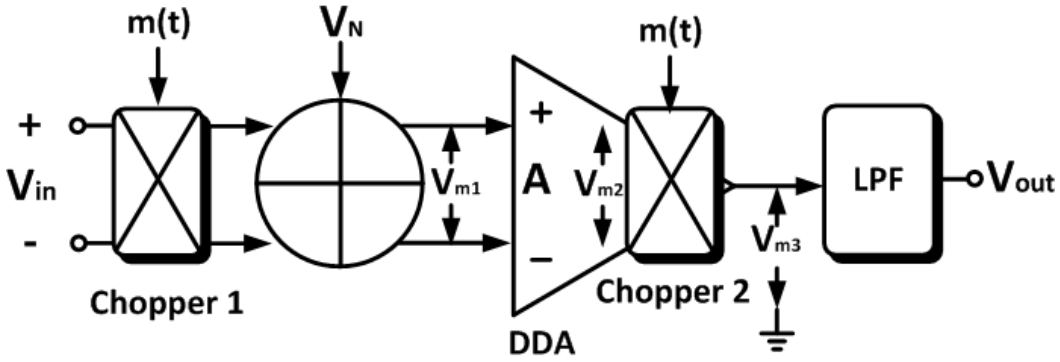


Fig. 5.2-2 Concept of the analog front-end with chopper technique

Chopper technique is used to lower the noise effect in this circuit. We can use Fig. 5.2-2 to analyze the signal and noise of the analog front-end with chopper technique. The differential ECG signal is modulated by chopper switch (Chopper 1) and the modulated signal at the input pair can be written as:

$$V_{m1} = V_{in} m(t) + V_N \quad -(5.1)$$

Just like we have introduced in Chapter 4, V_{N1} contributes the DC offset and flicker noise to the input pairs, and m(t) is the chopping signal taking values of +1 and -1 at

the chopping frequency f_c. After amplifying by programmable gain differential difference amplifier, we obtain the equation below:

$$V_{m2} = A[V_{in}m(t) + V_N] = A \cdot V_{in} \cdot m(t) + A \cdot V_N \quad -(5.2)$$

After the demodulator (Chopper 2), V_{m2} is demodulated back to the baseband spectrum, and the undesired component V_N is modulated to the odd harmonics of chopping frequency f_c. Then V_{m3} can be written as:

$$V_{m3} = m(t)[A \cdot V_{in} \cdot m(t) + A \cdot V_N] = A \cdot V_{in} + A \cdot V_N \cdot m(t) \quad -(5.3)$$

As the equation (5.3) shows, the last term signal contains the undesired component V_N is modulated to the odd harmonics of chopping frequency f_c. V_N can be removed after the signal passes through the low pass filter. Then equation (5.3) can be modified like this:

$$V_{out} = A \cdot V_{in} \quad -(5.4)$$

Compare with the equation (4.6) in chapter 4, we remove the terms of V_{N2} by using the structure in this chapter. That means we can reduce the noise effect to lower level.

Traditionally, we use an analog-to-digital converter (ADC) to serve as an interface between analog and digital signals. However, it is difficult to design a high resolution ADC due to the reduced of supply voltage V_{DD}. A pulse-width modulation (PWM) circuit is proposed to be another way that uses time-proportioning technique to represent the analog signal in time domain, and the digital circuit can use high-resolution counter to digitalize the signal.

5.3 Circuits Implementation

In this section, we will introduce about the building blocks of the analog-front end system and pulse-width modulation circuit. The former includes a programmable gain differential difference amplifier incorporate with chopper technique, a low pass filter (LPF), and an on-chip oscillator with non-overlapping clock generator. The later includes a sample and hold circuit, a ramp wave generator, and a comparator.

5.3.1 Programmable gain differential difference amplifier

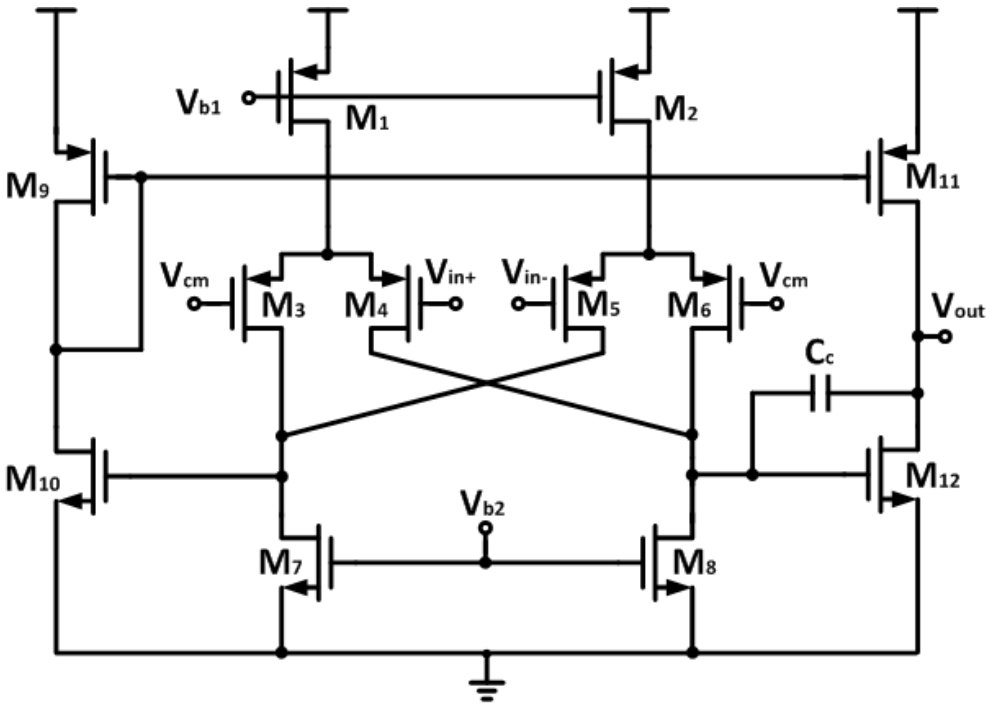


Fig. 5.3.1-1 Schematic of the differential difference amplifier (DDA)

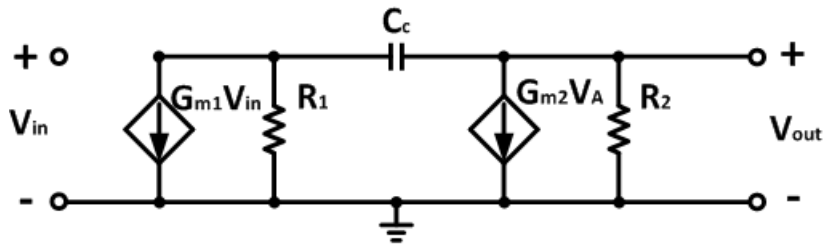


Fig. 5.3.1-2 Equivalent small signal model of DDA

Fig. 5.3.1-1 shows the schematic of the differential difference amplifier (DDA). As we can see, the structure of the DDA is based on the two-stage op topology. Compare with other opamp topologies, two-stage op has the advantage of high gain, high output swing and low output impedance. Due to the characteristic of low output impedance, the topology is suitable for resistive feedback. Compare with the OTA structure that has mentioned in chapter 4, there is no need for buffer to add at the output of the amplifier.

To analyze the differential difference amplifier, we can use the equivalent small signal model that shown in Fig. 5.3.1-2. Here the G_{m1} is the g_m of the transistor M_4 (or M_5), R_1 is r_{o4} // r_{o6} //r_{o8} or r_{o3} // r_{o5} //r_{o7}. G_{m2} is the g_m of the transistor M_{12}, R_2 is r_{o11} // r_{o12}. Miller capacitor C_c is needed for stabilization of the circuit. The open loop gain of the amplifier can be express as:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{(g_{m4}V_{sg4} + g_{m6}V_{sg6}) \cdot (r_{o4} // r_{o6} // r_{o8}) \cdot g_{m12} \cdot (r_{o12} // r_{o11})}{V_{sg4}} \quad -(5.5)$$

If $g_{m4}V_{sg4} = g_{m6}V_{sg6}$. We can simplify equation (5.5) into:

$$A_V = \frac{V_{out}}{V_{in}} = 2g_{m4} \cdot (r_{o4} // r_{o6} // r_{o8}) \cdot g_{m12} \cdot (r_{o12} // r_{o11}) \quad -(5.6)$$

The output resistance R_{out} can be written as:

$$R_{out} = r_{o12} // r_{o11} \quad -(5.7)$$

Compare with equation (4.28), the R_{out} value in equation (5.7) is much smaller than that in equation (4.28). Therefore, we do not need a buffer to lower the R_{out} at the output of amplifier.

In order to lower the noise effect, we also adopt chopper technique in this amplifier. Fig. 5.3.1-3 shows how we implement output chopper modulator (Chopper 2 in Fig.5.2-2). Since it is not a fully differential structure, the amplifier has only one output. Therefore, the output chopper modulator must be realized as Fig. 5.3.1-3 depicts. Besides, by using differential in, single out structure, it is not necessary to add a CMFB circuit to define the output common mode level. Thus, the output swing can be maximized and the power can be saved.

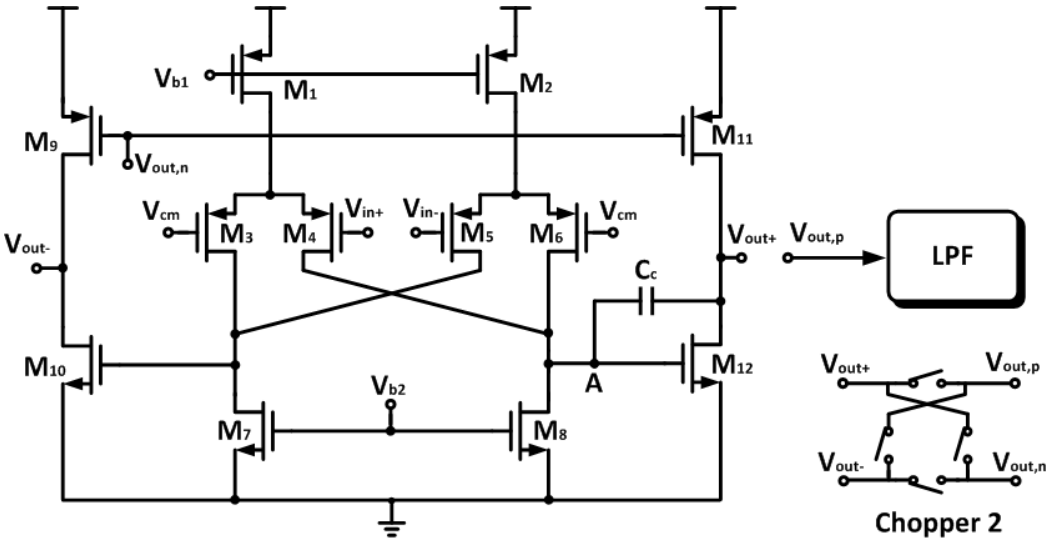


Fig. 5.3.1-3 Implement an output chopper modulator in a single output amplifier

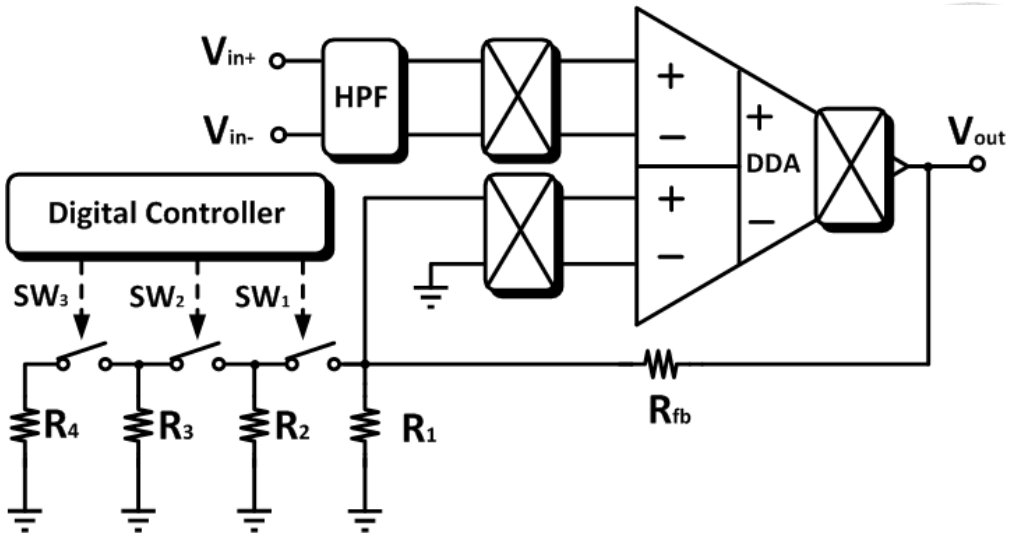


Fig. 5.3.1-4 Programmable gain differential difference amplifier with chopper technique

The programmable gain differential difference amplifier with chopper technique is depicted in Fig.5.3.1-4. It includes a differential difference amplifier (DDA), a poly resistor string of R_1-R_4, and seven transmission gate switches of SW_1-SW_3. The variable gain is obtained by poly resistor string of R_1-R_4 along with seven transmission gate switches of SW_1-SW_3 and the gain setting is selected according to the digital controller. Based on the variable resistances controlled by the CMOS switches, programmable gain is defined as:

$$V_{out} = \left(1 + \frac{R_{fb}}{R_i}\right)\left(V_{in+} - V_{in-}\right) \quad -(5.8)$$

$$R_i = R_1,\ or\ R_1 // R_2, or\ R_1 // R_2 // R_3, or\ R_1 // R_2 // R_3 // R_4 \quad -(5.9)$$

5.3.2 Rail-to-rail amplifier

The reason to require a rail-to-rail input range is to be able to maintain the same Signal-to-Noise ratio for smaller supply voltages. Certainly, signal swings decrease with the supply voltages. A rail-to-rail swing at input is the highest that can be obtained. However, a rail-to-rail input stage is not always required for all the circuitry. Fig. 5.3.2-1 shows three types of amplifier [5]. An inverting amplifier that shown in Fig. 5.3.2-1(a) has almost no swing at all at the inputs since the gain of the amplifier is quite large. This also applies to the non-inverting amplifier that shown in Fig. 5.3.2-1(b). The only configuration which needs a rail-to-rail input swing is the unity-gain buffer. Due to the unity gain, a rail-to-rail output requires the input to follow. Another application of a rail-to-rail input stage is the CMFB circuit. However, it is difficult to be realized at high frequencies with limited power consumption. Therefore, in this chapter, we abandon the fully-differential structure so that we do not need a CMFB circuit.

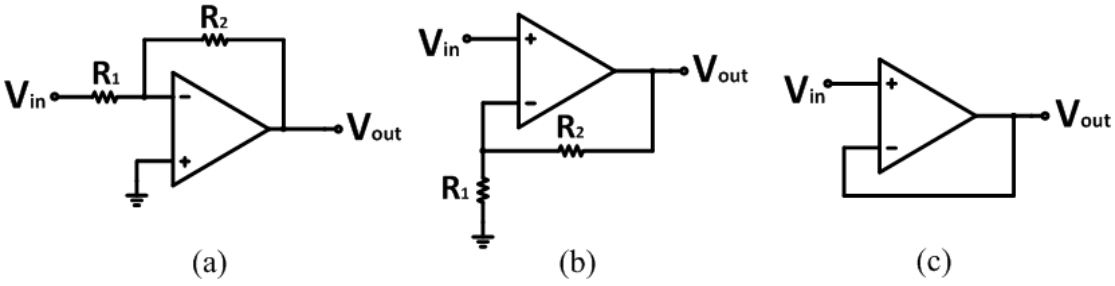


Fig. 5.3.2-1 (a) Inverting amplifier (b) Non-inverting amplifier (c) Buffer

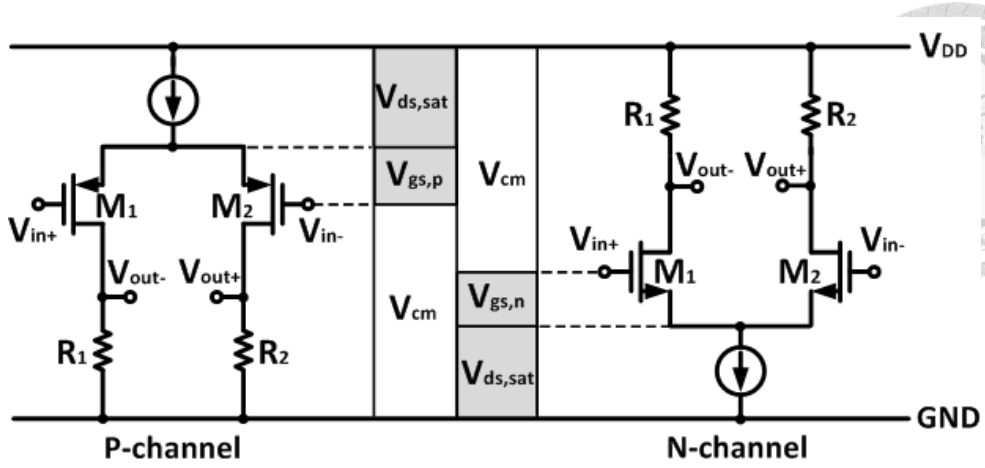


Fig. 5.3.2-2 Common-mode input range of NMOS and PMOS input pairs

Fig. 5.3.2-2 shows the differential voltage ranges for NMOS and PMOS input pairs [33]. The PMOS input pair operates at the voltage of $V_{cm} < V_{DD} - |V_{gs,p}| - V_{ds,sat}$. Where $|V_{gs,p}|$ is the gate-source voltage of the PMOS transistor, and $V_{ds,sat}$ is the voltage across the current source. The NMOS input pair is operates at the voltage of $GND + V_{gs,n} + V_{ds,sat} < V_{cm}$. Where $V_{gs,n}$ is the gate-source voltage of the NMOS transistor.

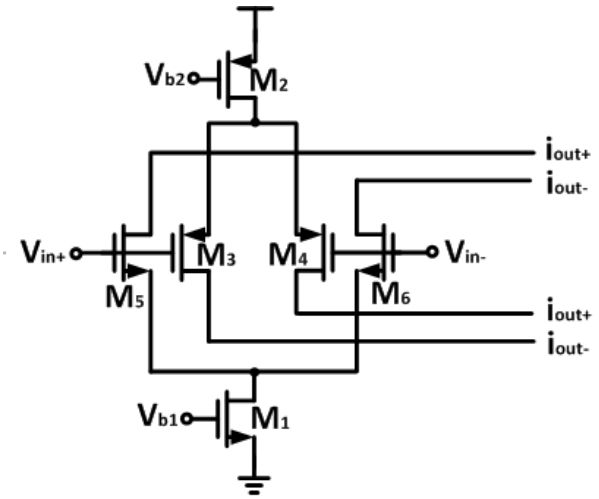


Fig. 5.3.2-3 Rail-to-rail input stage

The way to reach a rail-to-rail input swing is to use two folded cascodes in parallel. The rail-to-rail input stage is shown in Fig. 5.3.2-3 [5]. To understand the operation mode of the rail-to-rail input stage, we can use Fig. 5.3.2-4 and Fig. 5.3.2-5 to explain it [22].

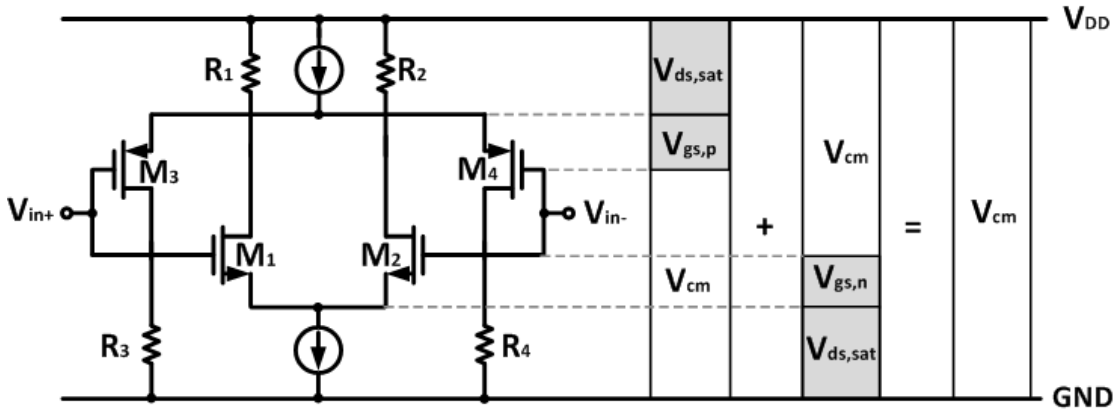


Fig. 5.3.2-4 Common-mode input range of rail-to-rail input stage. The supply voltage is larger than $|V_{gs,p}| + V_{gs,n} + 2V_{ds,sat}$

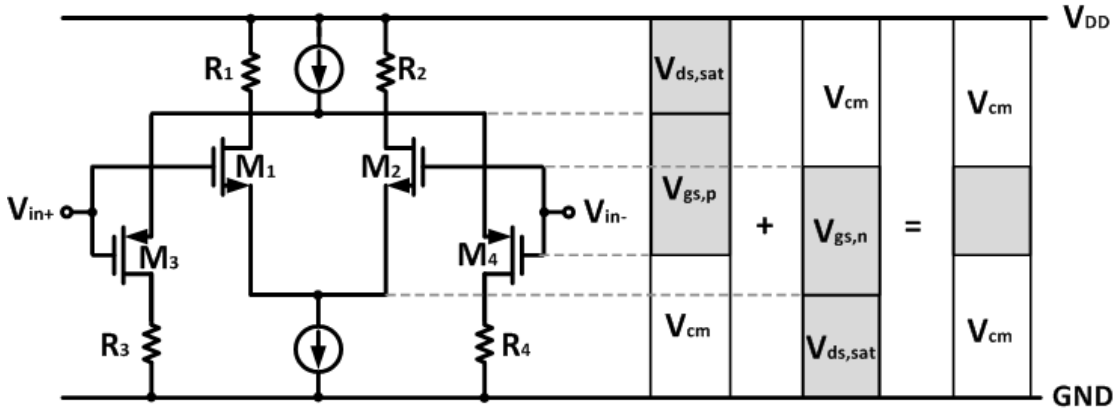


Fig. 5.3.2-5 Common-mode input range of rail-to-rail input stage. The supply voltage is smaller than $|V_{gs,p}| + V_{gs,n} + 2V_{ds,sat}$

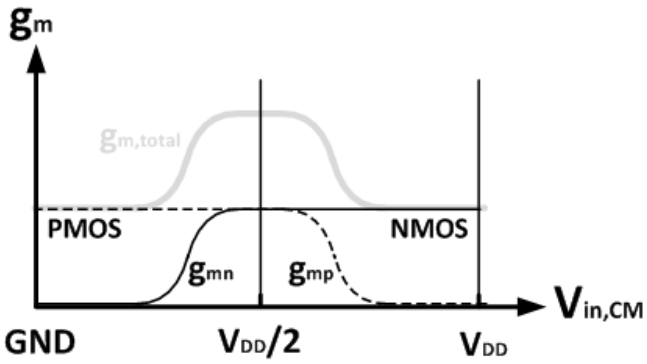


Fig. 5.3.2-6 Transconductance (g_m) versus Common-mode inputvoltage ($V_{in,CM}$) for rail-to-rail input stage. The supply voltage is larger than $V_{gs,p} + V_{gs,n} + 2V_{ds,sat}$

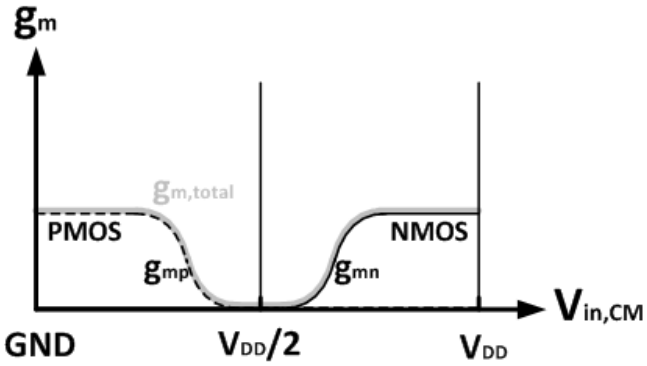


Fig. 5.3.2-7 Transconductance (g_m) versus Common-mode input voltage for ($V_{in,CM}$) rail-to-rail input stage. The supply voltage is smaller than $V_{gs,p} + V_{gs,n} + 2V_{ds,sat}$

Fig. 5.3.2-4 shows the common-mode input range of rail-to-rail input stage with the supply voltage V_{DD} is larger than $| V_{gs,p} | + V_{gs,n} + 2V_{ds,sat}$. Although the common-mode input voltage can operates from GND to V_{DD}, it meets a problem when $V_{in,CM}$ operates in the middle voltage range. For $V_{in,CM}$ operates in the middle voltage range, both input pairs are operational so the g_m value is doubled, just as Fig.

5.3.2-6 shows. As a result, transconductance value is not constant in different common-mode level. This would give a large amount of distortion.

Besides, Fig. 5.3.2-5 shows the common-mode input range of rail-to-rail input stage with the supply voltage V_{DD} is smaller than $| V_{gs,p} | + V_{gs,n} + 2V_{ds,sat}$. In this case, the input stage ceases to operate in the middle voltage region, as shown in Fig. 5.3.2-7.

To solve the problems that we have mentioned above, we make the sum of the g_m value constant. We set the $| V_{gs,p} | + V_{gs,n} + 2V_{ds,sat}$ equals to V_{DD} so that at half of the supply voltage V_{DD}, the g_m of both pairs are reduced to half. Another important key point is that the value of g_{mn} must be equal to g_{mp}. Therefore, the current source of the PMOS input pair should be twice to the current source of the NMOS input pair [5]. Fig. 5.3.2-8 illustrates the concept of constant g_m.

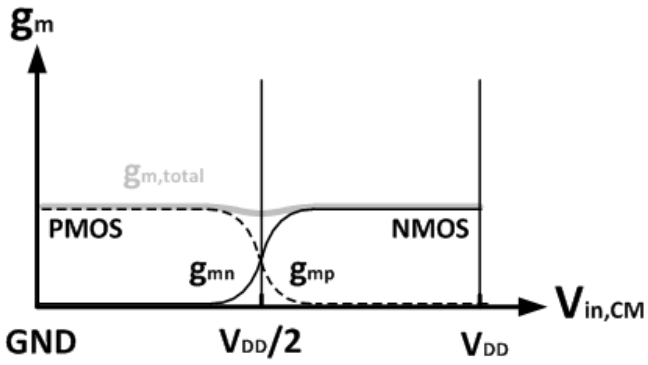


Fig. 5.3.2-8 Designing g_m value to be constant

Fig. 5.3.2-8 depicts the schematic of rail-to-rail opamp. It consists of a simple double input stage and an output stage to drive the next stage circuit.

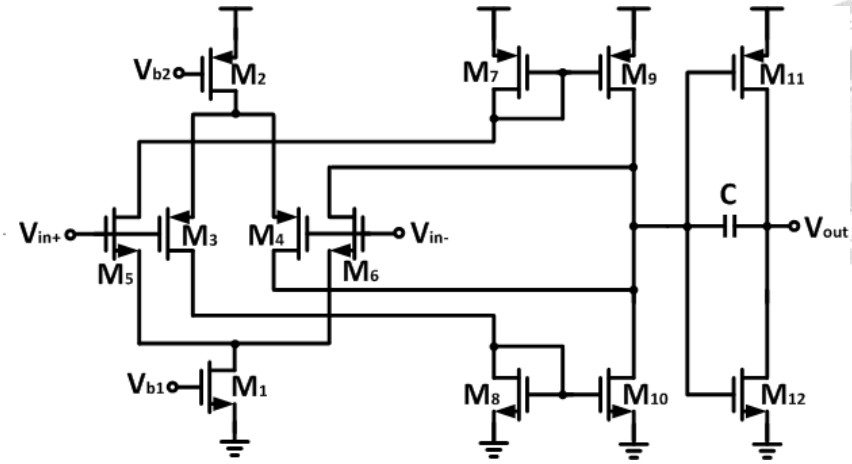


Fig. 5.3.2-9 Schematic of rail-to-rail opamp

5.3.3 Filter

As we have mentioned in section 5.3.2, the rail-to-rail output of the unity gain buffer requires the input to follow. Therefore, the unity gain Sallen-Key low pass filter needs rail-to-rail opamp to act as its core amplifier. The design principle of the filter and rail-to-rail opamp has been introduced in section 4.3.3 and 5.3.2, respectively. Fig. 5.3.3-1 shows the second-order Butterworth low pass filter based on rail-to-rail opamp.

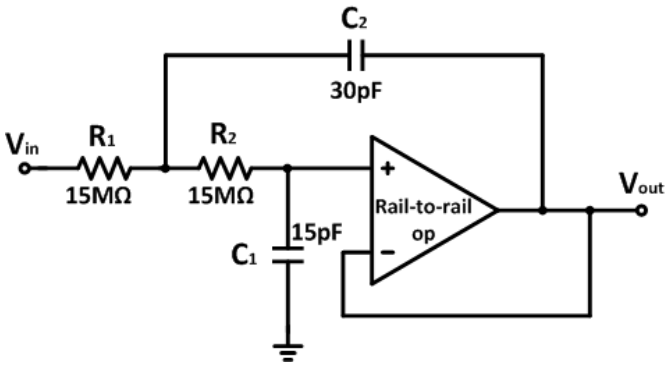


Fig. 5.3.3-1 Second-order Butterworth low pass filter based on rail-to-rail opamp

5.3.4 PWM Circuit

Traditionally, we use analog-to-digital converter (ADC) to act as an interface between analog signal and digital signal. However, it is not an easy task to design a high resolution SAR ADC in such a low voltage supply application and low power consumption limitation. The DACs play an important role in a SAR ADC design. The layout of the capacitor array should be taken into concern carefully because the mismatch in the capacitance will degrade the performance of the SAR ADC significantly. In this thesis, we provide another solution to convert analog signal into digital signal. Fig. 5.3.4-1 shows a block diagram of PWM circuit [26]. It includes a sample and hold circuit, a ramp wave generator, and a rail-to-rail comparator. After obtaining a PWM signal, we use a serial-to-parallel circuit to convert it into 10-bit representation. Then the DSP circuit can deal with it by using discrete wavelet transform technique.

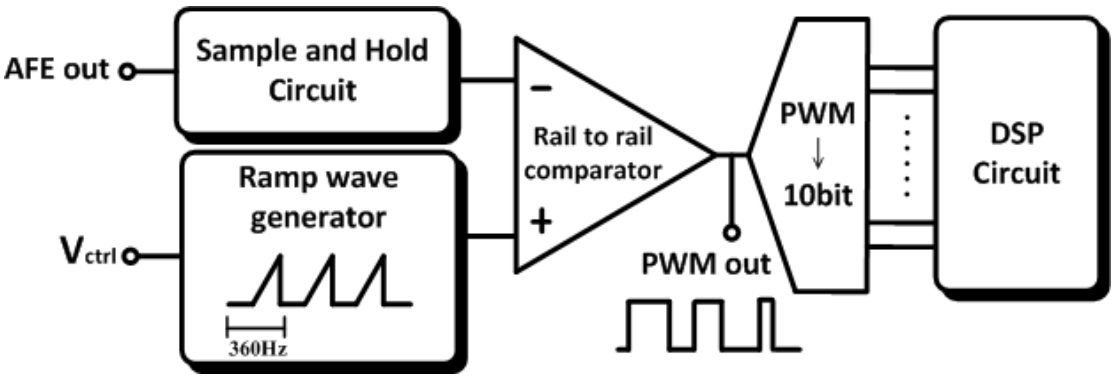


Fig. 5.3.4-1 Block diagram of PWM circuit

5.3.4.1 Ramp wave generator

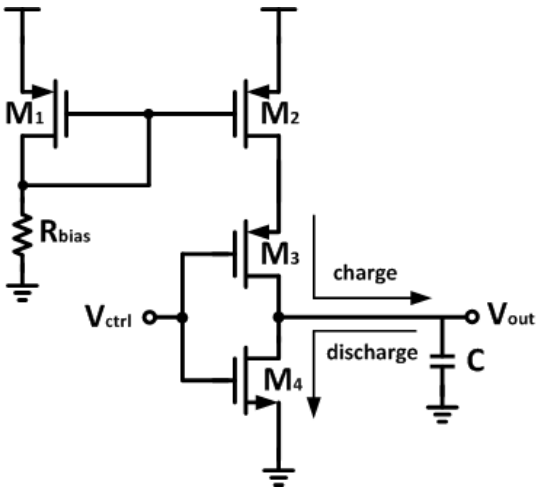


Fig. 5.3.4.1-1 Schematic of ramp wave generator

Fig. 5.3.4.1-1 is the schematic of ramp wave generator. V_{ctrl} is the signal that is controlled by UART circuit. Fig. 5.3.4.1-2 shows the wave function of V_{ctrl} and V_{out}. When V_{ctrl} is low, PMOS M_3 is on and NMOS M_4 is off, resulting in the current will charge the loading capacitor. When V_{ctrl} is high, PMOS M_3 is off and NMOS M_4 is on, resulting in the current will be discharged from the loading capacitor.

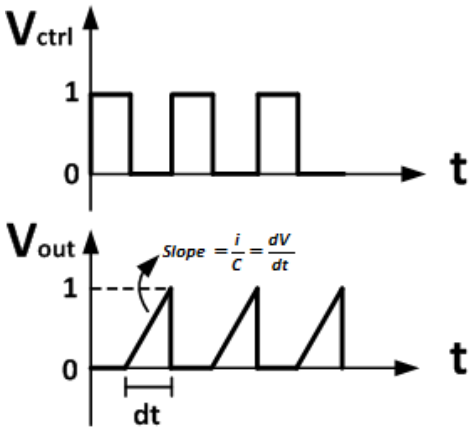


Fig. 5.3.4.1-2 Wave function of V_{ctrl} and V_{out} in ramp wave generator

The slope of the ramp wave can be express as:

$$Slope = \frac{i}{C} = \frac{dV}{dt} \quad -(5.10)$$

Where dV is 1V, and dt is determined by the sample rate of DSP circuit. In ECG monitoring system, the sample rate of the DSP circuit is 360Hz. That means the slope of the ramp wave must be $\frac{1}{\frac{1}{360 \times 2}} = 720$ (V/t). By choosing the value of capacitor and current, we can generate a ramp wave that meets the require condition.

5.3.4.2 Sample and hold circuit (S/H)

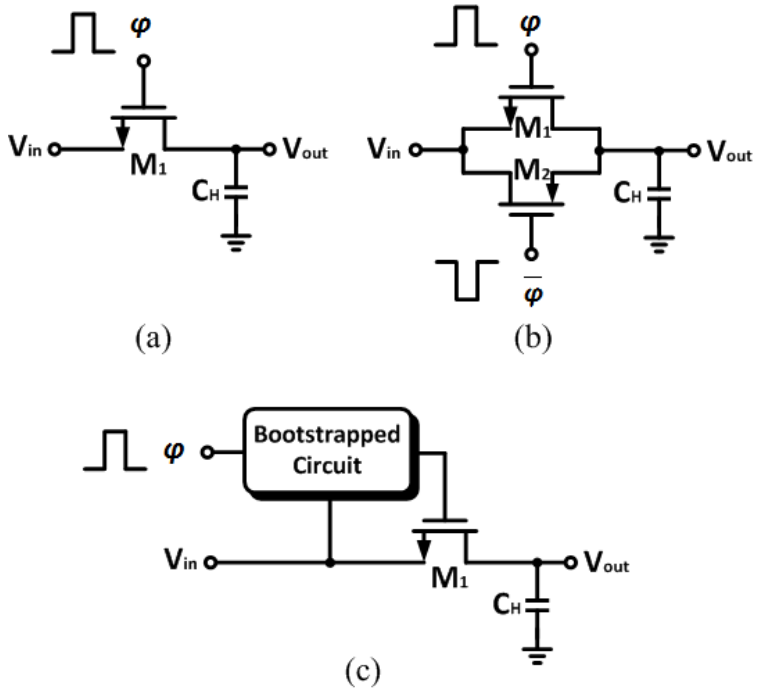


Fig. 5.3.4.2-1 Sample and hold circuit realize by (a) Simple NMOS switch (b) Transmission gate switch (c) Bootstrapped switch

As shown in Fig. 5.3.4.2-1(a), in the simplest case, a S/H circuit can be achieved using only one NMOS switch and a capacitor. When MOS is off, it operates in cutoff region and has large impedance. When MOS is on, it operates in triode region and act as a linear resistor. The equivalent impedance can be written as:

$$R_{on,n} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{GS} - V_{th,n}\right)} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{in} - V_{th,n}\right)} \quad -(5.11)$$

From equation (5.11), we can know that $R_{on,n}$ varies with signal V_{in}. The input signal dependent property on $R_{on,n}$ will cause non-linear effect on signal [1]. Therefore, a modified switch should be applied.

Transmission gate switch is an easy way to solve this problem. Fig. 5.3.4.2-1(b) depicts the S/H circuit using transmission gate switch. The NMOS transistor is parallel to the PMOS transistor. The equivalent impedance can be written as:

$$R_{on,eq} = R_{on,n} // R_{on,p}$$
$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{th,n}\right) - \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_n - \mu_p C_{ox}\left(\frac{W}{L}\right)_p\right] V_{in} - \mu_p C_{ox}\left(\frac{W}{L}\right)_p \left|V_{th,p}\right|} \quad -(5.12)$$

If $\mu_n\left(\frac{W}{L}\right)_n = \mu_p\left(\frac{W}{L}\right)_p$, then $R_{on,eq}$ is independent of input signal. Fig. 5.3.4.2-2 plots the behavior of $R_{on,eq}$, revealing much less variation than that corresponding to each switch alone [1].

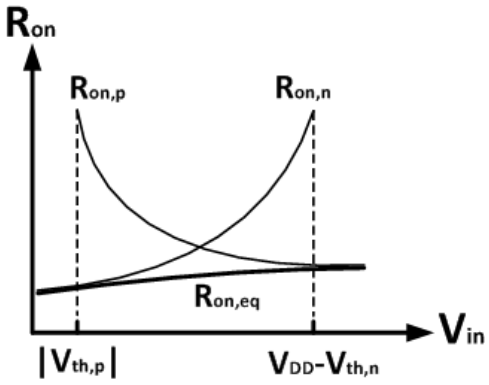


Fig. 5.3.4.2-2 On-resistance of the transmission gate switch

However, in low voltage supply application, the V_{GS} will be too small to turn on the switch. If we apply a single MOS switch or transmission gate switch under 1-V operation, the on-resistance will be very large when input signal is at common-mode voltage.

In order to solve the problems that we have mentioned above, a bootstrapped circuit is applied. As Fig. 5.3.4.2-1 (c) depicts, a bootstrapped circuit is inserted between the gate and source terminal of the transistor. The schematic of the bootstrapped circuit is shown in Fig. 5.3.4.2-3 [24]. The V_{GS} of the sampling transistor is fixed by the bootstrapped circuit at the supply voltage V_{DD}. We can have on-resistance equals to:

$$R_{on,n} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{th,n}\right)} \quad -(5.13)$$

With the bootstrapped circuit, the on-resistance is a small constant value and thus improves the switch linearity.

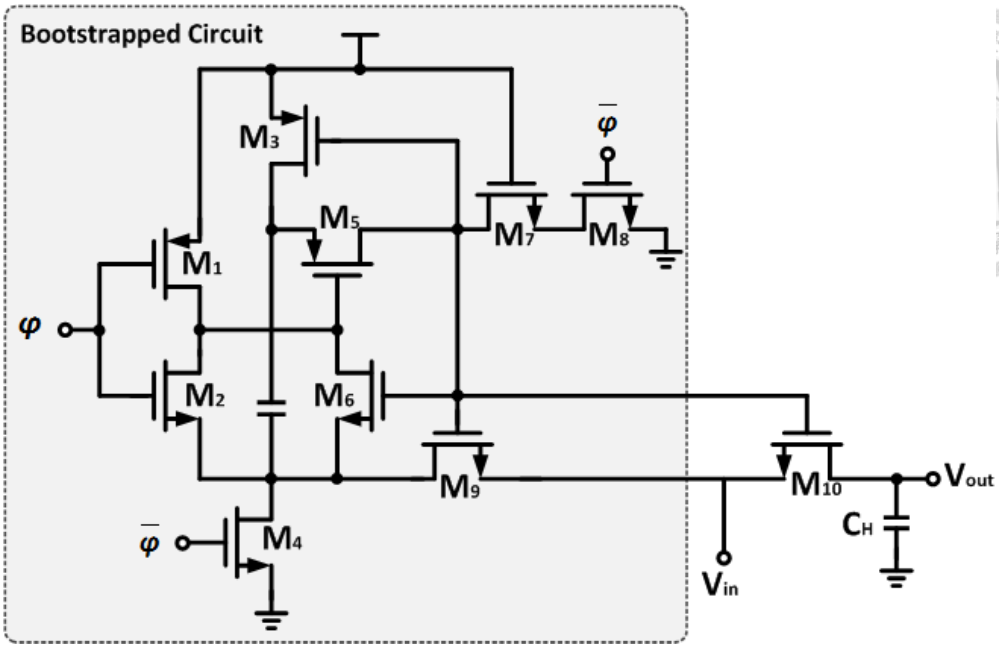


Fig. 5.3.4.2-3 Schematic of the bootstrapped circuit

5.3.4.3 Rail-to-rail comparator

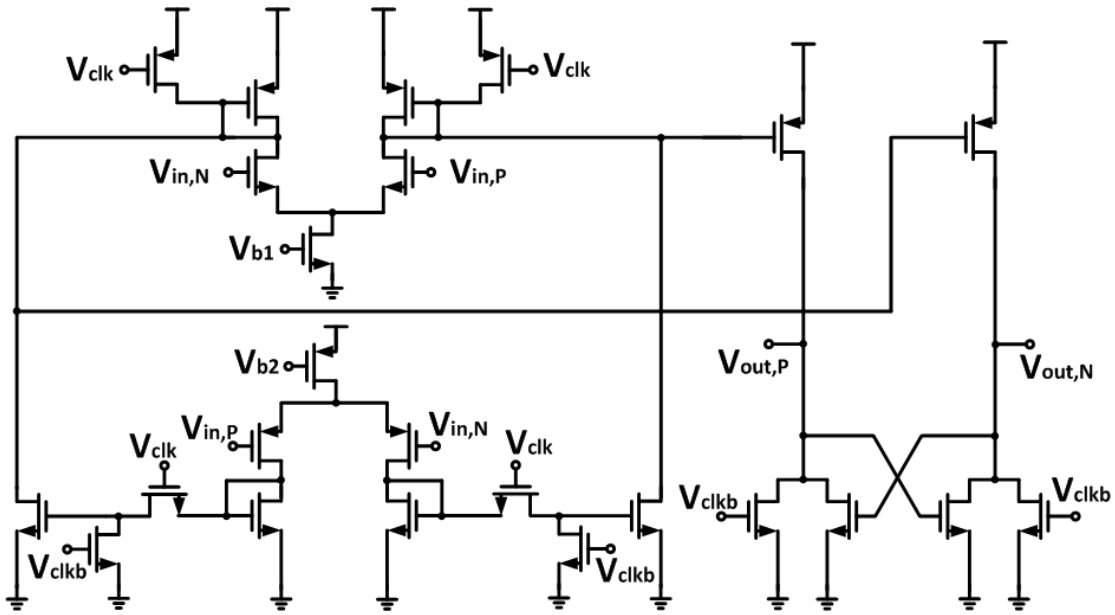


Fig. 5.3.4.3-1 Schematic of the rail-to-rail comparator

Fig. 5.3.4.3-1 shows the schematic of the rail-to-rail comparator. Since the input signal has been amplified by analog front-end, we must implement a rail-to-rail input stage in comparator. One of the inputs connects to the output of ramp wave generator. The others connects to the output of sample and hold circuit. Once the value of ramp wave overtakes the value of hold signal, the output of the comparator would turns from 0 (GND) to 1 (VDD). Then the SR latch would preserve the previous output value. Schematic of the SR latch is shown in Fig. 5.3.4.3-2. Rail-to-rail output can be obtained via SR latch and node V_{out} would present the digital value.

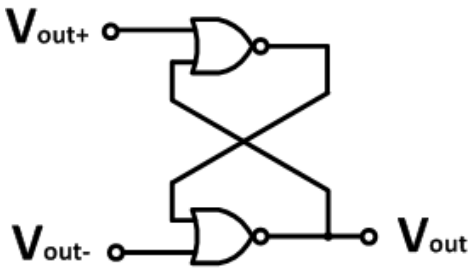


Fig.5.3.4-2 Schematic of the SR latch

5.3.5 On-chip oscillator [33]

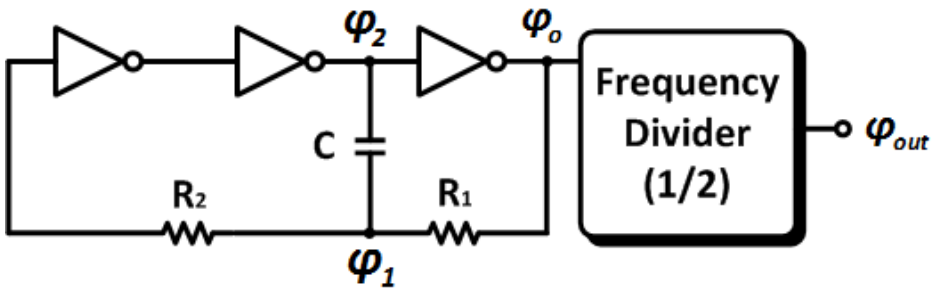


Fig.5.3.5-1 On-chip CMOS oscillator

We can design a square wave oscillator by using CMOS logic elements. Fig.5.3.5-1 illustrates an on-chip CMOS oscillator consists of a three-gate oscillator and a frequency divider with a division of 1/2 factor. Contrast to crystal oscillators, the CMOS oscillators has the advantage of low power consumption and easy to be integrated on chip. To obtain the oscillation frequency of the on-chip oscillator, we can derive it from the following equation:

$$f \cong \frac{1}{4\pi CR_1\left(\frac{0.45R_2}{R_1+R_2}+0.693\right)} \cong \frac{1}{4\pi C\left(0.45R_{eq}+0.693R_1\right)} \quad -(5.14)$$

$$\text{Where } R_{eq} = \frac{R_1R_2}{R_1+R_2}$$

$$\text{If } R_1 >> R_2,\ f \cong \frac{0.115}{R_1 \cdot C} \quad -(5.15)$$

5.4 Simulation

Fig. 5.4-1 shows the AC response simulation result of the DDA. The f_t is at 3M Hz, the gain is 80dB, and the phase margin is 50°. Fig. 5.4-2 shows the AC response simulation result of the rail-to-rail opamp. The f_t is at 500k Hz, the gain is 100dB, and the phase margin is 45°. Fig. 5.4-3 shows the AC response simulation result of the second-order Butterworth low-pass filter. The f_{3dB} is about 500Hz, and the gain is 0. The overall programmable gain DDA simulation result is shown in Fig. 5.4-4 with the

gain of 30dB, 37dB, 43dB, and 50dB. The simulation result of the CMRR is about 106dB in this AFE system, as shown in Fig. 5.4-5. The simulation result of the PSRR is about 82dB in this AFE system, as shown in Fig. 5.4-6. The overall AFE system only consumes 8uA with the 1V supply voltage (V_{DD}).

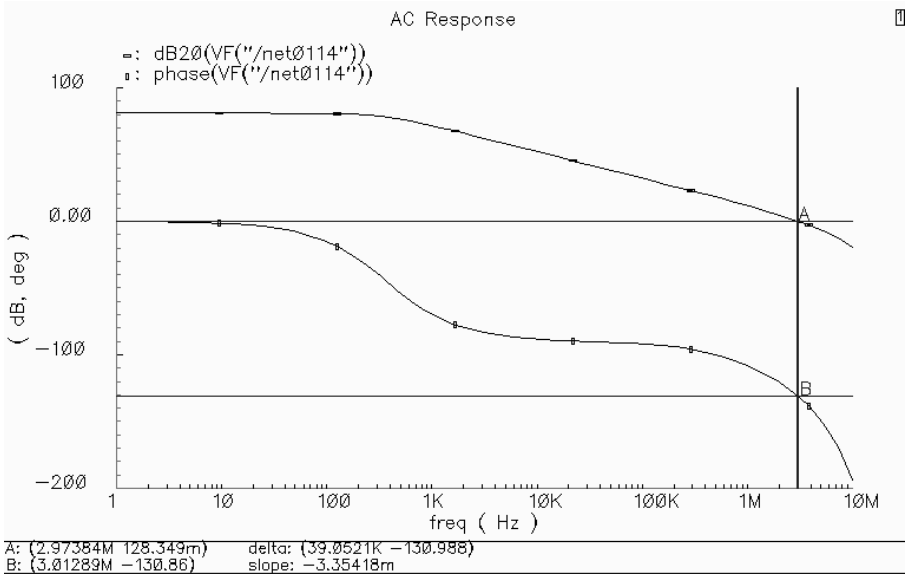


Fig.5.4-1 AC response simulation of DDA

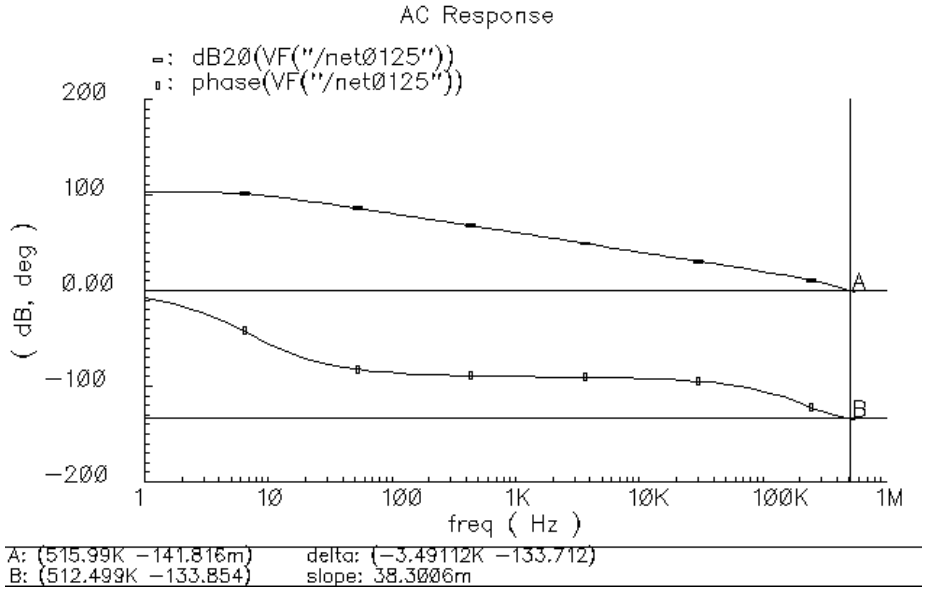


Fig.5.4-2 AC response simulation of Rail-to-rail opamp

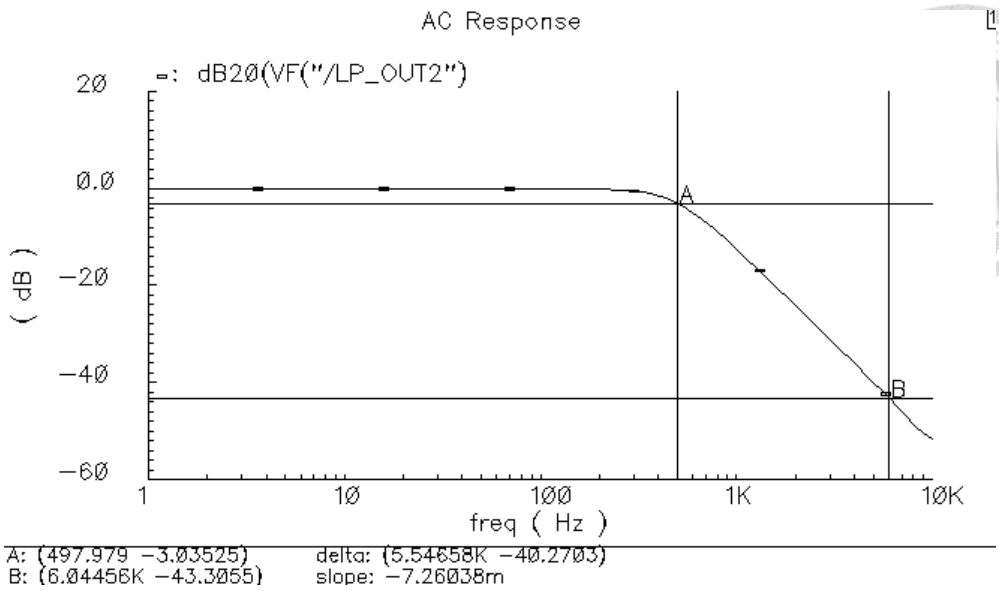


Fig.5.4-3 AC response simulation of Low-pass filter

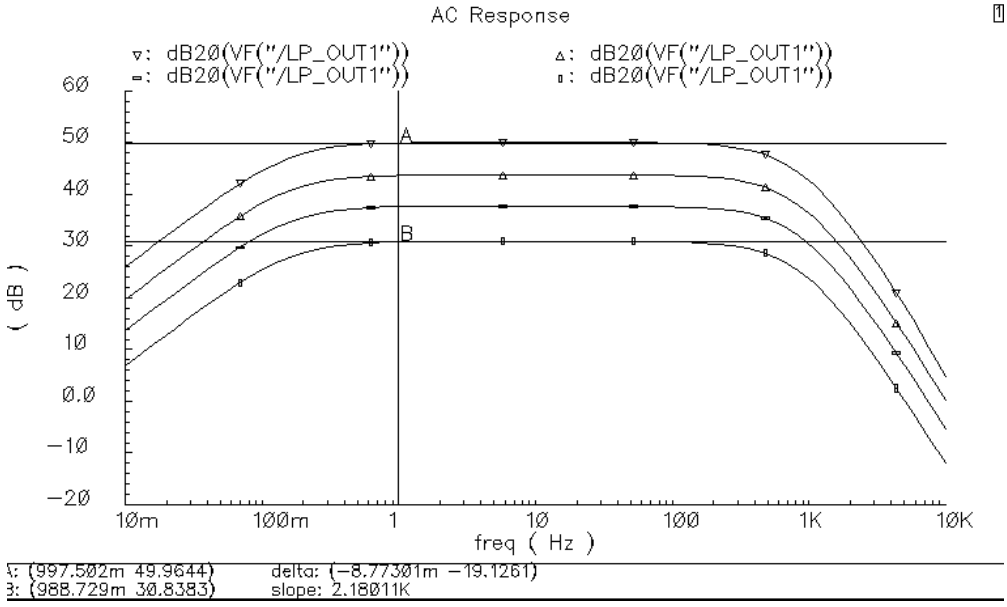


Fig.5.4-4 AC response simulation of programmable gain DDA

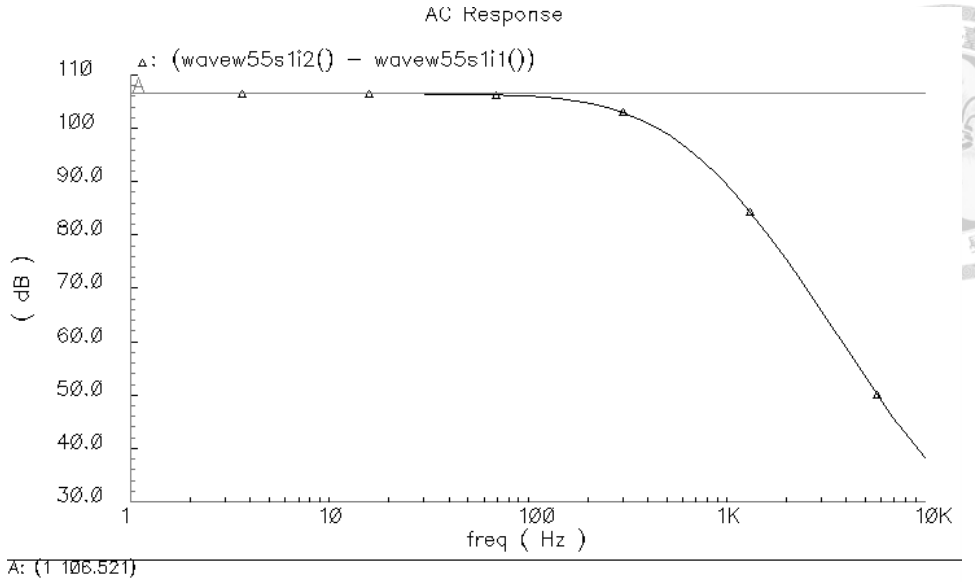


Fig. 5.4-5 CMRR Simulation of AFE

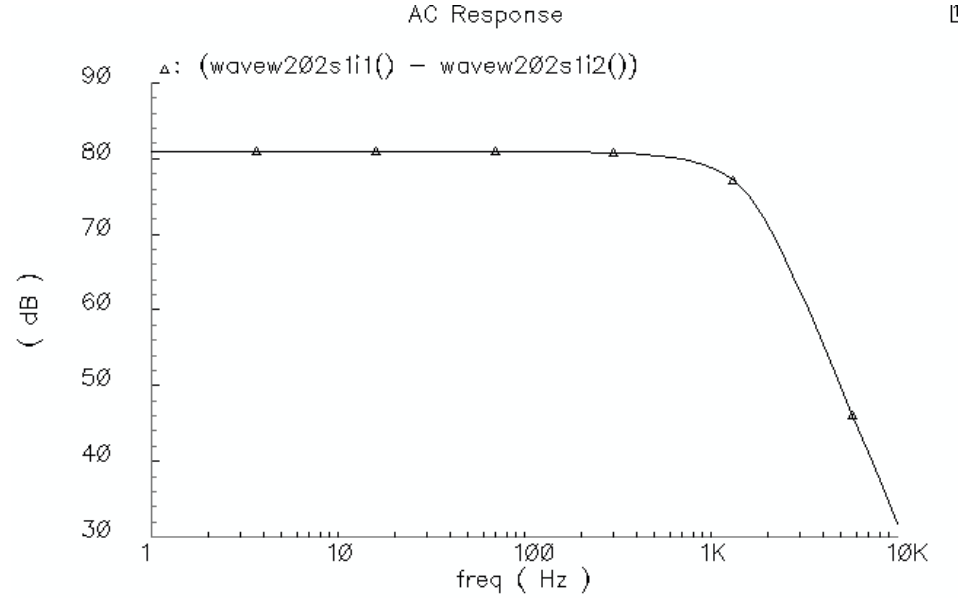


Fig. 5.4-6 PSRR Simulation of AFE

Fig. 5.4-7 shows the input common mode range simulation result of the DDA. Since the input ECG signal is small, the figure shows that the DDA is good enough to deal with the ECG signal. In addition, the DC gain shows in Fig.5.4-8, achieve not only the high DC gain but also nearly rail-to-rail output signal swing.

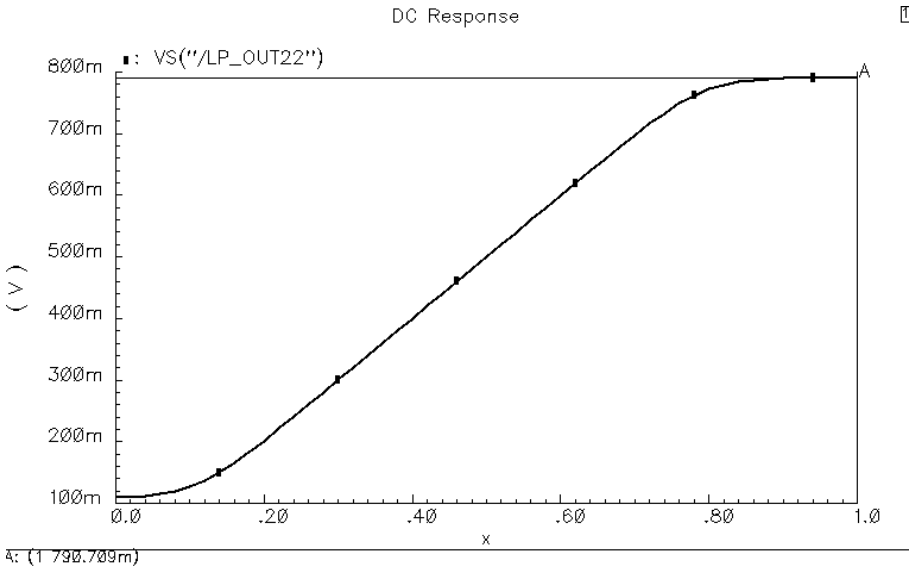


Fig.5.4-7 Input common mode range simulation of DDA

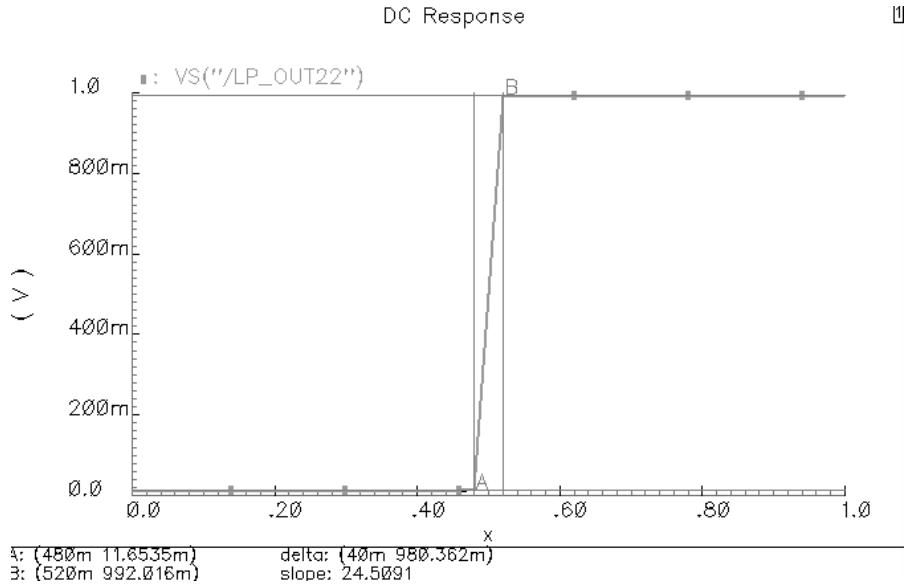


Fig.5.4-8 Output swing simulation of DDA

Fig. 5.4-9 shows the input common mode range simulation result of the rail-to-rail opamp. Since the ECG signal has been amplified by programmable gain DDA, the input common mode range must be large. As we can see in Fig. 5.4-9, input common mode range is nearly rail-to-rail.

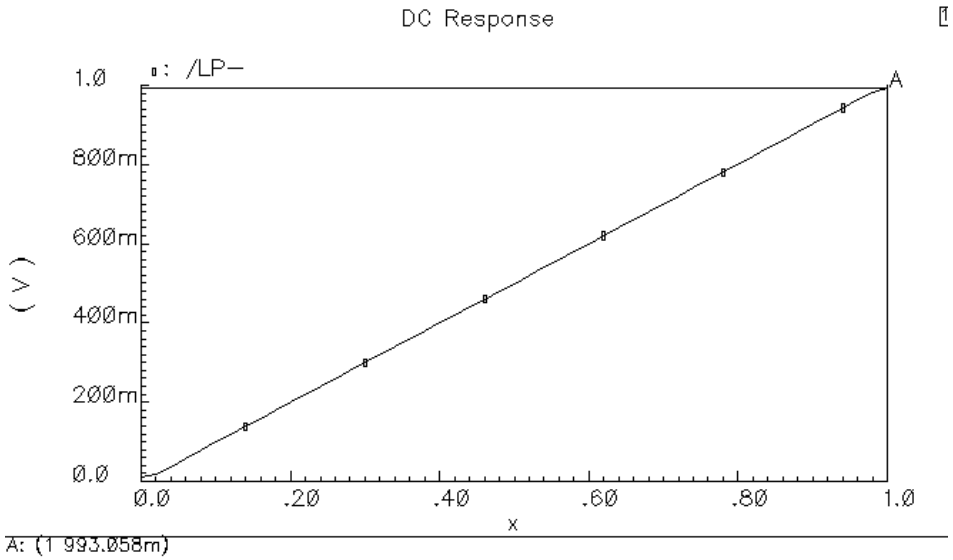


Fig.5.4-9 Input common mode range simulation of Rail-to-rail opamp

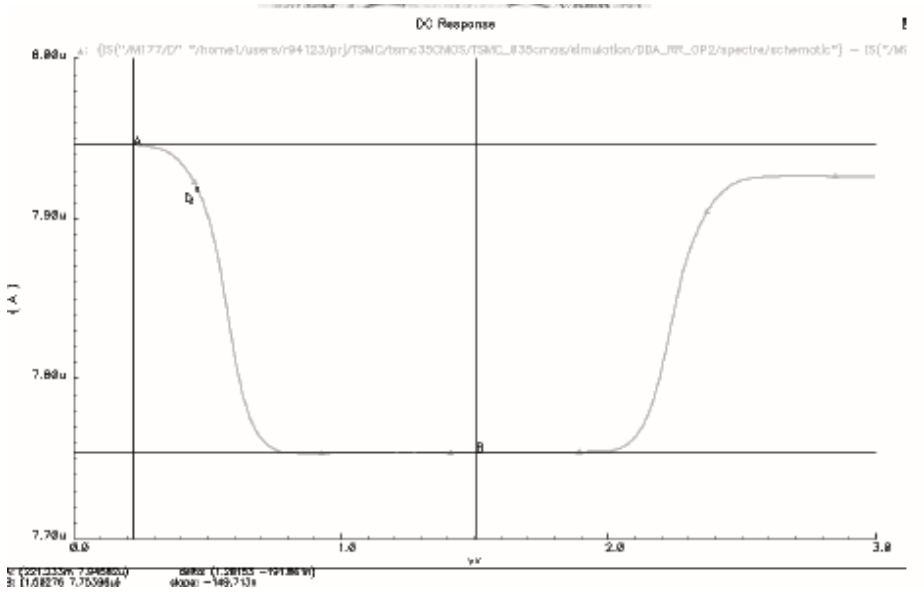


Fig. 5.4-10 Transconductance (g_m) simulation of the Rail-to-rail input stages

Fig. 5.4-10 shows the transconductance (g_m) simulation result of the Rail-to-rail input stages. The variation of the g_m value is about 3%.

Fig. 5.4-11 shows the input-referred-noise simulation result of the AFE. Here we choose chopping frequency f_c = 4k Hz. Therefore, Fig. 5.4-12 shows that the noise will be chopped to 4k Hz. Fig. 5.4-13 shows the noise simulation result after the noise is removed by the low-pass filter. Compare with Fig. 5.4-11, the noise at the baseband has been reduced due to the chopper technique.

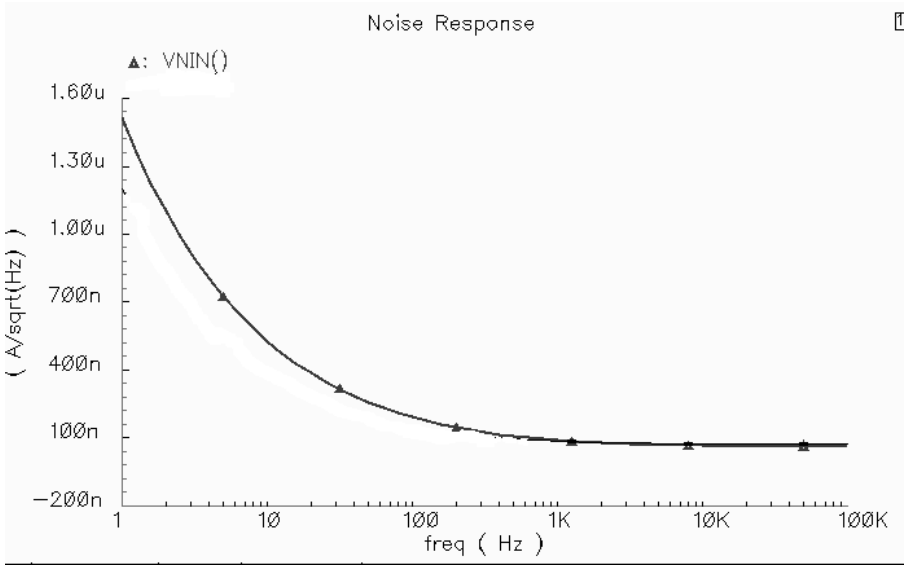


Fig. 5.4-11 Noise response simulation of AFE

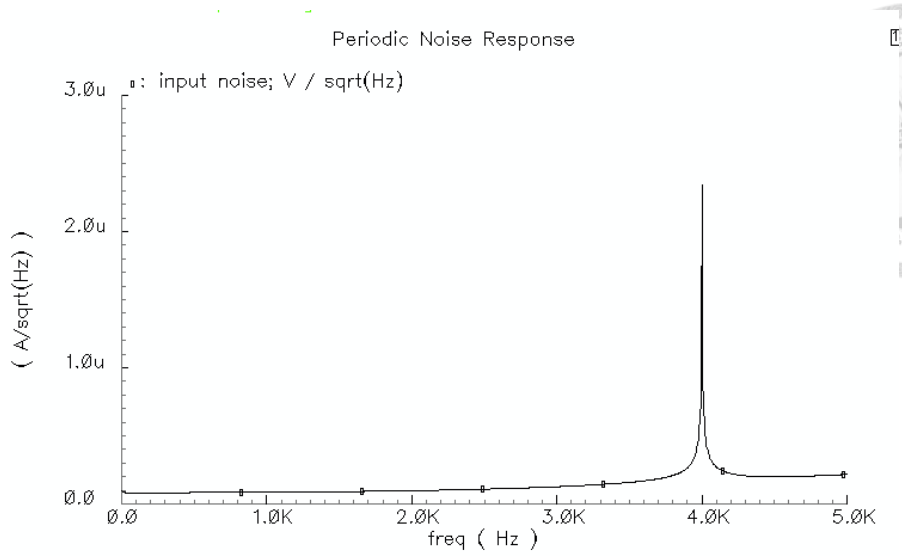


Fig. 5.4-12 Noise response simulation of AFE with chopper modulation

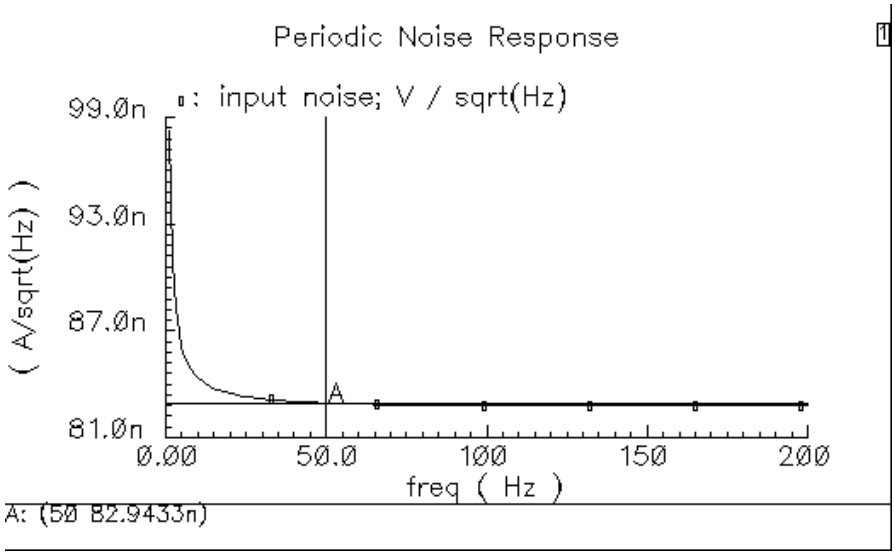


Fig. 5.4-13 Noise response simulation at the output of LPF

The PWM circuit consists of a ramp wave generator, a sample and hold circuit, and a comparator. Fig. 5.4-14 shows the waveform of the ramp wave generator. The slope of the ramp wave is 720 V/t. Fig.5.4-15 shows the simulation result of the

sample and hold circuit. We can see that the gate voltage of transistor varies with V_{in} and the difference between is a constant value, just as equation 5.13 shows. The transient response simulation result of the comparator is shown in Fig.5.4-16. As the value of ramp wave overtakes the value of hold signal, the output of the comparator would turns from 0 (GND) to 1 (VDD).

The overall system testing is shown in Fig.5.4-17 and Fig.5.4-18. At the input of the AFE, we import a small sine wave to test the function of the whole system. The green line represents the output signal of the AFE, and the black line represents the sample and hold result. The hold value will compare with the ramp wave, which is shown in red line. At last, the PWM wave (blue line) is obtained.

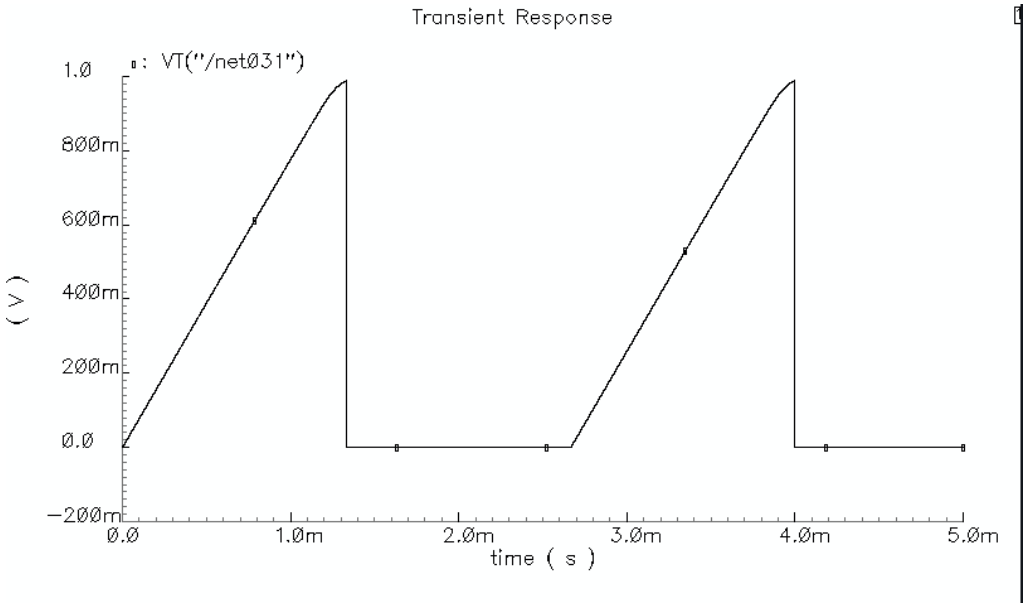


Fig.5.4-14 Transient response simulation of ramp wave generator

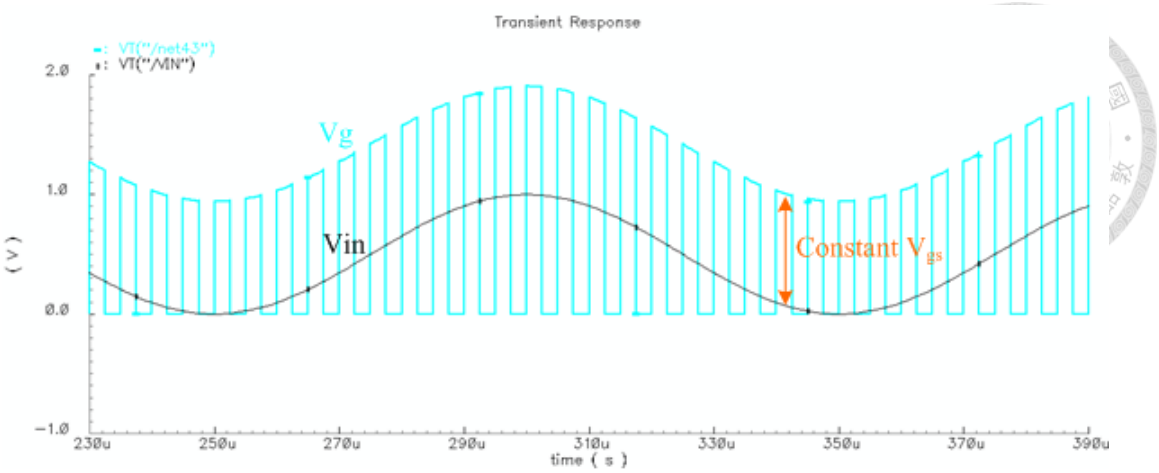


Fig.5.4-15 Transient response simulation of sample and hold circuit

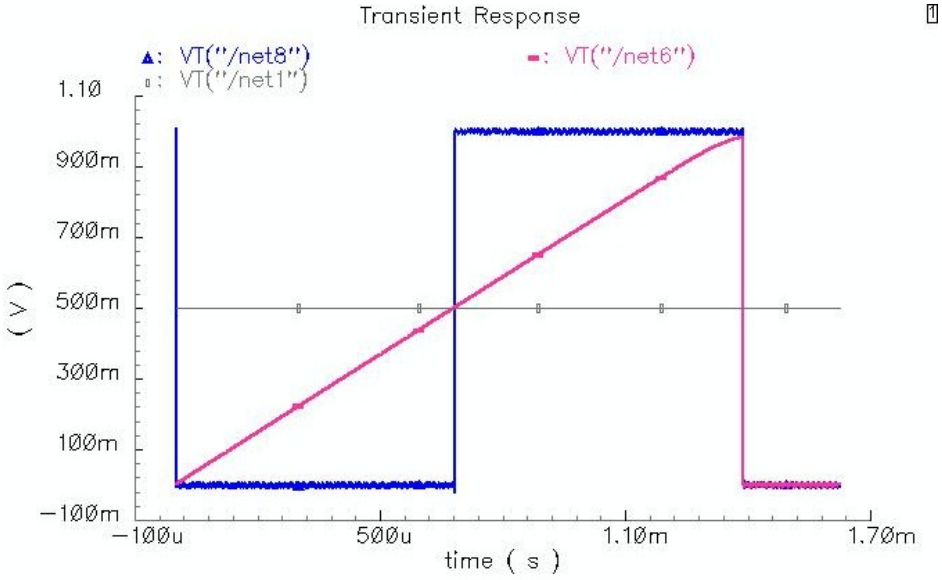


Fig.5.4-16 Transient response simulation of comparator

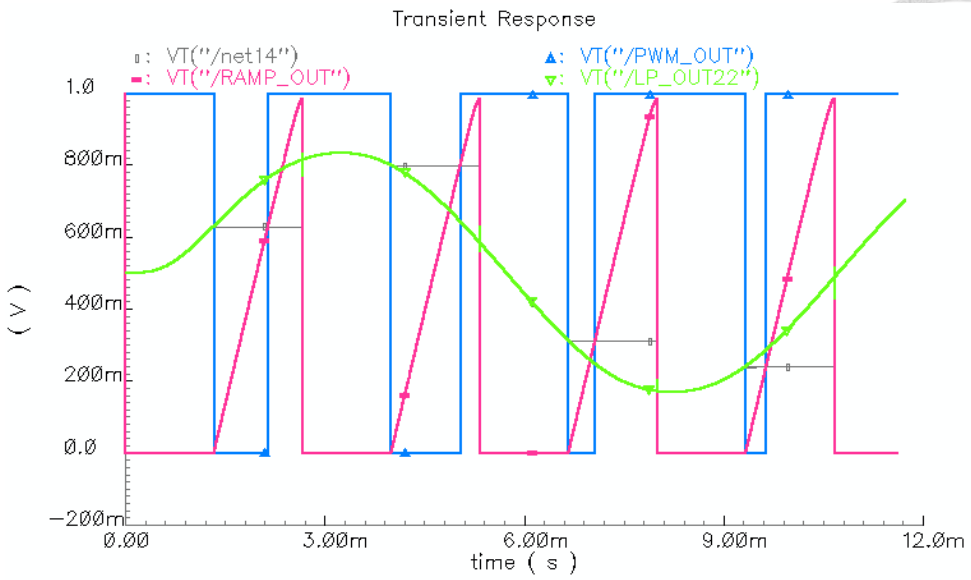


Fig.5.4-17 Transient response interface simulation from AFE to PWM circuit (1)

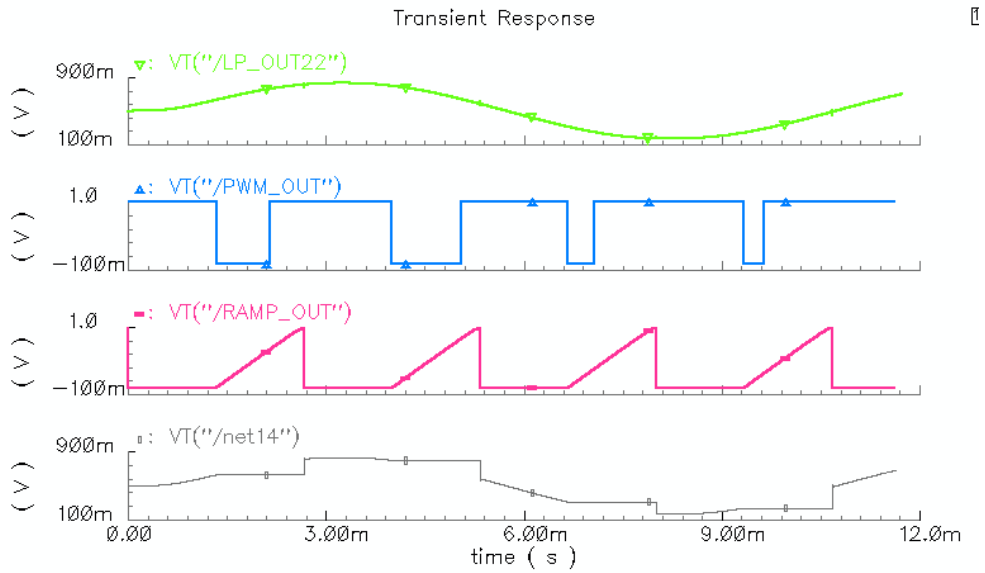


Fig.5.4-18 Transient response interface simulation from AFE to PWM circuit (2)

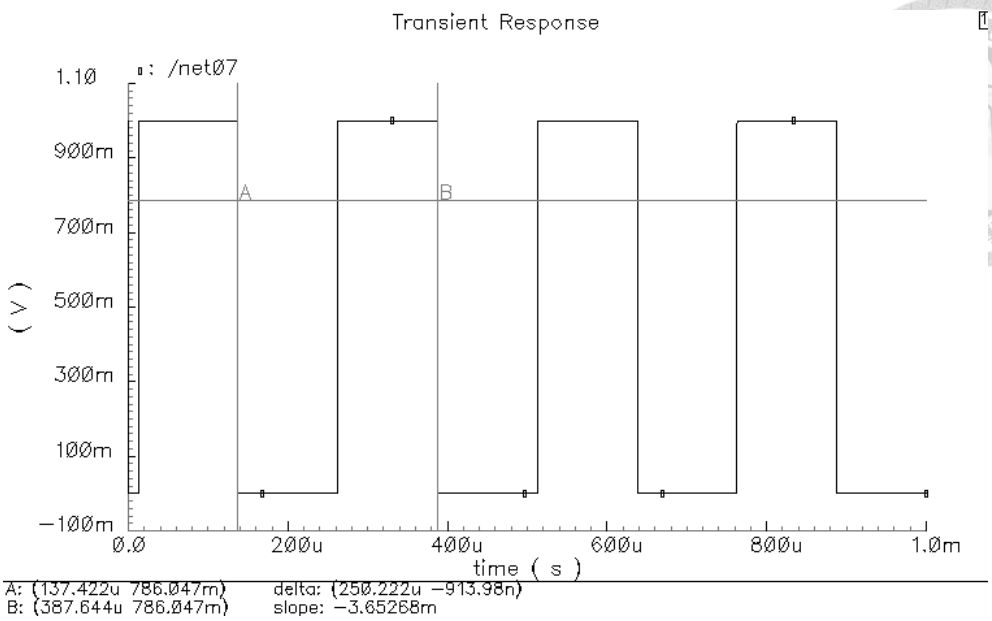


Fig.5.4-19 Transient response simulation of on-chip oscillator

Fig.5.4-19 shows the transient response simulation of on-chip oscillator. The oscillating frequency is 4k Hz. Table 5.4-1 shows the simulation results of this work.

Table 5.4-1 Summary of simulation result

Features		**Performance**
Power supply		1V
Power	AFE	8uW
	PWM	5uW
Chopper frequency		4k Hz
Programmable gain selection		30dB, 37dB, 43dB, 50dB
Output swing		0V~1V
3dB frequency		500Hz
Input-referred noise density		82.9nV/$\sqrt{Hz}$
CMRR		106dB
PSRR		82dB

5.5 Layout

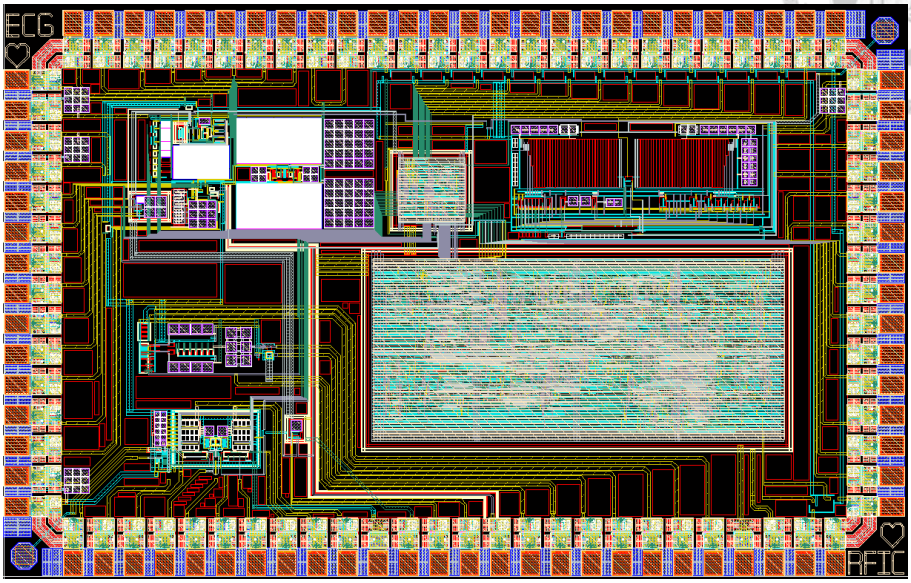


Fig.5.5-1 Layout of the ECG monitoring system (Ver.2)

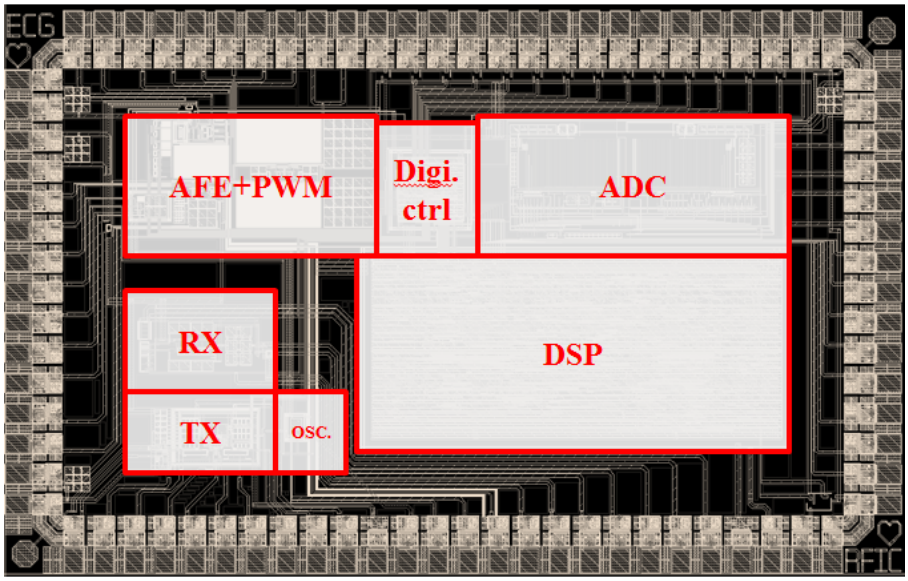


Fig.5.5-2 Layout floor of the ECG monitoring system (Ver.2)

Fig. 5.5-1 and Fig. 5.5-2 show the layout and the layout floor plain of the ECG monitoring system (Ver.2). The analog-front end and PWM circuit are integrated in this system.

5.6 Measurement

5.6.1 Die photo and PCB design

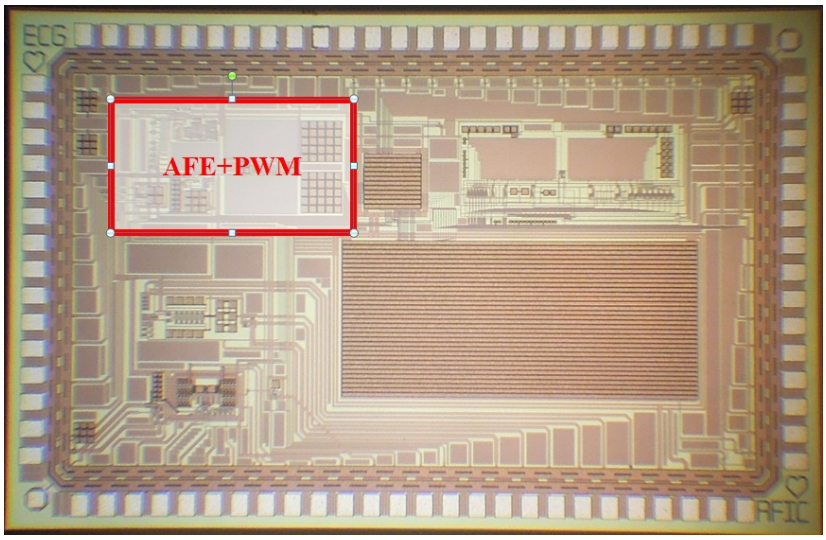


Fig. 5.6.1-1 Die photo of ECG monitoring system (Ver.2)

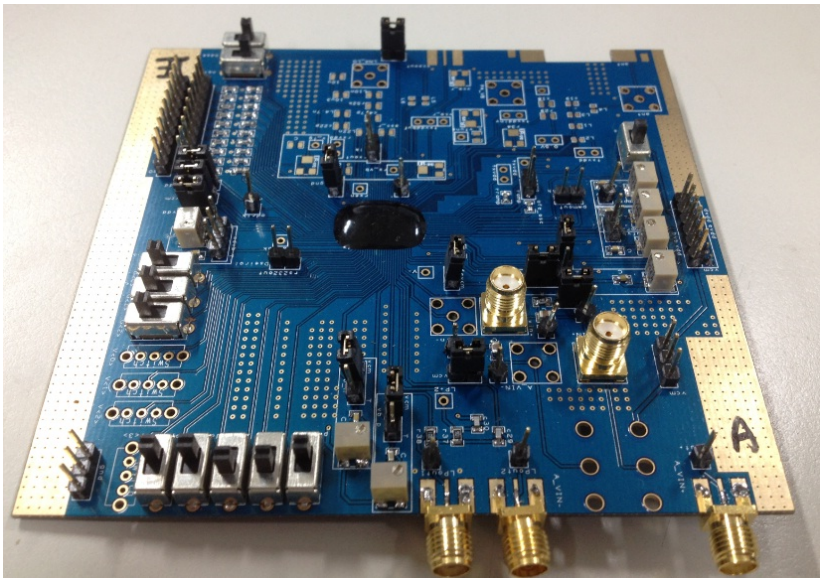


Fig. 5.6.1-2 PCB design of ECG monitoring system (Ver.2)

The die photograph and corresponding PCB design of the ECG monitoring system chip are shown in Fig. 5.6.1-1 and Fig. 5.6.1-2.

5.6.2 Measurement setup

We have introduced the AC response, noise, CMRR, and PSRR measurement setup in chapter 4. Here we introduce the ECG signal monitoring setup, just as Fig. 5.6.2-1 shows.

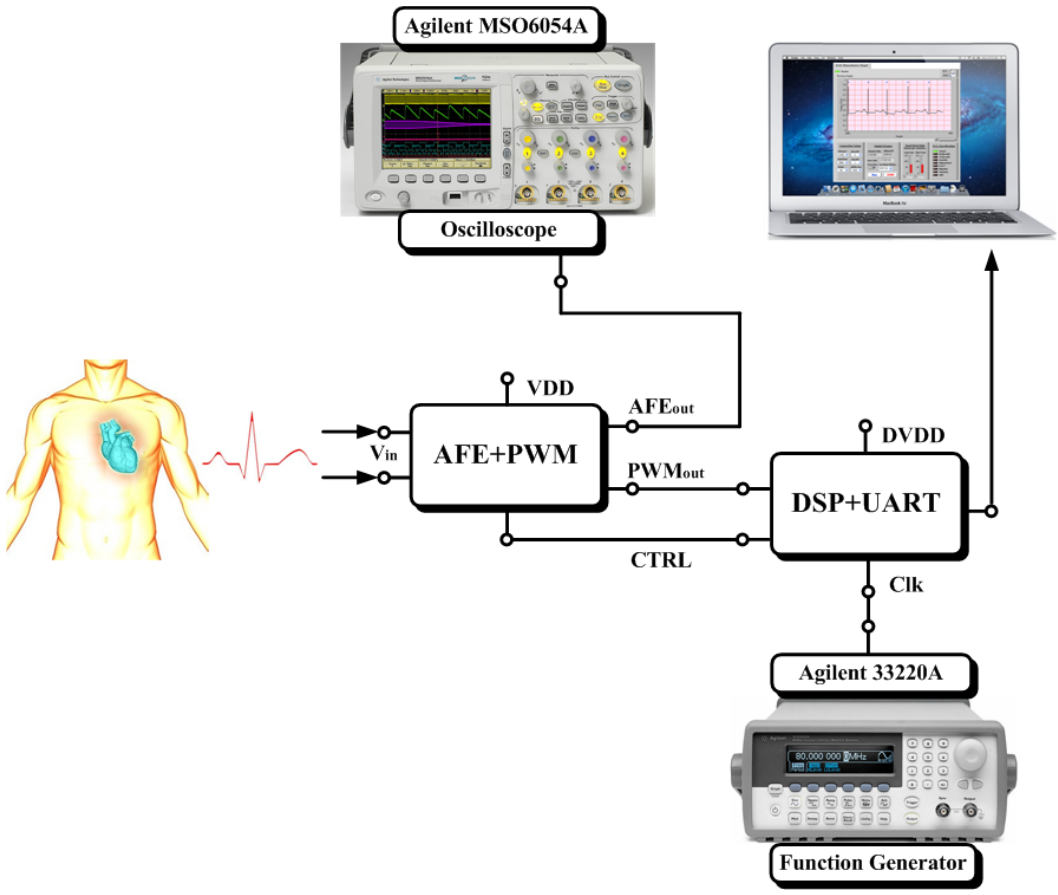


Fig. 5.6.2-1 ECG signal monitoring setup

The PWM circuit acts as an interface between the AFE and DSP circuit. First, the PWM circuit converts the analog signal into PWM signal. Then DSP circuit use counter to convert it into 10-bit data. After processing by the DSP circuit, the DSP circuit will transform the signal into RS232 format. Then the ECG signal will appears on the screen of laptop by using LabVIEW.

5.6.3 Measurement result

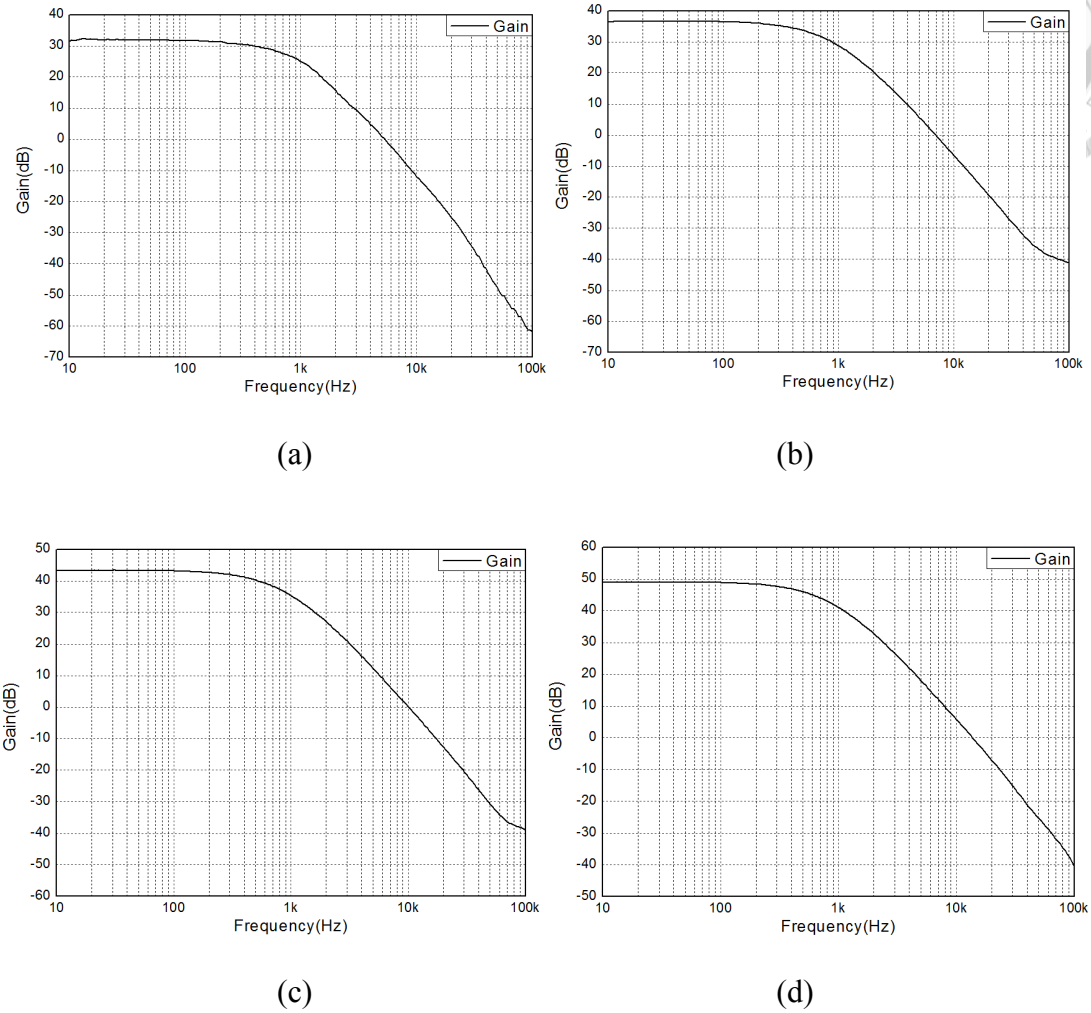


Fig. 5.6.3-1(a)(b)(c)(d) AC response measurement result of the AFE

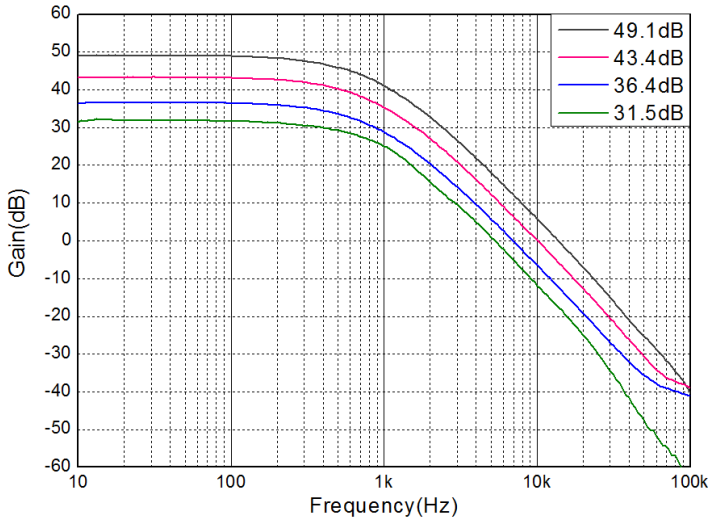


Fig. 5.6.3-2 AC response measurement result of the AFE

Fig. 5.6.3-1(a), (b), (c), and (d) depict the AC response measurement result of the AFE, respectively. Fig. 5.6.3-2 depicts the all the gain selection measurement result of the AFE in a picture. The gains are 31.5dB, 36.4dB, 43.4dB, and 49.1dB. The bandwidth of the AFE is about 500Hz. The CMRR and PSRR measurement result are depict in Fig. 5.6.3-3 and Fig. 5.6.3-4. It shows that CMRR > 100dB, and PSRR > 80dB. Fig. 5.6.3-5 shows the DC gain of the AFE. We can see that the output swing of the AFE is from 0.02V to 0.95V. Fig. 5.6.3-6 shows the input common mode range of rail-to-rail opamp, which evidence that the input common mode range is nearly rail-to-rail.

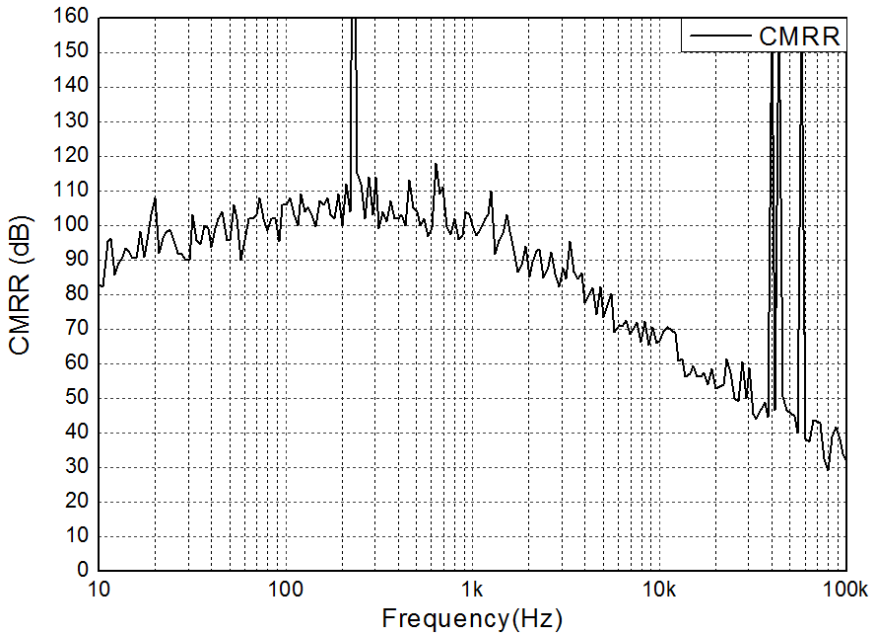


Fig. 5.6.3-3 CMRR measurement of the AFE

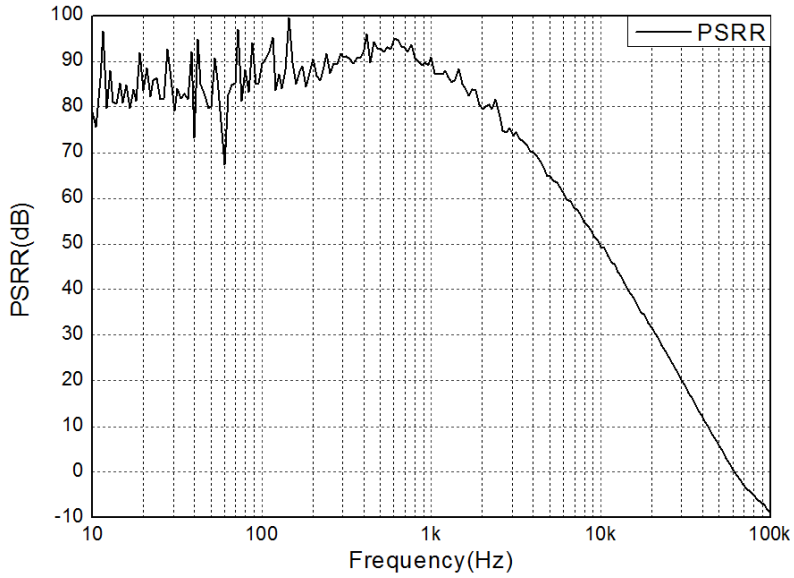


Fig. 5.6.3-4 PMRR measurement of the AFE

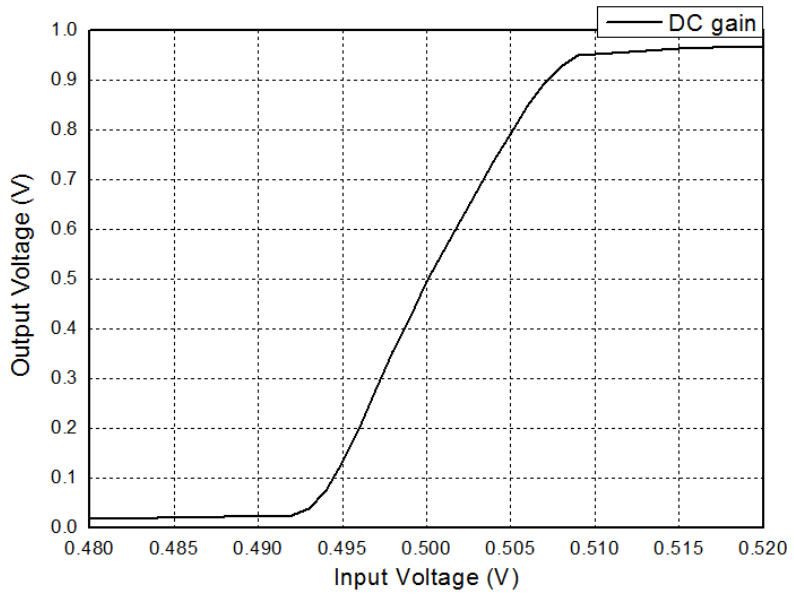


Fig. 5.6.3-5 DC gain of the AFE

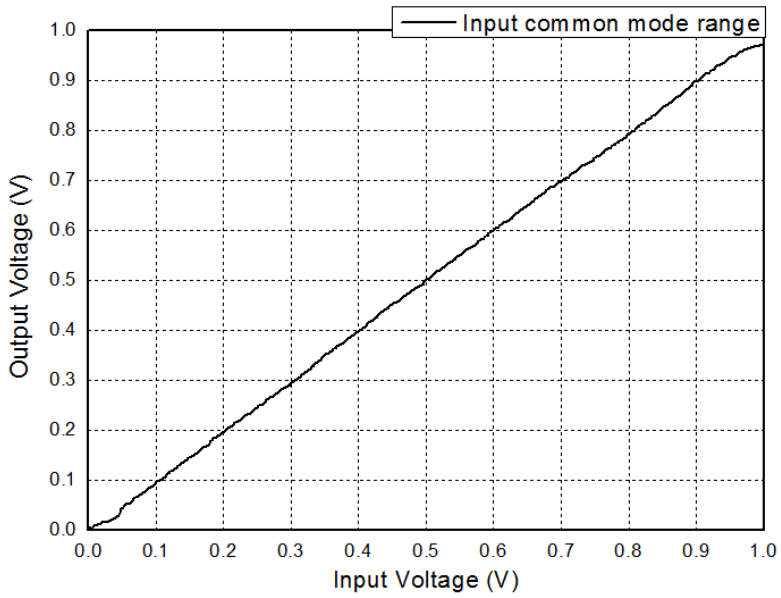


Fig. 5.6.3-6 Input common mode range of rail-to-rail opamp

Fig. 4.6.3-7 shows the input-referred noise spectrum of the AFE in log scale. We can see that with chopper technique, the flicker noise which is close to the baseband has been reduced. To see this figure in detail, we can examine Fig.5.6.3-8 and Fig.5.6.3-9, which depict the input-referred noise in log scale and linear scale, respectively. From these two pictures, it is obvious to know that the input-referred noise has been reduced to about 80 nV/$\sqrt{Hz}$. Fig. 5.6.3-10 depicts the output waveform of on-chip oscillator. The on-chip oscillator provides clock for chopper modulator. The chopping frequency here is about 4.3 kHz.

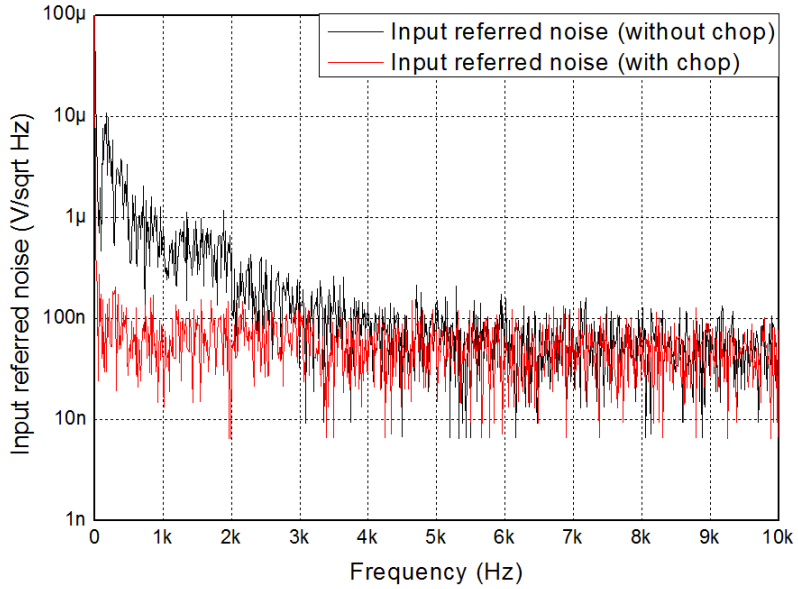


Fig. 5.6.3-7 Input-referred noise spectrum of AFE in log scale

(with and without chopper technique)

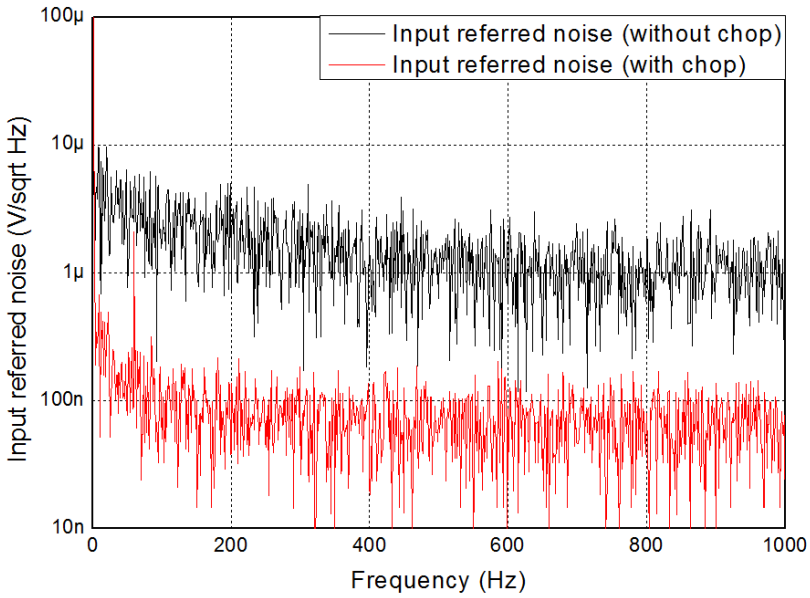


Fig. 5.6.3-8 Input-referred noise spectrum of AFE in log scale

(with and without chopper technique)

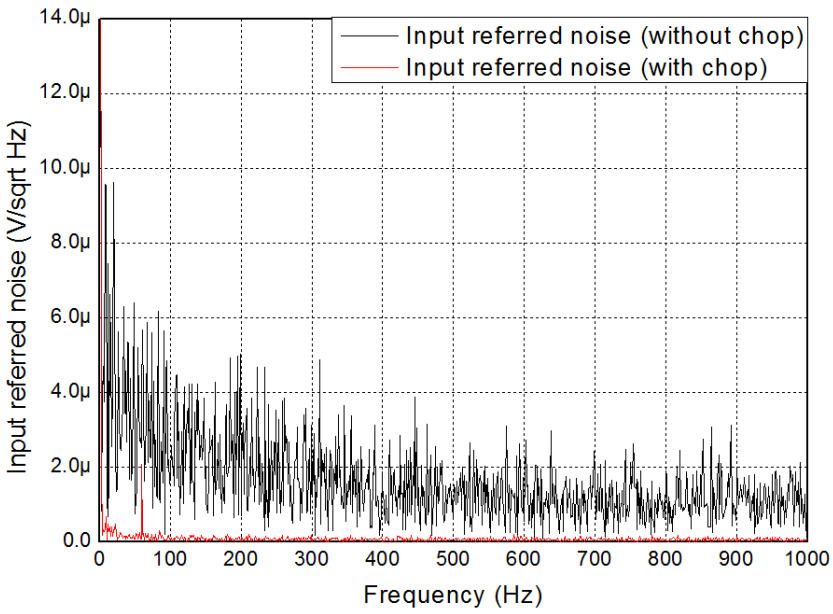


Fig. 5.6.3-9 Input-referred noise spectrum of AFE in linear scale

(with and without chopper technique)

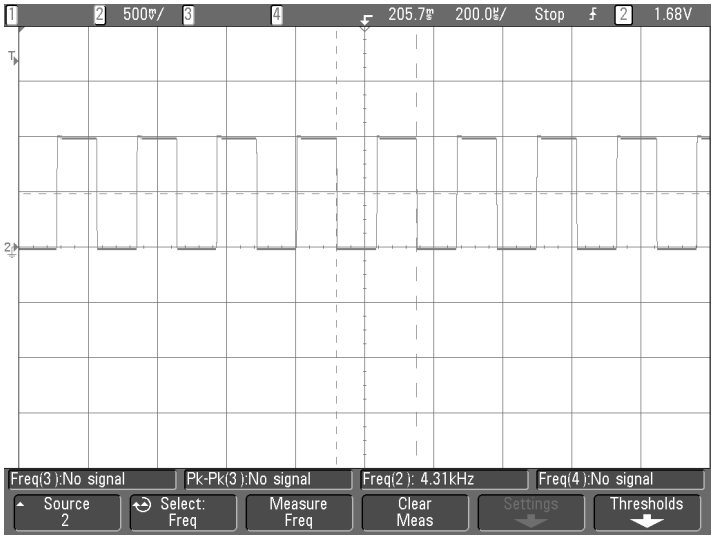


Fig. 5.6.3-10 Output waveform of the on-chip oscillator

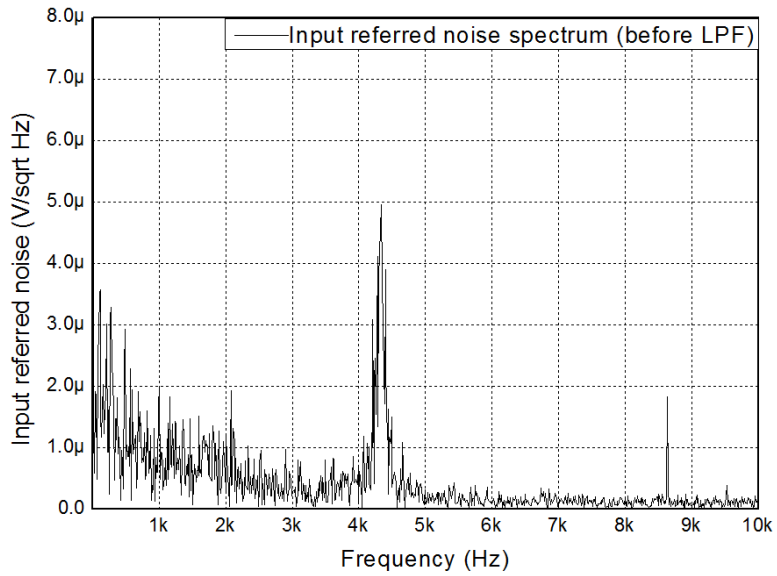


Fig. 5.6.3-11 Input-referred noise spectrum of AFE (before LPF)

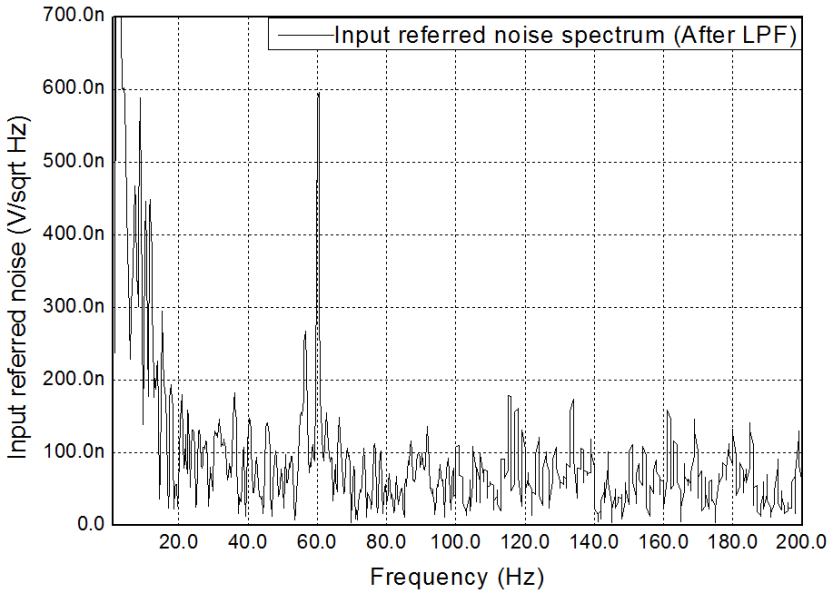


Fig. 5.6.3-12 Input-referred noise spectrum of AFE (after LPF)

Fig. 5.6.3-11 shows that before the signal enters the low pass filter, the noise will be chopped to the chopping frequency, which is 4.3 KHz here. Since the critical ECG signal bandwidth is located between 1Hz and 200Hz, we care about the input-referred

noise in this bandwidth. Fig. 5.6.3-12 shows the input-referred noise spectrum of the AFE in this bandwidth. The peak at 60Hz is the power line interference.

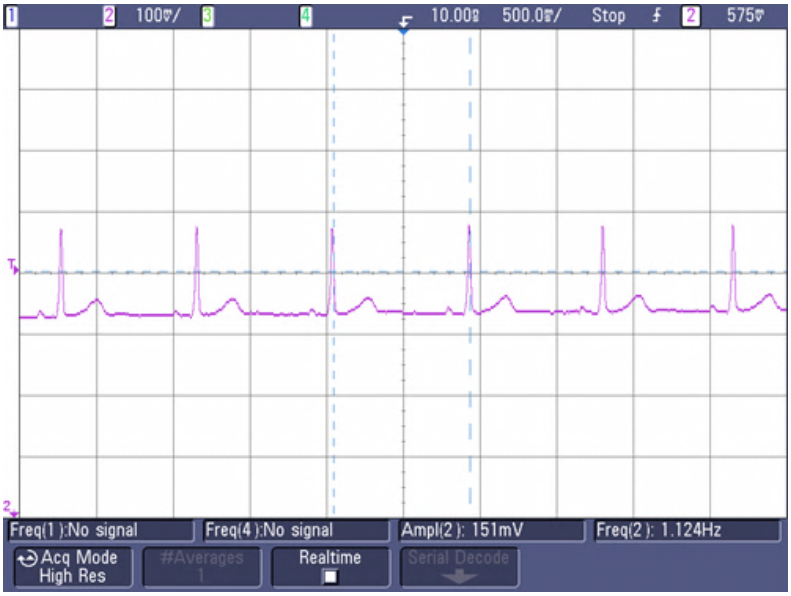


Fig. 5.6.3-13 ECG signal measurement result (analog signal)

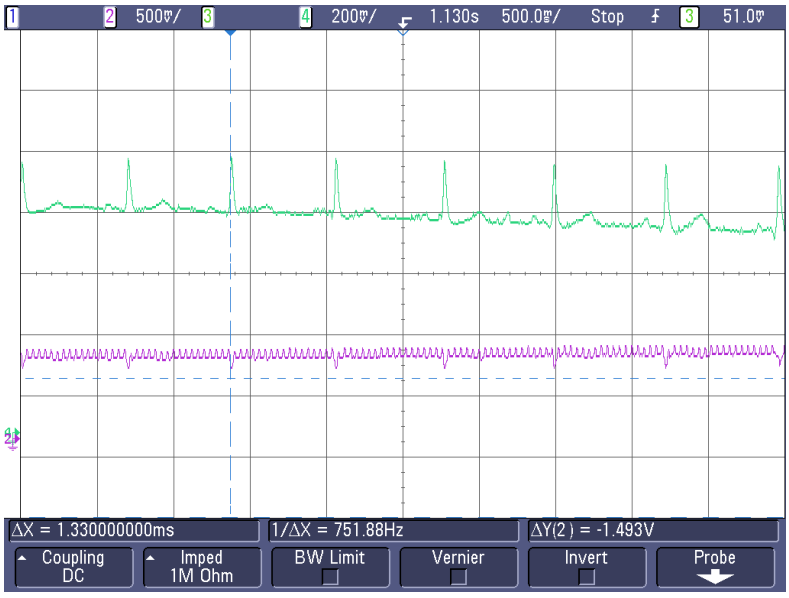


Fig. 5.6.3-14 ECG and PWM signal

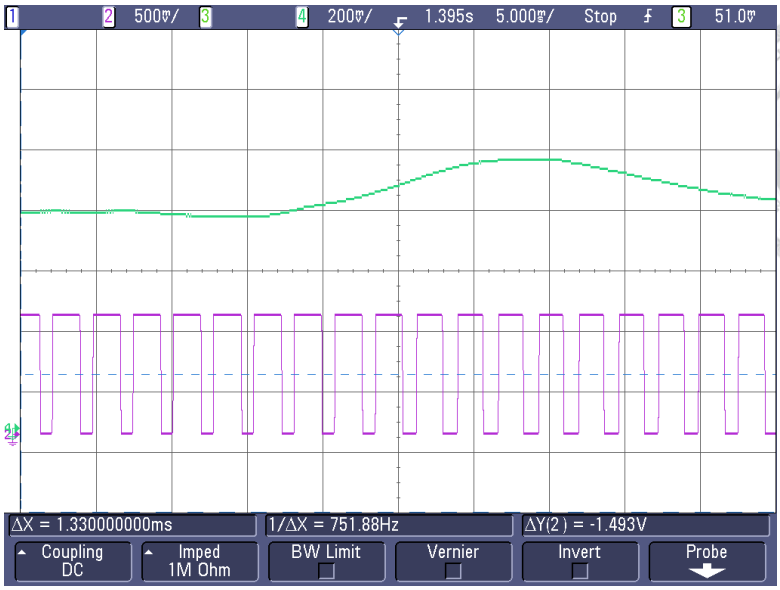


Fig. 5.6.3-15 ECG and PWM signal (Partial enlarged detail)

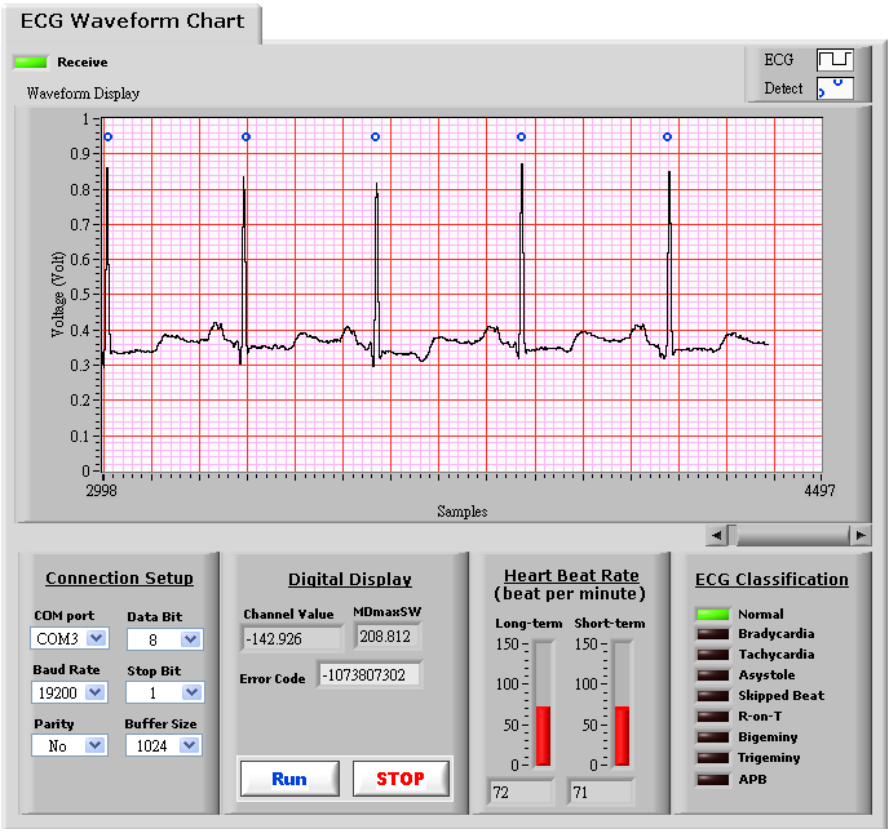


Fig. 5.6.3-16 ECG signal measurement result (digital signal)

The ECG signal measurement result is depicted in Fig. 4.6.3-13. The signal source is from a real person's heart and the measurement lead is Lead II. Fig. 5.6.3-14 and Fig. 5.6.3-15 shows the PWM interface testing result. The green line is ECG signal and the purple line shows the PWM signal. Due to the resolution of the oscilloscope, we must enlarge the scale of time domain to observe the PWM signal. Fig. 5.6.3-16 depicts the ECG signal, which is showing on the screen of laptop. We can see that the PWM interface is function work.

5.6 Summary

A biomedical analog front-end and pulse-width modulation circuit is presented and fabricated in TSMC 0.18μm 1P6M CMOS process. With the combination of instrumentation amplifier with chopper technique and programmable gain amplifier, the analog front-end can be simplified and the overall input-referred noise can be reduced. Besides, by using rail-to-rail amplifier for the core amplifier of the unity gain low-pass filter, the output swing can be enlarged nearly rail-to-rail. The pulse-width modulation circuit provides another solution to act as an interface between AFE and DSP. Table 5.6-1 shows the measured results of this work.

Table 5.6-1 Summary of measurement result

Features		**Performance**
Power supply		1V
Power	AFE	8uW
	PWM	5uW
Chopper frequency		4.3k Hz
Programmable gain selection		31.5dB, 36.4dB, 43.4dB, 49.1dB
Output swing		0.02V~0.95V
3dB frequency		450Hz
Input-referred noise density		80nV/$\sqrt{Hz}$
CMRR		>100dB
PSRR		>80dB

Chapter 6

Conclusion

With the growing pains suffered from chronic disease and the coming of aging society, there is a highly demand on personal telehealth systems. Fortunately, due to the dramatic development of semiconductor technology and the IC design industries, biomedical chips can be developed for sensing and monitoring bio-signals. It is possible for us to develop a wireless bio-signal monitoring SoC to realize telehealth service. It not only help people prevent illness in advance but also benefit their health that would increase their quality of life. To realize an ECG monitoring system, the analog front-end is a critical circuit block with the function of signal arrangement in the system. In this thesis, two kinds of low power and low noise analog front-end are proposed to lower the noise interference and provide a multiple gain selection.

In chapter 2, we introduce the ECG signal and the ECG monitoring system. At last, we focus on the introduction about the analog-front end for ECG signal monitoring application.

Chapter 3 begins with the discussion of noise and offset in CMOS circuits, then the low-noise and low-offset techniques such as auto-zero and chopper techniques are

introduced. The theory of chopper technique is especially discussed. In addition, sub-threshold conduction is also introduced in this chapter. Finally, some kinds of circuits in the analog front-end are presented.

In chapter 4, a current feedback instrumentation amplifier with a programmable gain amplifier for ECG signal detecting is proposed. By using chopper technique, the input referred noise of the CBIA is 90nV/$\sqrt{Hz}$ and the overall AFE is 1uV/$\sqrt{Hz}$. It provides four gain selections from 36dB to 54dB to meet the requirement for ECG signal detecting. The analog front-end only consumes 6uW based on the 1V voltage supply.

In chapter 5, an analog front-end with pulse-width modulation circuit is proposed. The pulse-width modulation circuit acts as an interface between analog front-end and digital signal processing circuit. The input referred noise of the analog-front end is 80nV/$\sqrt{Hz}$. Besides, it not only provides four gain selections from 30dB to 50dB, but also has high output swing. Based on the 1V voltage supply, the analog front-end consumes 8uW and the pulse-width modulation circuit consumes 5uW. Some parameters of AFE circuits are compared in table 6-1.

In conclusion, both of the simulation and measurement results show the high performance of the analog front-end proposed in this thesis. Thus, they are good for biomedical applications.

Table 6.1 Summary of measurement result

Features	[10] 2012 ISSCC	[9] 2011 JSSC	[33] Hsu Yu Pin	This work [Chap. 4]	This work [Chap. 5]
Process	0.18μm	0.5μm	0.35μm	0.18μm	0.18μm
Supply	1.2V	2V	3V	1V	1V
Power	9.6uW	10.6 uW	675 uW	6uW	8uW
Gain	NA	49.5dB, 53.9dB, 59dB, 62.3dB	58dB, 60dB, 64dB, 80dB	35.3dB, 41.1dB, 47.8dB, 53.3dB	31.5dB, 36.4dB, 43.4dB, 49.1dB
Output swing	NA	NA	0~3V	0.15V~ 0.75V	0.02V~ 0.95V
3dB frequency	NA	140Hz /170Hz	212Hz	450Hz	450Hz
Input referred noise density	130nV/$\sqrt{Hz}$	85nV/$\sqrt{Hz}$	70nV/$\sqrt{Hz}$	**CBIA** 90nV/$\sqrt{Hz}$ **AFE** 1uV/$\sqrt{Hz}$	80nV/$\sqrt{Hz}$
CMRR	120dB	>105dB	>100dB	>85dB	>100dB
PSRR	NA	NA	>80dB	>70dB	>80dB

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