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毫米波 *E* 頻段高頻譜效率互補式金氧半導體發射器之研究

E-band CMOS Transmitter Design for High Spectral Efficiency Wireless Communications

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煒恆

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摘要

本論文目的主要是討論利用台積電先進的 65 奈米互補式金氧半場效電晶體製程，設計 *E* 頻段高頻譜效率的次諧波直接昇頻發射器。首先針對多種在射頻發射鏈路傳輸的非理想效應，進行介紹與討論。為了改善上述非理想效應，我們透過對調變器負載的敏感度分析，設計一個在本地振盪器端寬頻帶低幅度與低相位失衡的 45°功率分配器，提供高階正交振幅調變訊號所需的高鏡像抑制機制。並藉由雙平衡次諧波吉伯特混頻器具有良好隔離度的特性，使用 65 奈米互補式金氧半場效電晶體製程，實現一個寬頻帶高鏡像抑制的 IQ 調變器。此調變器在 55 至 85 GHz 頻寬下，提供 0±1 dB 轉換增益。此外從 64 到 84 GHz，提供寬頻優於 40 dBc 的高鏡像抑制。

為了進一步驗證高速數位訊號調變的效能，我們設計高效率高增益四級功率放大器作為 60 GHz 高鏡像抑制的 IQ 調變器輸出級，以提高發射器的動態範圍。該發射器在 54 至 70 GHz 能提供 33 ± 0.5 dB 增益。以及在 114 毫瓦的總直流功率消耗下，有 11-dBm 的飽和輸出功率。發射器能在 1.7%誤差向量幅度之下，以 500 Mb/s 傳輸速率發射 1024-正交振幅調變信號。藉由本論文所提出的討論與分析，所設計的 60 GHz 高鏡像抑制發射器，其頻譜應用效率可以被進一步提升。

關鍵字：毫米波、互補式金氧半場效電晶體、鏡像抑制、1024-正交振幅調變、次諧波混波器

ABSTRACT

The main purpose of this dissertation is to design the *E*-band high spectral efficiency direct-conversion modulator and transmitter using TSMC 65-nm CMOS technology. First, the non-ideal effects on the RF transmitter are introduced and discussed. For high-order modulation scheme implementation, the RF impairments are mainly related to the non-linearity and in-phase/quadrature (IQ) imbalance. To maintain high image rejection ratio (low IQ imbalance) of the IQ modulator over a wide bandwidth, a load insensitive analysis and an local oscillator (LO) broadband 45° power splitter are proposed to achieve low amplitude and phase imbalanced structure. In addition, the doubly balanced sub-harmonic Gilbert-cell mixer with the advantages of good LO leakage suppression has been selected in the mixer design. The IQ modulator demonstrates a measured flat conversion gain of 0 ± 1 dB from 55 to 85 GHz. The image rejection ratio is better than 40 dBc from 64 to 84 GHz.

For the high speed digital modulation quality demonstration, the IQ modulator is integrated with a four-stage high gain high efficiency power amplifier (PA) to form a direct-conversion transmitter. The measured conversion gain of the transmitter is 33 ± 0.5 dB from 54 to 70 GHz. The saturated power is 11 dBm with total dc power consumption of 114 mW. A 1024-QAM modulated signal with a data rate of 500 Mb/s and 1.7% error vector magnitude (EVM) is successfully demonstrated at 65 GHz. Through the characteristics of high image rejection and the superior LO signal suppression, the system capacity of proposed 60-GHz direct-conversion transmitter can be further improved.

Index Terms — Millimeter-wave (MMW), CMOS, image rejection ratio (IRR), 1024-QAM, sub-harmonic mixer.

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Chapter 1 Introduction

1.1 Motivation

Due to the demand for multi-gigabit wireless links, many efforts have been devoted for broadband millimeter-wave (MMW) communication system. To achieve higher speed data transfer, more frequency bandwidth is needed. In recent years, as shown in Fig. 1.1, the released 57 to 64 GHz non-licensed band, and 71-76, 81-86 GHz light licensed band make them ideal for high data wireless communications [1], [2]. The huge bandwidth has made MMW radios promising candidates for multi-gigabit rates in point-to-multipoint and point-to-point applications. According to IEEE 802.15.3c standard, four channels of maximum 2.16-GHz bandwidth were defined around the 60-GHz frequency [3], [4]. This channel allocation is also common for IEEE 802.11ad [5], WiGig [6] and WirelessHD [7] standards, as shown in Fig. 1.2. It is capable of providing up to 6.75 Gbps throughput using approximately 2 GHz of spectrum at 60 GHz over a short range.

Consequently, many 60-GHz transceivers with different architecture implemented by different technology have been reported in this field [3], [4], [8], [9]. The 60 GHz

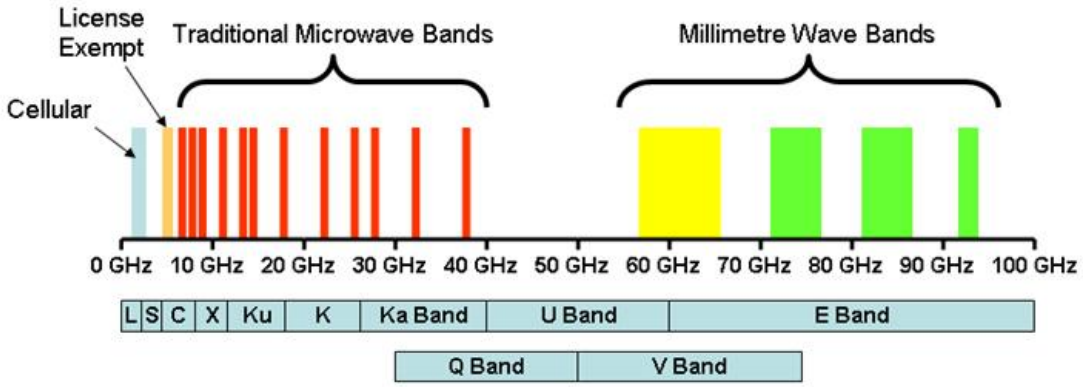


Fig. 1.1. All available frequency bands for microwave radio applications.

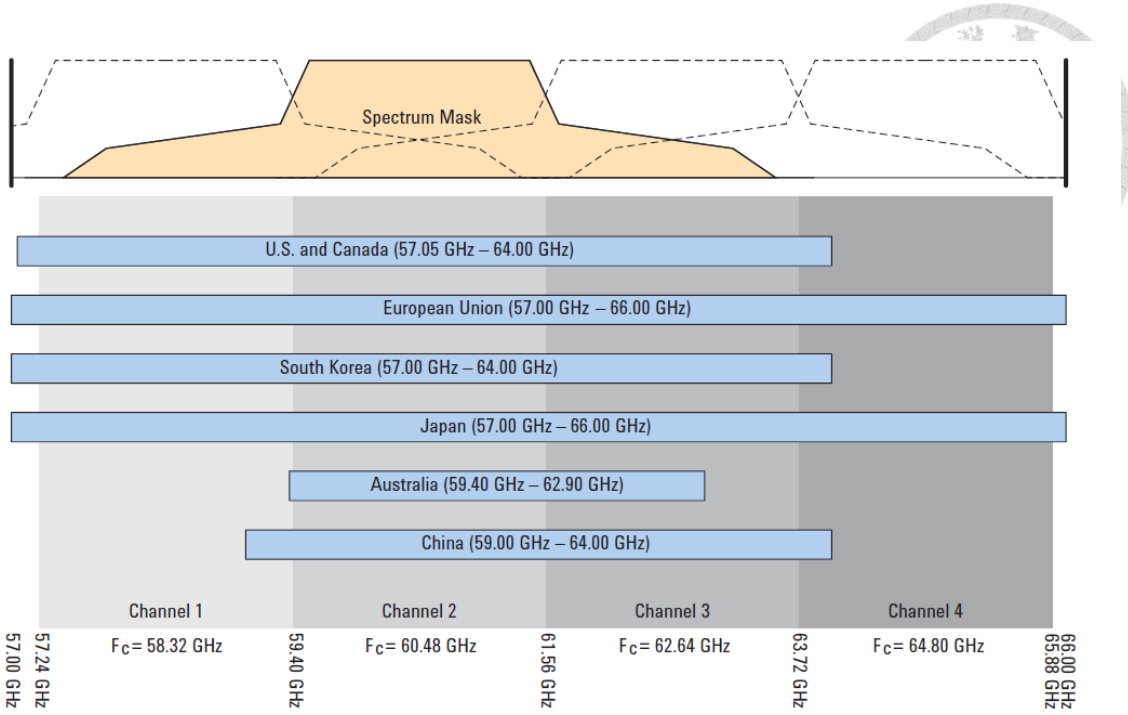


Fig. 1.2. The 60GHz band channel plan and frequency allocations by region.

wireless transceiver with the highest data rate 20 Gbps in 16QAM modulation is reported in 2013 [10]. However, the next question arises as to how much more efficiently bandwidth can be used in the modulation domain. Therefore, our research interests focus on improving the spectral efficiency of the system.

Besides, as the continued maturation of CMOS technology, the low power consumption and green-mode operation are increasing concerns at MMW band. The low power RF transceiver front-end is also discussed and designed in this dissertation.

1.2 Literature Survey

Nowadays the wireless communications and networks are moving toward high data-rate transmission and high spectral efficiency. The cost of using higher order QAM to improve spectral efficiency is that the transceiver requires a higher signal to noise ratio (SNR) with the same level of error rate performance. One of the dominant vectors

on SNR degradation is I/Q imbalance (gains and phases error) [11]. In practice, the imperfect components characteristics (exactly quadrature phase, equal gains, and so on) of the transceiver contribute to the IQ mismatch. For example, the finite sideband image of the transmitter signal from IQ mismatch degrades signal quality.

Therefore, many efforts have been devoted to IQ mismatch calibration. The predistortion filtering techniques [12]-[14] and the direct calibration approach [15] using digital signal processing (DSP) to compensate for IQ imbalance effects are investigated and presented. The other calibration methods based on the phase detector and power limiter are used in [16]-[17]. However, most of the compensation techniques result in limitation of bandwidth, which restrict to its development on wireless multi-gigabit data transmission. In addition, the digital compensation technique required detect and control circuits which increased additional dc power consumption and circuit area.

For MMW broadband communication applications, a hybrid compensation with phase calibration mechanisms on LO signal path and variable gain amplifiers (VGAs) on IF path to correct IQ magnitude mismatches has been reported and implemented within the 70-100 GHz band. With calibration, the image signal at 90GHz can be suppressed to below 40dB [18]. The other power-locked loop technique for amplitude calibration is proposed for V-band IQ modulator and demodulator design. Unrestricted to bandwidth limitations of couplers and process variations, this circuit demonstrates excellent SSR higher than 35 dBc from 51 to 68 GHz [19]. However, to obtain better accuracy and sensitivity of the calibration technique, it needs more power consumption and system complexity for control circuits.

1.3 Contributions

In this dissertation, we propose an effective compensation technique for direct-conversion IQ modulator and transmitter with reduced complexity and zero power consumption to solve IQ imbalance problem from practical imperfect MMW components, which can greatly reduce the amplitude and phase imbalance and then enhance the bandwidth efficiency of the system.

Briefly speaking, the proposed compensation mechanism is rendered the quadrature generator with ultra-low amplitude and phase imbalance. Firstly, a load-insensitive analysis is introduced to determine the topology with minimum performance deviation. Moreover, the proposed LO broadband 45° power splitter, as the quadrature generator of sub-harmonic mixer, is composed of the high-pass filter (HPF)/low-pass filter (LPF) section used for equal group delay generation [20] and the unequal power divider designed for amplitude mismatch compensation. With the combination of two modified sections, the amplitude imbalance is less than 0.04 dB, and the phase difference is less the 0.5° from 32 to 45 GHz for half-LO frequency.

In addition, for a high spectral efficiency modulator implementation, the RF impairments are also related to nonlinearity and LO leakage. To reduce the LO leakage, the doubly balanced sub-harmonic Gilbert-cell mixer with the advantages of superior isolation has been selected in the mixer design. The integrated MMW LO four-way quadrature divider is modified with low phase difference further improving the LO leakage suppression. According to the above, our IQ modulator demonstrates a measured image rejection ratio better than 40 dBc from 64 to 84 GHz.

Compared to the computational power of signal processing, which is a power hungry algorithm especially for multi-gigabit applications, the proposed compensation skill can

provide an ultra-low-power mismatch calibration for more than 10-GHz bandwidth.

Besides, for low-power high integrated transmitter front-end design, the high efficiency 60-GHz power amplifier is designed and implemented. In the past, the major concerns for the MMW front-end circuit design were area and performance. Recent advances in fabrication technology, low power has emerged as a principal issue of electronics industries. For the 60-GHz low-power application, this dissertation describes a broadband high efficiency power amplifier. By applying direct-combining topology and simplified first-order matching network, the MMIC demonstrates the highest PAE 23.4% and 42% drain efficiency at the 60-GHz band.

Additionally, owing to the increasing demand for low power application, the research in the 60-GHz low power low noise amplifier (LNA) is also investigated. By using forward body-bias technique, the 60-GHz LNA under 0.6-V and 4.8-mW dc power can achieve a peak gain of 16.5 dB at 58 GHz and 1-dB bandwidth from 54 to 61 GHz with a compact chip size. The experimental result shows the outstanding gain performance by the ratio of gain bandwidth product (GBP) to dc power for low power applications.

Furthermore, the high image rejection modulator with superior LO leakage suppression is integrated with high efficiency PA to form the 60-GHz transmitter. With all advantages and characteristics of our design, a 1024-QAM modulated signal is successfully demonstrated at 65 GHz. The 60-GHz direct-conversion transmitter shows a relatively cost-effective way to improve the capacity in high-speed application.

1.4 Organization of this Dissertation

The dissertation is composed of five chapters. The organization is outlined as follow:

In chapter 2, the non-ideal effects which degrade the SNR will be discussed. The proposed structure for MMW IQ-imbalance compensation is investigated. Then, an *E*-band high image-rejection sub-harmonic IQ modulator for a high-order QAM signal using standard 65-nm CMOS technology is designed and implemented. The design method and measured results are presented. The proposed scheme is verified to be valid and effective.

Chapter 3 introduces the design and implementation of the energy efficient V-band PA and LNA. A high efficiency PA in 65nm CMOS technology is introduced firstly. Then, another broadband 60-GHz LNA design for low power application using 90 nm CMOS process is presented.

In chapter4, the 60-GHz direct-conversion transmitter is designed and implemented. The transmitter composed of a high image rejection 60-GHz modulator and a four-stage linear amplifier is designed in 65-nm CMOS process. This monolithic microwave integrated circuit (MMIC) with high spectral efficient modulated 1024-QAM signal test is demonstrated.

In the end, chapter 5 gives the brief conclusions of this dissertation.

Chapter 2 High Image Rejection *E*-band Sub-Harmonic IQ-Modulator in 65-nm CMOS Process

2.1 Introduction

For the future cellular backhaul links, the demand of broad bandwidth to deliver multi-gigabit data transmission is significantly increased. In comparison with the traditional microwave bands, the 57–66-, 71–76-, and 81–86-GHz MMW bands offer multi-gigabit data rates through multi-gigahertz channels [21]. The direct conversion architecture with advantages of minimal hardware, no costly analog image rejection filter, and wider bandwidths is attractive for broadband MMW applications. However, the major drawback of the direct conversion transceiver implementation is the sensitivity degradation due to DC-offset generation, flicker noise, and inter-modulation distortion. Besides, the limited accuracy of the analog hardware causes amplitude and phase mismatches between the components in the I- and Q-branch of the transceiver, and is referred as I/Q imbalance. Nonideal quadrature splitting of the LO and/or gain mismatch between the I- and Q-channels will degrade EVM [22].

2.1.1 Error Vector Magnitude

EVM is a measure used to quantify the performance of how accurately a radio is transmitting symbols within its constellation. For the wireless communications systems, the various imperfections of limited accuracy in the implementation (such as carrier leakage, low image rejection ratio, phase noise etc.) cause the actual constellation points to deviate from the ideal locations [23]-[25].

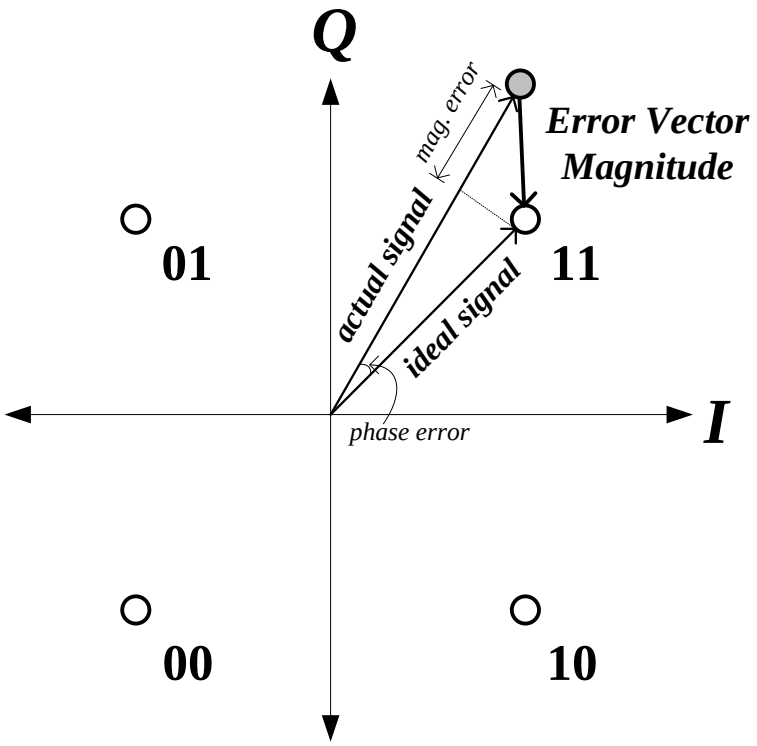


Fig. 2.1. The illustration of Error Vector Magnitude.

For example, in Fig. 2.1, we have a QPSK constellation with 2 bits per symbol. At this instant in Fig. 2.1, suppose we are transmitting the symbol pointed to by the ideal signal vector. The difference between the ideal signal vector and the actual signal vector is the error vector. The magnitude of the error vector is EVM. Hence, we can write EVM mathematically as:

$$EVM = 10\log\left(\frac{|Error\ Vector|}{Average\ Symbol\ power}\right)\ [\text{dB}] \quad . \tag{1}$$

2.1.2 IQ Imbalance and Image Rejection Ratio

As stated earlier, IQ imbalance has been identified as one of the most serious concerns in direct-conversion system, which causes the unwanted image signal, reduces SNR and

increases bit error rate (BER). The IQ imbalance between the I- and Q-branch upon the IF signal up-converting to RF output damages the constellation diagram distribution. Fig. 2.2 shows the constellation diagram asymmetry due to IQ impairment from amplitude and phase imbalance.

To discuss the influence of IQ imbalance on the RF transceiver, we assume that IF IQ signals have perfectly matched phase and amplitude, and all the amplitude and phase errors occur at LO injected signals. To simplify the problem, the amplitude and phase mismatch are denoted as and ε and $\phi/2$, respectively. After all the amplitudes of signals are normalized, the imbalanced IQ signals can be expressed, respectively, as

$$IF\_I = A_{IF}\cos(\omega_{IF}t) \tag{2a}$$

$$IF\_Q = A_{IF}\sin(\omega_{IF}t) \tag{2b}$$

$$LO\_I = (1+\varepsilon)A_{LO}\cos(\omega_{LO}t + \phi/2) \tag{2c}$$

$$LO\_Q = A_{LO}\cos(\omega_{LO}t + 45^{o}), \tag{2d}$$

respectively. The output signal of I-mixer and Q-mixer at RF output port can be written as

$$RF\_I = (1+\varepsilon)A_{RF}\cos(\omega_{2LO}t + \phi)\cos(\omega_{IF}t) \tag{3a}$$

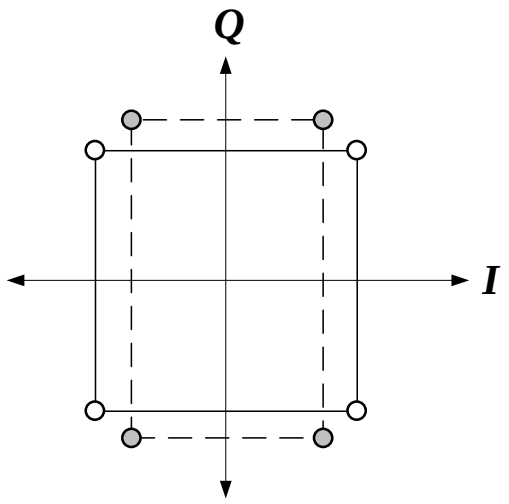
$$RF\_Q = -A_{RF}\sin(\omega_{2LO}t)\sin(\omega_{IF}t), \tag{3b}$$

respectively.

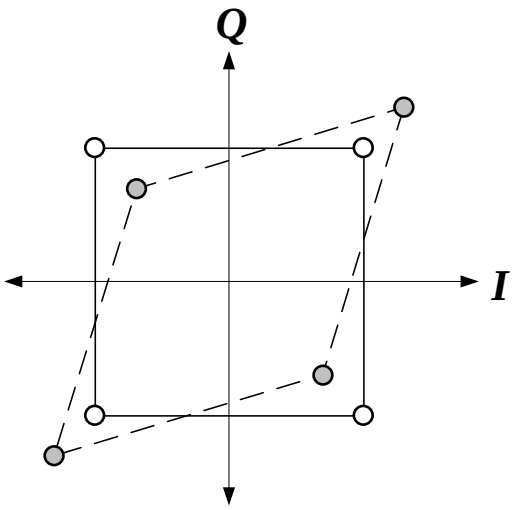
By trigonometric identities, we obtain

$$RF\_I = \frac{1}{2}(1+\varepsilon)A_{RF}\begin{Bmatrix}\cos\left[(\omega_{2LO}+\omega_{IF})t+\phi\right]+\\ \cos\left[(\omega_{2LO}-\omega_{IF})t+\phi\right]\end{Bmatrix} \tag{4a}$$

$$RF\_Q = \frac{1}{2}A_{RF}\left\{\left[\cos(\omega_{2LO}+\omega_{IF})t\right]-\left[\cos(\omega_{2LO}-\omega_{IF})t\right]\right\}. \tag{4b}$$



Amplitude Imblance



Phase Imblance

Fig. 2.2. The effect of I/Q gain and phase imbalance on QPSK signal.

Then we can separate the upper sideband (USB) and lower sideband (LSB) of RF output signal as:

$$\frac{RF_{lower}}{RF_{upper}} = \frac{\{(1+\varepsilon)cos[(\omega_{2LO}-\omega_{IF})t+\phi]-cos(\omega_{2LO}-\omega_{IF})t\}}{\{(1+\varepsilon)cos[(\omega_{2LO}+\omega_{IF})t+\phi]+cos(\omega_{2LO}+\omega_{IF})t\}}, \quad (5)$$

where

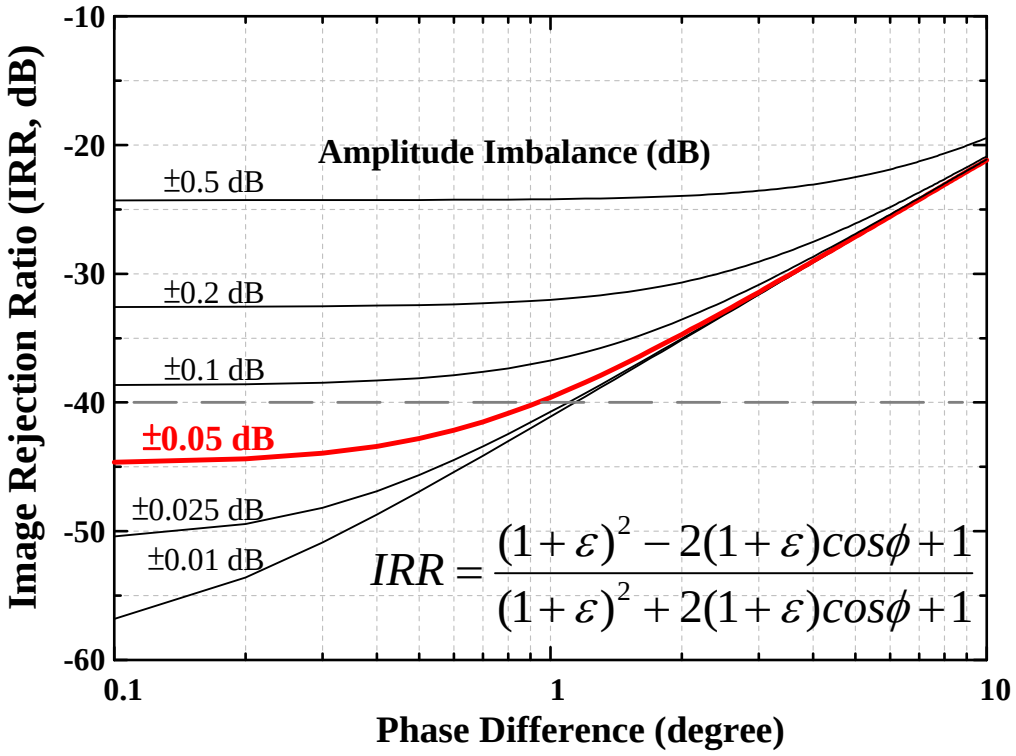


Fig. 2.3. The image rejection ratio (IRR) of Eq. (6) in a modulator with IQ amplitude and phase mismatch.

$$a = (1+\varepsilon)cos\left[(\omega_{2LO} + \omega_{IF})t + \phi\right],\ \ b = cos(\omega_{2LO} + \omega_{IF})t$$
$$c = (1+\varepsilon)cos\left[(\omega_{2LO} - \omega_{IF})t + \phi\right],\ \ d = cos(\omega_{2LO} - \omega_{IF})t\ .$$

The IRR was defined as average power of LSB (image signal) to USB (desired output RF signal) RF^2_{lower} / RF^2_{upper}:

$$IRR = \frac{RF^2_{lower}}{RF^2_{upper}} = \left|\frac{\int_T 4(c^2 - 2cd + d^2)dt}{\int_T 4(a^2 + 2ab + b^2)dt}\right| = \frac{(1+\varepsilon)^2 - 2(1+\varepsilon)cos\phi + 1}{(1+\varepsilon)^2 + 2(1+\varepsilon)cos\phi + 1}\ . \qquad (6)$$

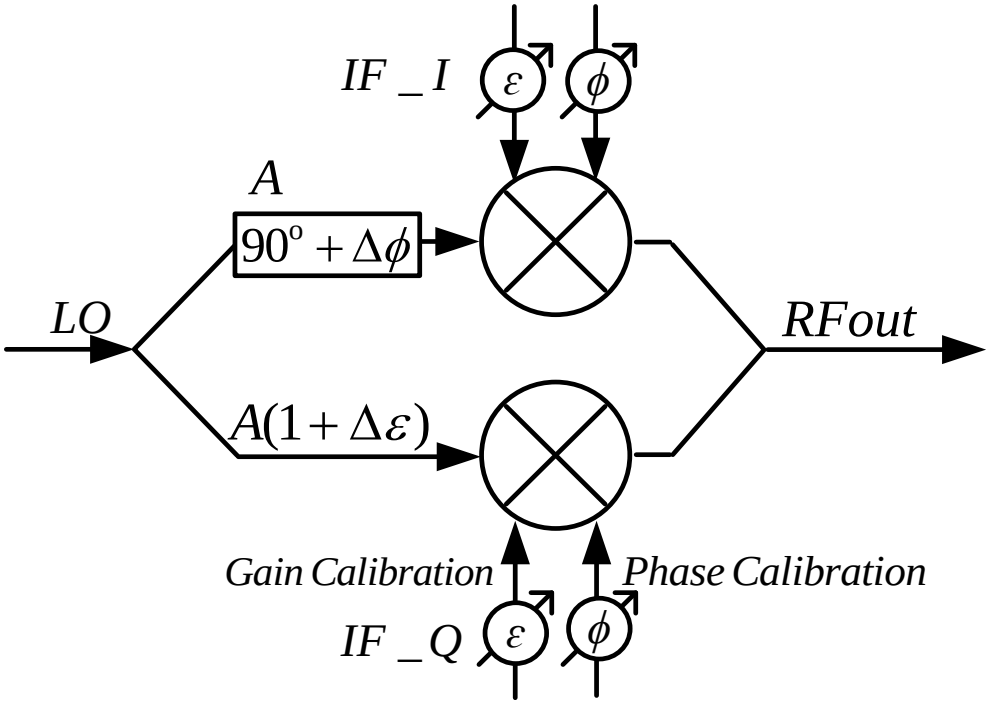
Fig. 2.3 plots the image rejection ratio versus amplitude and phase imbalance. To provide a high link spectral efficiency, a low IQ mismatch and high image rejection IQ modulator is a design issue. The quantitative relationship between the image rejection ratio of a receiver and the acceptable symbol error probability for system consideration

has been discussed in [24]. The IQ mismatch degrades the system performance with respect to the reference case of the balanced IQ signals. However, for high modulation orders, such as 64-QAM, an IRR in the order of -30 dBc to -40 dBc is sufficient to keep the system performance acceptable [24], [25]. As indicated in Fig. 2.3, to achieve an image rejection ratio of -40 dBc, the IQ imbalance should be within 0.5° phase difference and 0.05 dB amplitude imbalance. However, as the operation frequency moved toward MMW bands, the wavelength of I and Q signals are similar to CMOS chip size, thus it is difficult to maintain perfect IQ match. Therefore, a low amplitude and phase imbalanced design strategy will be discussed and demonstrated in the following section for broadband and high image rejection IQ modulator.

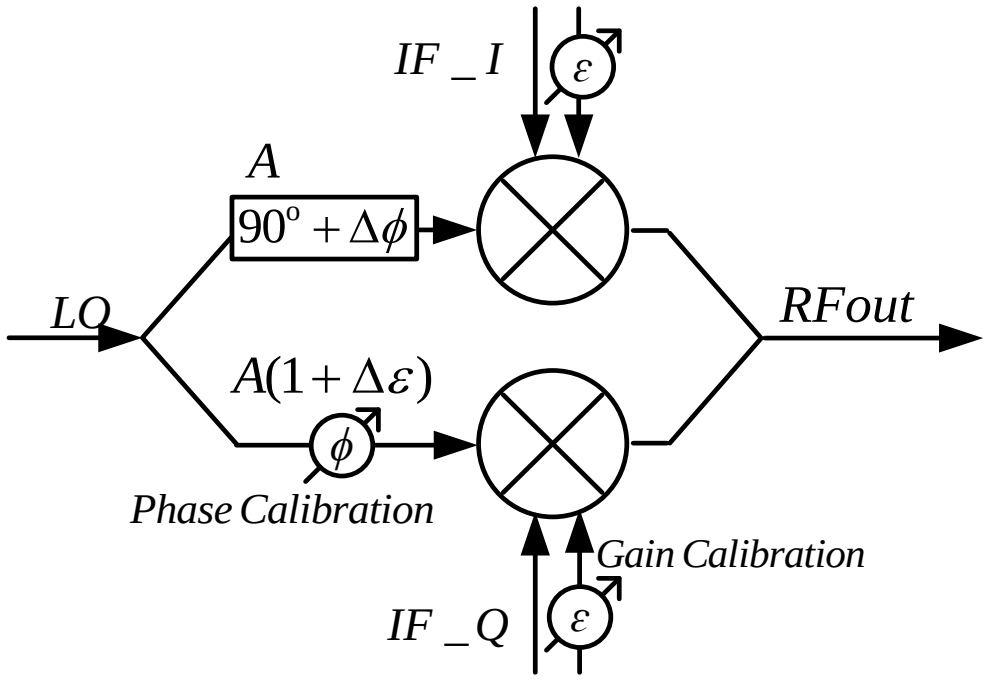
2.2 IQ compensation techniques

For high QAM modulator implementation, the RF impairments are mainly related to the nonlinearity and IQ mismatch. Although the linearity requirement can be reduced through power back-off, the IQ mismatch needs to be mitigated through careful topology selection and parasitic insensitive design methodology.

To solve the IQ mismatch, several calibration techniques are reported [11]–[19], [26]–[29]. The IF compensation using digital [26], [27] and mixed-mode [28] techniques for IQ mismatch compensation on IF path have been demonstrated under 2 GHz, as illustrated in Fig. 2.4 (a). However, the digital compensation technique required detect and control circuits which increase additional dc power consumption and circuit area. In addition, most of the IF compensation techniques result in limited of bandwidth. For MMW broadband communication applications, a hybrid IF/RF compensation with



(a)



(b)

Fig. 2.4. IQ compensation techniques: (a) Digital compensation on IF. (b) Phase compensation on LO and amplitude compensation on IF.

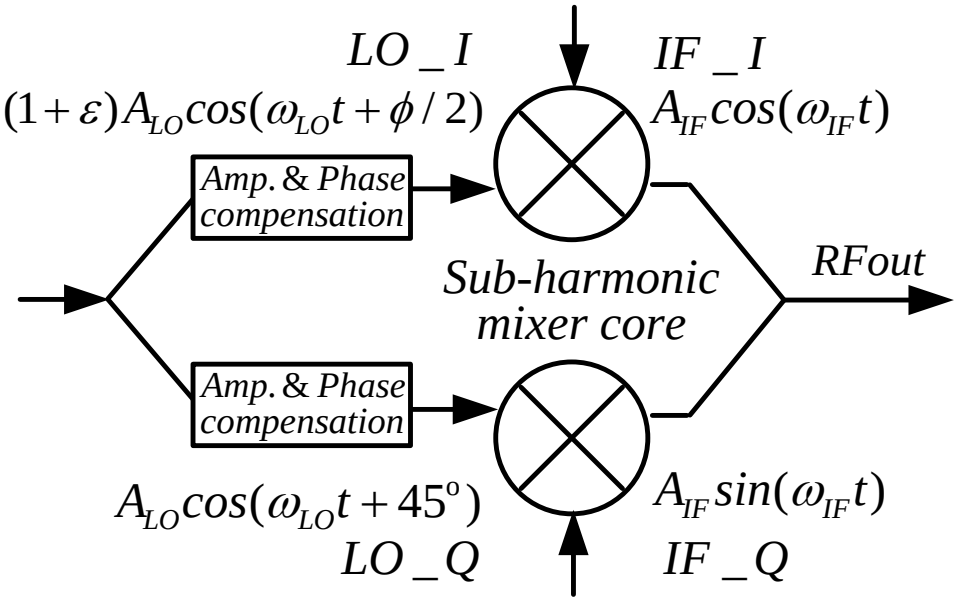


Fig. 2.5. Sub-harmonic IQ modulator with broadband phase and amplitude compensation on LO.

phase calibration on LO signal path and VGAs on IF path to correct I/Q magnitude mismatches is illustrated in Fig. 2.4 (b) [18]. The calibration mechanisms can be implemented within the 70–100-GHz band and the IRR can be suppressed below 40 dBc. A 256-QAM constellation with 3% EVM is demonstrated at 90 GHz.

In this chapter, a load insensitive analysis is proposed to achieve high IRR of the modulator over a wide bandwidth for high data-rate application. In addition, an LO broadband 45° power splitter with amplitude and phase compensation for a sub-harmonic IQ modulator is adopted to achieve a low amplitude and phase imbalanced structure, as shown in Fig.2.5.

Compared with IF path calibration, the LO path calibration can provide a broad bandwidth compensation. After the LO path IQ calibration, the IRR of the presented sub-harmonic IQ modulator is below 40 dBc over a wide bandwidth from 64 to 84 GHz.

2.3 Circuit Design

2.3.1 Sub-harmonic Gilbert-Cell Mixer with Built-in LO buffer Design

As previously discussed, the image rejection ratio is an important indicator of the balance condition between I- and Q-path in a high-order QAM modulator. However, before we concentrate on the problem of IQ mismatch in the circuit design, the LO leakage is also an important design issue in the RF transceiver system, especially for direct conversion architecture [30]. Since the LO and RF frequency is at the same band in the direct conversion system, the strong LO leakage power will desensitize the following stage PA of the transmitter. In addition, the LO leakage will degrade the EVM performance of the transmitter [31]. Hence, to reduce the burden on our design, we want to ameliorate the LO leakage problem through architecture selection before the face of the IQ mismatch problem.

To reduce the LO leakage, the sub-harmonic mixer is selected in our design. The primary advantage of implementing subharmonically pumped mixer is the inherent enhanced LO-to-RF isolation. Besides, the LO oscillator frequency is at half of the RF frequency, which is very desirable at upper millimeter wave frequency operation. And the RF and LO frequencies are widely separated, which facilitates the construction of the filter. These advantage directly translate to lower costs while maintaining the electrical performance of the system. As to the problems with large conversion losses and LO drivien power, we designed a built-in buffer with broadband matching network, which simultaneously lower the driven LO power and achieve good conversion gain performance. We will discuss in the following section.

Therefore the doubly balanced sub-harmonic Gilbert-cell mixer with the outstanding spur suppression is utilized in the proposed modulator design to substantially

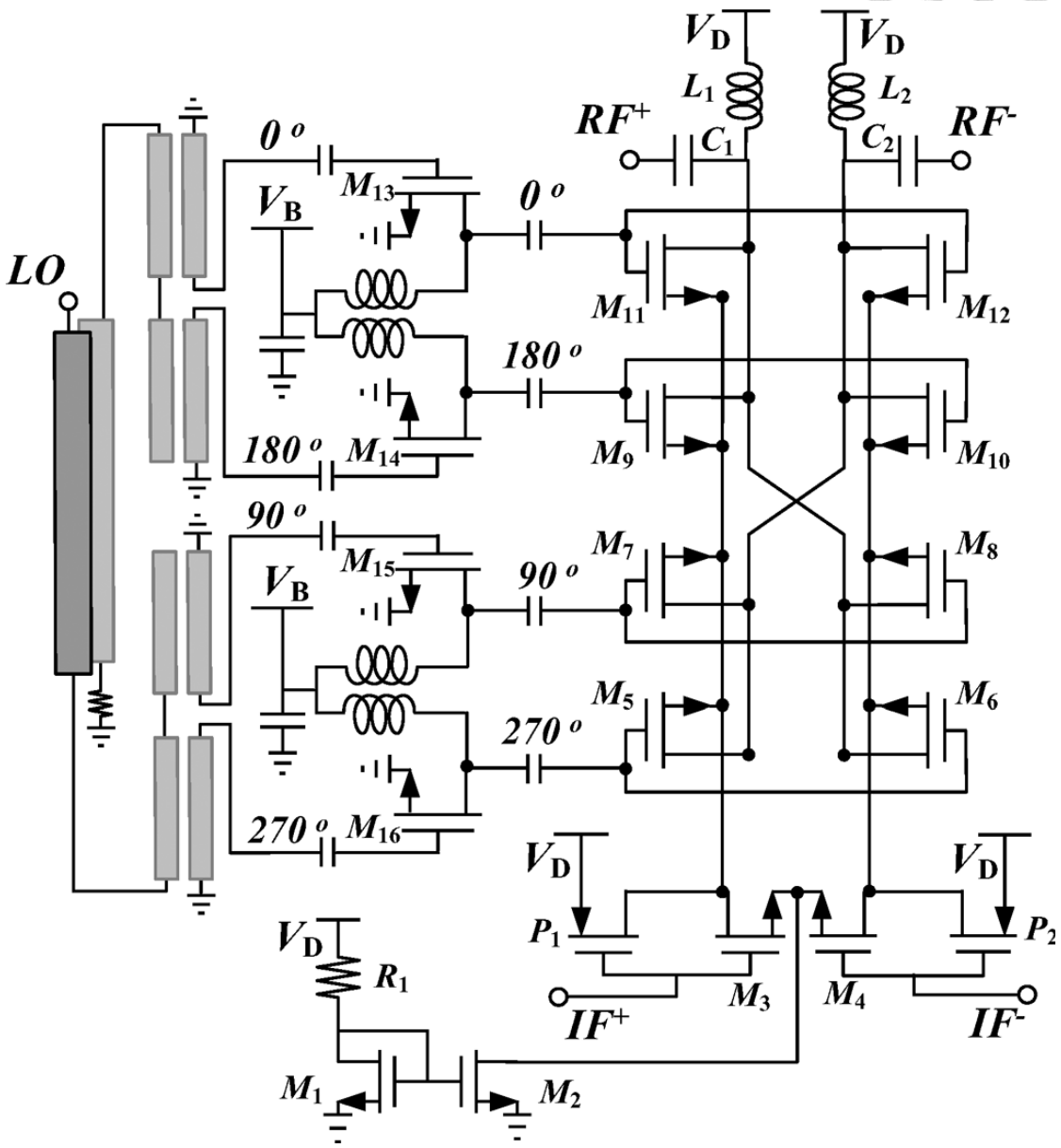


Fig. 2.6. Schematic of the *E*-band CMOS sub-harmonic up-conversion Gilbert-cell mixer.

alleviate the LO leakage problem [32], [33]. The schematic of the sub-harmonic Gilbert-cell up-conversion mixer is illustrated in Fig. 2.6. The current mirror source implemented by R1 (820 Ω), nMOS M_1 (128μm/0.06μm) and M_2 (8μm/0.06μm) is used to provide the tail current. The transconductance stage is realized by two inverter composed of nMOS M_3, M_4 (128μm/0.06μm) and pMOS P_1, P_2 (64μm/0.06μm).

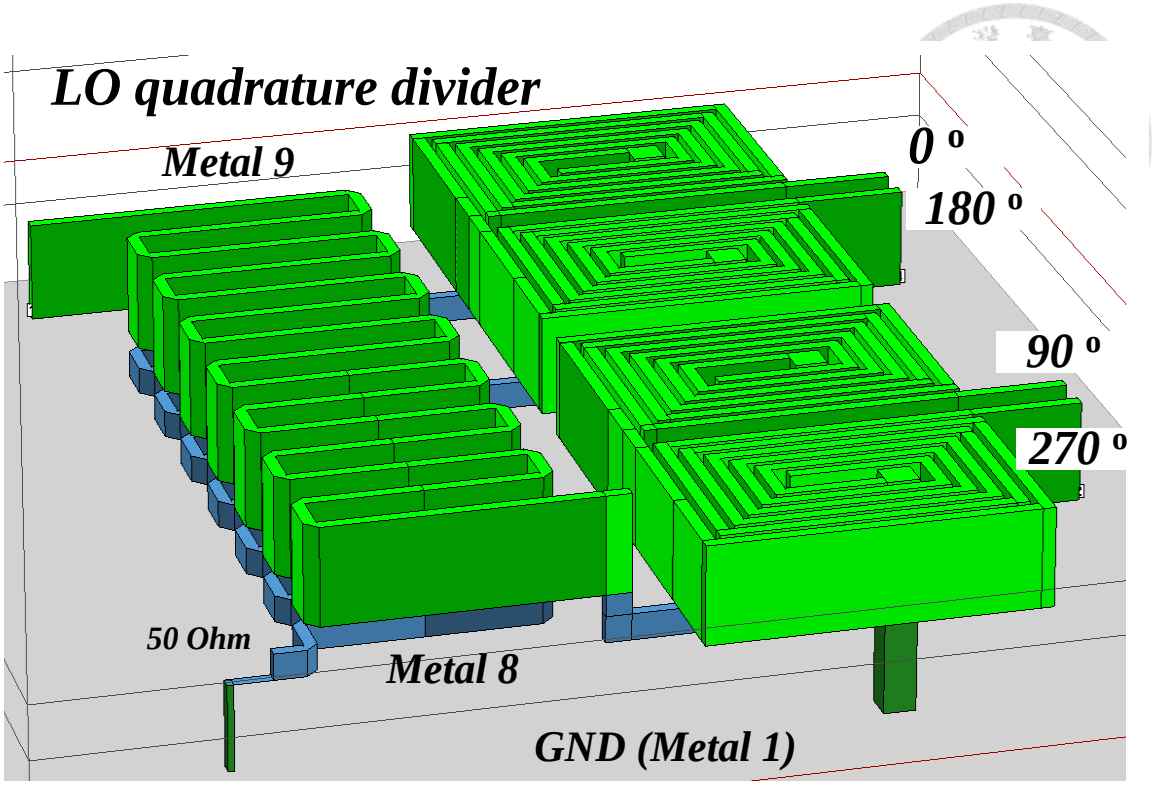


Fig. 2.7. MMW LO four-way quadrature divider.

To provide larger current at transconductance for gain and linearity consideration, the pMOSs for the current bleeding path can improve the IF-to-RF conversion gain and also reduce the bias current of the switching core for mixer noise reduction [34]. The sub-harmonic switching core consists of four parallel connected nMOS pairs. The IF signal is up-converted to *E*-band RF signal by switching the quadrature state of each nMOS pairs M_5 to M_{12} (20μm/0.06μm) alternatively. The lower current of switching core mitigates the voltage headroom problem concurrently. The inductors L_1, L_2 and C_1, C_2 capacitors are used for broadband matching network. Finally the differential RF signal is combined with a balun to generate single-ended signal.

For the sub-harmonically pumped Gilbert-cell mixer, the LO quadrature phase divider is important in our design. The four-way quadrature divider is composed of a 90° coupler and two 180° baluns as shown in Fig. 2.6. A Marchand-type transformer is used due to its excellent amplitude/phase match and broadband response. Two coupled lines

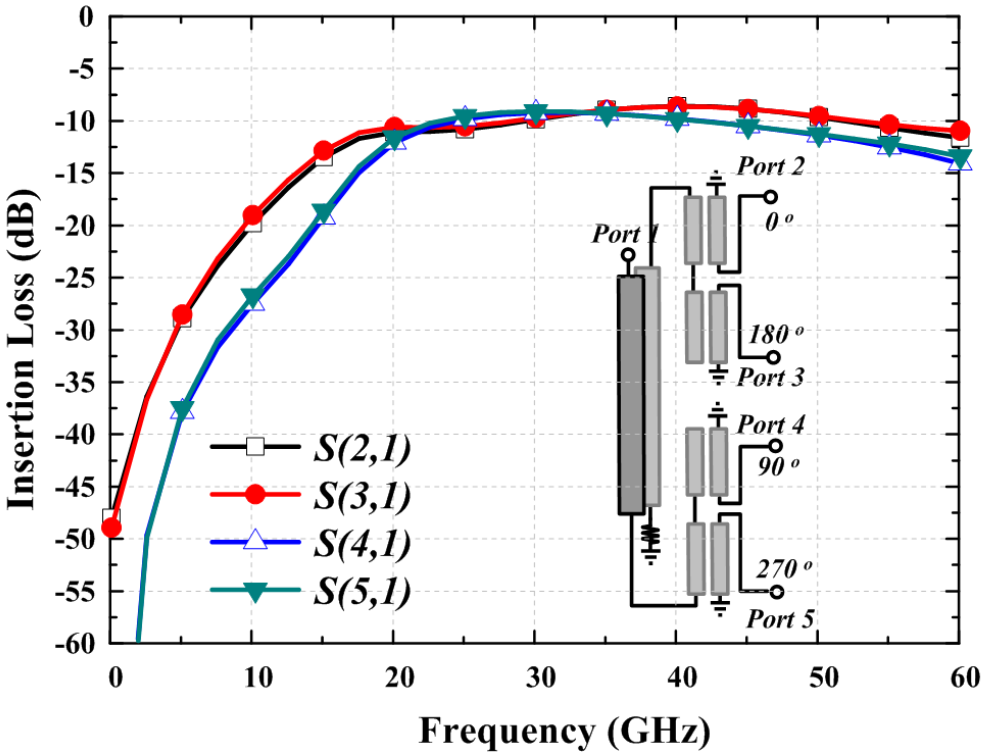


Fig. 2.8. The simulated insertion loss of the four-way quadrature divider.

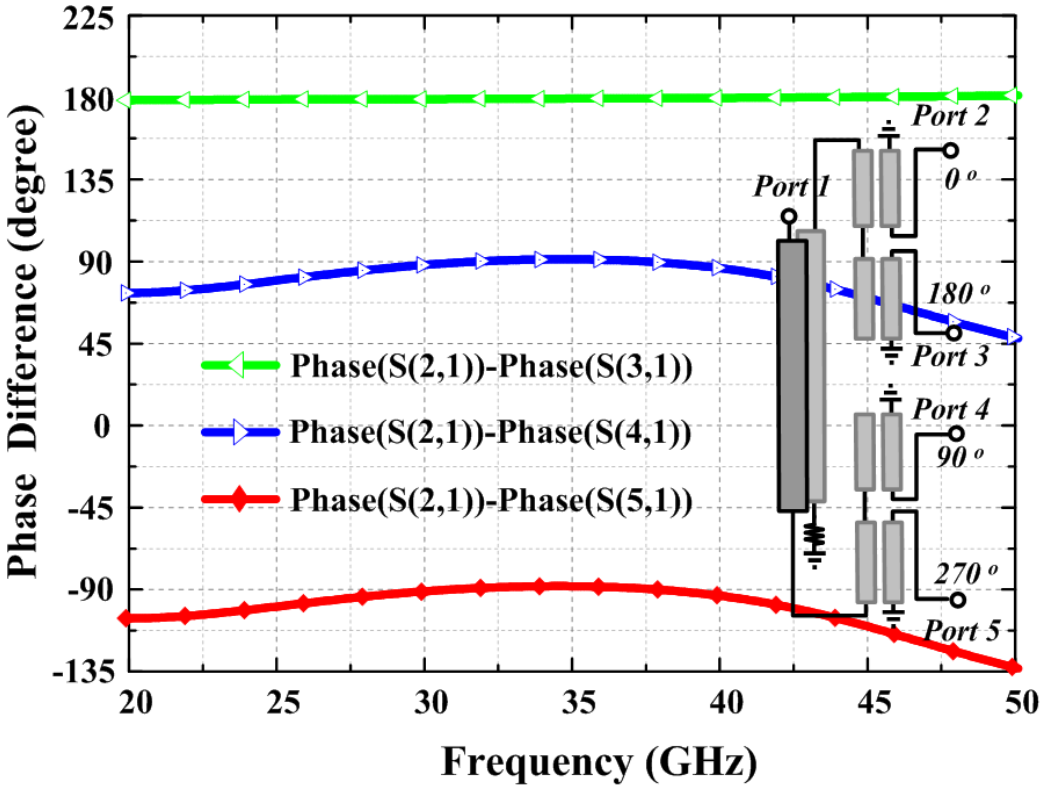
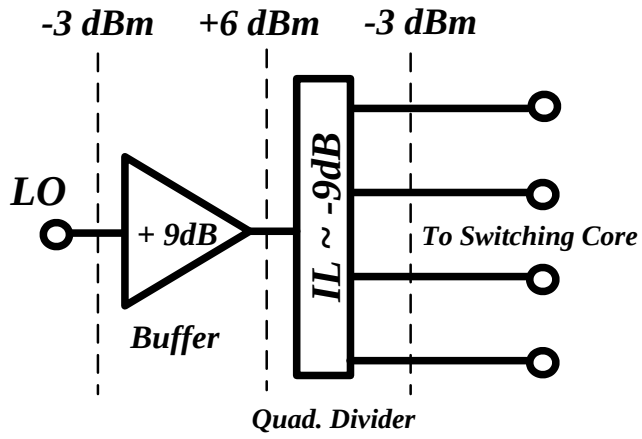
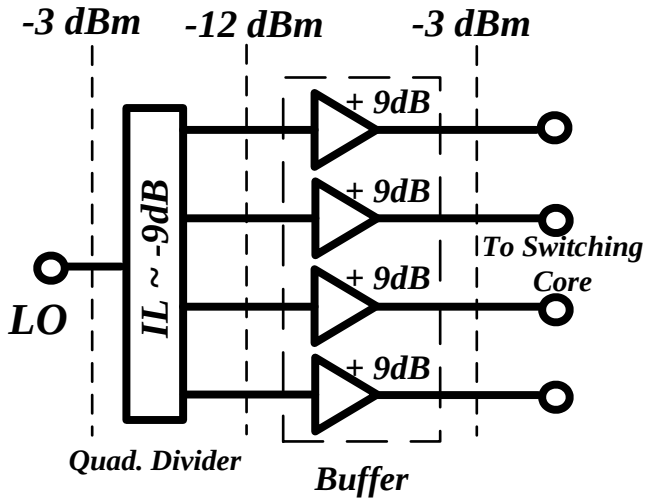


Fig. 2.9. The simulated frequency response of the four-way quadrature divider.



(a)



(b)

Fig. 2.10. (a) LO buffer placed in front of the quadrature divider. (b) LO buffer placed after the quadrature divider.

in the Marchand balun are constructed of edge coupled lines using metal layers 9 in this 65 nm CMOS process. These two coupled lines are wound into two coils with a width and gap both of 4 μm.

For the 90° coupler of the four-way quadrature divider, a broadside coupler is also implemented using the thin-film microstrip line (TFMS) structure. Since the gap between the edge coupler is too small to be fabricated for the required coupling, metal

layer 8 and 9 are used for the coupled lines of the broadside coupler due to the thick dielectric layer. The line width of the coupled line is 4 μm. The size is reduced by using meander TFMS. The symmetry of the layout for quadrature four way divider and mixer core is carefully considered in the design as shown in Fig. 2.7. The 90° coupler and 180° baluns are both calculated using the full-wave EM simulator (Sonnet software). Fig. 2.8 shows the insertion loss of quadrature four-way divider, the amplitude imbalance is less than ±1.5 dB from 20 to 43 GHz. The phase difference of the divider is less than $\pm 5^{o}$ with respect to the quadrature phase as shown in Fig. 2.9.

Nevertheless, the sub-harmonic Gilbert-cell mixer requires MMW quadrature phase generation to pump the switching core, which needs a large LO input power. The insertion loss of a Q-band quadrature divider in 65-nm CMOS process is around 9 dB based on the simulation, including 6-dB ideal four-way power splitter loss. To reduce the LO power requirement, an LO buffer with 9-dB gain is inserted to compensate the insertion loss. For dc power saving, there is a design trade-off between the efficiency of compensated buffer and LO power reduction.

In the *E*-band sub-harmonic Gilbert-cell mixer design, the driving power for each switching core is less than -3 dBm. Therefore, as shown in Fig. 2.10 (a), if the built-in LO buffer is placed in front of the quadrature divider, the total dc power consumption of LO buffer is about 20 mW by assuming a 6-dBm output power and a 20% PAE. In the case of Fig. 2.10 (b), if four small buffers of -3-dBm output power are placed after the quadrature divider, the total dc power consumption of four buffers becomes 10 mW under the same PAE assumption. The difference of dc power consumption is primarily due to the loss of quadrature divider. For power saving, Fig. 2.10 (b) with built-in LO buffers placed after the quadrature divider is clearly a better choice; however, if the

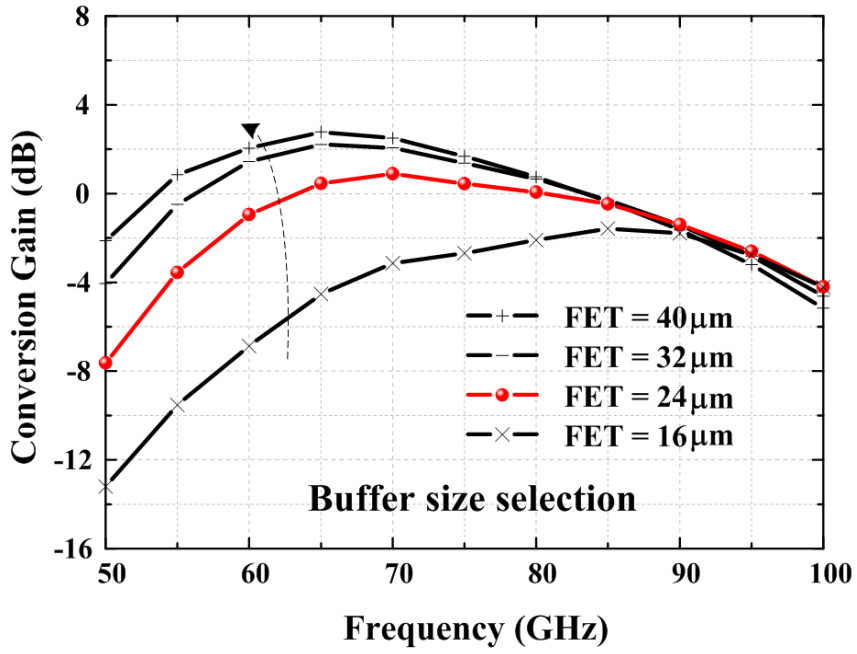


Fig. 2.11. The frequency response of conversion gain with different buffer device size under a -3-dBm LO pumping power. The nMOS, M_{13} to M_{16}, of 24μm/0.06μm are selected.

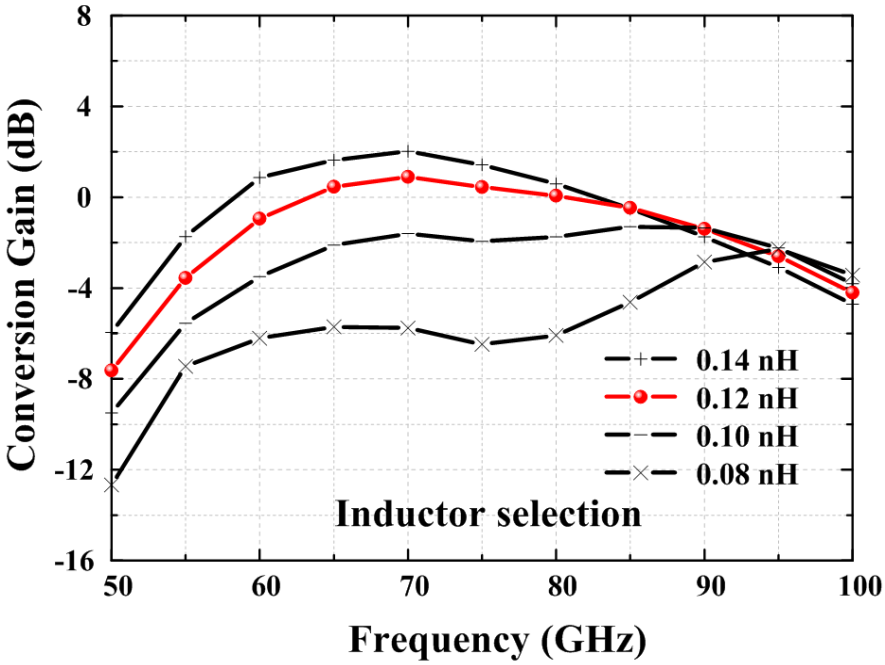


Fig. 2.12. The frequency response of conversion gain with different matching inductor under a -3-dBm LO pumping power. The 0.12-nH differential matching inductors next to nMOS, M_{13} to M_{16}, are selected.

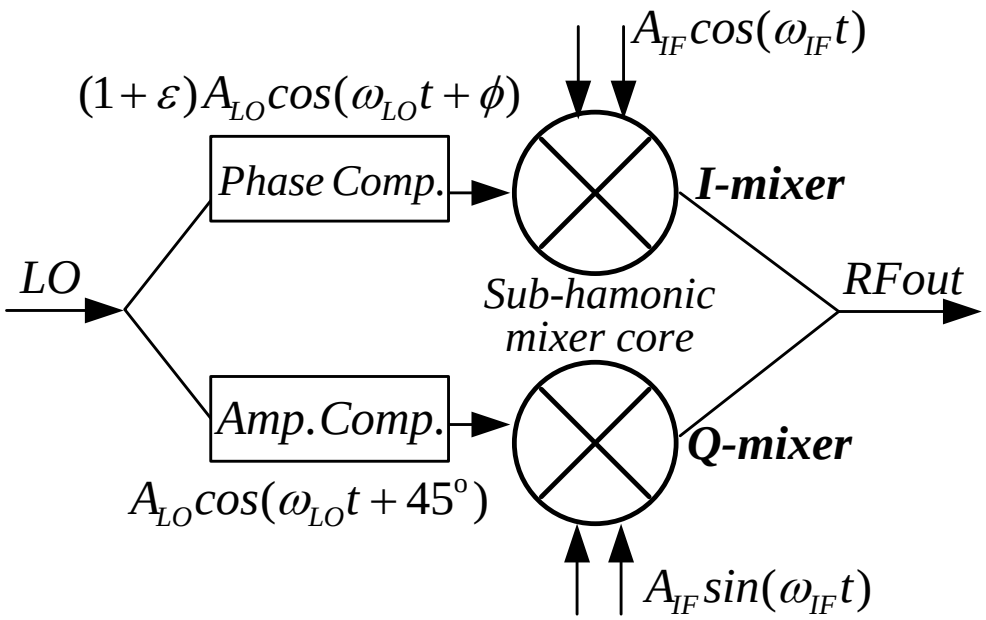
divider is ideal, the dc power consumption should be identical in both cases.

The broadband characteristic of the buffer design is also a design concern. Fig. 2.11 shows the frequency response of conversion gain with different buffer device size under a -3-dBm LO pumping power. As indicated in Fig. 2.11, while the large device can enhance conversion gain, it is also accompanied with more dc power consumption and limited bandwidth. Hence, the buffers with optimized 12-finger nMOS M_{13}–M_{16} (24μm/0.06μm) biased at 0.6 V with total current of 16 mA are utilized in the proposed design. Fig. 2.12 shows the frequency response of conversion gain with different matching inductor under a -3-dBm LO power. The 0.12-nH differential matching inductors next to nMOS M_{13}–M_{16} are selected for gain picking to widen the frequency response with a compact size. Utilizing the optimized buffer stage, the loss due to CMOS quadrature divider can be compensated, and the flatness of conversion gain can be achieved over the targeted frequency band.

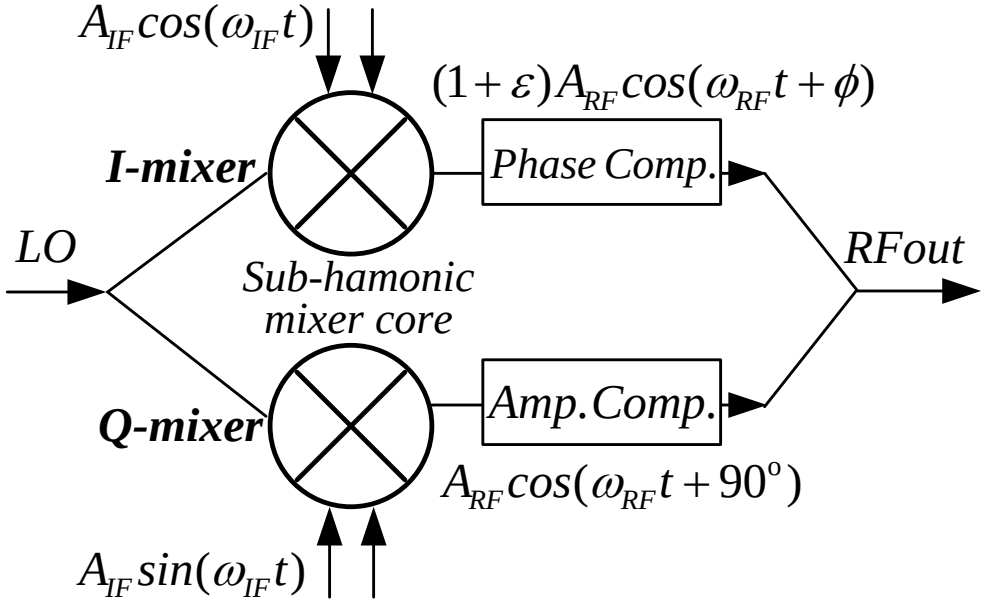
2.3.2 Load Sensitivity Analysis for Sub-harmonic IQ Modulator Design

In our design, to reduce the IQ mismatch problem, the IQ modulator has been incorporated amplitude and phase compensation. As the compensation circuits are adjusted, the matching conditions are changed accordingly, which results in the deviation of mixer performances at I and Q paths. The performance deviation of the I- and Q-mixers also causes IQ mismatch. Therefore, a load sensitivity analysis is adopted to select the proper topology of the sub-harmonic IQ modulator.

There are two practical topologies, as illustrated in Fig. 2.13, for sub-harmonic IQ modulator design. To investigate the impact on the mixer gain deviation with the imbalanced LO/RF load conditions of the compensation circuits, the two RF output ports are assumed to have identical frequency response, and the 45° power splitter is



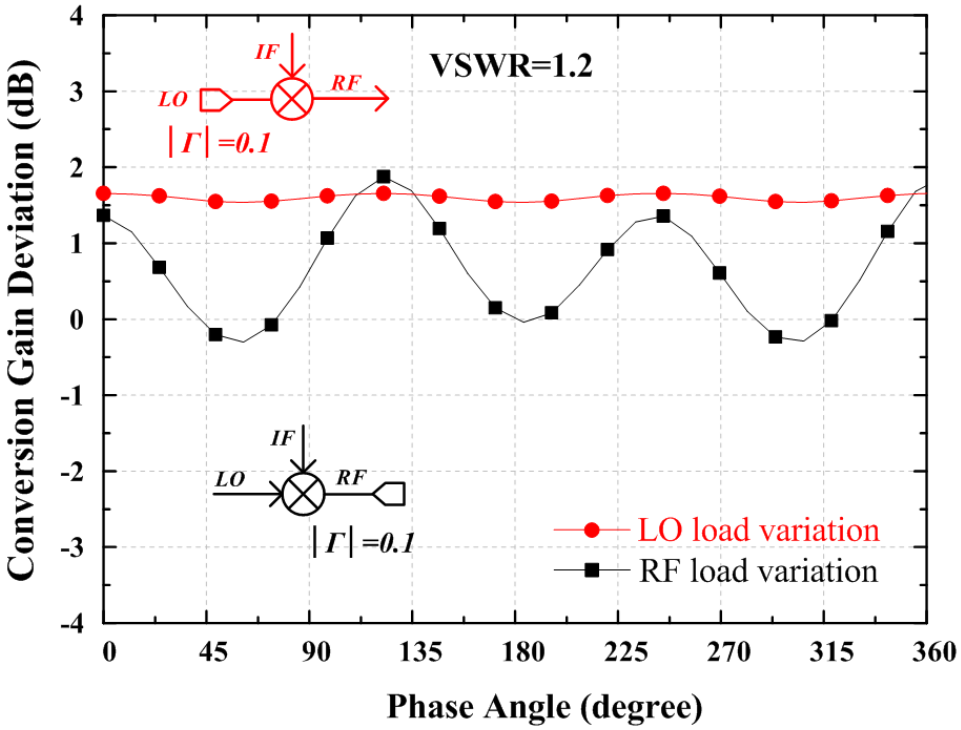
(a)



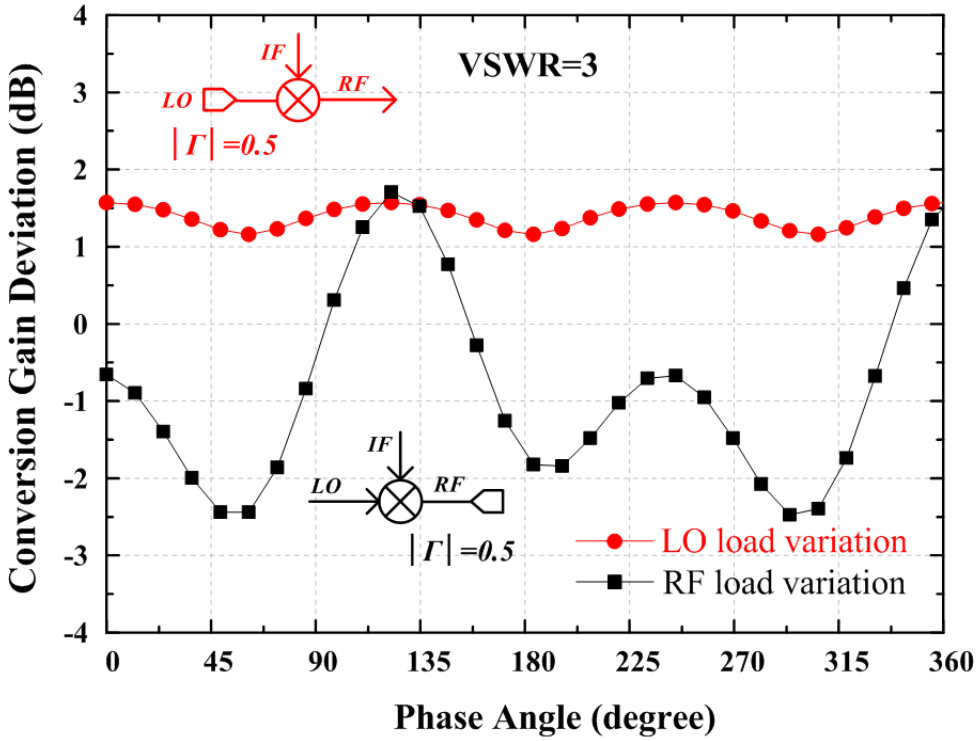
(b)

Fig. 2.13. (a) The quadrature mixing with phase and amplitude compensation circuits at the LO port. (b) The quadrature mixing with phase and amplitude compensation circuits at the RF port.

designed at LO ports for quadrature mixing in Fig. 2.13 (a). The LO ports of two sub-harmonic mixers are then assumed to be identical, and the quadrature combiner is

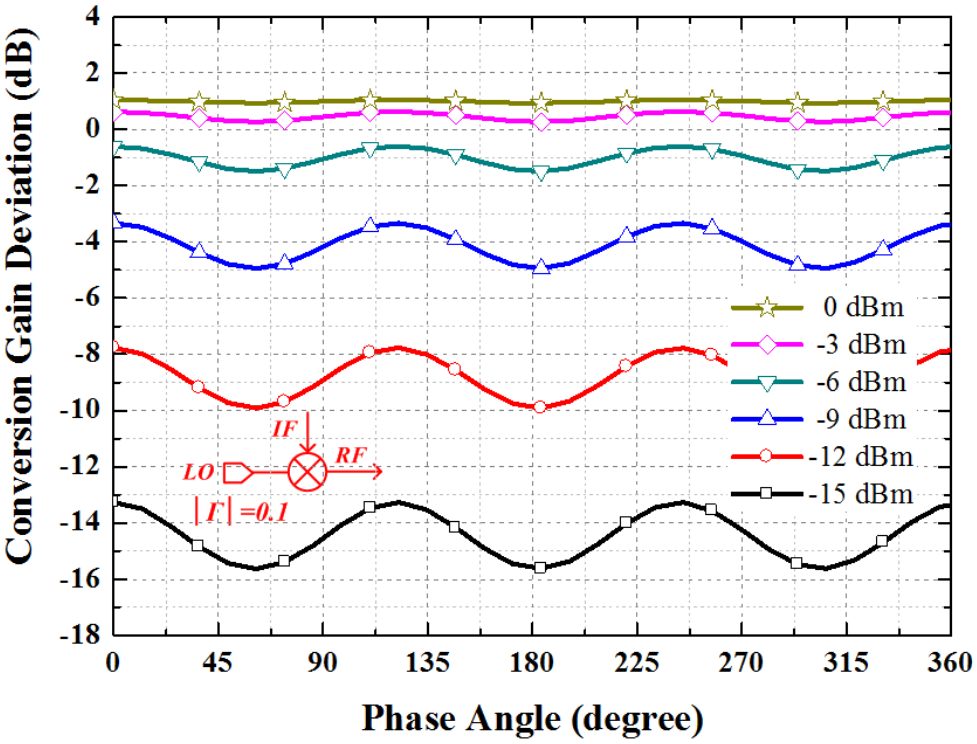


(a)

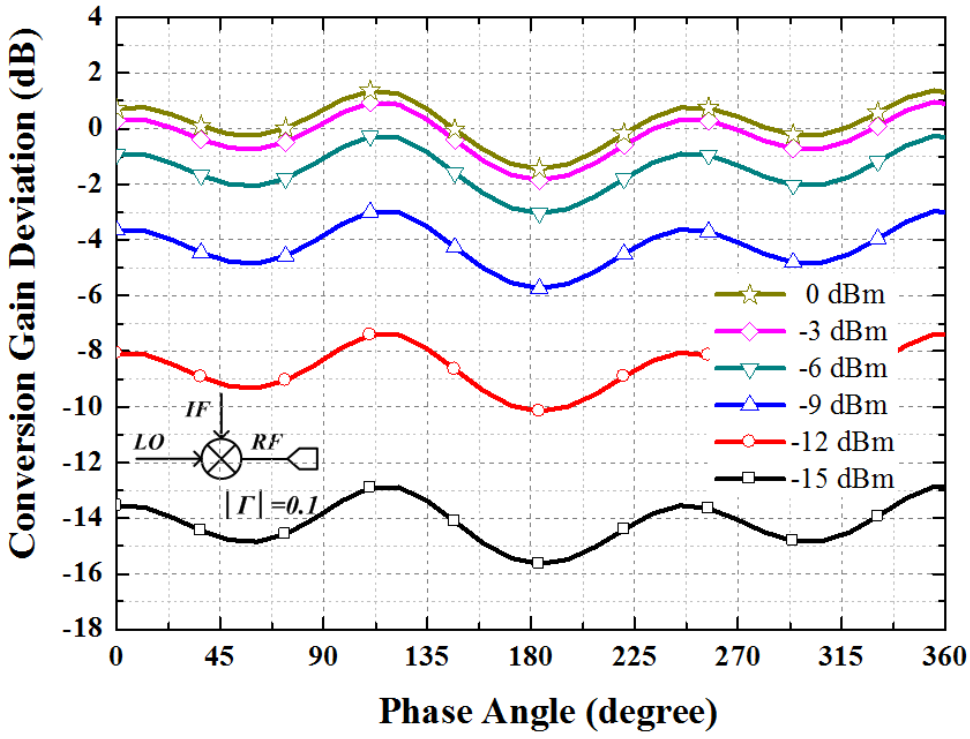


(b)

Fig. 2.14. The load variation of LO port and RF port with (a) VSWR=1.2 and (b) VSWR=3.0, at LO frequency of 37.5 GHz of single mixer core.



(a)



(b)

Fig. 2.15. The conversion gain deviation of (a) LO port and (b) RF port load variation , versus LO driven power from -15-dBm to 0-dBm with VSWR=1.2 at LO frequency of

designed at RF ports in Fig. 2.13 (b). A load with a fixed reflection coefficient as an imperfect load placed at the RF and LO port of a sub-harmonic mixer core are discussed, respectively.

Fig. 2.14 (a) shows simulation results of load variation over the imperfect LO- and RF-port terminations along a constant voltage standing-wave ratio (VSWR) circle on the Smith chart, corresponding to 1.2 VSWR (20-dB reflection coefficient). It shows the conversion gain deviation of RF load variation varies much more than that of LO load variation. As previously discussed, amplitude mismatch is an important factor to the IRR. According to Fig. 2.14 (a), assuming the matching networks at RF ports are carefully designed, the gain variation still has more than 2 dB under two imbalance loads. Furthermore, as shown in Fig. 2.14 (b), considering the design tolerance with a return loss of 6 dB, the large load variation along the 3:1 VSWR circle becomes unacceptable.

In the mixer design, the function of LO driven power is to switch the mixer fully on and off for lowest distortion. If LO signal is sufficiently high to provide enough voltage swing, the LO port matching is not a major concern. As shown in Fig. 2.15, the conversion gain deviation versus LO driven power of the LO port and RF port load variation with VSWR=1.2 at LO frequency of 37.5 GHz are used to explain the phenomenon.

Therefore, to avoid the performance deviation of the I- and Q-mixers, the phase and amplitude compensation circuits are considered to be placed in the load insensitive LO port for quadrature mixing. To provide the load-insensitive performance at the RF port, the Wilkinson combiner with good matching and isolation characteristics is utilized for the mixer RF output combining.

2.3.3 Broadband LO 45° Power Splitter with Amplitude and Phase Compensation

Since the LO frequency is equal to half of the RF frequency in the sub-harmonic mixer, an LO signal power splitter with 45° phase shift and low amplitude and phase imbalance is required for the I and Q mixer to produce quadrature mixing. To generate the 45° phase shift, the MMIC tunable phase shifter or polyphase filter has been proposed in [35]. However, the polyphase filter with the disadvantage of high insertion loss is unfavorable to be implemented at MMW bands. To achieve low insertion loss, broad bandwidth, and low-imbalance 45° equal group delay, the HPF and LPF structure are selected in this LO power splitter design. Furthermore, the amplitude and phase compensation circuits are adopted in the power splitter to reduce the IQ mismatch of the whole modulator. By the progressive phase of HPF structure and the phase delay of LPF structure, the 45° phase difference between two output ports can be achieved [20], [36], [37].

According to Fig. 2.3, the amplitude imbalanced has a significant impact on the image rejection. Therefore, to achieve a broadband image rejection performance in a sub-harmonic I-Q modulator, a low imbalance 45° phase shift with minimum amplitude imbalance in the targeted frequency region is an important design goal. Our proposed structure is shown in Fig. 2.16, which is composed by a LPF/HPF section used for equal group delay generation, and an unequal power divider designed for amplitude mismatch compensation.

Fig. 2.17 shows the frequency response of the compensation mechanism for the proposed structure. According to the characteristic of LPF/HPF, it provides broadband low-imbalance group delay. But because of the non-ideal properties of elements, the

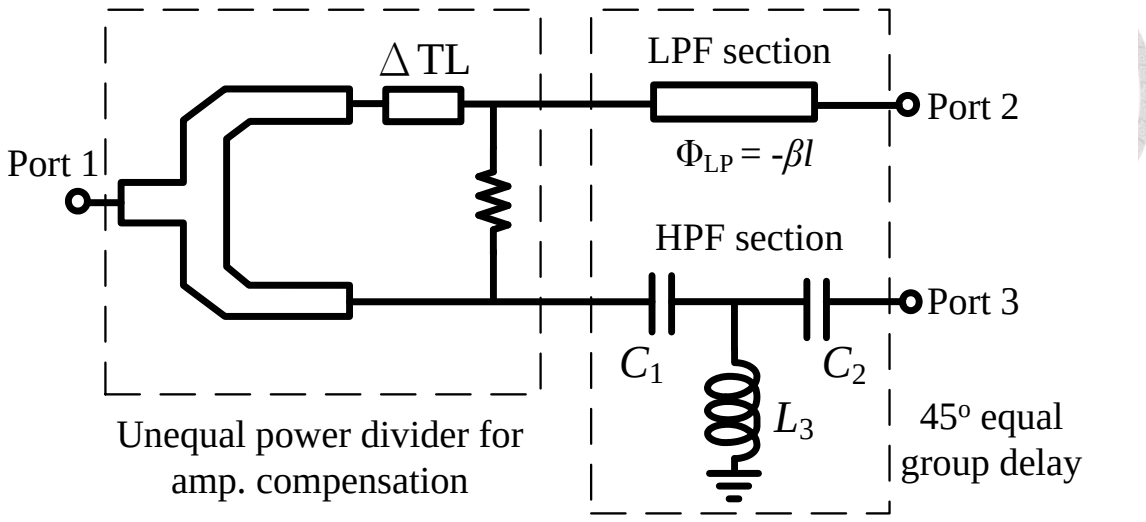


Fig. 2.16. Proposed broadband 45° LO power splitter with amplitude imbalance compensation.

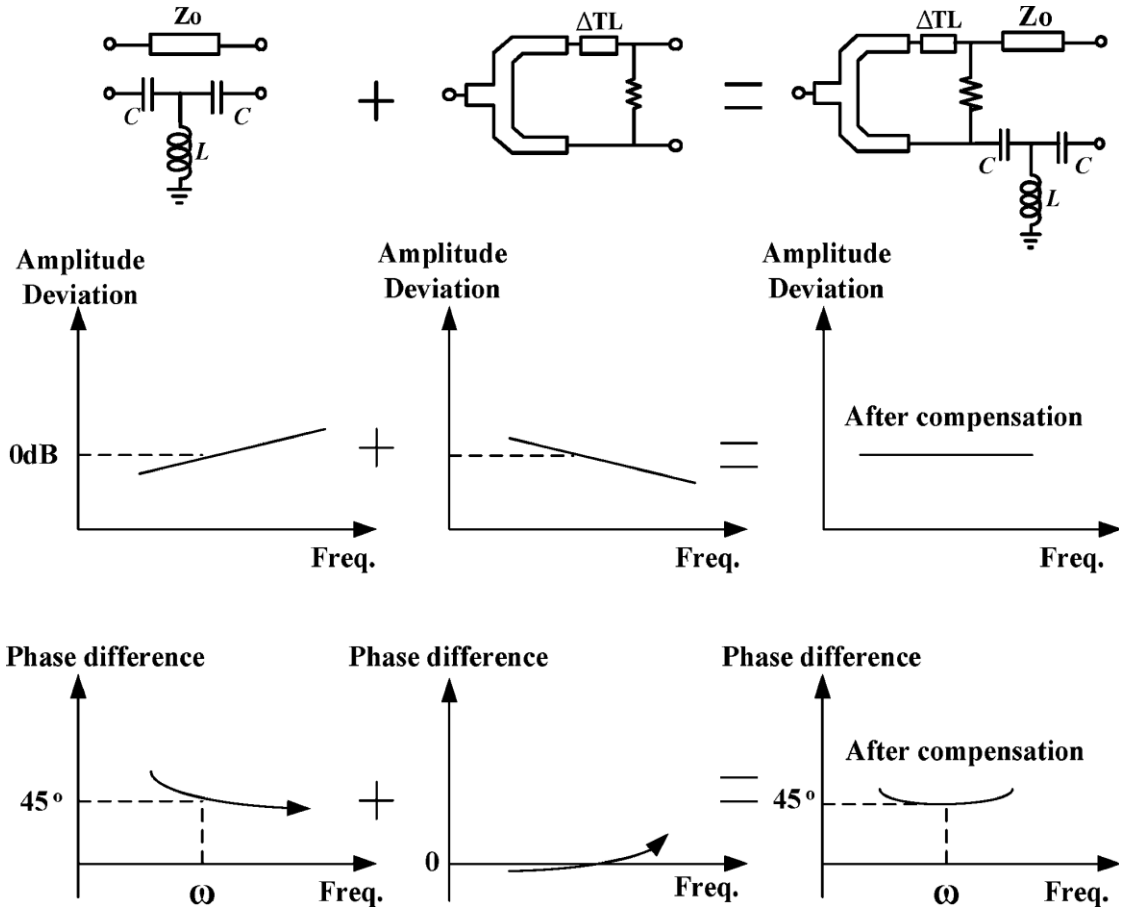


Fig. 2.17. The frequency response of the broadband compensation mechanism for proposed structure in Fig. 2.16.

unequal power divider is designed to compensate the amplitude imbalance. It takes advantage of that the opposite of phase and amplitude in two sections can be compensated reciprocally. The optimal circuit obtains a broadband low-imbalance 45°phase delay and balanced power division.

The low pass and high pass filter structures are used to generate 45° phase delay. The HPF is implemented by metal-insulator-metal capacitors (MiMcaps) and a short stub, and the LPF is implemented using TFMS. The HPF section can be considered as a two-port network, and the *S*-parameter can be acquired by using *ABCD* parameters. In order to simplify the derivation, the capacitors C_1 and C_2 are selected to be identical.

The conversion for the *ABCD* parameter to the scattering matrix are

$$S_{11} = S_{22} = \frac{A + B / Z_0 - CZ_0 - D}{A + B / Z_0 + CZ_0 + D}, \tag{7}$$

$$S_{21} = S_{12} = \frac{2}{A + B / Z_0 + CZ_0 + D}. \tag{8}$$

The transmission matrix is

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} (1 - \frac{1}{\omega^2 C_1 L_3}) & (\frac{2}{j\omega C_1} - \frac{1}{j\omega^3 C_1^{\,2} L_3}) \\ (\frac{1}{j\omega L_3}) & (1 - \frac{1}{\omega^2 C_1 L_3}) \end{pmatrix},$$

where ω is the radian frequency. We assume that the impedance matching is perfect at operation frequency ω_0, and get S_{11}=0, $A = D$, $B/ Z_0 = CZ_0$,

$$\left(\frac{2}{j\omega_0 C_1} + \frac{-1}{j\omega_0^{\,3} L_3 C_1^{\,2}} \right) / Z_0 = \frac{Z_0}{j\omega_0 L_3} \tag{9}$$

The inductance L can be obtained as

$$L_3 = \frac{1 + C_1^{\,2} \omega_0^{\,2} Z_0^{\,2}}{2 C_1 \omega_0^{\,2}}. \tag{10}$$

Then use the result to replace L_3 with the combination of C_1, Z_0 and ω_0 to calculate S_{21} of the HPF network as

$$S_{21} = \frac{1}{A + CZ_0} = \frac{1}{(1 - \frac{1}{\omega_0^2 C_1 L_3}) + (\frac{1}{j\omega_0 L_3})Z_0}, \tag{11}$$

$$S_{21} = \frac{1}{(1 - \frac{1}{\omega_0^2 C_1 L_3}) - j(\frac{Z_0}{\omega_0 L_3})} = \frac{C_1 \omega_0^2 L_3}{(-1 + C_1 \omega_0^2 L_3) - jC_1 \omega_0 Z_0}, \tag{12}$$

the phase of S_{21} can be obtained as

$$\phi_{HP}(\omega) = \tan^{-1} \frac{C_1 \omega_0 Z_0}{-1 + C_1 \omega_0^2 L_3} = \tan^{-1} \frac{2C_1 \omega_0 Z_0}{-1 + C_1^2 \omega_0^2 Z_0^2}. \tag{13}$$

The LPF section is implemented by the transmission line, and the phase frequency response can be written as

$$\phi_{LP}(\omega) = -\beta l = -\frac{2\pi}{v/f} l = -\frac{\omega}{v} l, \tag{14}$$

where l is the length of the LPF and v is the phase velocity.

For the broadband low-imbalance group delay, the phase different is 45°, and the phase variations of LPF/HPF is set to be equal.

$$\phi_{HP}(\omega_0) = \pi/4 - \phi_{LP}(\omega_0) \tag{15}$$

$$\phi_{HP}'(\omega_0) = \frac{2}{C_1 \omega_0^2 Z_0} = -\frac{l}{v} = \phi_{LP}'(\omega_0) \tag{16}$$

It can be derived as

$$v = \frac{C_1 \omega_0^2 Z_0 l}{2}. \tag{17}$$

Substituting (9) by (7), (8) and (11), the equation can be expressed as

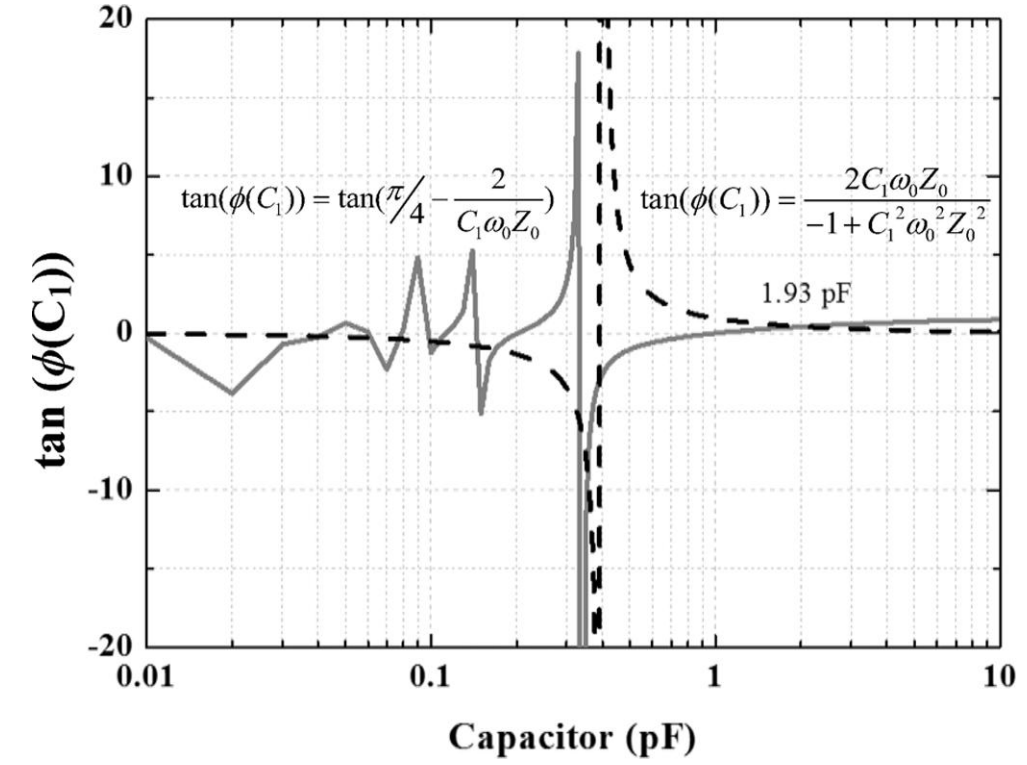


Fig. 2.18. The function graph of Eq. (18) for numerical root search of $\tan(\phi(c_1))$.

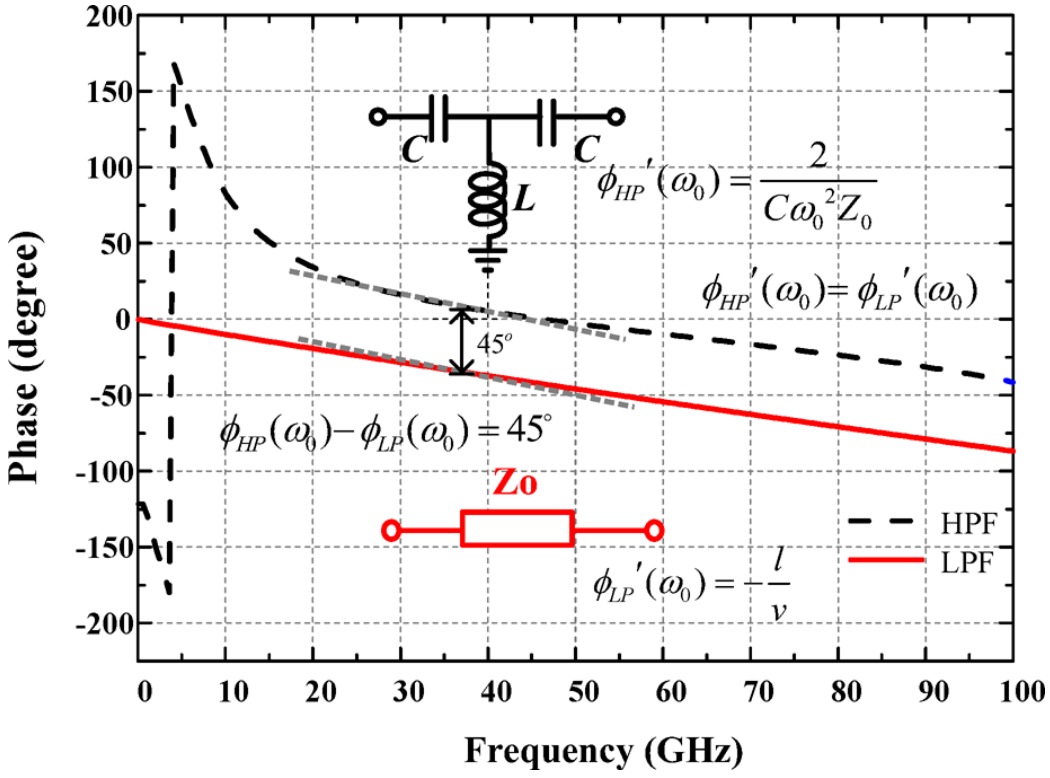


Fig. 2.19. The simulated frequency response of HPF and LPF structures.

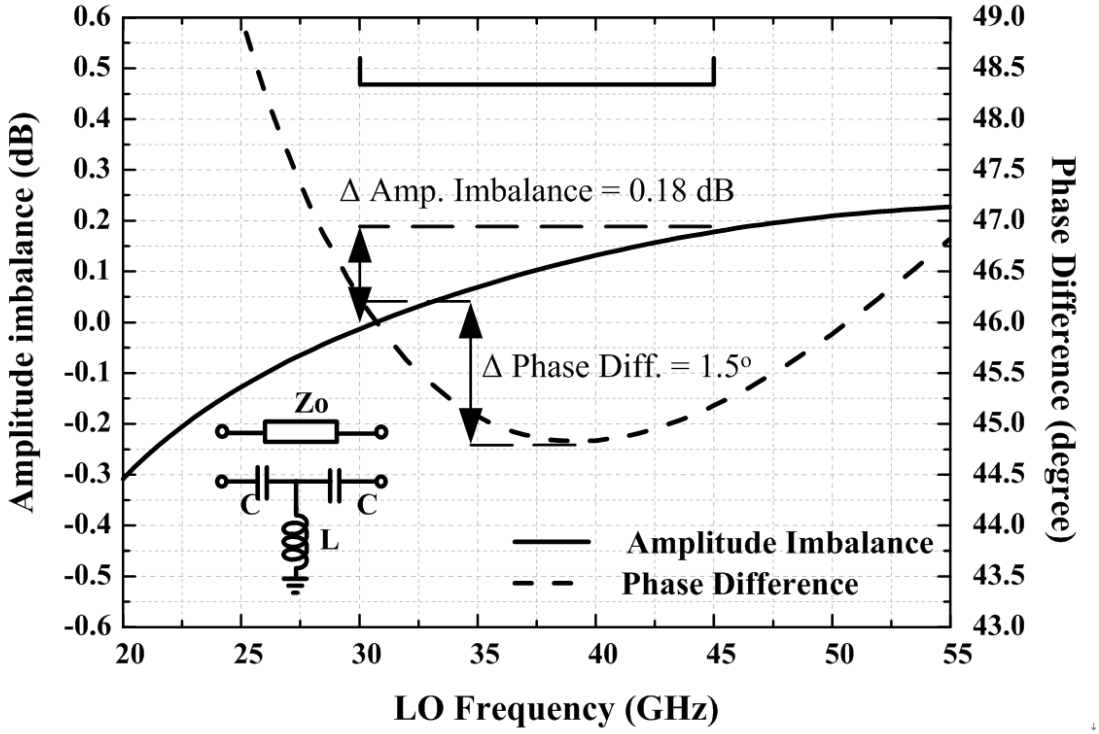


Fig. 2.20. The simulated amplitude imbalance and phase difference of LPF and HPF structures.

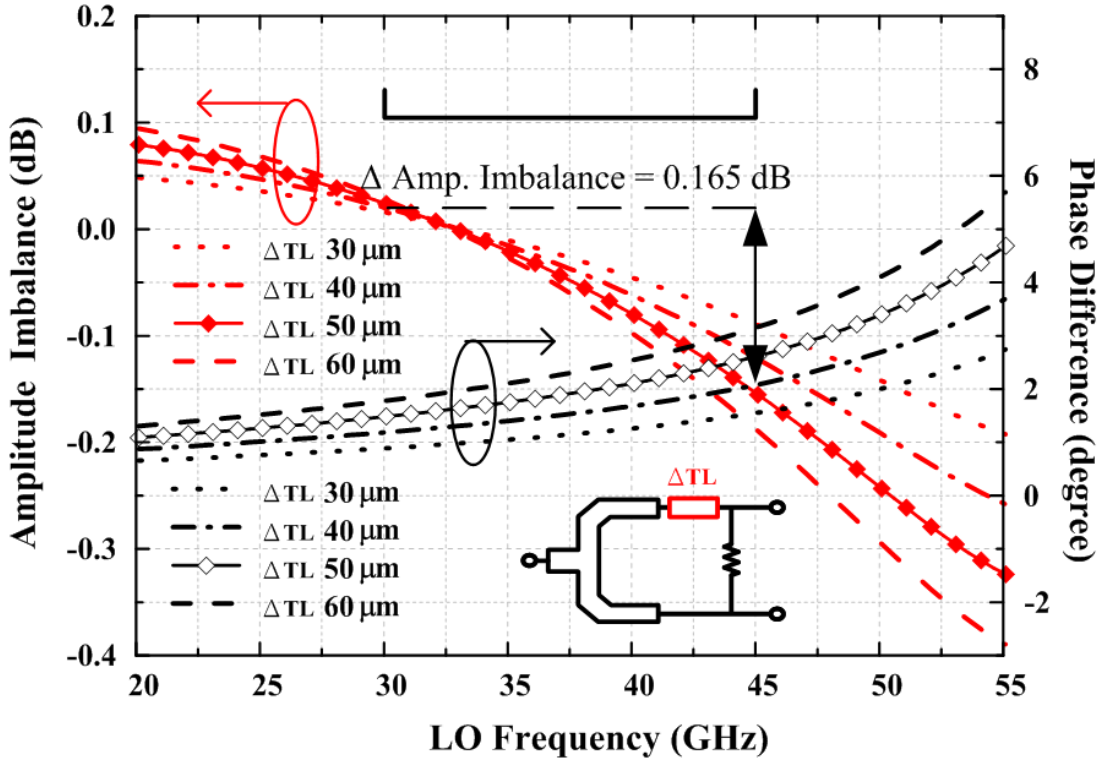


Fig. 2.21. The simulated frequency response of the amplitude compensation structure.

$$\phi(C_1) = \pi/4 - \frac{2}{C_1\omega_0 Z_0} = \tan^{-1}\frac{2C_1\omega_0 Z_0}{-1 + C_1^2\omega_0^2 Z_0^2}. \quad (18)$$

Fig. 2.18 is plotted using (18), and the initial value of 1.93pF for the capacitance can be obtained. Fig. 2.19 shows the simulation phase frequency response of HPF and LPF.

However, since the on-chip MiMcaps, inductors and transmission lines are not ideal, for the case of 45° phase delay, the non-ideal loss of these components will result in the amplitude imbalance. Fig. 2.20 shows the simulation of amplitude imbalance and phase difference of LPF/HPF. The amplitude imbalance needs to be compensated.

The proposed compensation structure uses a short delay line in the power divider design. It can provide a proper slope of the amplitude difference by changing the length of delay line as shown in Fig. 2.21. It shows the simulation result of the amplitude imbalance and phase difference of the unequal power divider section. The specified length, 50-μm line, is selected properly to compensate the amplitude imbalance caused by the LPF/HPF structure. Compared to the Wilkinson divider with a delay line, the proposed power divider can provide the larger slope value at operating frequency to sufficiently compensate the amplitude difference from the LPF/HPF structure as shown in Fig. 2.22. Besides, as shown in Fig. 2.23, the flatter and smaller phase difference frequency response in operating band is more suitable for our design.

For the phase shift arising from the compensated TL length, we slightly adjust the center frequency and shift the phase difference 2° to 3° of LPF/HPF design, so that the phase and amplitude mismatch can be minimized, simultaneously. The design flow is shown Fig. 2.24. Fig. 2.25 shows the amplitude and phase difference simulation result of our proposed broadband 45° power splitter. With the combination of two modified sections, the amplitude imbalance is less than 0.04 dB, and the phase difference is less the 0.5^{o} from 32 to 45 GHz for LO frequency.

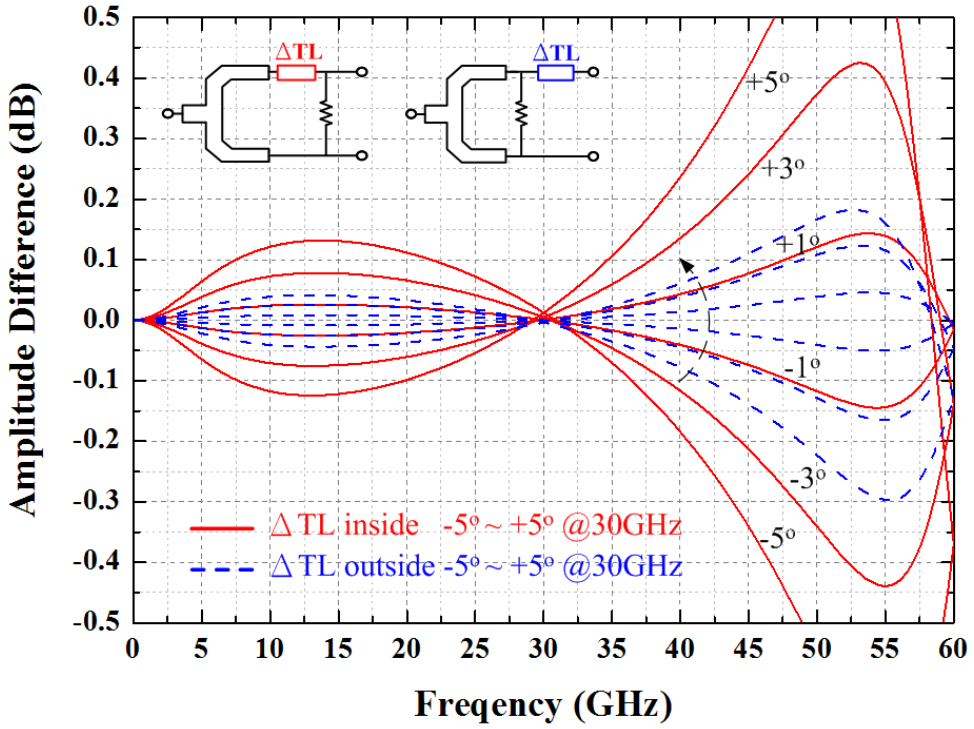


Fig. 2.22. The simulated amplitude difference of the proposed power divider (solid line) and the Wilkinson power divider with a delay line (dashed line).

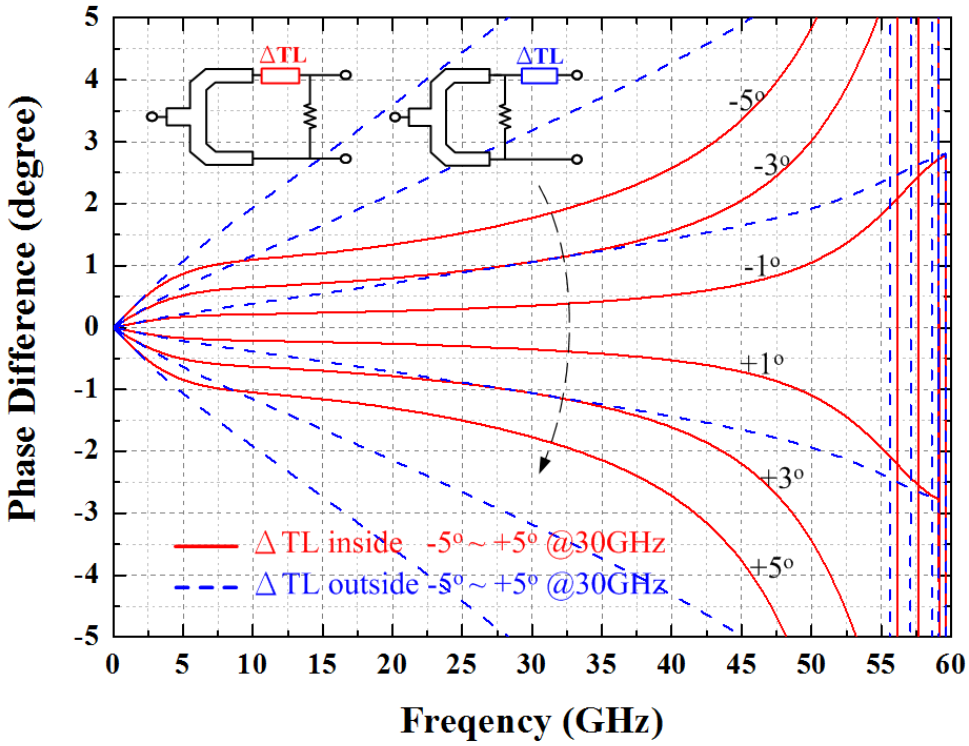


Fig. 2.23. The simulated phase difference of the proposed power divider (solid line) and the Wilkinson power divider with a delay line (dashed line)

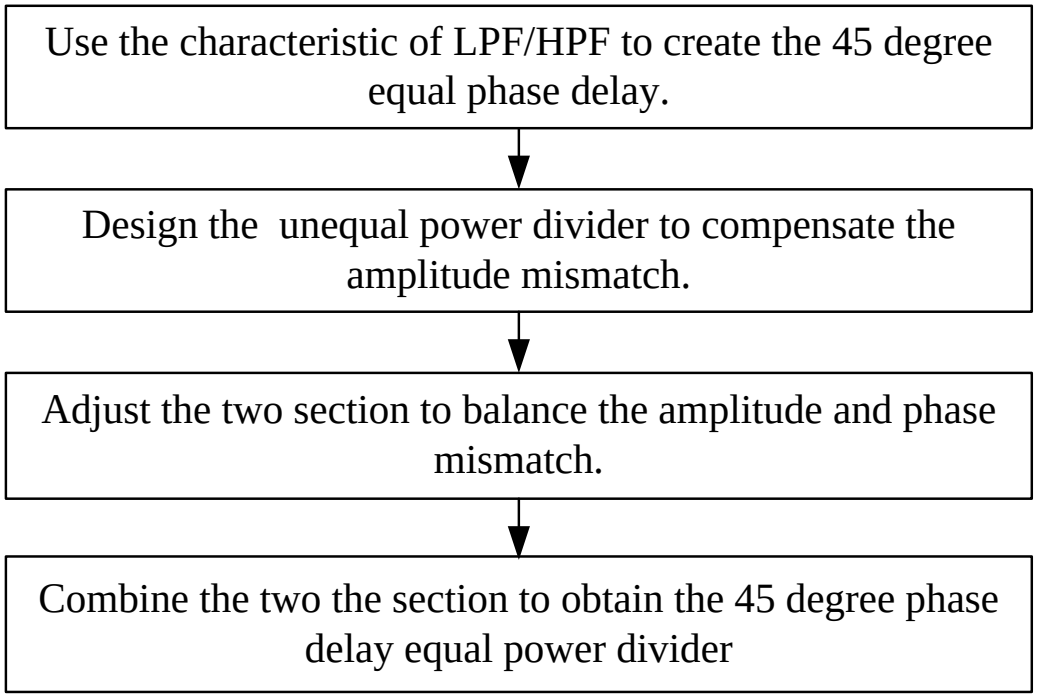


Fig. 2.24. Design flow of phase and amplitude compensation.

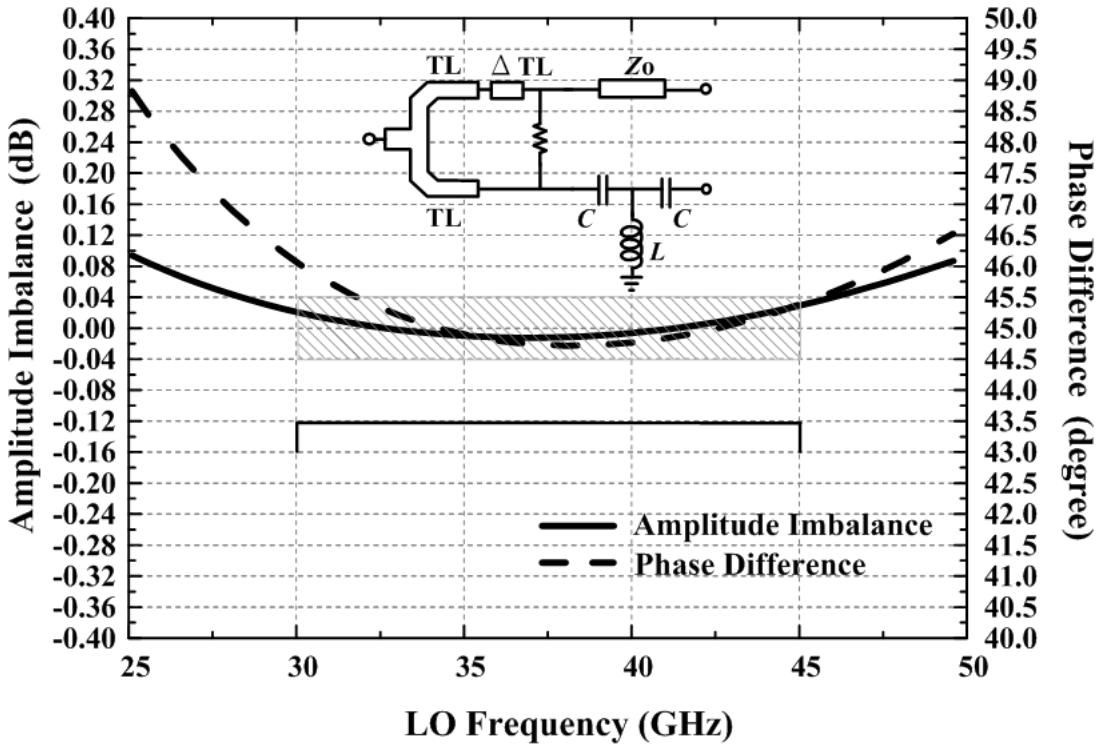


Fig. 2.25. The total amplitude and phase difference for proposed structure in Fig. 2.16.

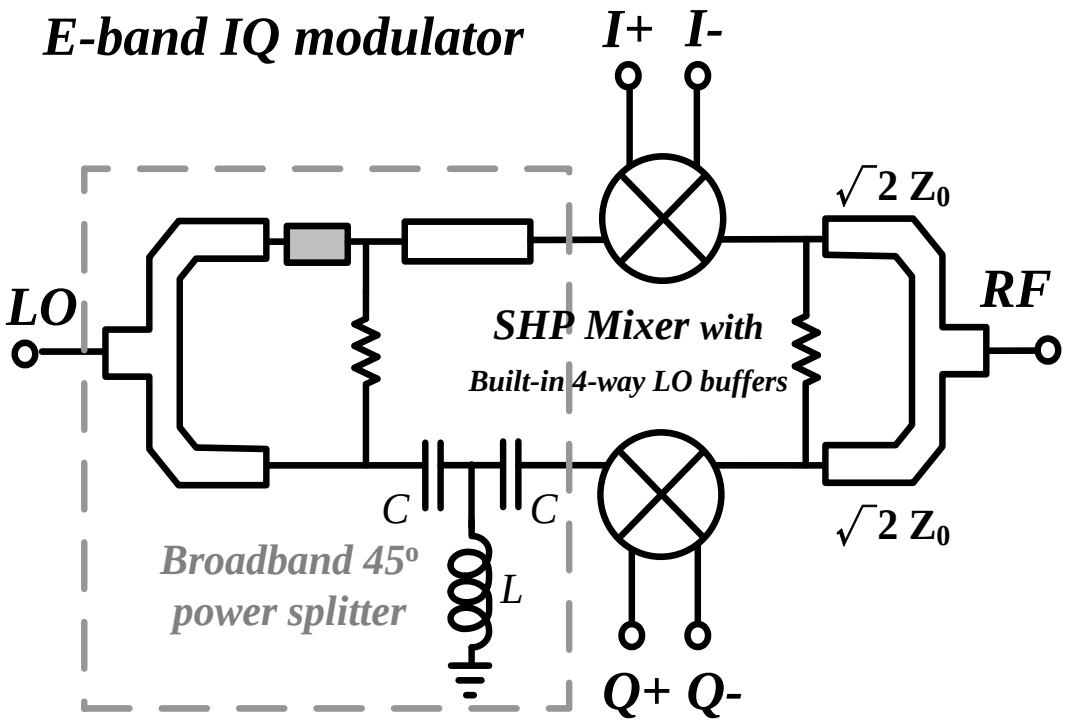


Fig. 2.26. The block diagram of the *E*-band modulator.

2.3.4 IQ Modulator Design

To verify the presented structure, an *E*-band sub-harmonic IQ modulator with proposed compensated technique is designed and implemented on standard 65-nm CMOS technology. The system block diagram of the IQ modulator is shown in Fig. 2.26. The doubly balanced sub-harmonic Gilbert-cell mixer is adopted in the IQ modulator. As described above, taking into account the sensitivity of the RF mixer load variation, an in-phase Wilkinson combiner with identical input port impedance is utilized at RF port to combine the I/Q modulated RF signals. The proposed broadband 45° power splitter is utilized to generate the quadrature phase LO signals at the load insensitive LO-port for the sub-harmonic mixer. Moreover, the two identical LO four-way quadrature dividers of SHP mixers with good impedance matching connected behind the 45° LO power splitter is an advantage in our design.

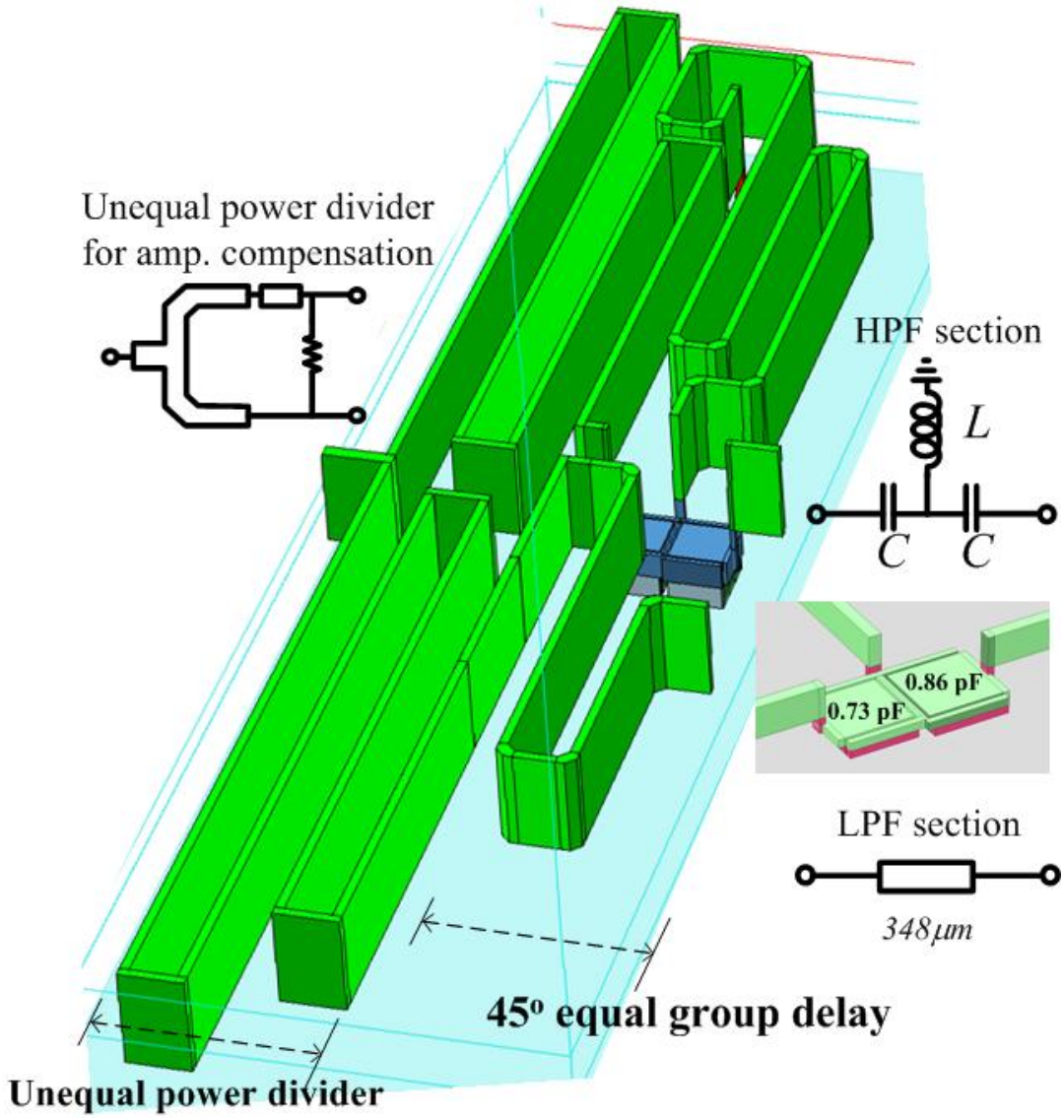


Fig. 2.27 The layout of proposed broadband 45° LO power splitter.

To provide an IRR of 40 dBc, the IQ imbalance should be within 0.5 phase difference and 0.05-dB amplitude imbalance, so that the careful EM simulation is important. Besides, the HPF section as the inter-stage of unequal power divider and mixer LO input port, slightly adjusting the two capacitances to improve the matching condition helps us to preserve the broadband high image rejection performance. Fig. 2.27 shows the layout geometry, the HPF section is realized by two MiMcaps and a 710-μm short stub TFMS. The two modified capacitance value are 0.73 pF and 0.86 pF, respectively.

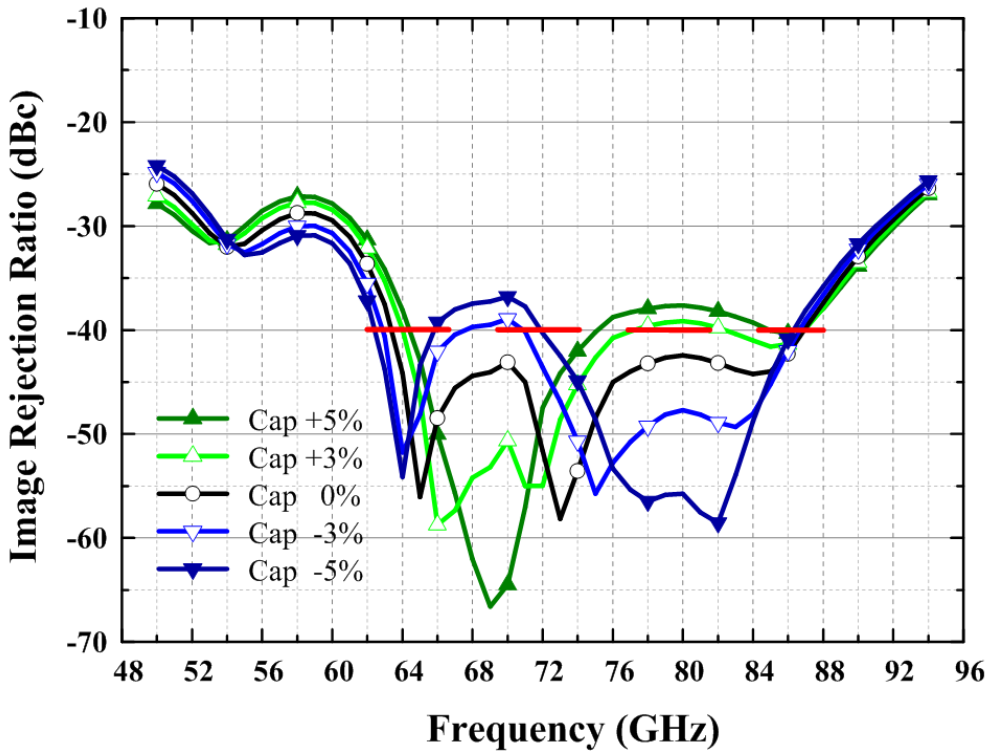
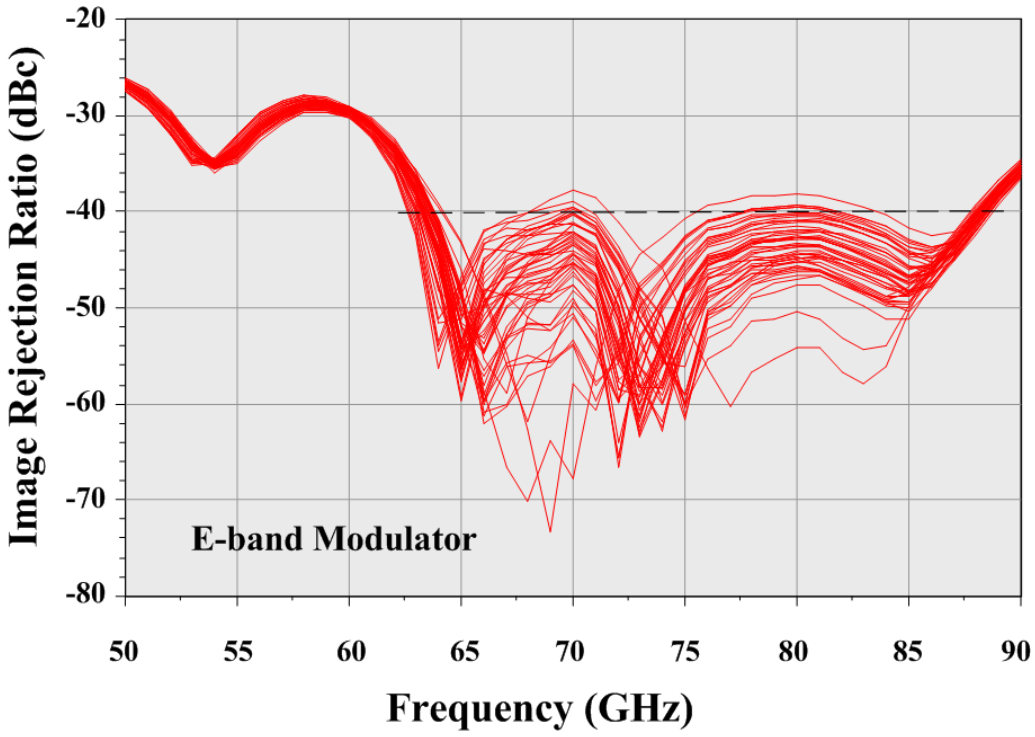


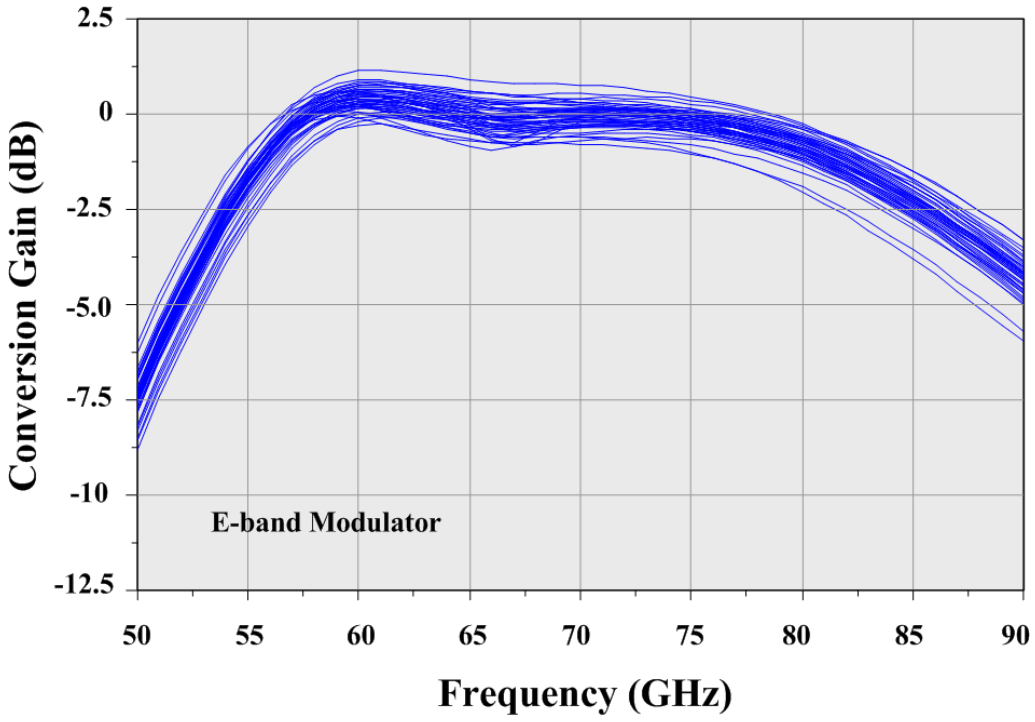
Fig. 2.28. The effects of capacitance variation on image rejection ratio.

Fig. 2.28 shows the effects of capacitance variation on image rejection ratio. It can be observed that the image rejection ratios of the *E*-band modulator are acceptable and tolerances within ±3% capacitance variation.

Furthermore, the image rejection ratio is decided not only by LO amplitude/phase mismatch, but also by device/layout mismatch (such as switch cores and LO buffers). To investigate the effects of process variation, the monte-carlo analysis and the PVT corner simulations provided by ADS are used. Fig. 2.29 shows the monte-carlo simulations with 10% variation using a Gaussian distribution for the component value on all transistors of the mixer core. The two mixer cores are considered as having identical behavior in the simulation. The simulated conversion gain is around 0 dB with the 3-dB bandwidth from 55 to 85 GHz. The simulated image rejection ratio of basically under -40 dBc is achieved over 64 to 84 GHz. The PVT corner simulations are shown in Fig. 2.30.

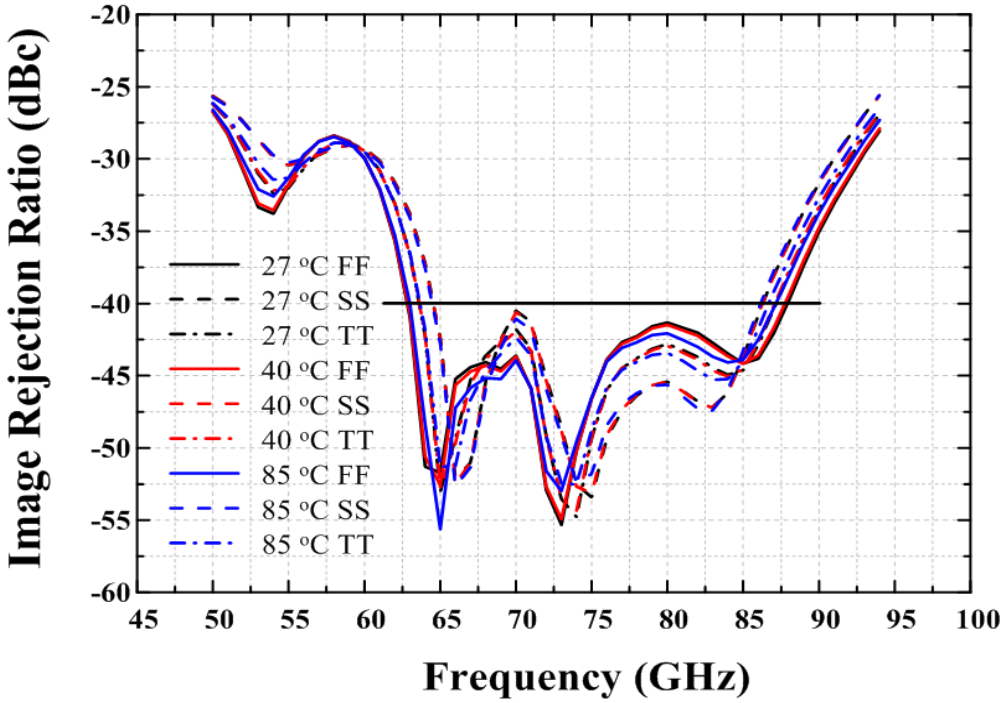


(a)

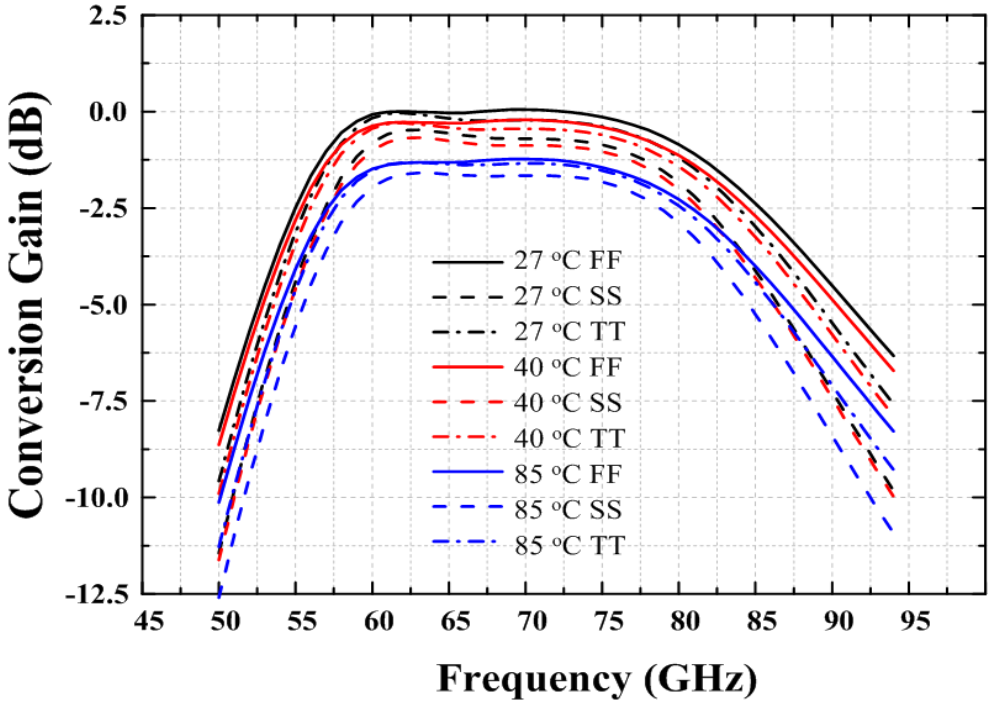


(b)

Fig. 2.29. (a) The image rejection ratio of the monte-carlo simulations, and (b) The conversion gain of the monte-carlo simulations of the *E*-band modulator.



(a)



(b)

Fig. 2.30. (a) The image rejection ratio of the PVT corner simulations, and (b) The conversion gain of the PVT corner simulations of the *E*-band modulator.

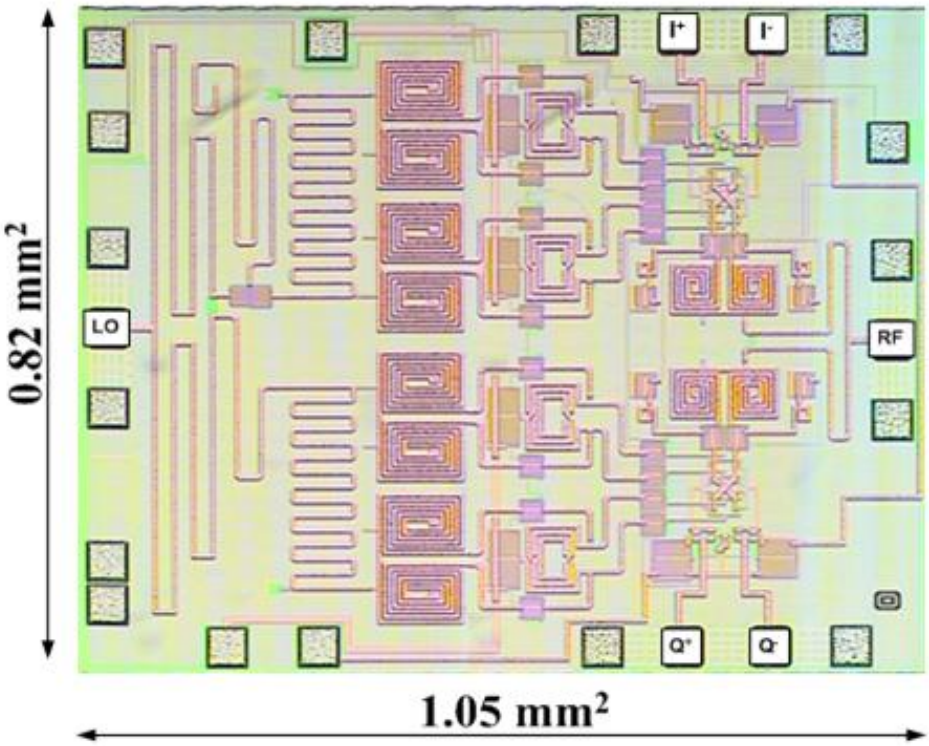


Fig. 2.31. Die photo of *E*-band modulator.

2.4 Experimental Results

2.4.1 Full *E*-band High Image Rejection Modulator Characteristic

The chip photo of the sub-harmonic IQ modulator is shown in Fig. 2.31, and the die sizes are 1.05 mm × 0.82 mm. The MMICs are tested via on-wafer probing with a good repeatability.

The V-band output spectrum of the modulator is observed by a spectrum analyzer (Agilent E4448A) and a preselected millimeter mixer (Agilent 11974V). The probe and cable loss from DUT to the preselected millimeter mixer is around 8.5 dB. Because the minute unwanted image signal is not easy to observe, we need to increase the input baseband signal for measurement. Fig. 2.32 shows the measured output spectrum of the CMOS sub-harmonic IQ modulator with an RF frequency of 66 GHz, an LO frequency

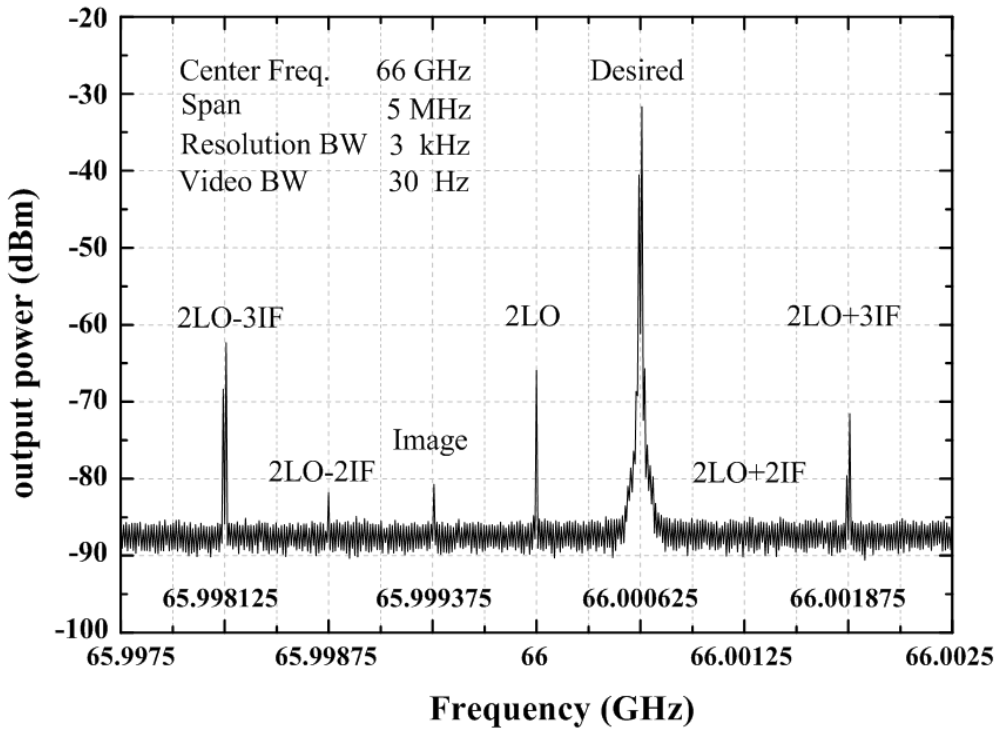


Fig. 2.32. Measured output spectrum of the *E*-band CMOS I/Q modulator with an 2LO frequency of 65 GHz and a IF frequency of 0.625 MHz.

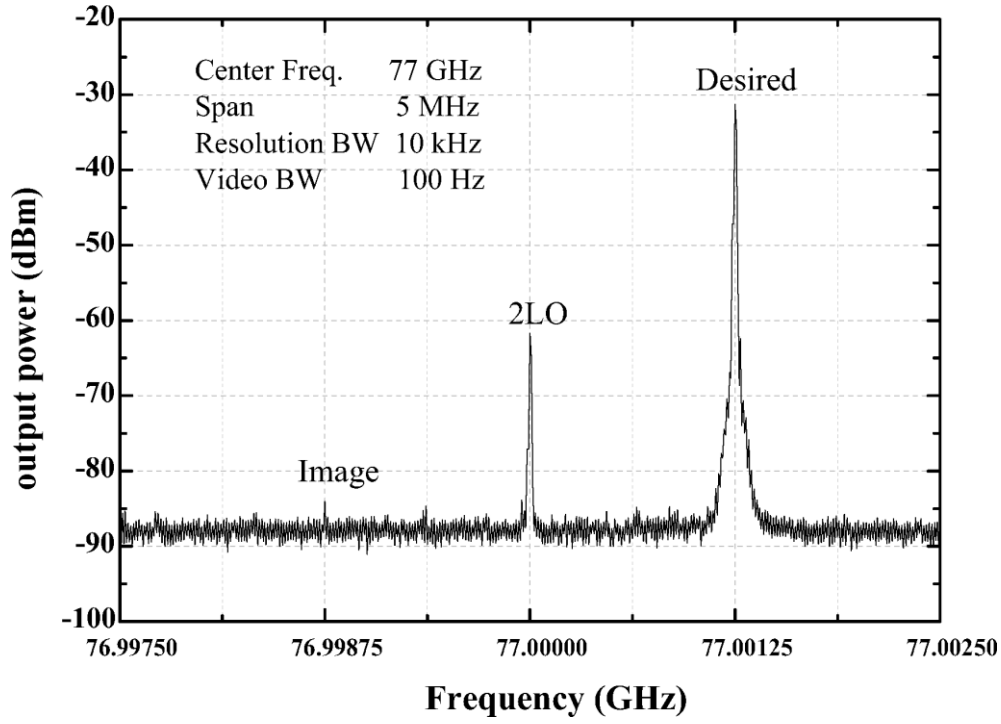


Fig. 2.33. Measured output spectrum of the E-band CMOS I/Q modulator with an 2LO frequency of 77 GHz and a IF frequency of 1.25 MHz.

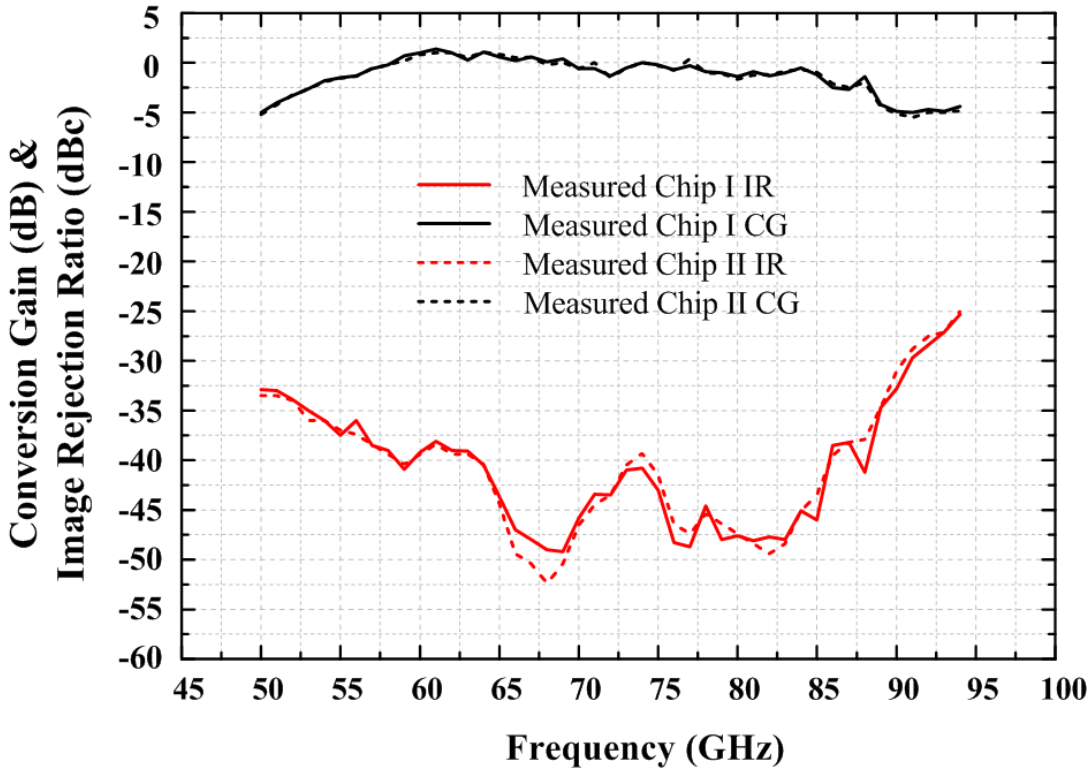


Fig. 2.34. The measured results of two *E*-band modulator chips.

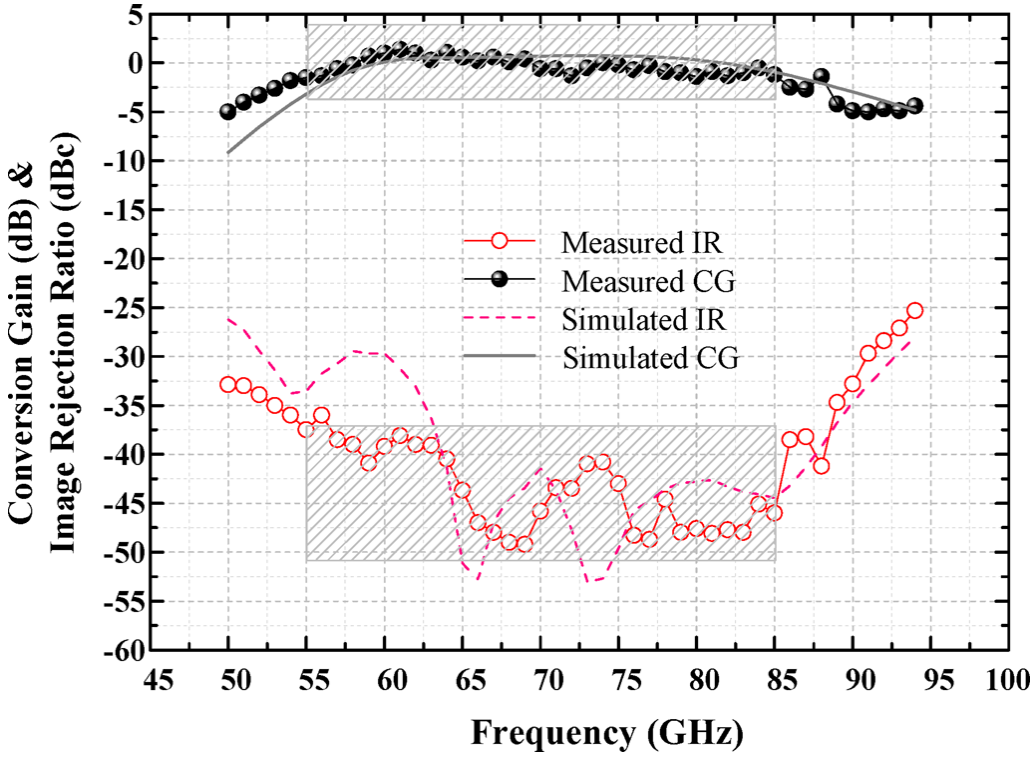


Fig. 2.35. Measured and simulated conversion gain and image rejection of the *E*-band modulator.

of 33 GHz, and a baseband frequency of 0.625 MHz, where the upper sideband is the desired signal and the lower sideband is the image signal. The measured output power of the modulator signal is -31.6 dBm including 8.5 dB path loss with the optimal LO drive power of 2 dBm and baseband input of -22 dBm. The measured image rejection is 49.1 dBc. The measured 2LO leakage power is -65.9 dBm; as a result, the 2LO to RF port isolation (LO leakage) is 59.4 dB. And the 2LO suppression is 34.3 dBc, referring to the desired output power. As the increased baseband power more than input 1-dB compression, the third-order intermodulation (2LO±3IF) components are incremental. The measured third-order and second-order IMD products are smaller than -30.7 dBc and -50.1 dBc referring to the desired output power, respectively.

The W-band output spectrum of the modulator is observed using a spectrum analyzer (Agilent E4448A) and a unpreselected harmonic mixer (Agilent 11970W). The unpreselected harmonic mixer is directly connected to probe. Fig. 2.33 shows the output spectrum with RF frequency of 77 GHz, LO frequency of 38.5 GHz, and baseband frequency of 1.25 MHz, where the upper sideband is the desired signal and the lower sideband is the image signal. The measured output power of the modulator signal is -31 dBm including 1.8 dB loss of the probe with the optimal LO drive power of 2 dBm and baseband input of -29 dBm. The measured image rejection is 48.7 dBc. The measured 2LO power suppression is 30 dBc, referring to the desired output power.

Fig. 2.34 shows the measured results of two *E*-band modulator chips. Based on the measurement results, our modulator exhibits good repeatability. The measured and simulated conversion gain and image rejection of the IQ modulator from 50 to 95 GHz are plotted in Fig. 2.35. The measured conversion gain is 0 ± 1 dB from 55 to 85 GHz with the total dc power consumption of 40.8 mW at 1.2-V supply. After adopting a load sensitivity analysis and a LO broadband 45° power splitter with amplitude and phase

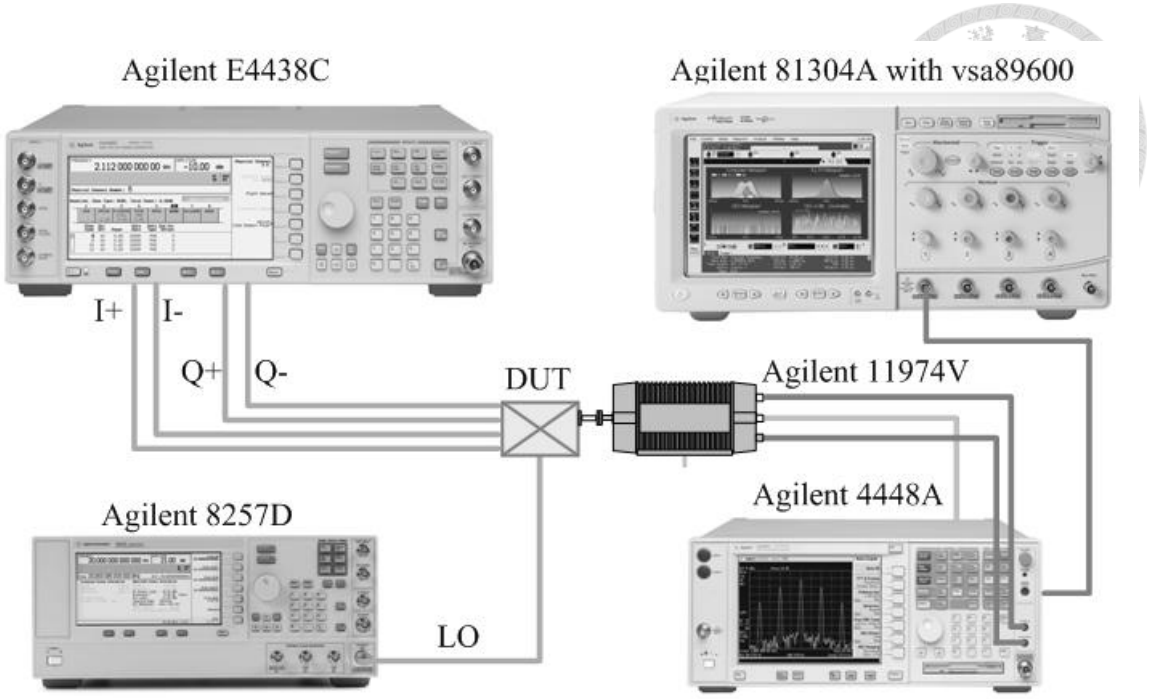


Fig. 2.36. Block diagram of the vector signal measurement system for the *E*-band modulator.

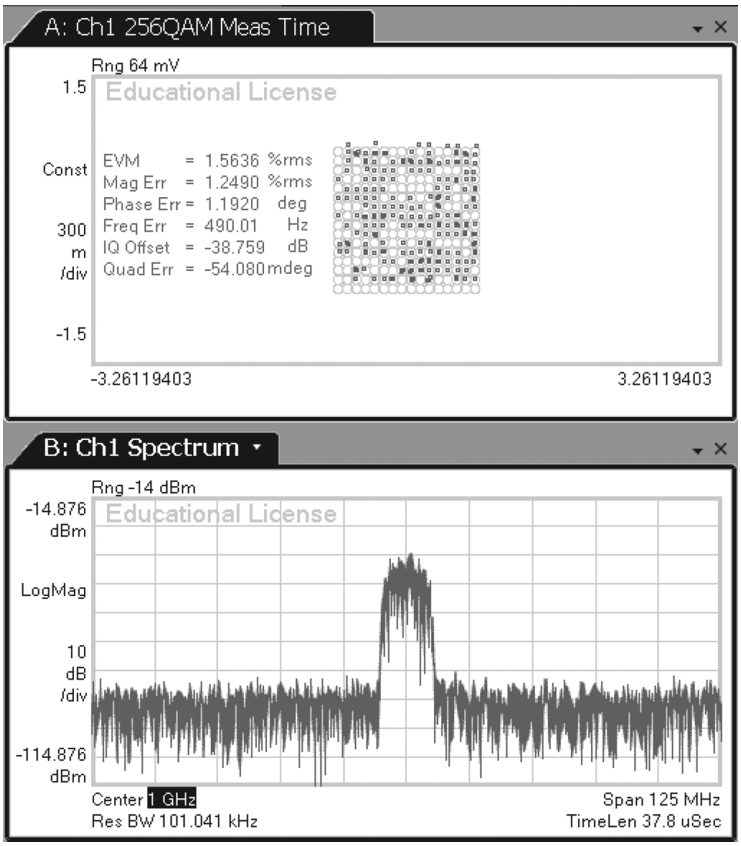


Fig. 2.37. Measured constellation diagram of the *E*-band modulator at 70 GHz with a 40 Mb/s 256-QAM modulation.

compensation, an image rejection ratio of more than 40 dBc is achieved over 64 to 84 GHz. The performance of our work with previously published MMW sub-harmonic mixers and modulators are summarized in Table 2-1.

To verify the digital modulation quality of the MMICs, the setup block diagram of the vector signal measurement system is shown in Fig. 2.36. The baseband IQ sources are generated by ESG vector signal generators (Agilent E4438C). The LO source of the modulator is provided by the signal generator (Agilent E8257C). The output spectrum is observed by using a preselected millimeter mixer (Agilent 11974V) and a spectrum analyzer (Agilent E4448A). The spectrum analyzer is also used for high-quality down-conversion of the output signal to an IF (321.4 MHz). This 321.4-MHz IF signal is fed into an oscilloscope (Agilent 54855A) with the software VSA 89600A for the analysis in the digital modulation. The sub-harmonic IQ modulator is evaluated by a 256-QAM modulation with a data rate of 40 Mb/s with the 7.5-dB back-off output power from 1-dB compression point from 64 GHz to 75 GHz. The measured output spectrum and constellation diagram of the IQ modulator with 70 GHz RF output signal is plotted in Fig. 2.37. The measured EVMs are all below 1.6%.

TABLE 2-1
PERFORMANCES COMPARISONS OF THE REPORTED CMOS MMW SUB-HARMONIC MIXERS AND MODULATORS

Reference	[33]	[38]	[39]	[40]*	[41]*	[42]*	This Work
Technology	0.13 μm CMOS	90 nm CMOS	90 nm CMOS	0.18μm CMOS	SiGe HBT	90 nm CMOS	65 nm CMOS
RF Freqency (GHz)	35–65	30–65	50–62	24	56–65	30–100	64–84
Conversion Gain (dB)	-6	-8	-13	1.5	-8	0	0 ± 1
Image Rejection Ratio (dBc)	20	< -12.5	< -20	0.6 dB/ 3.53°	N/A	N/A	< -40
2LO to RF port Isolation (dB)	> 50	> 42.5	> 40	-60	N/A	> 50	> 50
LO power (dBm)	8	4	4	6	5.5	10	2
DC power (mW)	75.9	21	0	10.05	0	58	40.8
Chip size (mm^2)	0.98×0.8	0.89×0.56	0.85×0.6	1.02×0.72	1.5×1.5	0.61×0.58	1.05×0.82

*down-conversion mixer

Chapter 3 CMOS 60-GHz Front-End Amplifiers

In the last few years, 7 GHz bandwidth of 60 GHz in the U.S. (57–64 GHz) and Japan (59–66 GHz) have been opened for unlicensed use [5]. This has led to significant progress of 60-GHz communications systems for a variety of applications including gigabit/s point-to-point links, wireless local area networks (WLANs), short-range high data-rate wireless personal area networks (WPANs) [43]. To fulfill market's needs for these applications, CMOS technology with advantages of low cost, low power consumption and high-level integration is tempting to develop the 60-GHz transceiver front-ends [44], [45]. In the past, the major concerns for the MMW front-end circuit design were area and performance. Recent advances in fabrication process with shrinking technology, low power has emerged as a principal issue of electronics industries. One of the most power-hungry circuits of a transceiver is the front-end amplifiers, especially power amplifiers. Thus, to improve the power efficiency of the PA is effective to reduce the overall electric energy consumption.

In this chapter, a high efficiency power amplifier in 65nm CMOS technology is introduced firstly. Then, another broadband 60-GHz LNA design for low power application using 90nm CMOS process is presented.

3.1 A 57-66 GHz 12.9-dBm Miniature Power Amplifier with 23.4% PAE in 65-nm CMOS

3.1.1 Introduction

For green electronics and mobile system design, minimizing the power consumption in the power amplifier is important. Several reported 60-GHz CMOS amplifiers have demonstrated good gain and power performance [46]-[50]. As reported, power combining topologies, such as Wilkinson power combining [46], transformer-based power combining [47]-[48], and direct power combining [45], are commonly used to achieve higher output power with low-voltage CMOS devices. Despite these efforts, further improvement in the efficiency of CMOS PA for 60-GHz low-power applications continues to challenge the designers.

To produce a high efficiency and sufficient gain, this section describes a broadband high efficiency power amplifier for the 60-GHz low-power applications. The regulations in some countries, mandates a 10-dBm transmit power limit, as shown in Fig. 3.1 [51]. The main goal of this work is to maximize the efficiency of a 10-dBm power amplifier with a 9-GHz operating bandwidth (from 57 to 66 GHz). To deliver such a power level with high efficiency, the low-loss direct combining topology with two optimized transistors is used. First-order matching networks are used for minimum-loss and broadband gain-flatness consideration. The PA provides 16.7-dB peak gain and 12.9-dBm saturated power while drawing 57 mA under a 1.2-V supply, and achieves drain efficiency of 42% and peak power added efficiency (PAE) of 23.4%. If the supply is set to be 1.0 V, the PA achieves 11.5 dBm of saturated power and 22.3% of peak PAE. To the best of authors' knowledge, this PA achieves the best PAE among the reported 60-GHz bulk CMOS PAs.

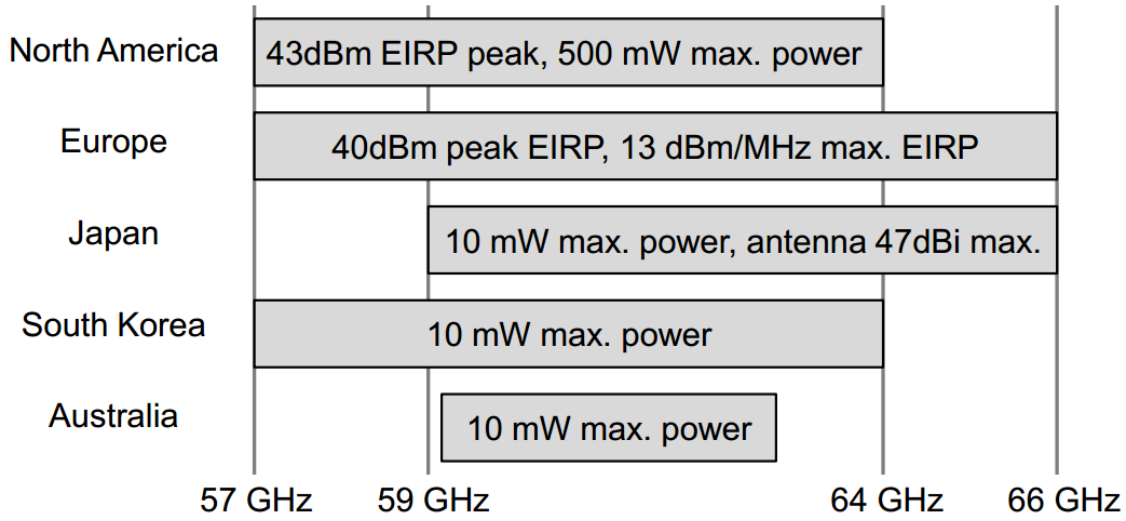


Fig. 3.1. Regulation of the 60-GHz band in regions

3.1.2 Device Characteristic and MMIC Process

This 60 GHz PA prototype is implemented in TSMC commercial standard bulk 65nm 1P9M CMOS process. This process provides single poly layer for the gates of the MOS and nine metal layers with ultra-thick top metal (metal 9) of 3.4 μm. The RF performance of the 2-μm 24-finger FET biased at 1.2 V has a maximum frequency of oscillation (fmax) of 190 GH. Passive elements including MiMcaps are available between metal 8 and metal 7. Two types of polysilicon resistors are provided by choosing the individual dose of ion-implantation separately from the gate electrode doping process.

3.1.3 Circuit Design

As shown in Fig. 3.2, the PA is a two-stage common-source topology with the transistor size ratio 1:2. The first stage of PA is designed as a driver stage, and the output stage is designed for high efficiency with 10-dBm output power. The two parallel

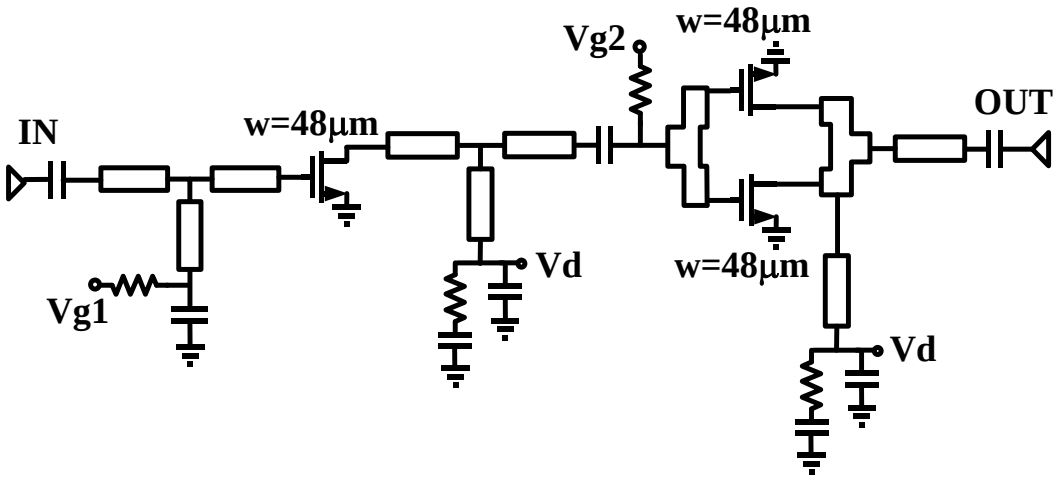


Fig. 3.2. Schematic of the 2-stage CMOS PA.

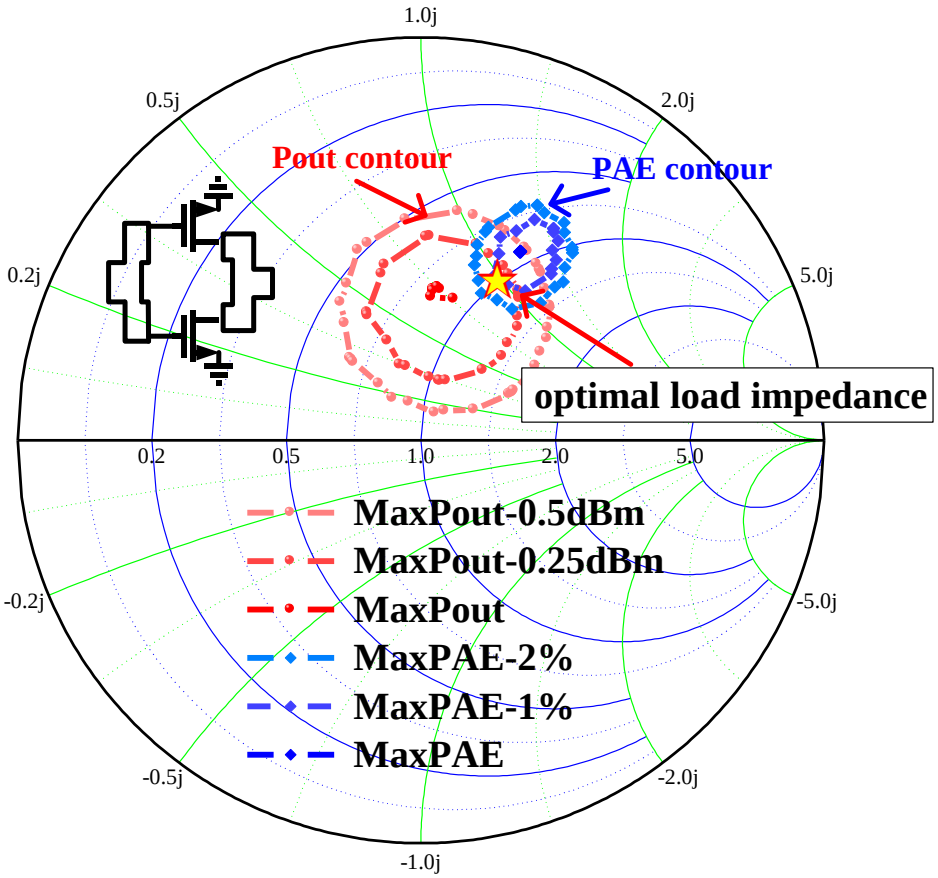


Fig. 3.3. The output load-pull power contour and PAE contour of two combined transistors (the Smith chart with the center impedance re-normalized to 12.5-Ω.).

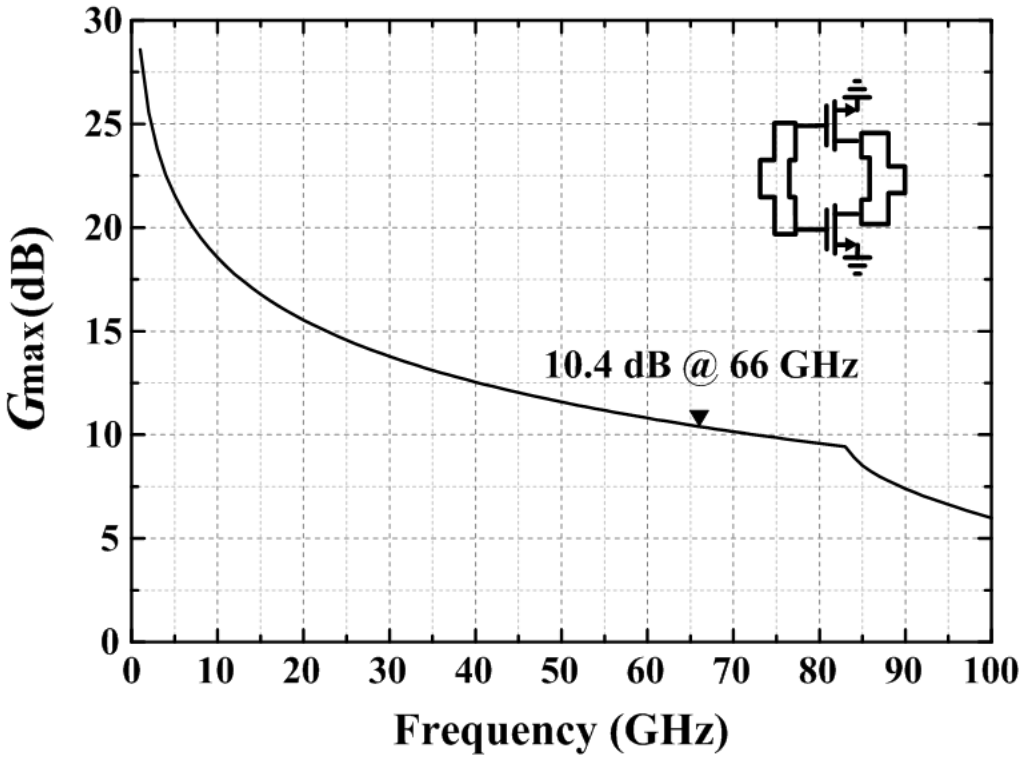


Fig. 3.4. The simulated maximum available gain (Gmax) for the devices.

combined transistors with gate periphery of 48 μm at the output stage are selected to produce target output power and sufficient gain. Fig. 3.3 shows the output power contour and PAE contour of two combined transistors of the load-pull data on the Smith chart with the center impedance re-normalized to 12.5-Ω. The 12+j12 Ω optimized load impedance is a compromise between high efficiency and output power.

To reduce the loss from matching networks, TFMS lines are adopted for the matching circuits and interconnections. Using TFMS for matching elements, we can easily realize the broadband load-pull matching. The simplified output-matching with a shunt stub and a series stub is designed to transfer the optimal load of the FET to 50 Ω and to provide the dc path. Also the input and inter-stage matching networks are all realized by first-order matching networks, which simultaneously achieve broadband matching, low path loss, and compact chip size. Fig. 3.4 shows the simulated maximum available gain (Gmax) for the two combined transistors. The simulated minimum insertion loss of

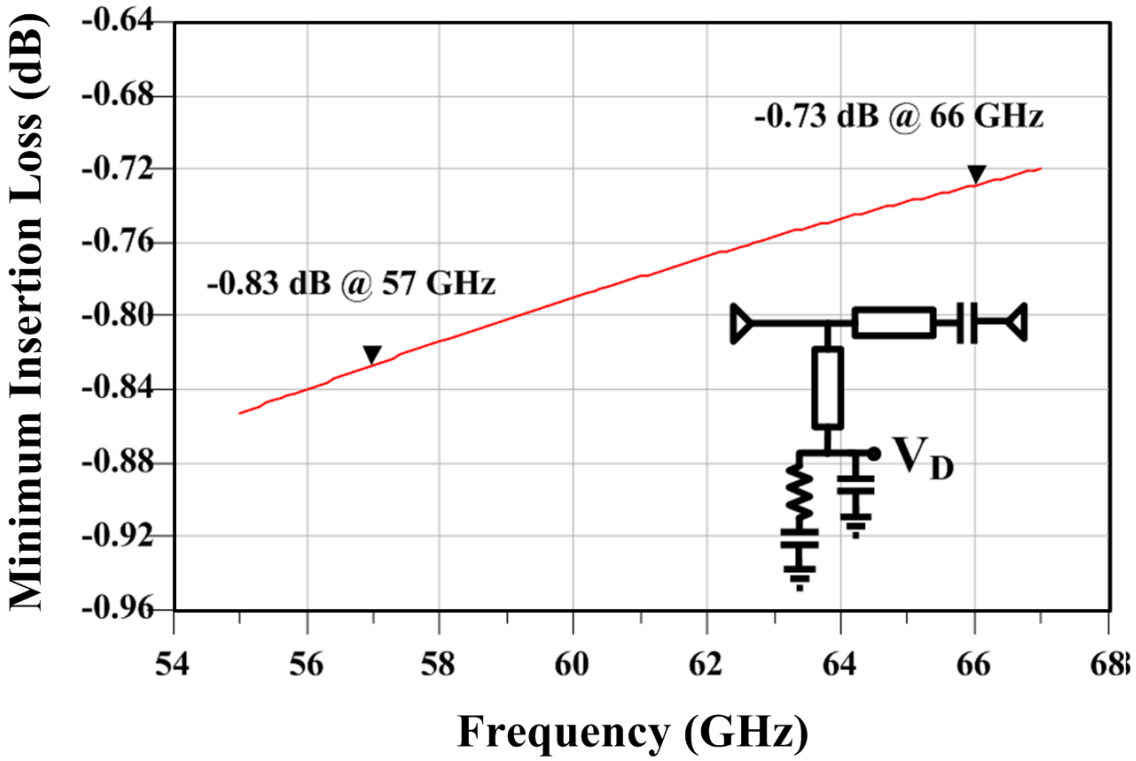


Fig. 3.5. The simulated matching loss of output stage matching network.

output, input and inter stage matching network are shown in Fig. 3.5, Fig. 3.6 and Fig. 3.7. The 1.84-pF capacitors are used for in-band RF bypass network. The shunt 4.53-pF and 20 Ω bypass networks are used to ensure low-frequency stability. The passive components including the TFMS lines, discontinuities, and capacitors are simulated by a full-wave EM simulator (Sonnet software). The whole circuit of the amplifier is simulated with Agilent ADS. Fig. 3.8 shows the simulated small signal S-parameter for 1.2-V supply. It has a flatness simulated small signal gain around 16 dB at 1.2V bias over the frequency range of 57 to 66 GHz. Fig. 3.9 shows the simulated gain, output power and PAE versus input power from 57 to 66 GHz under 1.2-V supply. The simulated output 1-dB compression point (OP_{1dB}) of the amplifier is more than 10 dBm from 57 to 66 GHz. The PAE at OP_{1dB} and the peak PAE are above 15 % and 25% from 57 to 66 GHz, respectively. The die photo is shown in Fig. 3.10.

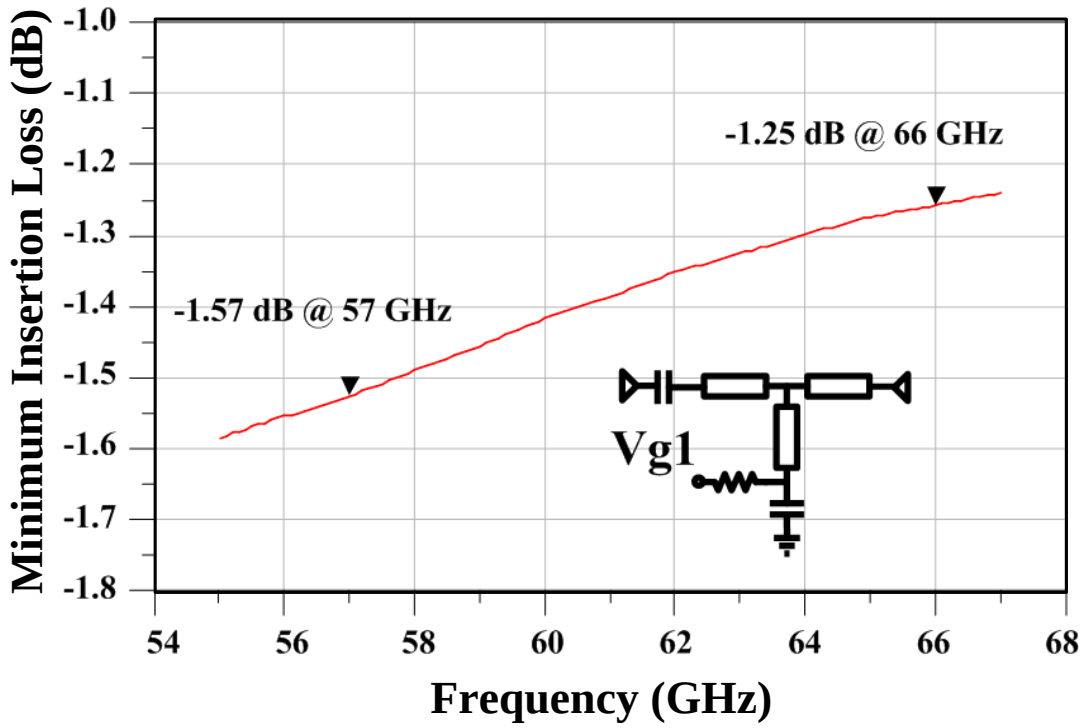


Fig. 3.6. The simulated matching loss input stage matching network.

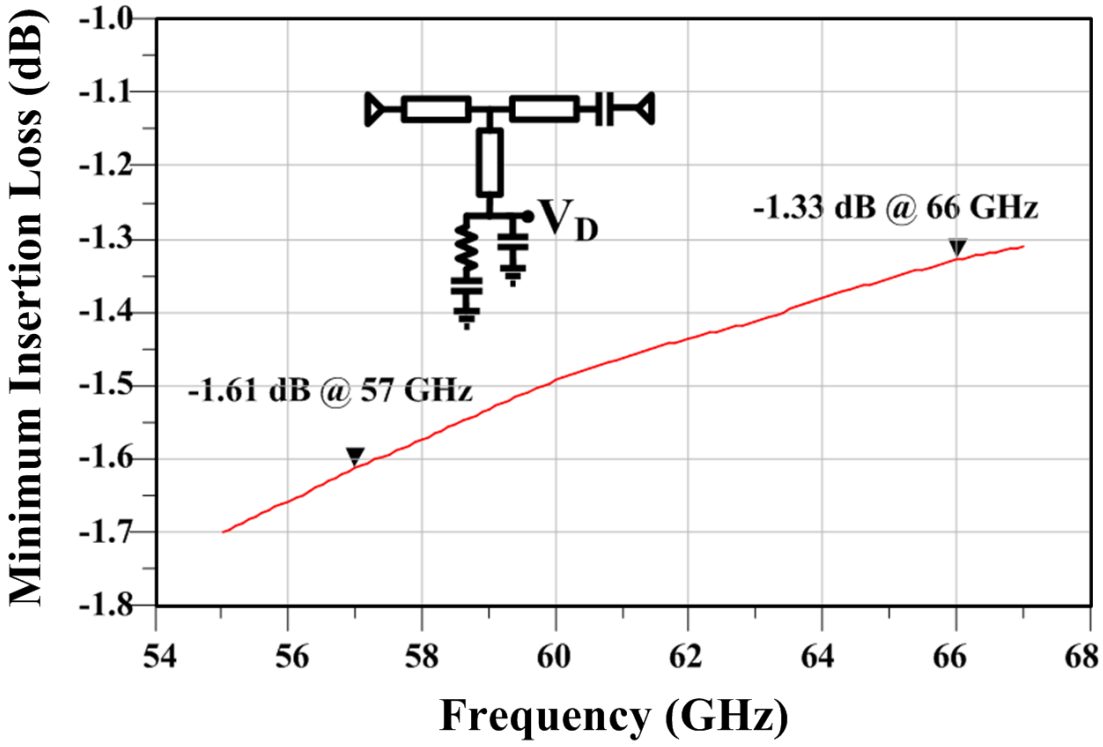


Fig. 3.7. The simulated matching loss of inter stage matching network.

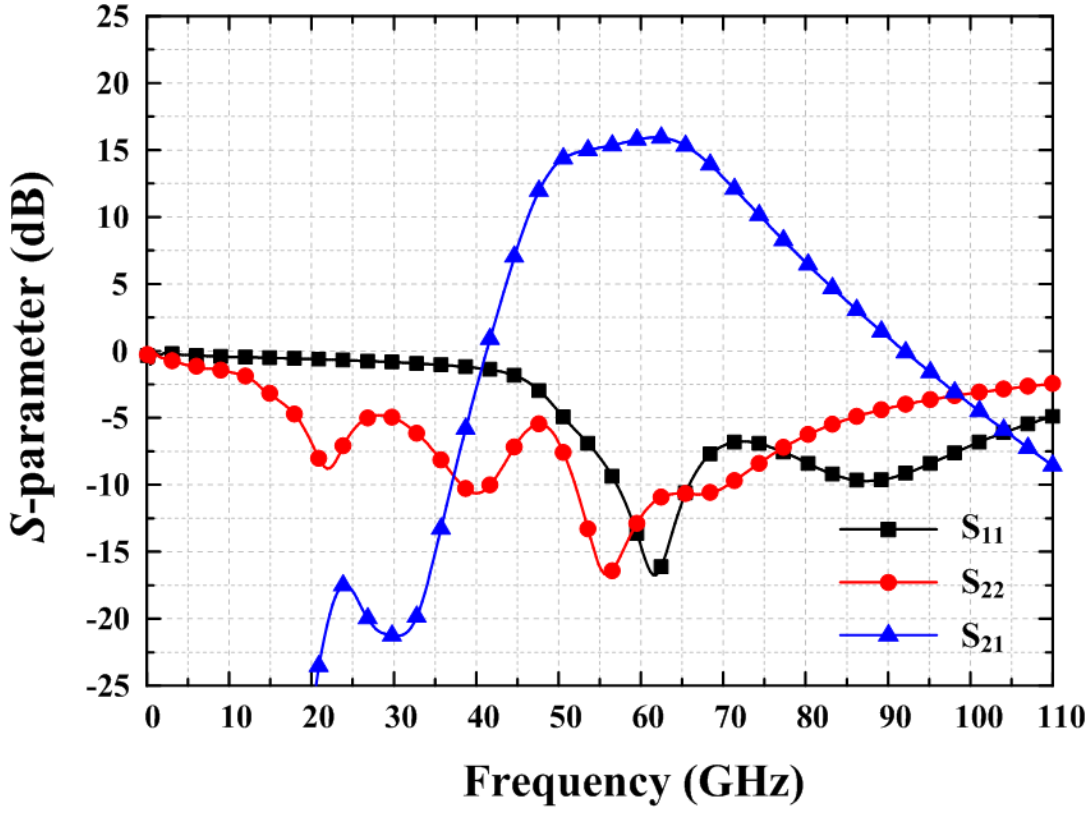


Fig. 3.8. The simulated small signal S-parameter for 1.2-V supply.

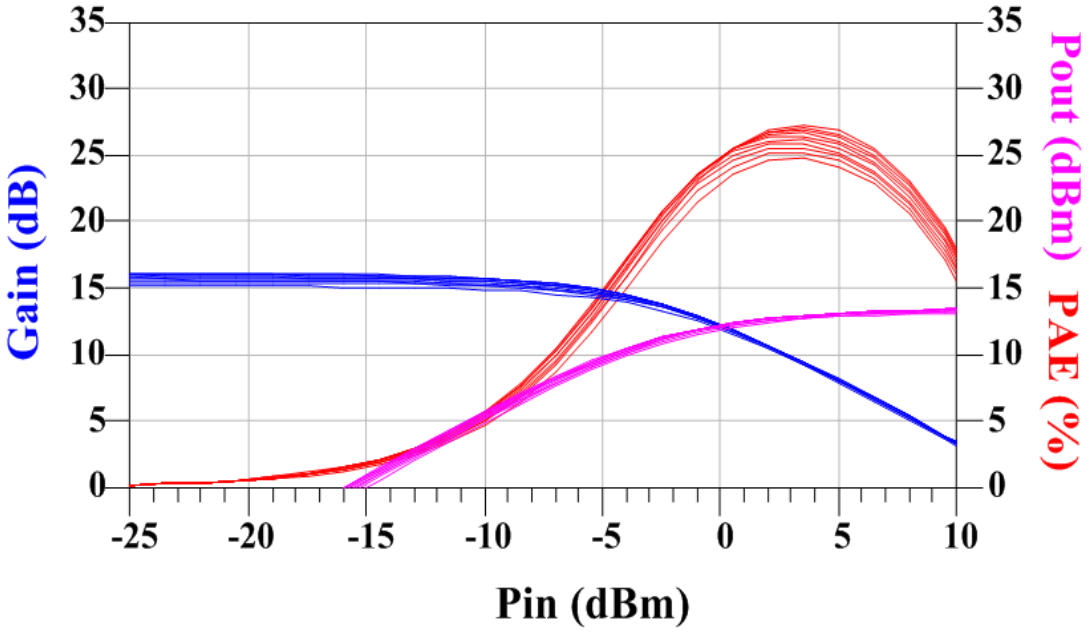


Fig. 3.9. The simulated gain, output power and PAE versus input power from 57-66 GHz under 1.2-V supply.

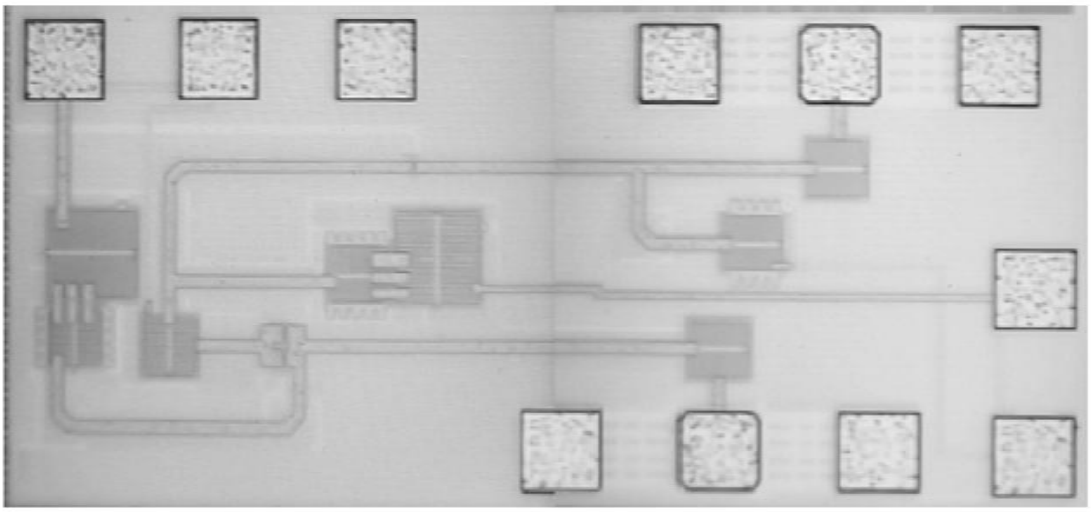


Fig. 3.10. The chip photo of 60 GHz CMOS LNA with die size of 0.3 mm x 0.67 mm.

3.1.4 High Efficiency Power Amplifier Characteristic

Three PA chips were measured using on-wafer probing with a good repeatability. Fig. 3.11 plots the small signal S-parameters from 30 to 67 GHz and shows good fit between the simulated and measured data for 1.2-V supply.

Fig 3.12 plots the measured small signal S-parameters from 30 to 67 GHz at 1.2V and 1.0V drain bias with total static current of 51mA and 46mA, respectively. The measured small signal gain is 16.2±0.5 dB at 1.2V bias and 15.6±0.5 dB at 1.0V bias, respectively, over the frequency range of 57 to 66 GHz. The input and output return losses achieve the consistent results of less than -10 dB for both biases at 60 GHz. The measured Pout, power gain, and PAE versus Pin characteristics at 64.5 GHz are plotted at Fig. 3.13. The measured output 1-dB compression point (OP1dB) of the amplifier is 9.4 dBm, and Psat is 12.9 dBm under the 1.2-V supply and the 57-mA dynamic drain current at Psat. At 12.9-dBm saturated output power, there is a 39-mA dynamic current comes from the last satge, which is corresponding to the 42% drain efficiency. The PAE at OP1dB and the peak PAE are 13.6 % and 23.4%, respectively. If the supply is set to be 1.0 V, the

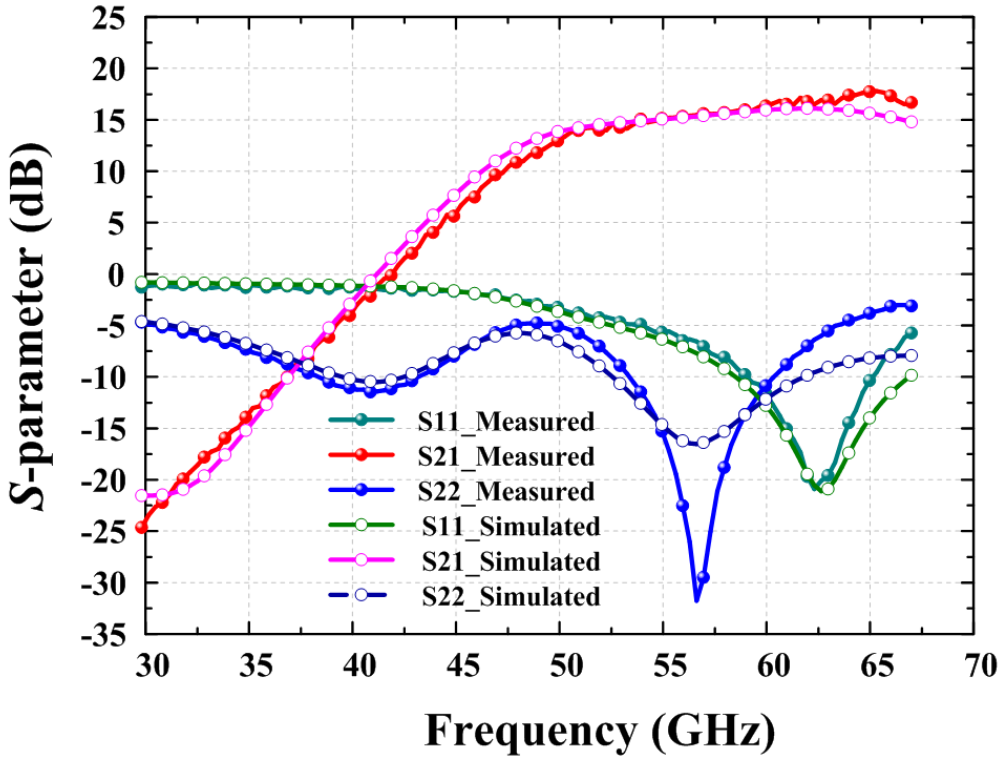


Fig. 3.11. Simulated and Measured small signal S-parameter for 1.2-V supply.

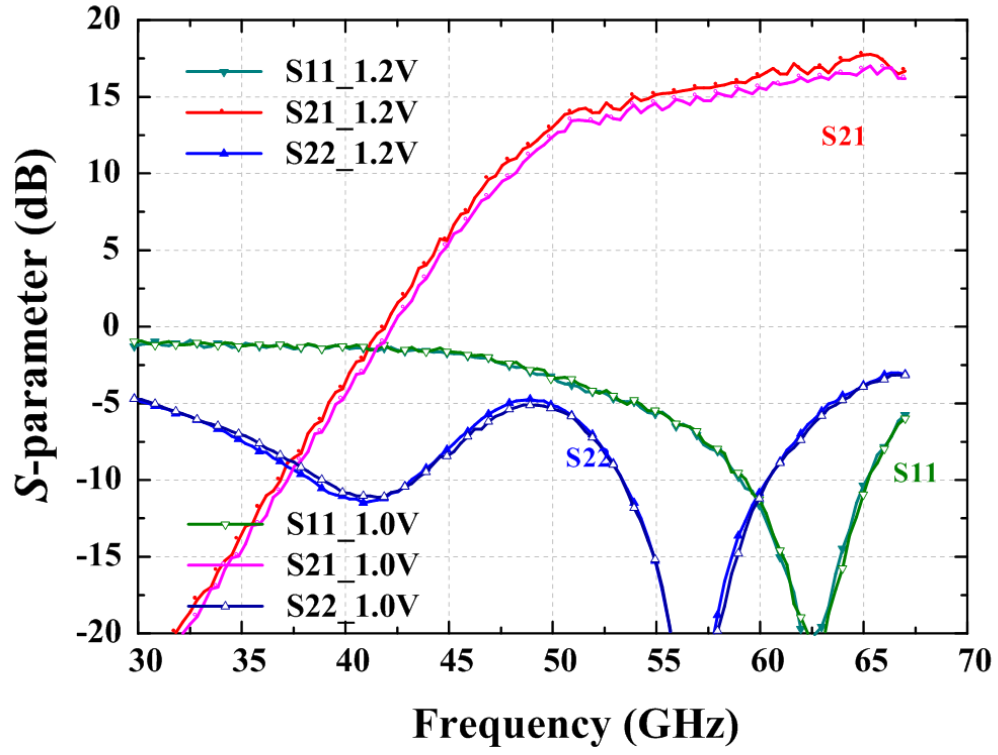


Fig 3.12. Measured small signal S-parameter for 1.2 and 1.0-V supply.

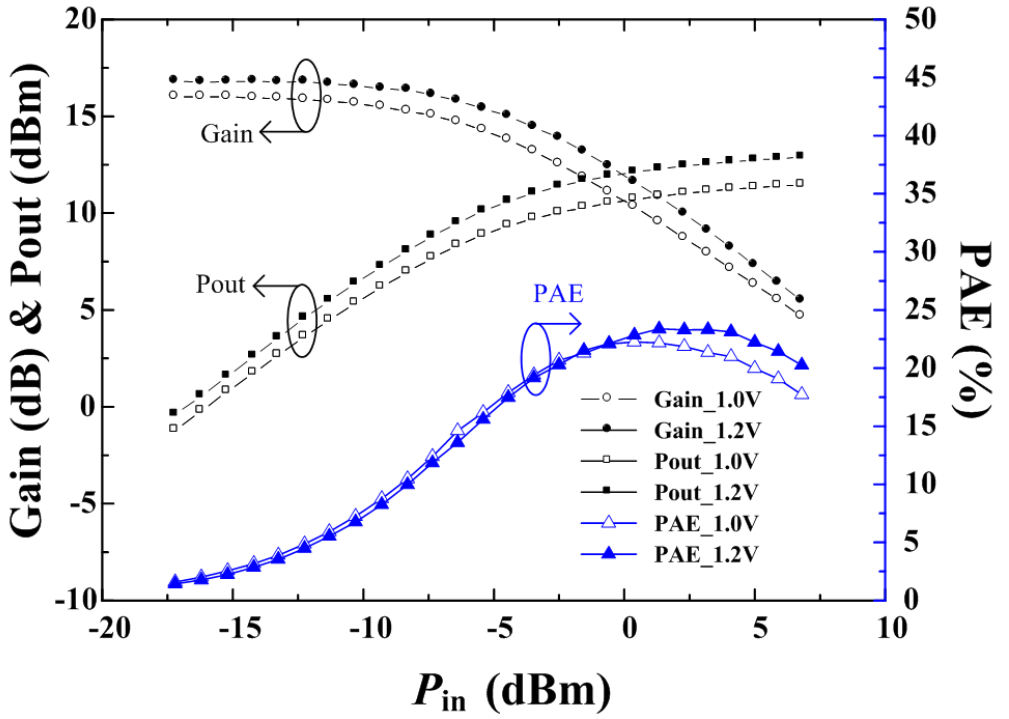


Fig. 3.13. The measured gain, output power and PAE versus input power at 64.5 GHz under 1.2 and 1.0-V supply.

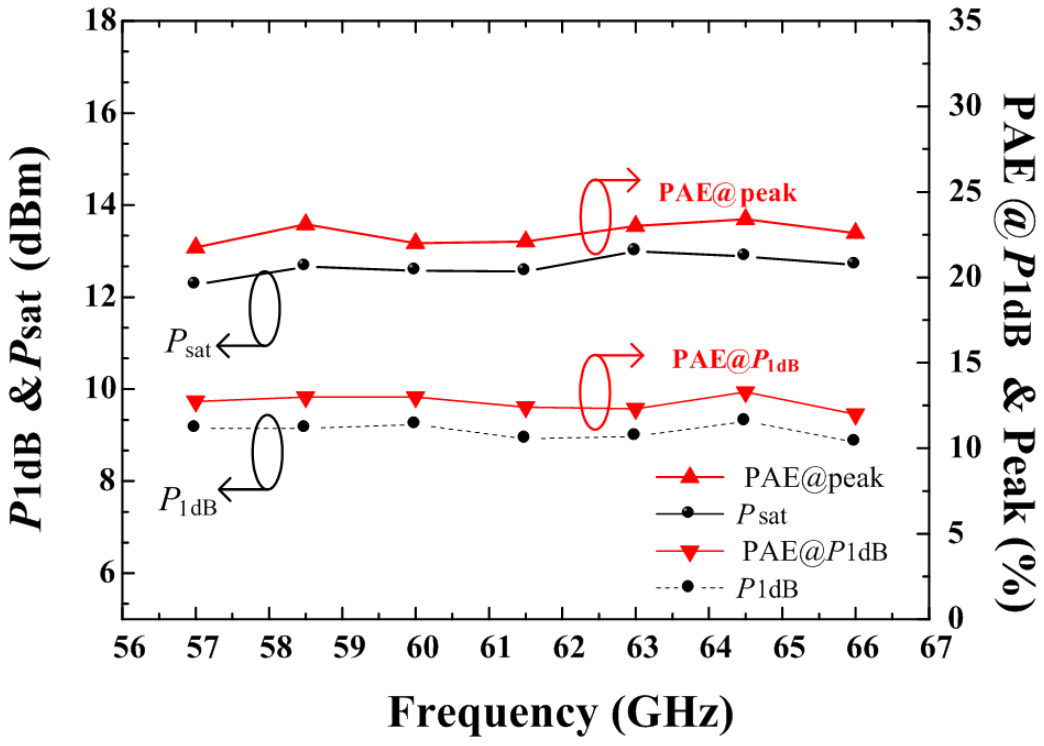


Fig. 3.14. Measured PAE and P_{out} versus frequency for 1.2-V supply.

OP1dB is 7.7 dBm and Psat is 11.5 dBm. The PAE at OP1dB and the peak PAE are 12.4 % and 22.3%, respectively.

Fig. 3.14 shows the broadband characteristic of this PA. The measured 1-dB compression point and saturated output power with their PAE at 1.2-V bias are plotted from 57 to 66 GHz. The OP1dB of 9.2±0.2 dBm, and the PAE at OP1dB of 12% to 13.6% are obtained in the range of 57 to 66 GHz. The measured Psat is 12.6±0.3 dBm and the corresponding peak PAE is greater than 22% over the 60-GHz band. Since both the power performance and high efficiency are achieved over the full band, this PA demonstrates the capability for multiple channel operation in the worldwide unlicensed 60-GHz band.

Table 3-1 summarizes the reported state-of-the-art performances of the CMOS PAs. Although medium to high power amplifiers have been demonstrated in CMOS processes, we further improve the efficiency in this design. By applying direct-combining topology, this PA demonstrates the highest PAE 23.4% and 42% drain efficiency for 1.2 supply among these reported 60-GHz bulk CMOS PAs. The performance is comparable to the PA in SOI process [52] . For the integrated phased-array systems and the handset devices, this PA design is a good candidate due to its high efficiency performance and small size.

TABLE 3-1
PERFORMANCE SUMMARY

Technology	90nm CMOS [46]	65nm CMOS [47]	65nm CMOS [48]	65nm CMOS [49]	40nm CMOS [50]	65nm CMOS SOI[52]	This Work	This Work
Topology	CS**	CS*	CS*	CS***	CS***	CAS	CS	CS
Voltage (V)	1.2	1.0	1.0	1.2	1.2	1.8	1.2	1.0
Peak PAE (%)	14.2	11.1	15.1	10	7	25	23.4	22.3
P1dB (dBm)	18.2	15.7	15	19.6	17	12.7	9.3	7.7
Psat (dBm)	19.9	17.9	18.6	23.2	22.6	14.5	12.9	11.5
Gain (dB)	20.6	19.2	20.3	16.3	29	16	16.7	16.1
Core size (mm^2)	<1.665	0.83	0.11	2.04	2.16	0.573	0.11	0.11

CS: Common-Source, CAS: Cascode, * transformer power combiner, ** 4-way power combining, *** 32-way power combining.

3.2 A 0.6-V 60-GHz Low-Power LNA with Forward Body Bias Technique in 90 nm CMOS Process

3.2.1 Introduction

To achieve high gain performance in MMW design, it usually requires considerable power to boost the transistor performance. The cascode configuration is widely used in LNA design [53]. However, the low power consumption and green-mode operation are increasing concerns for portable devices. The cascode configuration with a higher supply voltage is not suitable for low voltage application. As the gate length of the CMOS transistor continues to shrink, the supply voltage is scaled down accordingly [54]. The CMOS device reliability issue sets a limit to the supply voltage, which has been previously discussed in a 60-GHz amplifier design [45]. Unfortunately, the low supply voltage may degrade performances as well. Therefore, to reduce supply voltage and power consumption while maintaining good performance is a design challenge for 60-GHz amplifier.

In this section, we present a 60-GHz miniature three-stage common source LNA in 90-nm CMOS process. To further reduce supply voltage, our LNA using forward-body-biased technique that make this MMIC operate under 0.6-V and 4.8-mW dc power, in the meanwhile, achieves a peak gain of 16.5 dB at 58 GHz and 1-dB bandwidth from 54 to 61 GHz with a compact chip size. Since the power consumption and amplifier gain bandwidth product (GBP) are usually design trade-offs, it is observed that the proposed LNA outperforms all the reported CMOS amplifiers around 60 GHz with good small signal gain, low power consumption, and the lowest supply-voltage.

This section also discusses the eligibility of the general purpose (GP) and low power (LP) 90nm CMOS technologies, to meet the low power dissipation challenge using

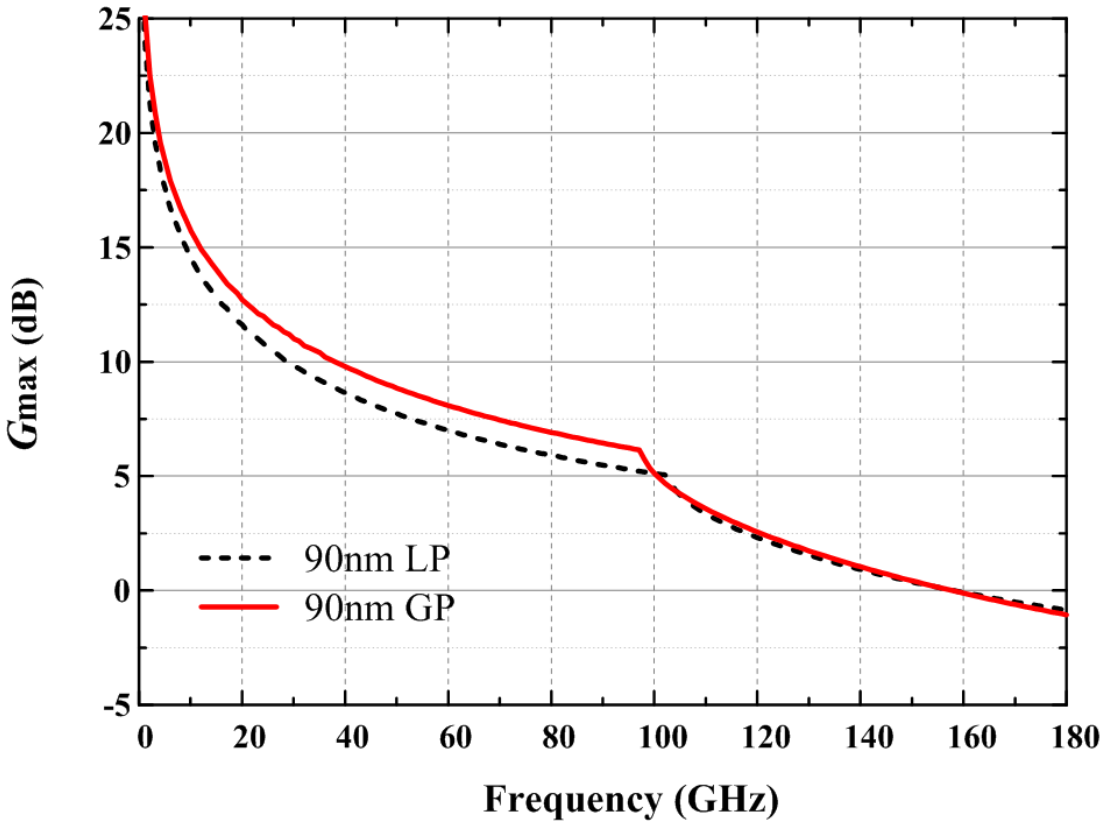


Fig. 3.15. Comparison of maximum available gain of NMOS transistor of 1.6 μm 10 fingers under same dc power consumption with GP and LP process.

forward-body-biased technique without compromising the high frequency performance.

3.2.2 Device Characteristic and MMIC Process

The 60-GHz LNA is fabricated using TSMC commercial standard bulk 90-nm 1P9M CMOS GP and LP processes. The biggest difference between GP and LP processes are the dc characteristic and frequency response of MOSFET. In addition, the threshold voltage in the GP process is lower than that in the LP process. Fig. 3.15 shows the comparison of maximum available gain of 16-μm NMOS transistor with GP and LP process under same dc power consumption. A RF NMOS transistor of 1.6 μm 10 fingers

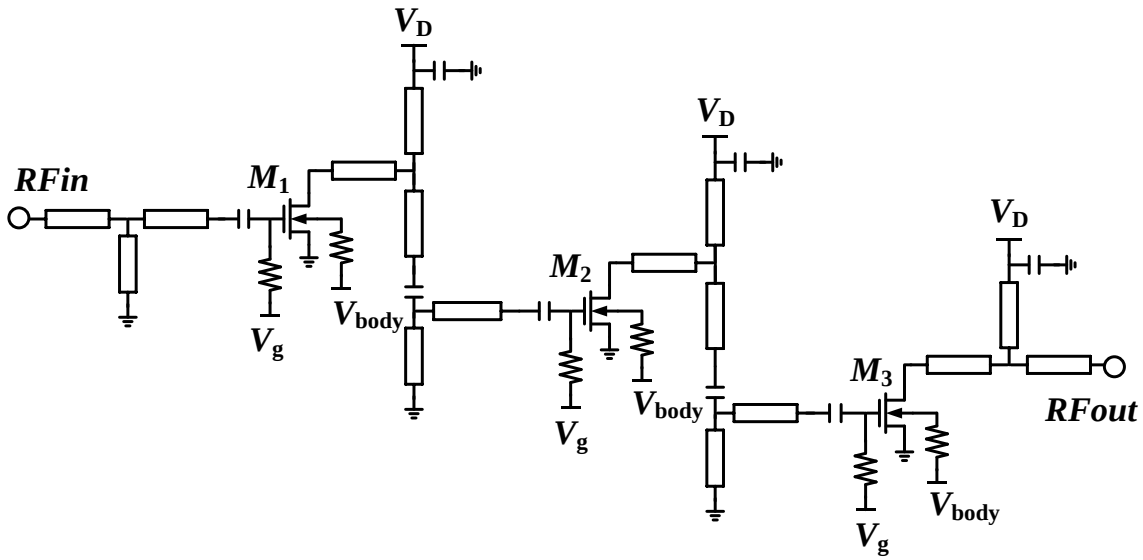


Fig. 3.16. The schematic of 60 GHz CMOS three-stage common source LNA.

using GP process biased at 0.6 V has the maximum frequency of oscillation (f_{max}) of 158 GHz and the maximum available gain (MAG) of 8.08 dB at 60 GHz. The same size transistor using LP process biased at 0.7 V has the f_{max} of 160 GHz and 6.99 dB MAG at 60 GHz. Apart from the characteristic of transistors, the two processes all provide single poly layer for the gates of the MOS and nine metal layers with ultra-thick top metal (metal 9) of 3.3 μm [55]. Passive elements including MiMcaps are available between metal 8 and metal 7. Two types of polysilicon resistors, with several Ω/□ and kΩ/□, are provided by choosing the individual dose of ion-implantation separately from the gate electrode doping process.

3.2.3 Circuit Design

To operate the LNA at reduced supply voltage and low power consumption condition while providing sufficient gain, a body forward bias technique is introduced in [56] at 5 GHz. Forward body bias technology is used to further reduce V_{th}. The threshold voltage of MOSFET is well known as

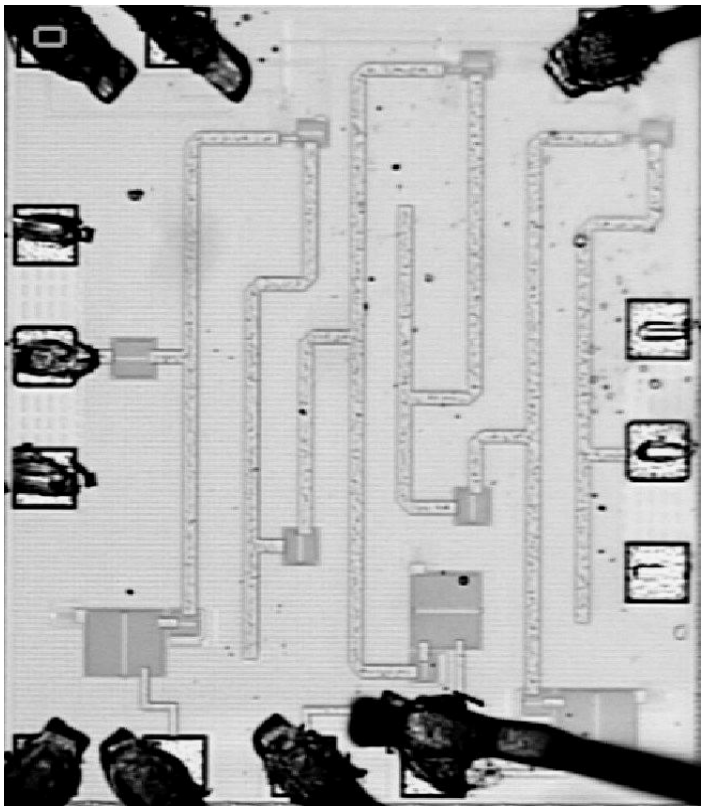


Fig. 3.17. The chip photo of 60 GHz CMOS LNA with die size of 0.65 mm x 0.54 mm.

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}\right) \tag{1}$$

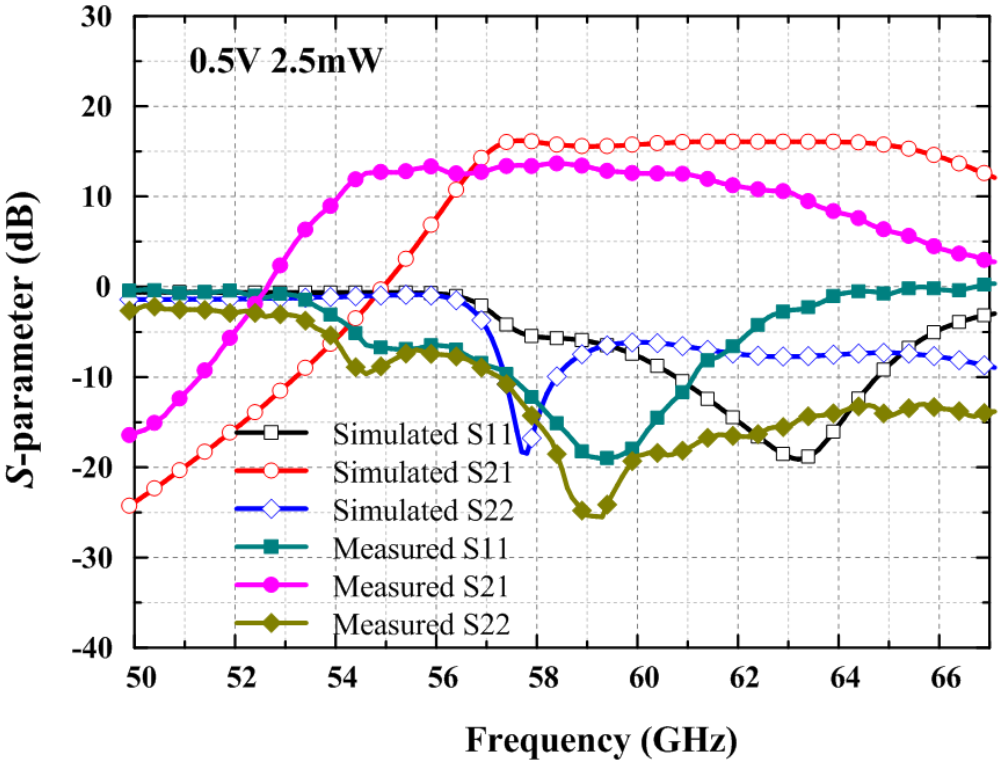
where V_{th0} is the threshold voltage when V_{bs} = 0, γ is the body-effect coefficient, φ_f is the bulk fermi potential, V_{bs} is the voltage between body and source. Thus, changing V_{bs} can modify V_{th}, which can achieve a dynamic threshold voltage MOSFET (DTMOS) [56]. The forward body bias technology has been presented in low frequency design, and this LNA shows the feasibility of this technique in MMW frequency application.

The 60-GHz LNA is a three-stage common source design. Fig. 3.16 shows the schematic of the amplifier. TFMS lines are used for the matching circuits and interconnections [55]. The matching networks consist of series and shunt TFMS lines. All lines are kept as short as possible to minimize loss and the circuit size. Because of the advantage of the ground plane shielding to isolate the conductive substrate, the

matching network can be meandered in a very compact area to reduce the circuit size without suffering the coupling effect. And taking into consideration the high-frequency radiation, the corner of meander TFMS lines is smoothly curved with arcs to prevent the abrupt change in the signal field direction. The transistors in each stage are 10 fingers with a total gate periphery of 16 μm (each with 1.6-μm unit finger length). The 0.6-pF capacitors are used for in-band RF bypass network. Several shunt RC bypass networks are used to ensure low frequency stability. The passive components including the TFMS lines discontinuities and capacitor were simulated by a full-wave EM simulator (Sonnet software). The whole circuit of the amplifier was simulated with Agilent ADS. It draws total of 8-mA dc current from the 0.6-V supply voltage with the GP devices. A 0.25-V forward body bias is used to make the transistors in strong inversion region. Fig. 3.17 illustrates the chip photograph of the fabricated 60-GHz CMOS LNA (GP and LP). The chip size is only 0.65 x 0.54 mm^2 including all testing pads and dummy metal.

3.2.4 Experimental Results

The 60-GHz CMOS LNA chips were measured via on-wafer probing. Fig. 3.18 plots the simulated and measured S-parameters of the 90nm GP process from 50 to 67 GHz at 0.5 V and 0.6 V drain bias with total current of 5 mA and 8 mA, respectively. At a supply voltage of 0.5 V, the measured small signal gain has a peak gain of 13 dB at 58 GHz. Under 0.6-V supply, the measured small signal gain has a peak gain of 16.5 dB at 58 GHz with 1-dB bandwidth of 7 GHz from 54 to 61 GHz. The input and output return losses are better than 10 dB from 57 to 61 GHz. With regard to using 90-nm LP process, the simulated and measured S-parameters of the 90nm LP process is shown in Fig. 3.19. It shows that the measured small signal gain is 13 dB with 1-dB bandwidth from 54.5 to 61 GHz. According to the measured results, it can be observed that the frequency



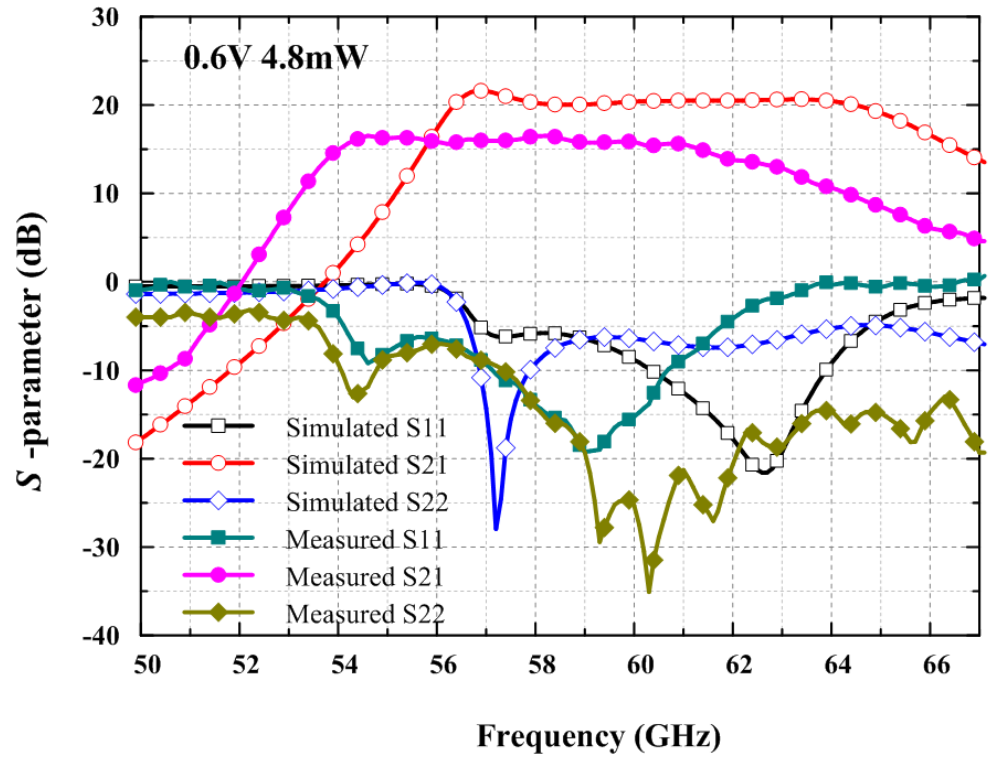


Fig. 3.18. The measured S-parameters of the 60 GHz CMOS LNA at 0.6-V supply voltage 4.8mW and 0.5-V supply voltage 2.5 mW.

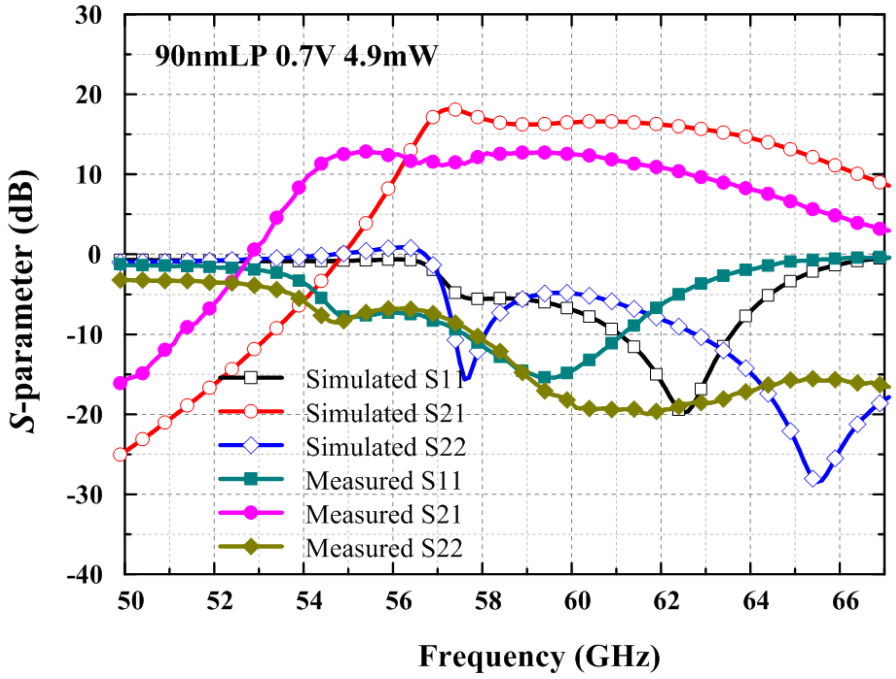


Fig. 3.19. The measured S-parameters of the 60 GHz CMOS LNA at 0.7-V supply voltage 4.9mW.

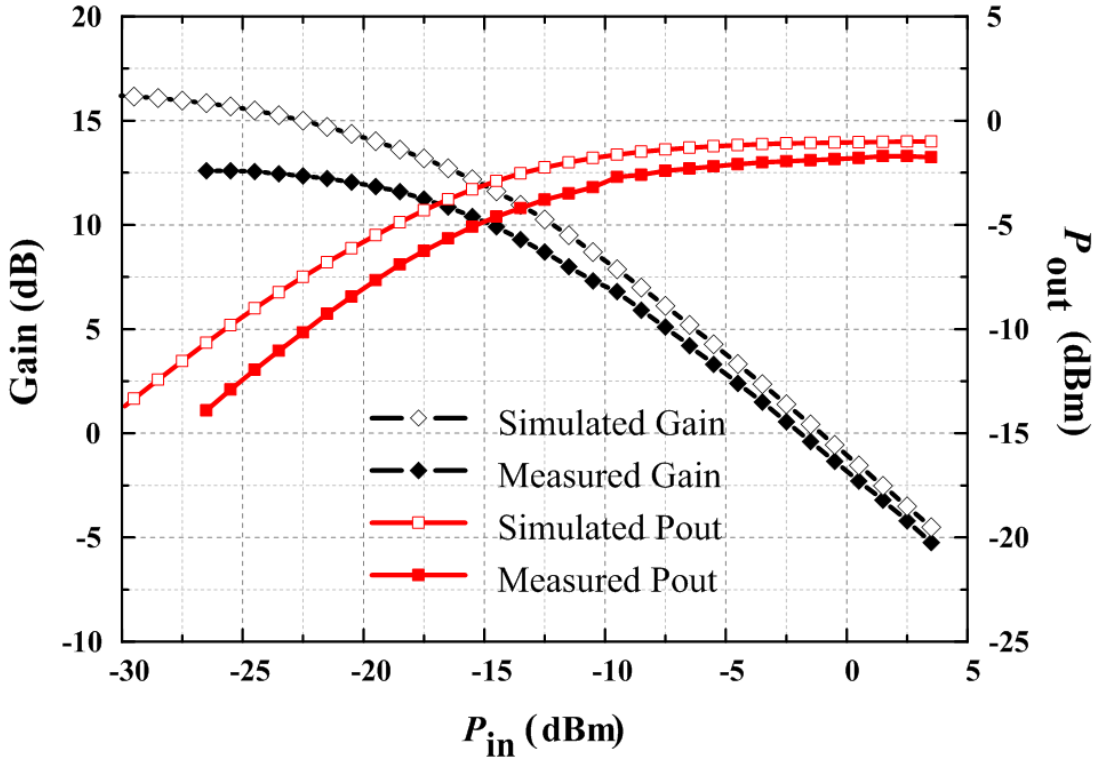


Fig. 3.20. The measured P_{in} - P_{out} and P_{in} -Gain characteristics at 60 GHz at 0.7-V supply voltage and 4.9 mW.

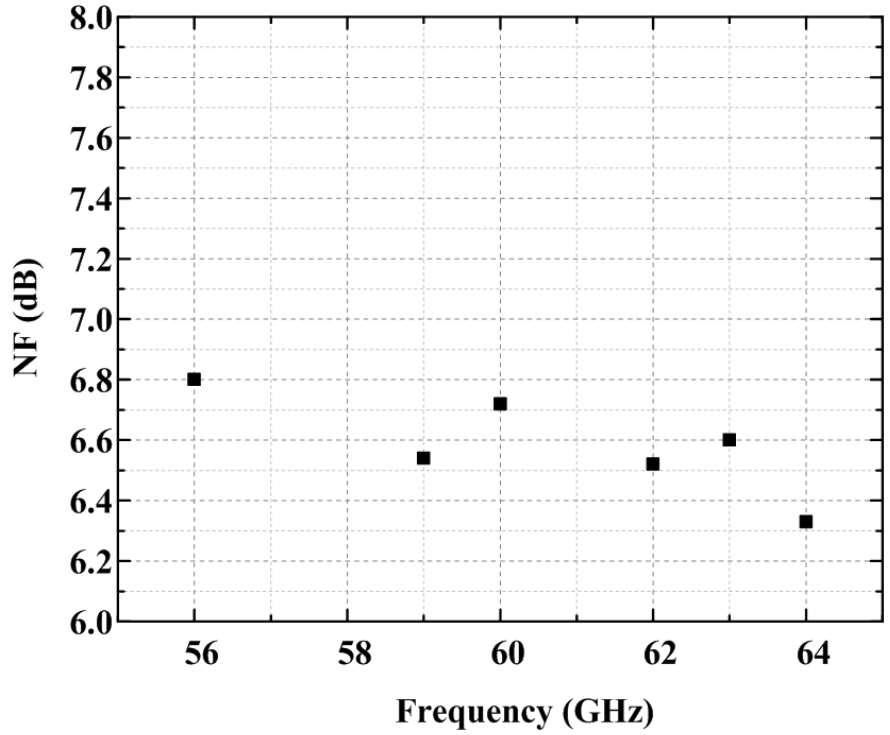


Fig. 3.21. The measured noise figure at 0.7-V supply voltage and 4.9 mW.

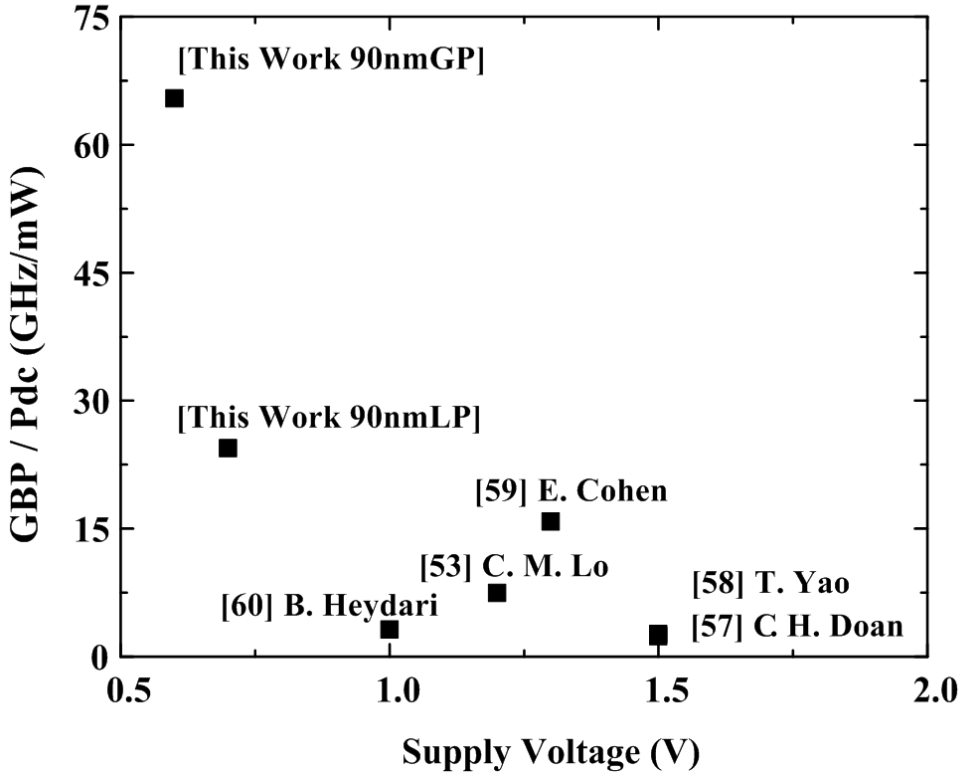


Fig. 3.22. The ratio of GBP to DC consumption vs. Supply Voltage.

responses have approximately 3-GHz shift. The discrepancies between simulated and measured results are possibly due to the uncertainty of the device model. This disagreement in frequency shift may result in degradation in S_{21}. The simulated and measured P_{in} versus P_{out} characteristics at 60 GHz are plotted in Fig. 3.20. The measured output 1-dB compression point of the amplifier is -7 dBm, and the saturated output power is -1.7 dBm at 60 GHz. The measured noise figure at the same bias condition is shown in Fig. 3.21, and it exhibits a minimum of 6.3 dB at 64 GHz. All experimental results are measured including the pad parasitic.

To emphasize the flat gain characteristic for broadband application, we use the 1-dB bandwidth to calculate the gain-bandwidth product (GBP), and use the ratio GBP to power consumption to compare with the current publications. Fig. 3.22 shows that the lower supply voltage in our design can also achieve the high performance for broadband amplifier design. The experimental results show that the proposed MMW LNA is suitable for low power and low voltage applications in both 90 nm GP and LP process. Table 3-2 summarizes the recently reported performance of 60-GHz CMOS amplifiers. It can be observed that the superior gain performance of this design by the ratio of GBP to dc power, especially when considering this LNA only operates such a low supply voltage.

TABLE 3-2
PERFORMANCE COMPARISON OF CMOS 60-GHZ BROADBAND LNAS

Ref.	Tech.	Freq. (1dB-BW)	Topology	Gain[dB]	NF[dB]	Vdd[V]	P_D[mW]	GBP/ P_D [GHz/mW]
This work	90-nmLP CMOS	54.5-61 GHz (6.5)	3-stage CS (TFMS)	13	6.3	0.7	4.9	26.47
	90-nmGP CMOS	54-61 GHz (7)	3-stage CS (TFMS)	16.5	N/A	0.6	4.8	65.14
[57]	130-nm CMOS	53-62 GHz (9)	3-stage CAS (CPW)	12	8.8	1.5	54	2.64
[58]	90-nm CMOS	57-59 GHz (2)	2-stage CAS (Lumped0	14.6	<5.5	1.5	24	2.4
[59]	90-nm CMOS	57-59 GHz (2)	3-stage CS (Lumped)	15	4.4	1.3	4	15.81
[60]	90-nm CMOS	61-63 GHz (2)	2-stage CS (CPW)	12.2	6	1	10.5	3.16

CS: Common-Source, CAS: Cascode, TFMS: Thin-Film microstrip line

Chapter 4 1024 QAM 60-GHz IQ Transmitter in 65-nm CMOS Process

4.1 Introduction

The 60 GHz band with a massive amount of spectral space (5 GHz) has been allocated worldwide for dense wireless local communications. Much effort has been carried out to develop for high-speed multi-gigabit wireless systems for the assignment of the large bandwidth around 60 GHz. Currently, the draft of the IEEE 802.11ad 60-GHz standard defines the highest data rate up to 7 Gbs with a 64 quadrature amplitude modulation (QAM) [5]. The requirement for high-speed communications, such as a huge data file transmission and real-time video streaming, are extremely increasing. With the increased demand, the 60-GHz spectrum may no longer be able to accommodate all application needs. As a result, using the advanced modulation scheme, 1024 QAM, is a relatively cost-effective way to improve the capacity in high-speed application. Compared with 64-QAM and equivalent coding rates, 1024-QAM provides 1.67x (67%) efficiency gains. However, as the price paid for the high spectral efficiency, the 1024-QAM systems place more stringent requirements than the slow-data rate modulations. There are several kinds of factors such as IQ mismatch, LO phase noise, local oscillator spur, non-linearity and analog-to-digital converter (ADC) resolution.

In this chapter, the high image rejection 60-GHz direct-conversion transmitter is designed and implemented for 1024 QAM data transfer. The presented transmitter with 33-dB conversion gain and the 11-dBm saturated power improves the dynamic range for the measurement consideration. Through the characteristics of the high image rejection, the good LO signal suppression, the direct-conversion transmitter MMIC with the

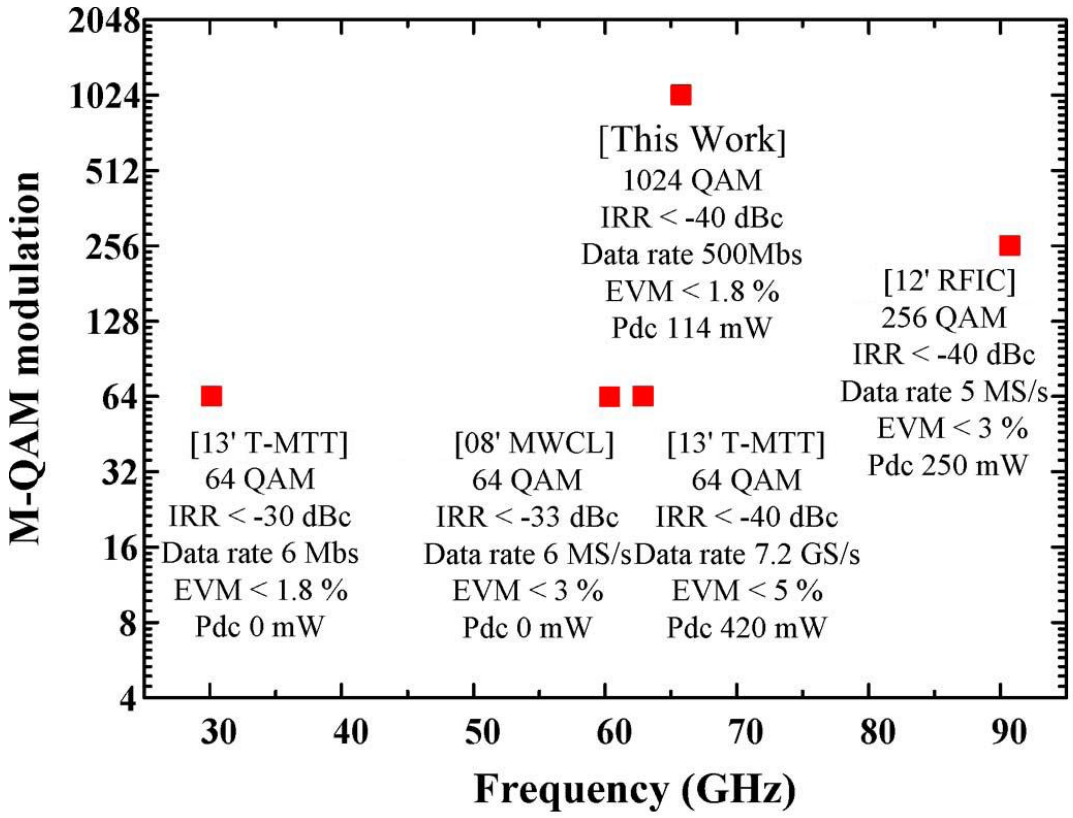


Fig. 4.1. Millimeter-wave high-order QAM modulation comparison.

10-dB back-off output power from 1-dB compression point demonstrates a 1024-QAM modulated signal (modulation capability) with a data rate of 500 Mb/s and the EVM results are within 1.7% at 65 GHz. Fig. 4.1 shows a comparison between our design and other works of MMW high-order QAM modulation [18], [19], [61], [62].

4.2 Circuit Design

To use the advanced modulation scheme, a 60-GHz linear high image rejection direct-conversion 60-GHz transmitter is designed in 65-nm CMOS process. The transmitter consists of a sub-harmonic modulator and four stage amplifier, as shown in

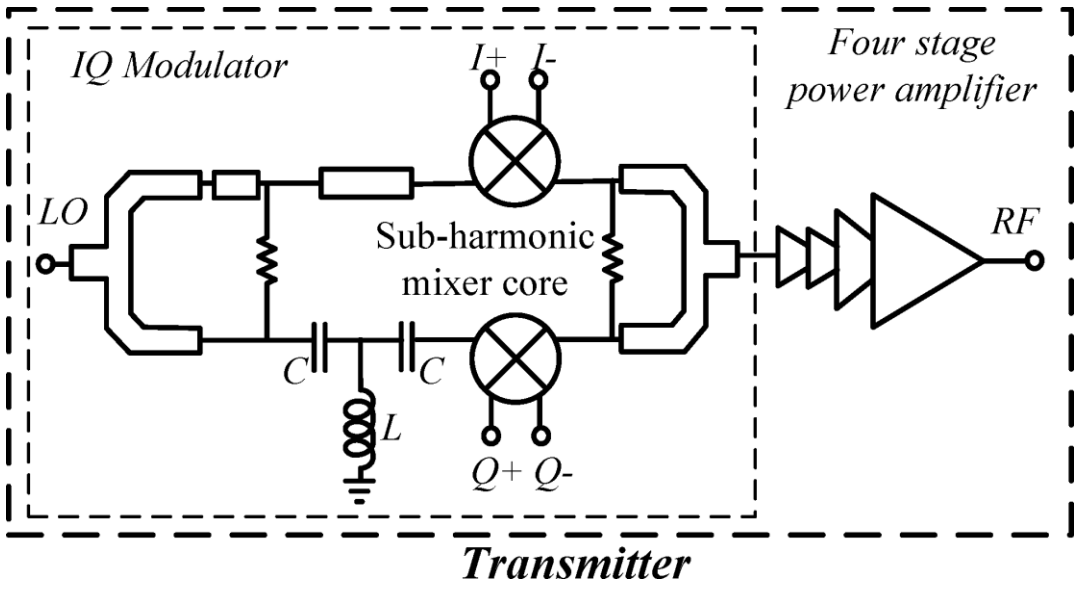
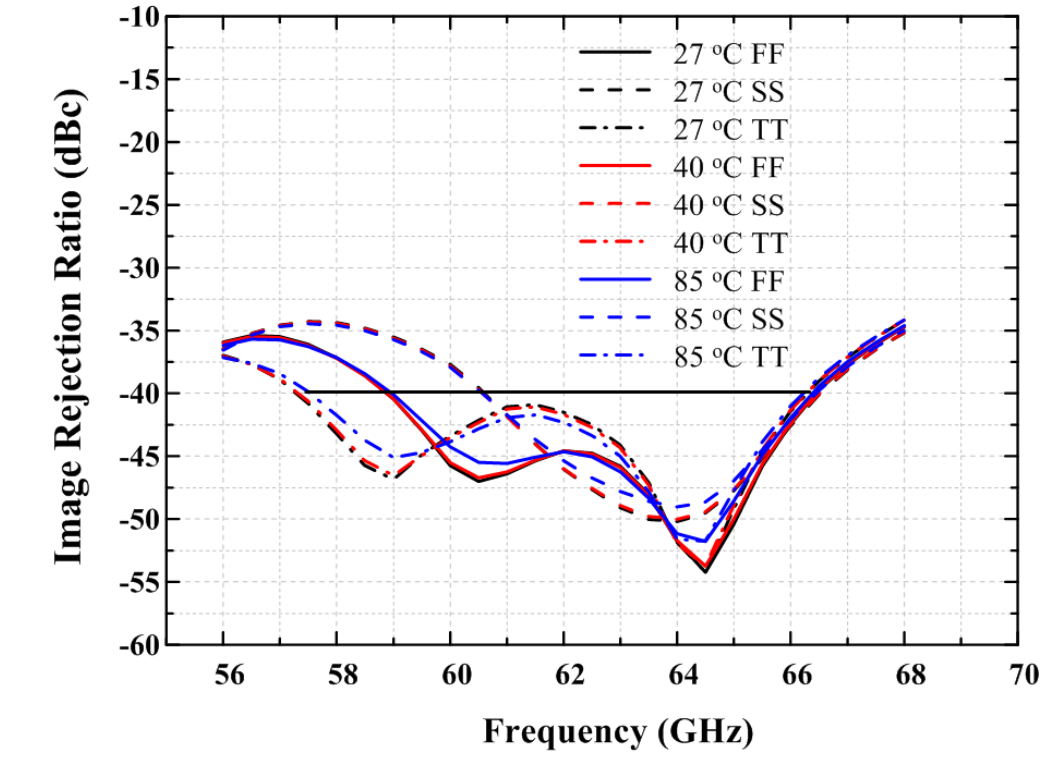


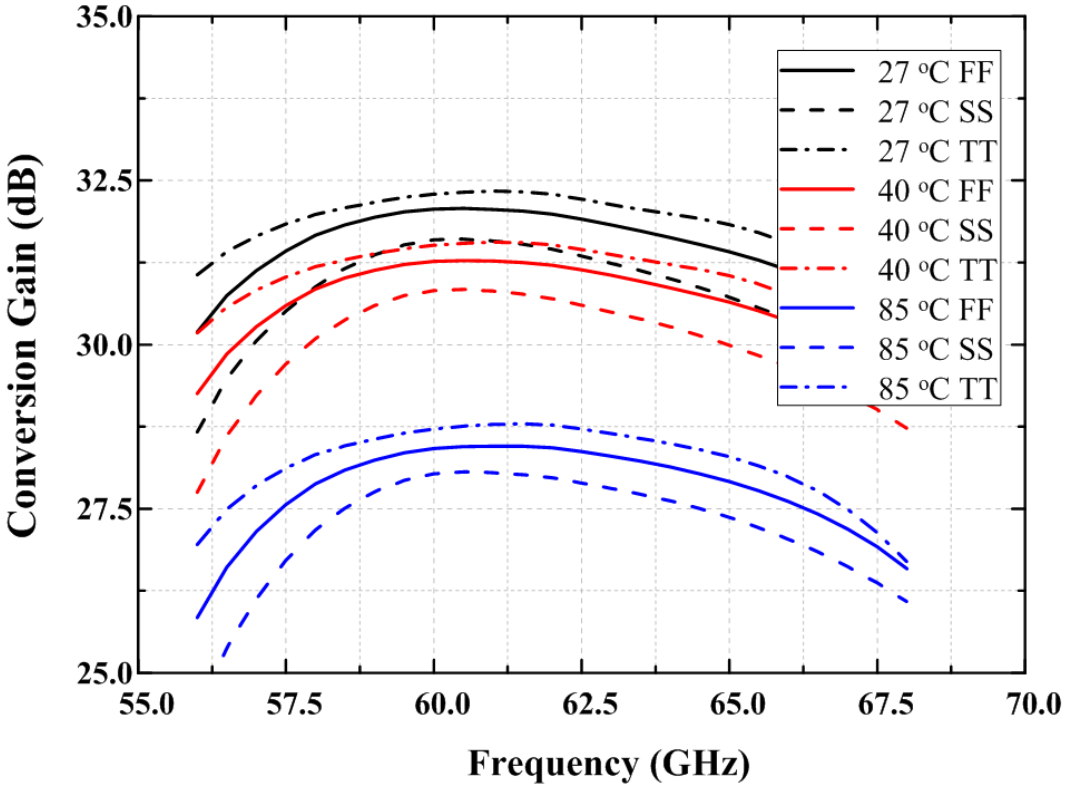
Fig. 4.2. The block diagram of the 60-GHz transmitter.

Fig. 4.2. The advantage of the subharmonically pumped mixer in MMW application has been described. The modulator design is similar to previous discussion in chapter 3. The size of the switching core is modified to 24 μm, which provides higher conversion gain and output power at 60-GHz band. The matched built-in LO buffers with 28 μm is selected for 30-GHz LO operation. In addition, the four-stage common-source configuration amplifier is used as the buffer and PA in the transmitter, as shown in Fig. 4.2. To produce a high efficiency and sufficient gain, two parallel combined transistors with the same size, 48 μm, at the output stage were selected in this design [63]. The size ratio of these four stages is close to 1:1:2:4 to make sure that the signal is amplified in the linear region.

The full-wave EM simulation is carried out on Sonnet, and the circuit is simulated by Advanced Design System (ADS). The PVT corner simulations and the monte-carlo analysis with 10% variation on all transistors are used to show the effects of process

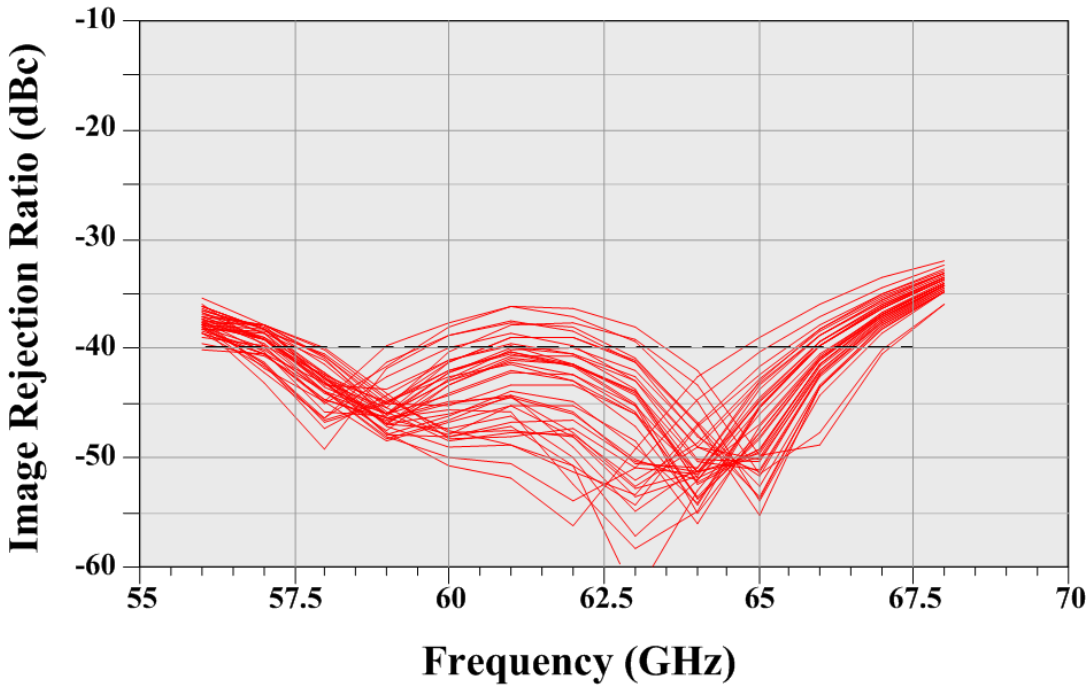


(a)

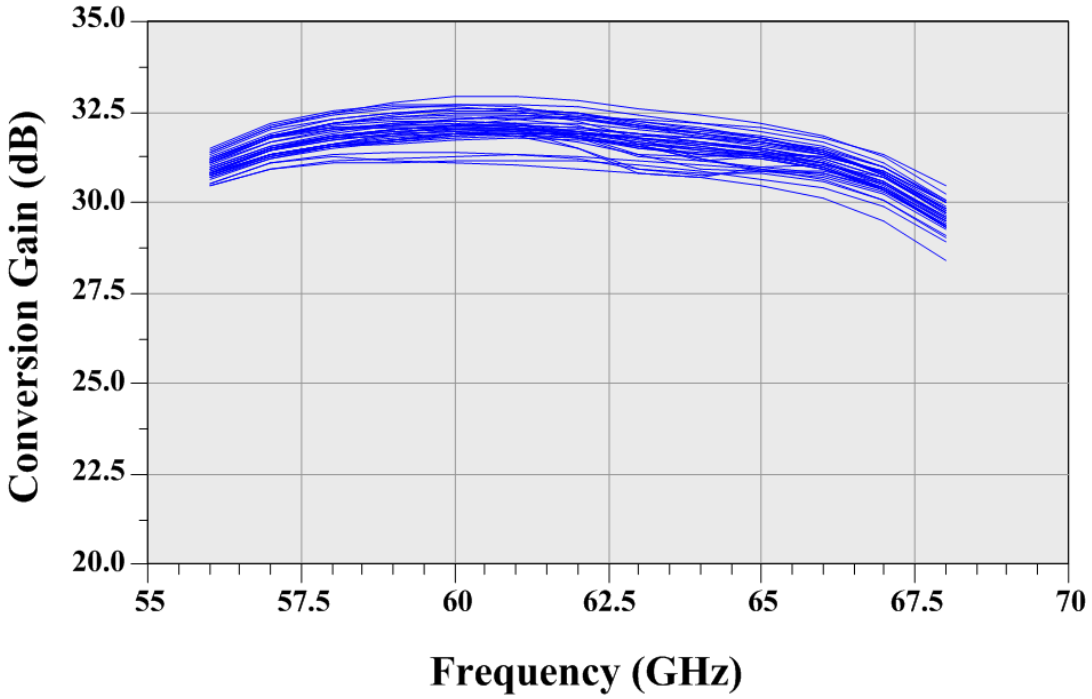


(b)

Fig. 4.3. (a) The image rejection ratio of the PVT corner simulations, and (b) The conversion gain of the PVT corner simulations of the 60-GHz transmitter.



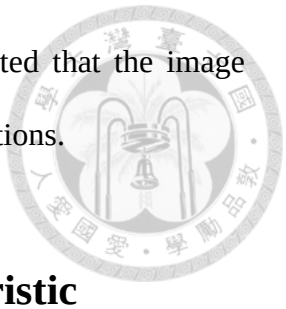
(a)



(b)

Fig. 4.4. (a) The image rejection ratio of the monte-carlo simulations, and (b) The conversion gain of the monte-carlo simulations of the 60-GHz transmitter.

variation, as shown in Fig. 4.3 and Fig. 4.4, respectively. It is noted that the image rejection ratio is not under -40-dBc for slow-slow (SS) corner simulations.



4.3 1024 QAM 60-GHz Transmitter Characteristic

The chip photo of the 60-GHz IQ transmitter is shown in Fig. 4.5, the die sizes is 1.26 mm × 0.82 mm. The MMICs are tested via on-wafer probing with a good repeatability.

The output spectrum of the transmitter is observed by a spectrum analyzer (Agilent E4448A) with a 20-dB attenuator. Fig. 4.6 shows the measured output spectrum of the 60 GHz transmitter with RF frequency of 66 GHz, LO frequency of 38.5 GHz, and baseband frequency of 1.25 MHz, where the LSB is the desired signal and the USB is the image signal. The measured output power of the desired signal is -22.2 dBm with the optimal 0-dBm LO drive power and baseband input of -24 dBm. The output spectrum is including -32 dB loss from the probe, cable and attenuator. The MMIC shows the superior 49-dBc measured image rejection ratio and the 41-dBc 2LO power suppression, referring to the desired output power. Fig. 4.7 shows the measured and simulated conversion gain versus LO power of the 66-GHz.

Fig. 4.8 shows the measured results of two chips. Based on the measurement results, the transmitter exhibits good repeatability. The measured and simulated conversion gain and image rejection of the 60-GHz direct-conversion transmitter from 52 to 73 GHz is shown in Fig. 4.9. The measured conversion gain is 33 ± 0.5 dB from 54 GHz to 70 GHz with 0-dBm LO drive power and total dc power consumption of 114 mW at 1.2 V supply. An image rejection of more than 40 dB is achieved over 63 to 69 GHz.

Fig. 4.10 shows the measured and simulated IF input power versus conversion gain and RF output power of 60-GHz transmitter at 60 GHz with a 0 dBm 30 GHz LO drive

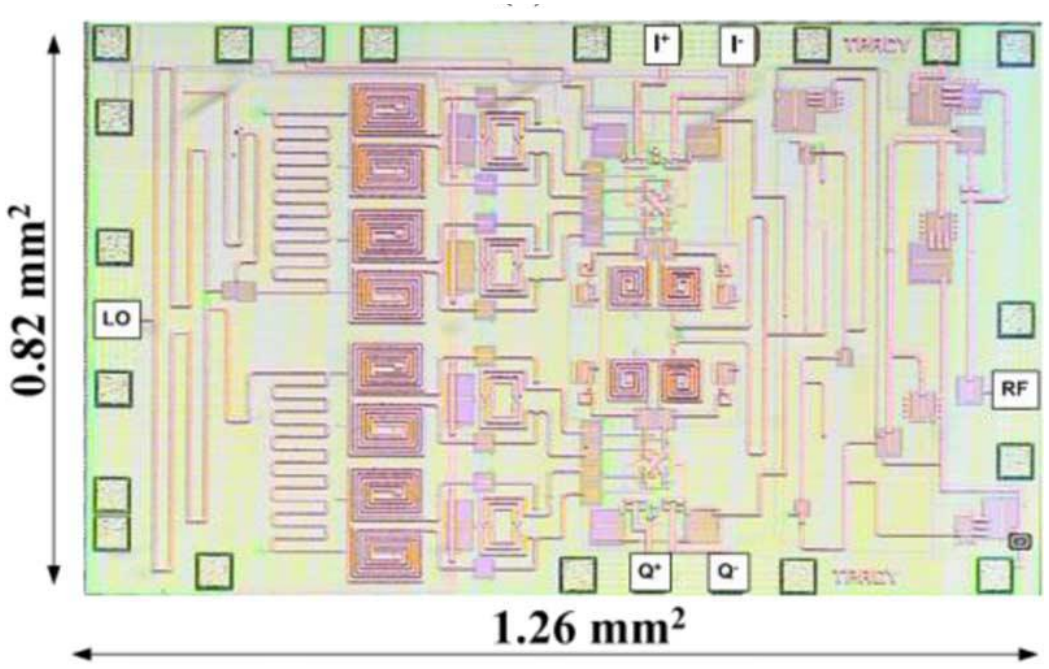


Fig. 4.5. Die photo of 60-GHz transmitter.

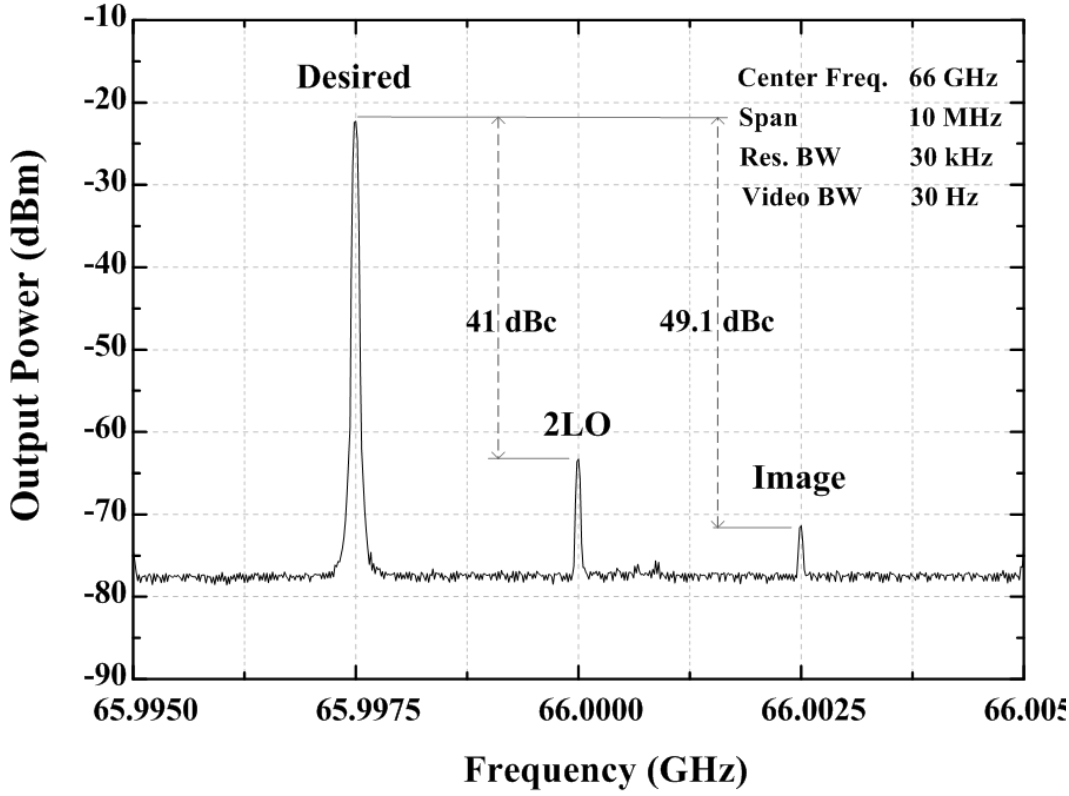


Fig. 4.6. Modulated output spectrum of the 60-GHz transmitter with an 2LO frequency of 66 GHz and an IF frequency of 1.25 MHz.

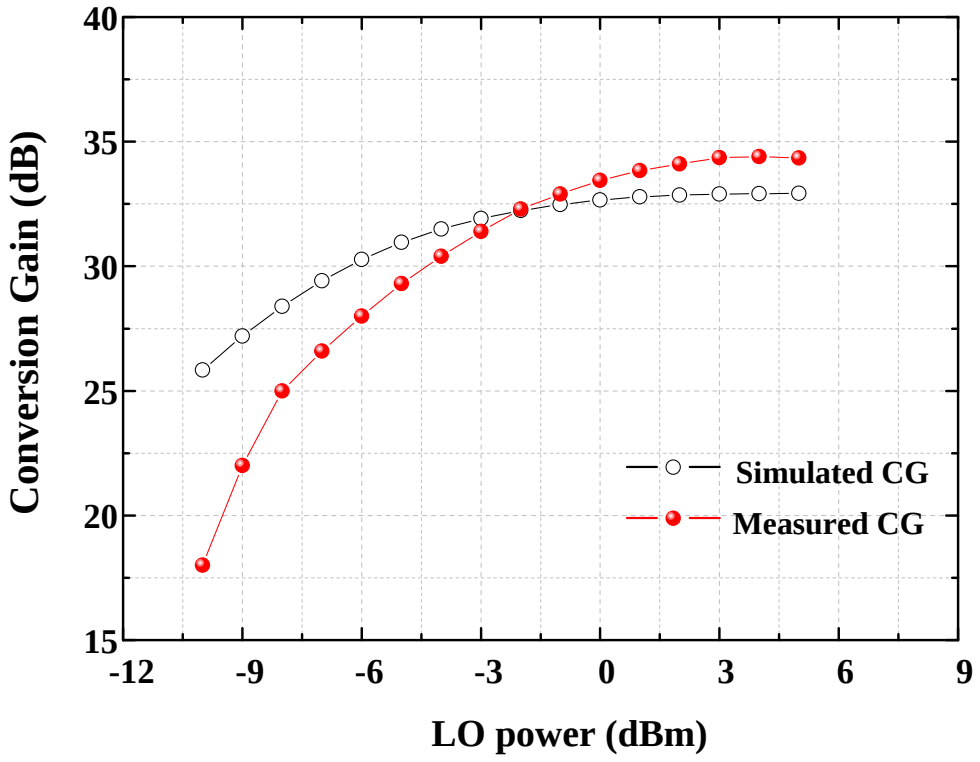


Fig. 4.7 . Measured and simulated conversion gain versus LO power of the 66-GHz.

power fixed IF frequency of 1.25 MHz. The measured output 1-dB compression point is 8.3 dBm and the saturated power is 11 dBm.

Fig. 4.11 is the measured and simulated conversion gain versus the baseband frequency from 5 MHz to 9 GHz with an LO frequency of 30 GHz. The transmitter features a 1-dB flatness modulation bandwidth above 1.5 GHz. In addition, the transmitter is evaluated with 1- and 2-Gb/s data rates in a pseudorandom bit stream (PRBS) from an Agilent pattern generator (N4901B series BERT). The measured output spectrum of the BPSK at 60 GHz is plotted in Fig. 4.12.

To verify the high data rate digital modulation quality of the MMICs, the setup block diagram of the vector signal measurement system is shown in Fig. 4.13. The baseband IQ sources are generated using arbitrary waveform generator (Tektronix AWG7122C). Due to the 40 MHz bandwidth digitizer measurement limit of the SA, the Quinstar

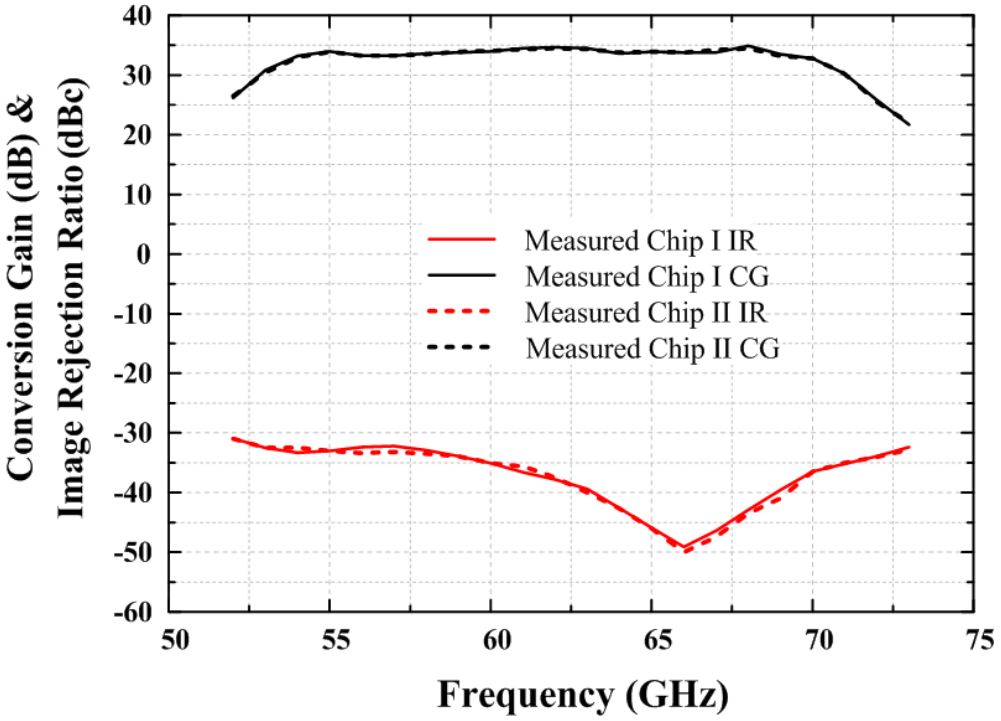


Fig. 4.8. The measured conversion gain and image rejection of two 60-GHz transmitter chips.

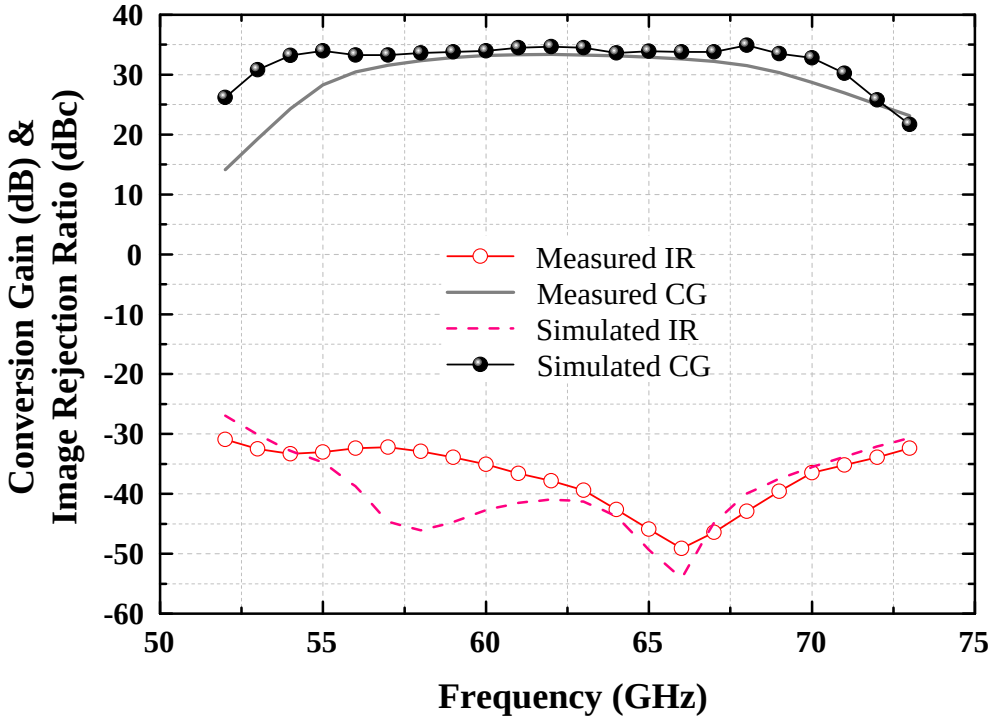


Fig. 4.9. Measured and simulated conversion gain and image rejection of 60-GHz transmitter from 52 to 73 GHz.

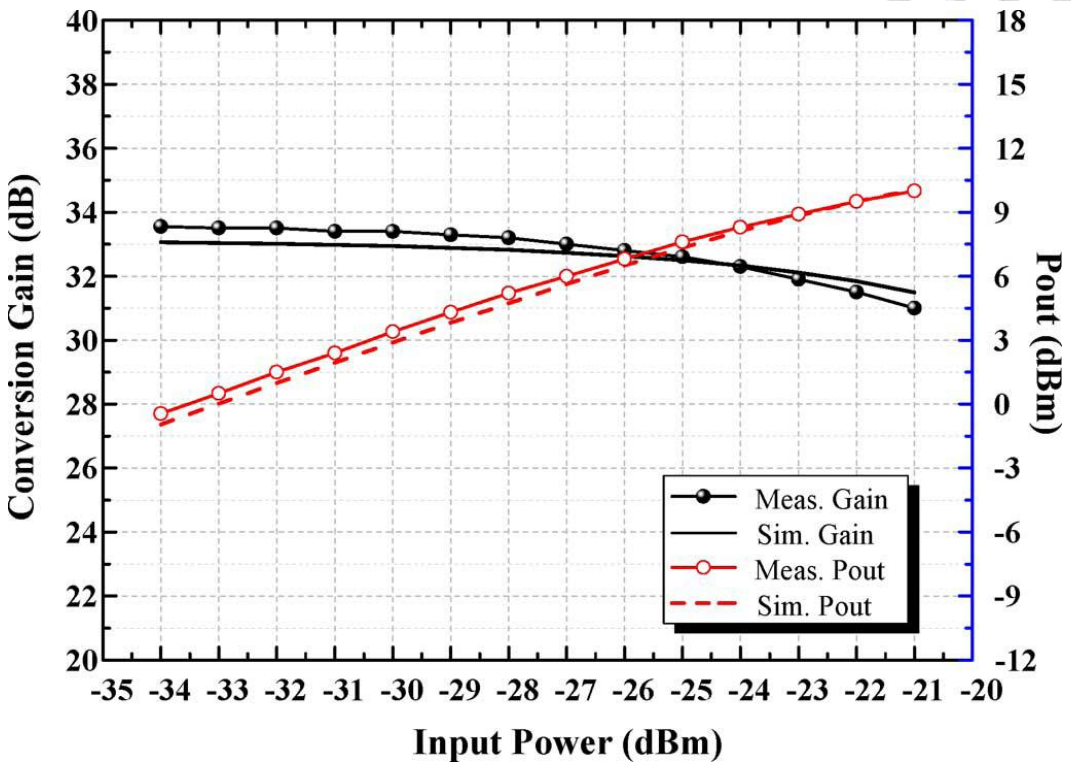


Fig. 4.10. Measured and simulated IF input power versus conversion gain and RF output power of 60-GHz transmitter at 60 GHz.

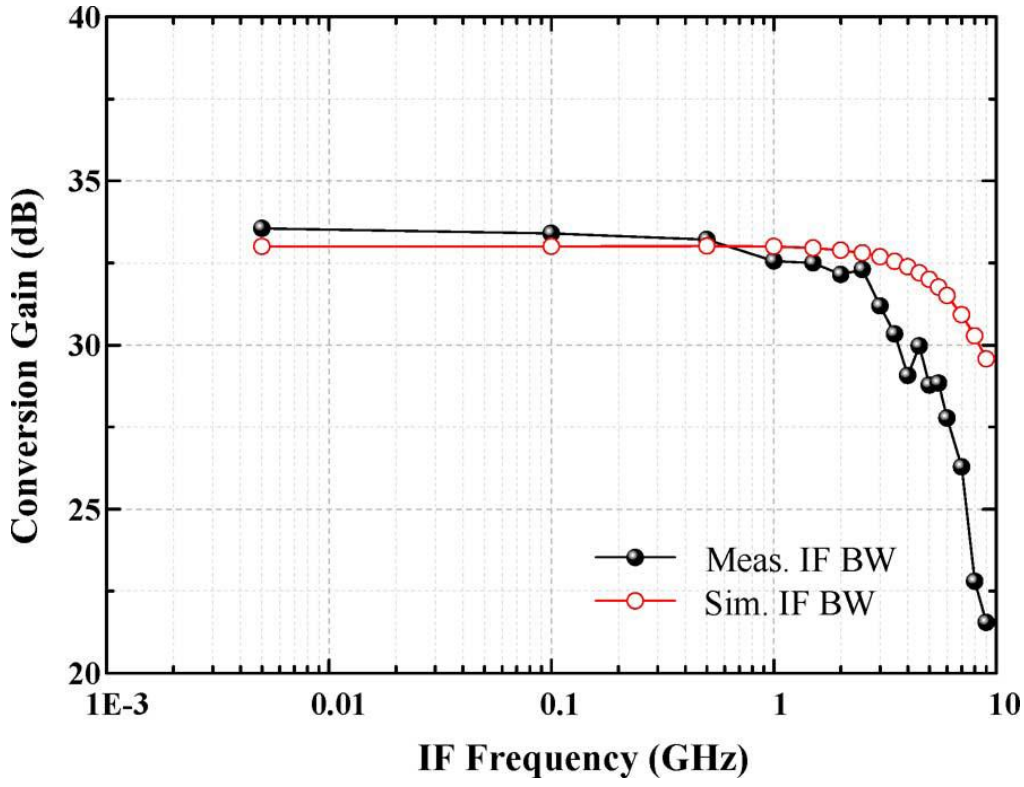
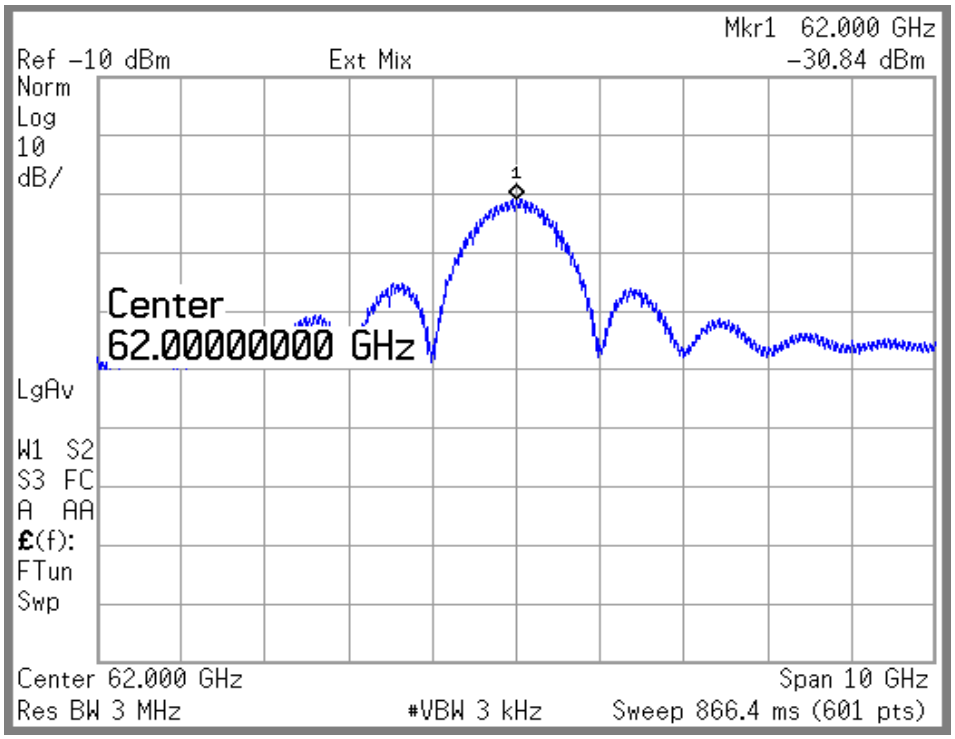
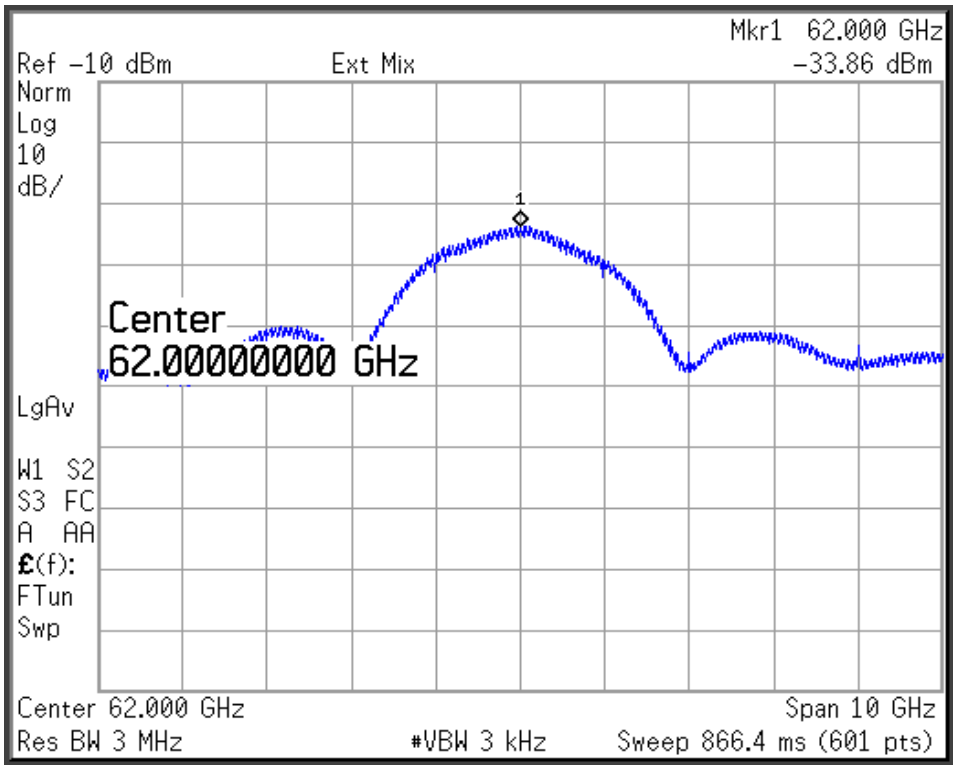


Fig. 4.11. Measured and simulated IF bandwidth of 60-GHz transmitter.



(a)



(b)

Fig. 4.12. Measured output spectrum of the BPSK modulator at 60 GHz with (a) 1- and (b) 2.-Gb/s data rates in PRBS.

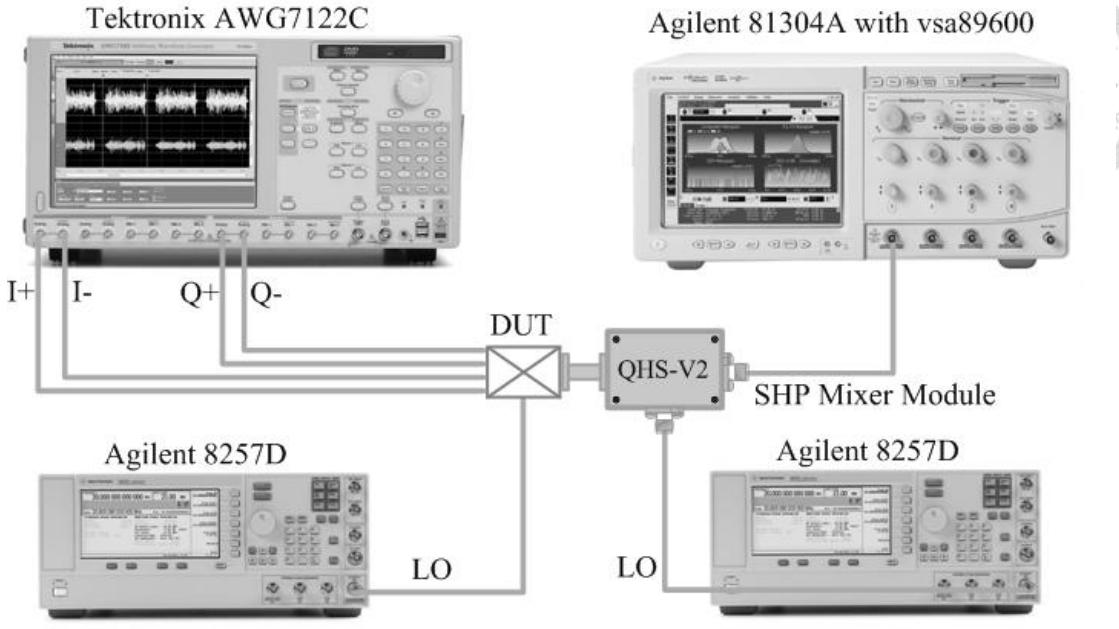
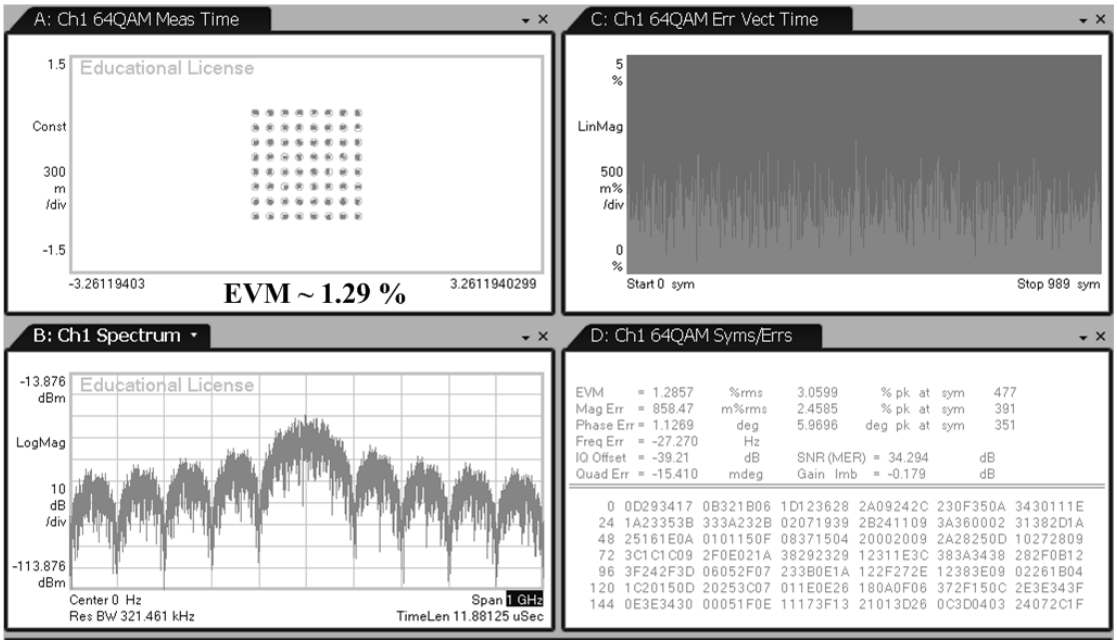


Fig. 4.13. Block diagram of the vector signal measurement system for the 60-GHz transmitter.

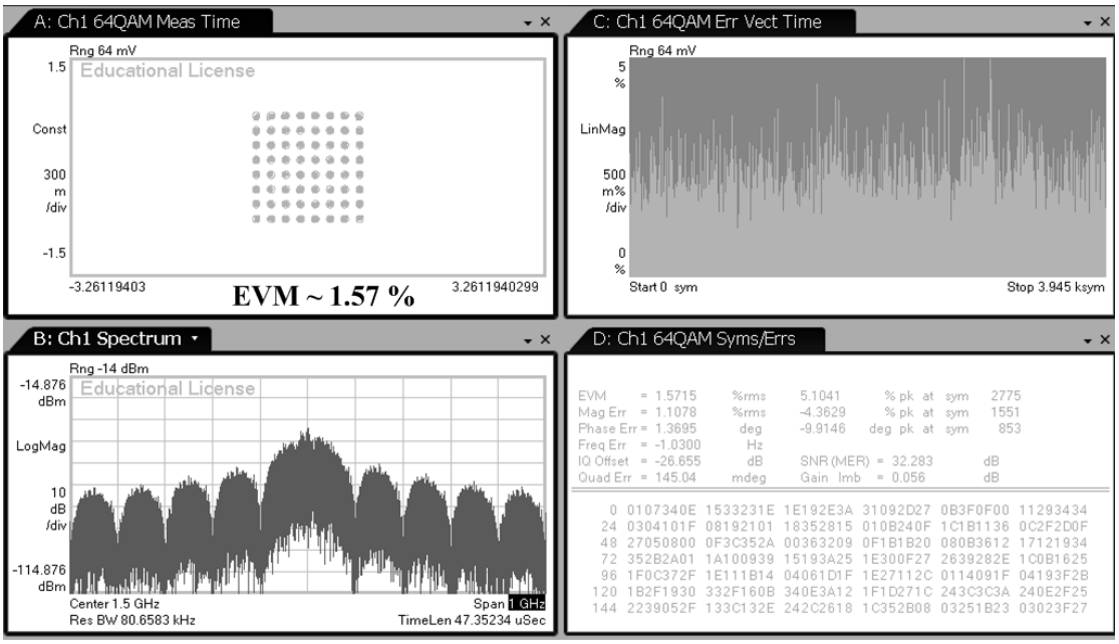
sub-harmonic mixer module (QHS-V2) is used to down-convert the high speed modulated signal to IF signal. The mixer module can provide -10±2 dB conversion gain with 9.5-dBm optimum LO driven power from 51-70 GHz and over 5-GHz IF bandwidth. The IF signal is fed into an oscilloscope for the analysis in the high data rate digital modulation.

The LO source of the module and DUT are provided by the two signal generators (Agilent E8257C). Fig. 4.14 (a) shows that the instrument provides the 1.29% EVM with 600 Mb/s 64-QAM modulated signal. Through the DUT, the measured constellation and output spectrums diagram is shown in Fig. 4.14 (b). A 64-QAM modulation with a data rate of 600 Mb/s with the 1.57% EVM is measured with the 6-dB back-off output power from 1-dB compression point.

It is noted that we did not apply any IF gain/phase calibration while measuring image rejection ratio, we neglect that the mismatch of the quadrature IF signal source of the

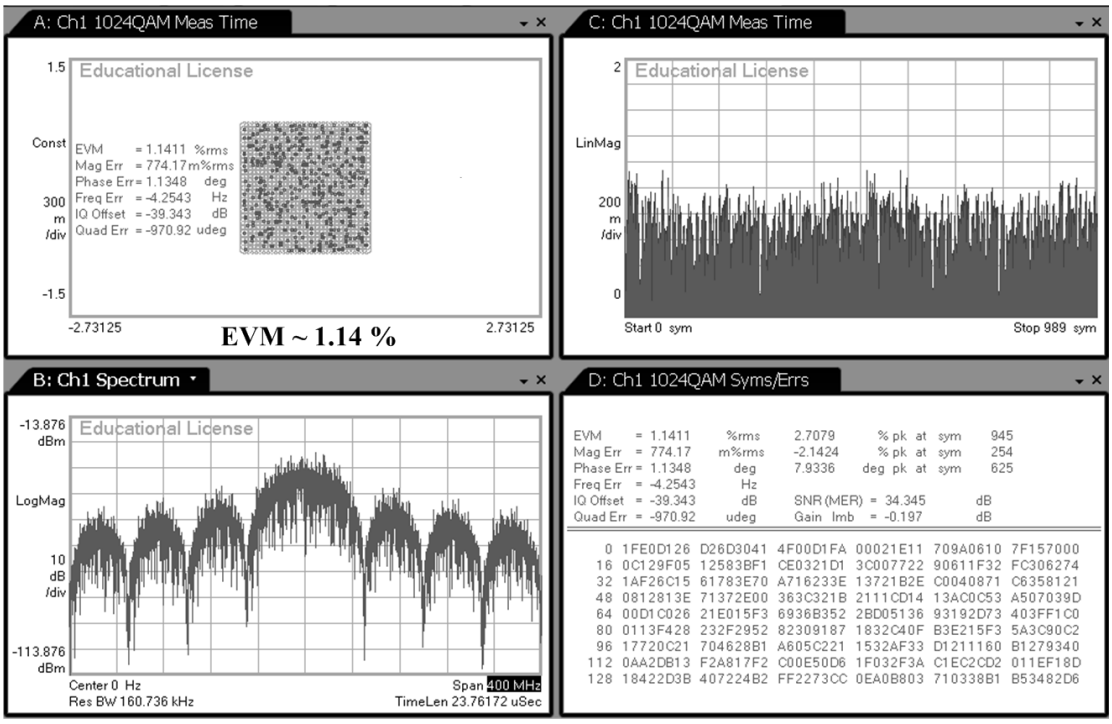


(a)

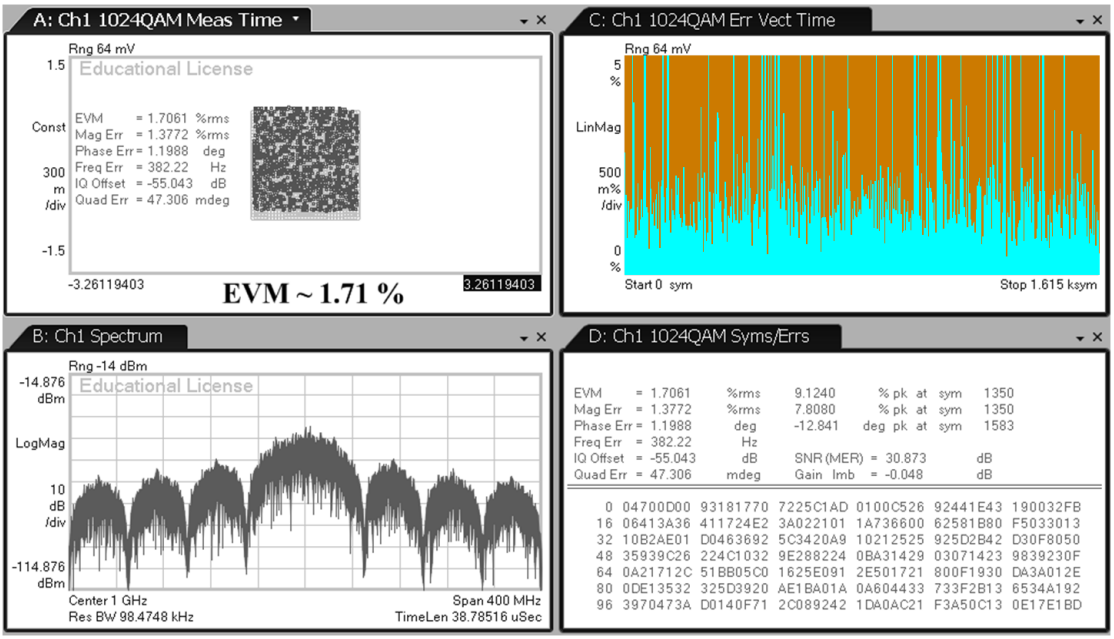


(b)

Fig. 4.14. Measured constellation and output spectrums diagram of (a) instrument (1.29% EVM) (b) the 60-GHz transmitter (1.57% EVM) at 65 GHz with a 600 Mb/s 64-QAM modulation.



(a)



(b)

Fig. 4.15. Measured constellation and output spectrums diagram of (a) instrument (b) the 60-GHz transmitter at 65 GHz with a 500 Mb/s 1024-QAM modulation.

	DVB-C		DVB-C2	
	64	256	1024	4096
In-home network				
Splitter (dB)	3		3	
Coaxial cable (dB)	4		4	
Receiver				
Thermal floor (dBμV)	4		4	
Required SNR for error-free transmission (dB)	26	32	29	35
Implementation loss (dB)	11		11	12
Minimum Signal Level @ system outlet (dBμV)	**48**	**54**	**51**	**58**

Fig. 4.16. DVB-C2 signal level requirement

test instrument arbitrary waveform generator and the other setup mismatch including non-identical cables, connecters and probes. As the symbol rate of instrument get faster, it is more difficult to provide perfect quadrature IF signal source accurately. As mentioned previously, the 1024-QAM systems place more strict requirements than the 64-QAM modulations. In this work, the LO source was provided by high performance signal generator and the linearity requirement was reduced through power back-off. The characteristics of the high image rejection and the good LO signal suppression of our proposed transmitter is considered to minimize the IQ mismatch and other imperfections.

To further test the limits of the system, the transmitted 1024-QAM constellations measured by instrument and our MMIC are shown in Fig. 4.15. The instrument provides the 1.14% EVM with 500 Mb/s 1024-QAM modulated signal, as shown in Fig. 4.15 (a). The EVM is less than 64-QAM modulation with a data rate of 600 Mb/s, but the constellation is not stable. Fig. 4.15 (b) shows the measured spectrum and constellation of the 60-GHz transmitter with 65 GHz RF output signal with the 10-dB back-off output

power from 1-dB compression point. A 1024-QAM modulation with a data rate of 500 Mb/s with the 1.71% EVM is demonstrated. The highest symbol rate that our transmitter can be measured is limited by 50 MS/s. It may be affected by signal source accurately.

Consulting the specification of DVB-C2 for our reference, the required SNR of 1024QAM for error free transmission in DVB-C2 signal level is 29dB, as shown in Fig. 4.16. As for 4096 QAM modulation, the required SNR is 35 dB (1.78 %EVM). Consequently, the transmitter may be considered a good candidate for a cost-effective way to further improve the capacity in high-speed application at 60 GHz band. The performance of our work with previously published MMW high image rejection modulators are summarized in Table 4-1.

TABLE 4-1
PERFORMANCES COMPARISONS OF THE REPORTED MMW HIGH IMAGE MODULATORS

Reference	[18]	[19]	[29]	[61]	[62]	This Work
Technology	0.18μm SiGe BiCMOS	0.15μm GaAs pHEMT	0.15μm GaAs pHEMT	0.13 μm CMOS	0.5μm E/D pHEMT	65nm CMOS
RF Freqency (GHz)	70–100	51–65	57–65	20-40	30–70	60–71
Conversion Gain (dB)	N/A	-14±2	18.3***	> -13	-7 ~ -13	33 ± 0.5
Image Rejection Ratio (dBc)	< -40	< -40	-49.3 @ 61GHz	< -40 @ 27-30 GHz	< -33	< -36
Modulation Scheme	256 QAM	64 QAM	N/A	64 QAM	64 QAM	1024 QAM
Data Rate (Mb/s)	5 Ms/s	7.2 Gb/s	N/A	6 Mb/s	6 Mb/s	500 Mb/s
EVM (%)	< 3	< 5	N/A	1.8	< 3	< 1.8
LO to RF port Isolation (dB)	N/A	> 40*	N/A	> 40	N/A	> 50*
LO power (dBm)	N/A	-1.5	4.5	10	N/A	0
DC power (mW)	250	420**	278	0	0	114
Chip size (mm2)	1.7×2	3.2×1.4	3.4×1.8	0.65×0.58	1×1	0.82×1.26

*2LO to RF port Isolation, **with buffer amplifier and OPA, ***peak gain @ 62 GHz.

Chapter 5 Conclusion

This dissertation presents the research on MMW transmitter and key components of the MMW Gigabit communication systems. For high speed wireless communications, an *E*-band high image rejection sub-harmonic IQ modulator and a direct-conversion 60-GHz transmitter for high-order QAM signal is designed and implemented on standard 65-nm CMOS technology.

To maintain high image rejection ratio of the IQ modulator over a wide bandwidth for high data rate application, a load insensitive analysis and an LO broadband 45° power splitter are proposed to achieve low amplitude and phase imbalanced structure. The design of the wideband low amplitude/phase imbalance 45° power splitter using an HPF/LPF structure to create 45° equal group delay with an additional delay line to compensate the amplitude imbalance is also described is this paper. In addition, the doubly balanced sub-harmonic Gilbert-cell mixer with the advantages of good LO leakage suppression has been selected in the mixer design. The IQ modulator demonstrates a measured flat conversion gain of 0 ± 1 dB from 55 to 85 GHz. The image rejection ratio is better than 40 dBc from 64 to 84 GHz.

For MMW high speed wireless communications, the proposed IQ modulator is integrated with the high efficiency PA and buffer amplifier to form a direct-conversion transmitter. By applying direct-combining topology, the two-stage PA achieves a flat Psat 12.6±0.3 dBm and high PAE above 22% from 57 to 66 GHz. The PA demonstrates the highest PAE 23.4% among these reported 60-GHz bulk CMOS PAs. The 60-GHz direct-conversion transmitter with 0-dBm LO drive power provides conversion gain of 33 ±0.5 dB from 54 to 70 GHz. The saturated power is 11 dBm with total dc power consumption of 114 mW through 1.2 V supply voltage. Via high image rejection and

good LO suppression of the modulator, a 1024-QAM modulated signal with a data rate of 500 Mb/s and 1.7% EVM is successfully demonstrated at 65GHz.

Besides, a low-voltage and low-power LNA for 60 GHz WPAN system applications using 90-nm CMOS technology is also presented. By employing three-stage common source configuration and forward-body-biased NMOS transistors, the fully integrated LNA can operate under the condition of a low supply voltage of 0.6 V, and 4.8 mW dc power consumption. The MMIC exhibits 16.5 dB power gain from 55-61 GHz and 6.5 dB average noise figure at operation frequency with good input and output matching. The experimental results show that the proposed MMW LNA is suitable for low power and low voltage applications.

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