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應用於毫米波波段之砷化鎵低雜訊放大器之設計與毫米波發射器元件與系統構裝之研究

Design of GaAs Low Noise Amplifier at Millimeter Wave and Research on Millimeter Wave System Package and Key Components

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毫米波發射器元件與系統構裝之研究

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本論文係 李祐棠 君（R01942008）在國立臺灣大學電信工程學研究所完成之碩士學位論文，於民國 104 年 01 月 16 日承下列考試委員審查通過及口試及格，特此證明

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中文摘要

在這本論文中，展示一個 E-band 低雜訊放大器和一個 W-band 寬頻三倍頻器晶片的設計與量測成果，以及 60 GHz 發射器系統的整合與量測。

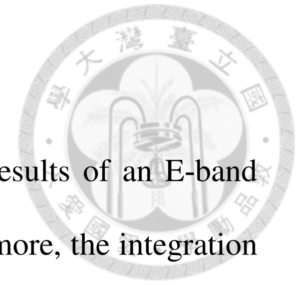
首先是預計應用在天文觀測 E-band 頻段接收機上，利用高速電子遷移率電晶體設計的低雜訊放大器，設計工作範圍為 60 至 77 GHz，設計過程中使用自建的小訊號模型進行模擬，模擬結果與量測結果相當符合，證實小訊號模型的準確性。

接著是預計作為 W-band 訊號源的寬頻三倍頻器，使用的製程為 65 奈米金氧半場效電晶體，此三倍頻器透過變壓器進行極間阻抗匹配，量測的結果與模擬也相當符合，最高的轉換增益可達到 1 dB，3 dB 頻寬輸出範圍為 57 至 78 GHz，達到 31 % 的比例頻寬。

最後則是 60 GHz 發射器系統的系統整合與量測，系統內電路使用 65 奈米金氧半場效電晶體製作，透過低溫共燒多層陶瓷(LTCC)組裝，與被動元件如天線、偏壓電路整合在一起；發射器的量測結果展示 28 dB 的小訊號增益，輸出飽和功率大於 7 dBm 和大於 3 dBm 的 1 dB 增益壓縮時的輸出功率(OP_{1dB})。

關鍵字：低雜訊放大器、高速電子遷移率電晶體、寬頻、三倍頻器、發射器、V 頻段、金氧半場效電晶體

ABSTRACT



In this thesis, we demonstrate the design and measurement results of an E-band low noise amplifier (LNA) and a W-band wideband tripler. Furthermore, the integration and measurements result of a 60 GHz transmitter system are also demonstrated.

First part is the low noise amplifier used in the application of radio astronomical telescope E-band receiver. The LNA is designed and fabricated in high electron mobility transistor using small-signal model. Targeted working range is 62 to 77 GHz. The measurement result and simulation result are in good agreement with each other, proving the accuracy of the model.

The next is a frequency tripler, which will be used as a W-band signal source, fabricated in 65-nm advanced CMOS technology. Transformer is used in this tripler to achieve impedance matching between stages. The measured performance fit well with simulation. Peak conversion gain of the tripler is larger than 1 dB, with 3 dB bandwidth from 57 to 78 GHz, which is 31 % of fractional bandwidth.

The last part is integration and measurement of a 60 GHz transmitter system. System circuits are fabricated in 65-nm CMOS technology. System is packaged in low temperature co-fired ceramic (LTCC), and integrated with passive components such as antennas and bias network. It shows small signal gain of 28 dB, saturation power larger than 7 dBm and output power at 1 dB compression over 3 dBm.

Index Terms – Low Noise Amplifier (LNA), HEMT, Broadband, Frequency Tripler, Transmitter, V-band, CMOS

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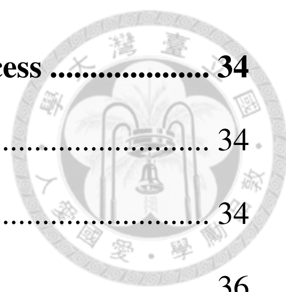

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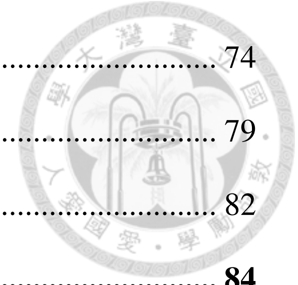

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Chapter 1 Introduction

1.1 Background and Motivation

In radio astronomical applications, receiver with high sensitivity is required. At E-band, which is relatively unexplored in the past in radio astronomy, the receivers are traditionally built by using superconducting mixers or hybrid amplifiers as the core components. However, SIS mixer usually has narrow instantaneous frequency (IF) bandwidth and small saturation power [1], whereas hybrid or MIC (microwave integrated circuit) amplifier is not suitable for mass-production at this frequency regime. For the next generation large array receivers like Atacama large millimeter/submillimeter array (ALMA) [2], MMIC-based receiver is an attractive alternative to SIS- and MIC-based receivers.

ALMA Band 2 covers the frequency range of 67 to 90 GHz [3]. Since the noise figure of the first LNA dominates the overall signal-to-noise ratio of the receiver, high performance LNA is required in radio astronomical receiver system with high sensitivity.

On the other hand, the demand on high data rate wireless communication grows rapidly in last decade. With low frequency band congested with mobile device like cell phone, researchers now look for higher frequency band to satisfy the demand of data transfer. At higher frequency, due to the parasitic effect and loss of the passive structure, the difficulty to implement an oscillator with low phase noise and high output power will also increase. It will be easier to cascade an oscillator with a frequency multiplier as

the high frequency source. Therefore, frequency multiplier becomes an important component in high frequency wireless communication systems.

Also, the IEEE 802.11ad standard utilized 57-64 GHz unlicensed industrial, scientific and medical (ISM) band [4] has been published for the demand of short-range communication capability. The millimeter circuits around this 9-GHz spectrum will become significant components. Owing to the advance in CMOS process, it is now possible to implement whole 60 GHz system-in-package (SIP) transceiver in CMOS process, lowering the cost and simplifying integration with digital circuits. The design techniques to overcome the weakness of CMOS process become an important challenge in the near future.

1.2 Literature Survey

1.2.1 LNAs around E-band and W-band

The previously LNAs published around E-band and W-band are listed in Table 1.1. Most LNAs are fabricated in HEMT devices due to their high gain and low noise characteristic over general silicon based devices. Well-known HEMT materials in research include InP [10], InAs/AlSb [13], and GaAs [15]. InP based HEMT device shows superior performance to the other process due to its high saturation velocity in the channel, but the high cost of mass-production is its main drawback. The InAs/AlSb device shows very low power consumption but available in experiment and research rather than commercial product. Though GaAs HEMT has lower saturation velocity in the channel compared with InP based HEMT device, and higher power consumption compared to

InAs/AlSb device, circuit using GaAs HEMT device is able to achieve comparable performance as the gate length shrink to 0.1 μm [15]. It is a mature MMIC process providing a balanced choice between circuit performance and fabrication cost.

Table 1.1. Published HEMT based LNAs in E-band and W-band.

Ref.	**Technology**	**BW (GHz)**	**BW (%)**	**Gain (dB)**	**P_{dc} (mW)**	**Noise Figure (dB)**	**Chip Area (mm^2)**	**FOM**
[10] 2009	NGST's 35-nm InP HEMT	70-92	27	26	16.8	3.1	2.1 × 0.8	500.4
[11] 2010	80-nm InP HEMT	68-110	42	18	12	3.5	0.55 × 0.75	178.3
[12] 2008	70-nm GaAs mHEMT	70-105	40	25	35	2.7*	2.8 × 1.8	366.8
[13] 2005	ABCS** 0.2-μm InAs/AlSb HEMT	85-102	18	18	6	3.9	1.75 × 0.7	122.9
[14] 2006	ABCS 0.2-μm InAs/AlSb HEMT	65-105	47	5.6	2	2.5	1.1 × 1.1	93.3
[15] 2012	0.1-μm GaAs mHEMT	60-90	40	19	56	2.5	3.5 × 1	54.7
[16] 2012	UMS 0.1-μm GaAs pHEMT	68-88	25.6	20	262	4.1	-	4.9

*: simulation result
**: ABCS: antimonide-based compound semiconductor

1.2.2 The W-band Tripler

Frequency multiplier is one of the basic components in millimeter wave application, and many literatures have published their multiplier designs in CMOS or HEMT process. Table 1.2 summarizes some published frequency multipliers with output around W-Band. In order to achieve high conversion gain and high output power, the multiplier usually need buffer to boost the performance. However this also increases the dc power consumption [26] [30] [31], otherwise it suffers from a low conversion gain and low saturation power [27] [28] [29]. Special type of multiplier uses injection lock mechanism to achieve high conversion gain and large output power, however the working range of this type multiplier is usually very narrow. [32]

Table 1.2. Published W-band frequency multipliers.

	Technology	Type	Output BW (3-dB BW)	CG/Reject (dB/dBc)	P_{sat}/P_{in} (dBm)	P_{dc} (mW)	V_d (V)	Size (mm^2)
[26] 2007	0.1-μm HEMT	X6	78-104 (28.6 %)	6/25	7/4	286	2	8
[27] 2010	0.15-μm mHEMT	X6	72-114 (45.2%)	>-17.9/40	-3.4/14.5	120	-	3.3
[28] 2012	0.18-μm SiGe BiCMOS	X3	80-100 (22 %)	-10.5/20	-10.5/0	75	2.5	-
[29] 2012	65-nm CMOS	X4	75-110 (-)	-24.3/30*	-14.3/10	16	1.5	0.342
[30] 2012	65-nm CMOS	X9	88-99.5 (12.2%)	-5.7/>31	8.5/13	438	2.4	0.45
[31] 2014	0.13-μm SiGe BiCMOS	X3	36-83 (79 %**)	0/10	-10/18	362	2.4	0.52
[32] 2014	65-nm CMOS	Injection Lock (X10)	77.8-78.9 (1.4%)	-/59(spur)	>8.8/-	265	1.8	0.53

*: Simulation Result.
**: Bandwidth of rejection larger than 10 dB.

1.2.3 V-band Transmitter System

There are many published full V-band (40-75 GHz) transmitter circuits chain, some of the most representative are surveyed and listed in Table 1.3. The [44] demonstrates a fully integrated phased-array transmitter with highest gain and highest output power by excellent performance of SiGe BiCMOS process, however it dissipates large dc power and great chip area. Ref. [45] fabricated in GaAs pHEMT process shows relative low gain and very large chip area.

Recently, silicon-based CMOS process has obtained many attentions with its low dc power consumption, compact layout and easily integration with baseband circuit [46]-[48]. Though electronic characteristic of silicon are inferior to other semiconductor materials, the rapidly progression in device geometry shrinkage compensates the disadvantage. Transmitter system using CMOS 65-nm process [48] exhibits a good performance comparable to [44], showing that advanced CMOS now has competitive performance to SiGe BiCMOS devices.

Table 1.3. Summary of the previously published V-band transmitter systems.

Ref	**[44]**	**[45]**	**[46]**	**[47]**	**[48]**
Topology	Super hetero-dyne	Direct conversion + LO multiplier	Direct con-version	heterodyne with sub-harmonic mixer	Super Het-erodyne
System Package	Integrated circuit	Integrated circuit	Integrated circuit	Integrated circuit	Integrated circuit
Process	0.12-µm SiGe BiCMOS	0.15-µm GaAs mHEMT	0.13-µm CMOS	90-nm CMOS	65-nm CMOS
Freq (GHz)	51-65	1.25-2.75 → 54-61	0.5 →57-65	0.1-20→57-62	53-62
Gain (dB)	35	5.2	-	13.1	20
LO Power (dBm)	-	-3	4	-	-
OP_{1dB} (dBm)	9-13.5	0	4	-1.3	6
P_{SAT} (dBm)	15	3.7±1.5	5±1.5	4.6	11
Image Rejection (dB)	-	-	-	-	25-28
LO Rejection (dB)	>20	-	>27	-	20
Area (mm^2)	6.5 × 6.75	5.7 × 5	8.4	1.2*	4.06
Power Con-sumption (mW)	3800-6400	820	-	113	590

*: including frequency synthesizer

1.3 Contributions

In this thesis, an LNA from 62 to 77 GHz in WIN 0.1-μm pHEMT process is designed and measured. To design the circuit, small-signal models on specific bias are first generated from measured devices results in our lab. The LNA measured results show consistency with simulation, indicating the accuracy of the models. This work exhibits an FOM of 180.9 (GHz/mW), which is highest compared to most published LNAs in this band. The measured performance is not wide enough but applicable in the ALMA project [2].

In the second part, a W-band tripler is designed. It utilizes transformers to achieve impedance matching and fundamental output suppression. Along with differential structure to eliminate even harmonic signal, no additional frequency filter needed in this tripler design. The tripler shows output ranges from 57 to 78 GHz with measured peak conversion gain of 1.3 dB in a compact chip size.

In the last part, a V-band heterodyne transmitter packaged on LTCC is measured. It demonstrates a full transmitter circuit chain from baseband to transmitting antenna, and also the potential ability of V-band system in package (SiP) in LTCC module. The transmitter is measured with conversion gain of 28 ± 1 dB, and saturation power and linear output power of 7 dBm and 3 dBm. Due to the image and harmonic terms generated by the up-conversion mixer and IQ mixer, the saturation power and linear output power of the transmitter do not agree with output power of the PA. However, the measurement proves the functionality of whole transmitter system integration.

1.4 Thesis Organization

The thesis organization is as follows.

In chapter 2, an E-band LNA in GaAs 0.1-μm low noise pHEMT process with high small signal gain is designed and measured. Step by step design procedures and model fitting are described in this chapter. Measurement results and simulation results are compared and discussed.

In chapter 3, a 57-78 GHz W-band tripler in 65-nm CMOS process is designed and measured. The detail design of transformer matching and full circuit is presented. The measurement result of this tripler is discussed and compared with other published frequency multipliers at W-band.

In chapter 4, a V-band super-heterodyne transmitter using 65-nm CMOS process is presented. The transmitter system is packaged with bias circuit and dual-polarization antenna in LTCC package. The chapter goes through brief introduction to each circuit component and the LTCC package design first. After that, the measurement results of transmitter are shown.

Conclusion of this thesis is given in chapter 5.

Chapter 2 Design of an E-band LNA in GaAs 0.1-μm Low Noise pHEMT process

The applications of E-band ranges from 60 to 90 GHz include high data rate point-to-point wireless communications [5], satellite communications, and astronomy observations.

In this chapter, we present an E-band MMIC low noise amplifier (LNA) using 0.1-μm GaAs pHEMT technology operating in 1 V and 2 V drain voltage. The E-band LNA shows small signal gain of 28 dB from 62 to 77 GHz with DC power consumption 44 mW. Noise measurement conducts in the package shows average noise figure about 4.5 dB from 75 to 90 GHz [6].

2.1 Circuit Design of the E-band LNA

2.1.1 Device Selection

The design goal is providing a LNA covering lower E-band from 60 to 75 GHz. Targeted gain is larger than 15 dB and noise figure as low as possible. Since the cryogenic operation might be needed, the dc power consumption is limited to 50 mW in order to minimize the impact of heat dissipation on cryogenic system.

The LNA is designed using 0.1-μm gate length GaAs based pHEMT devices provided by WIN technology. Fig. 2.1 shows the maximum gain and minimum noise of a 0.1-μm device and a 0.15-μm one. Device size and drain bias are both 2 × 25 μm and 4 V. Gate bias of 0.1-μm device and 0.15-μm device are -0.35 V and -0.02 V, respectively.

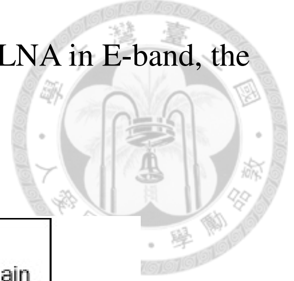
With drain current both 15.2 mA, 0.1-μm device provides 3 dB higher maximum gain, and lower noise figure at E-band.

There are two commonly used device configuration for amplifiers: common source (CS), and cascode. In this circuit, common source topology is chosen because of its simplicity in layout. Fig. 2.2 shows the dc-IV curves of the device with 2 finger and total gate width 50 μm (abbreviated as 2f50 in the rest of the thesis). It shows that transistor enters saturation region when drain voltage is higher than 1 V. To limit the power consumption, drain voltage is set to 1 V, rather than the normal bias 4 V. Drain current versus gate voltage is shown in Fig. 2.3. By setting gate voltage lower than -0.3 V, the drain current of each stage will not exceed 15 mA thus allowing at least three stages topology. Finally, the transconductance g_m, which directly affects the small-signal gain of the transistor, is swept by gate voltage in Fig. 2.4. Since the transconductance g_m shows little difference when V_d biases above 1 V, the low drain voltages save dc consumption without degrading the small signal gain.

In order to achieve the largest gain performance, gate voltage is chosen at -0.35 V with the highest g_m. However, in order to have good noise performance, gate voltage of the front stages is biased at 50 %-70 % I_{dsp} (current at peak g_m). Fig. 2.5 shows the maximum gain and minimum noise figure simulation of device size 2 × 25 μm under different gate bias. Biasing at peak transconductance shows maximum gain about 3 dB higher at E-band, but the noise figure is also higher. In order to have lower noise, the gate bias of first two stages is set to -0.6 V.

To decide device size, the maximum gain and minimum noise figure of the devices size 2 × 25 μm, 2 × 50 μm, 4 × 25 μm, and 4 × 50 μm biased at V_d = 1 V and V_g = -0.35 V are shown in Fig. 2.6. The maximum gain shows little difference from 60 to 75 GHz.

In order to minimize the noise figure and power consumption of the LNA in E-band, the devices size of 2×25 μm is chosen.



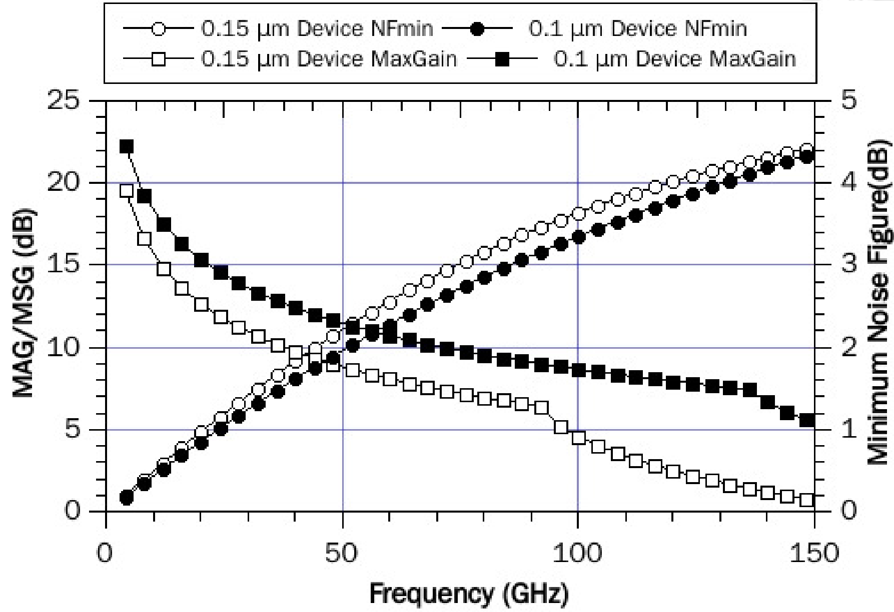


Fig. 2.1. Maximum gain and minimum noise figure of 0.1-μm device and 0.15-μm device under identical drain current.

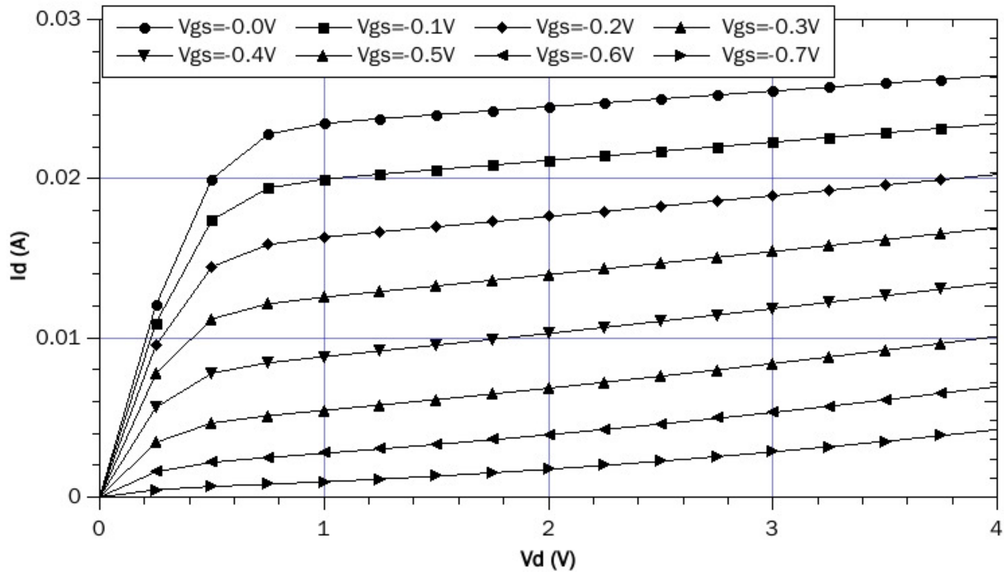


Fig. 2.2. The dc-IV curves of device size 2f50.

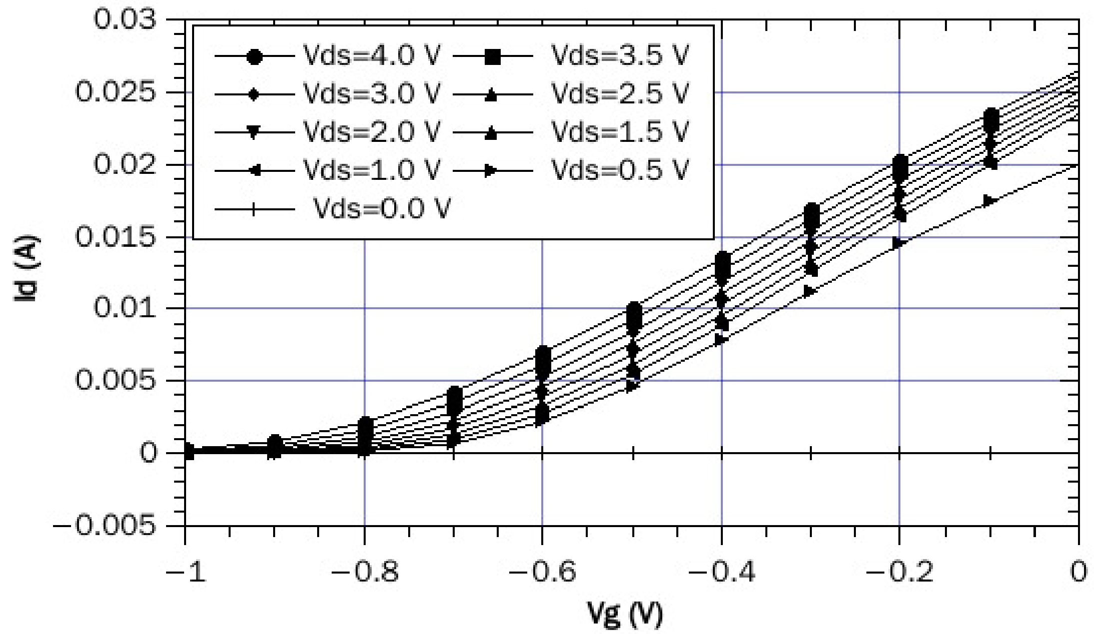


Fig. 2.3. Drain current versus V_g of device size 2f50.

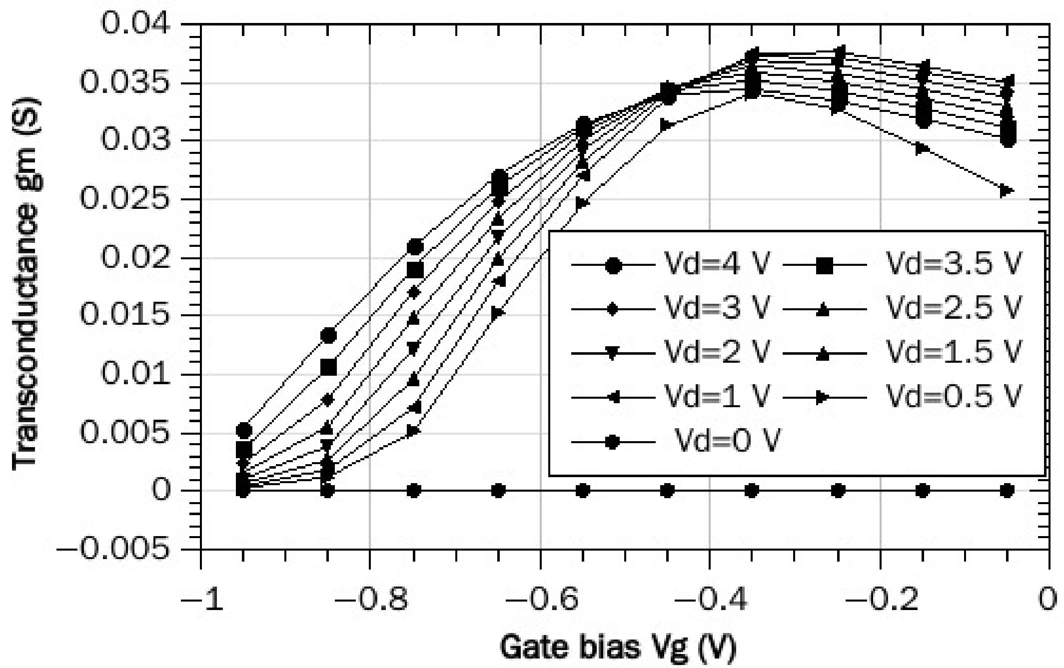


Fig. 2.4. Transconductance of the device size 2 × 25 μm under different drain bias.

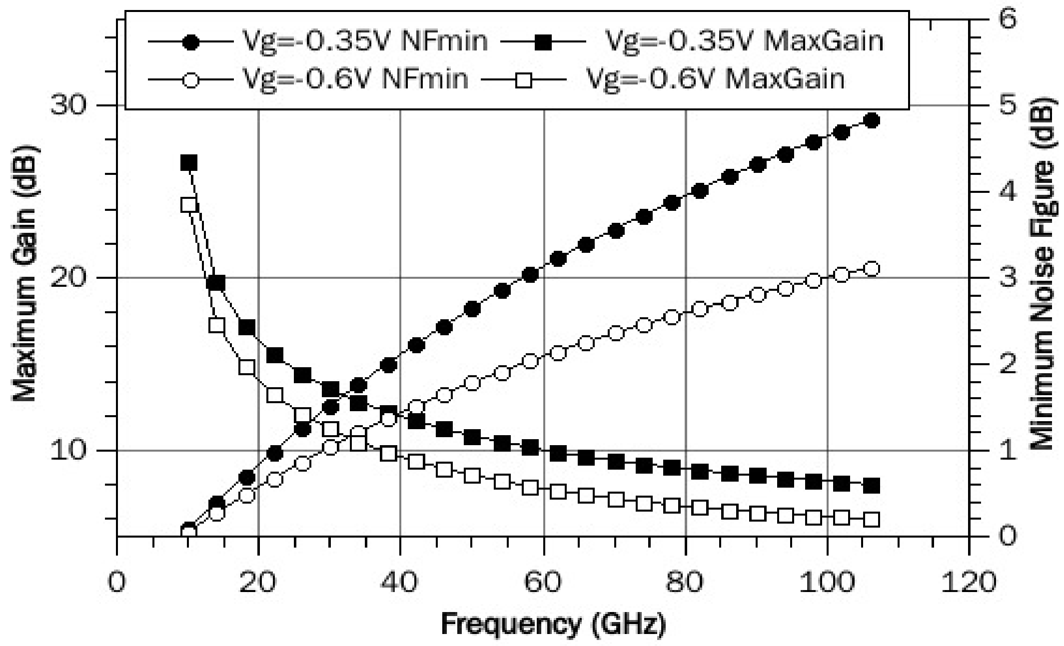


Fig. 2.5. Maximum gain and minimum noise figure of the device size 2 × 25 μm under different gate bias.

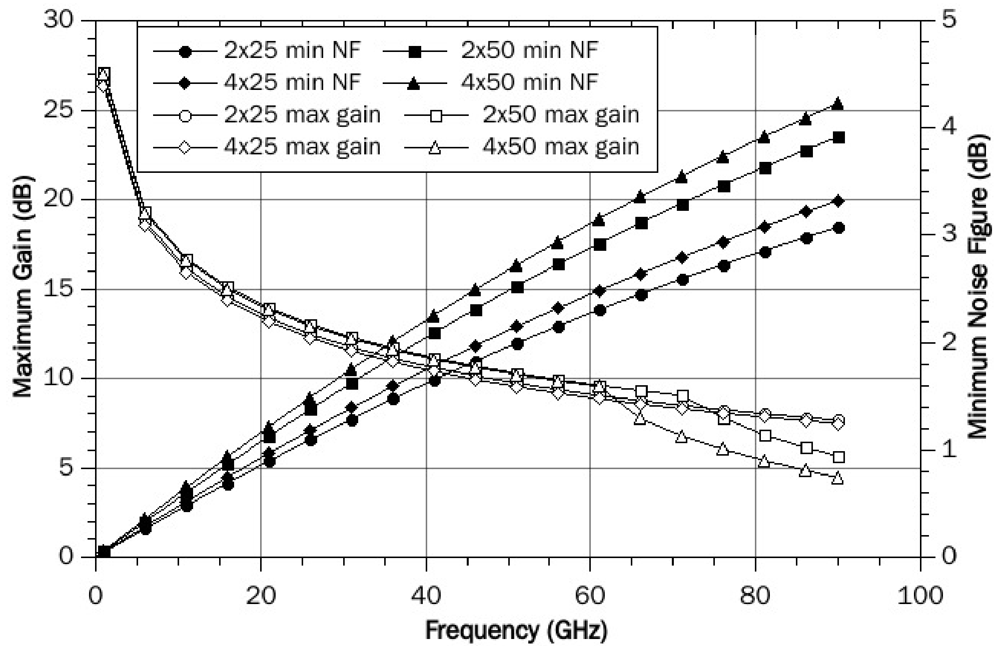


Fig. 2.6. The maximum gain and minimum noise figure of the devices size 2 × 25 μm, 2 × 50 μm, 4 × 25 μm, and 4 × 50 μm.

The gate bias of the 1st and 2nd stages is V_g = -0.6 V, generating less noise while providing enough small signal gain. The 3rd and 4th stages are biased at maximum g_m V_g= -0.35 V in order to boost up the gain. The bias voltage and current of each stage are summarized in Table 2.1. Drain bias of first two stages are set to 2 V due to stability issue.

Table 2.1. Drain bias and drain current of each stage

	Stage 1	**Stage 2**	**Stage 3**	**Stage 4**
V_d	2 V	2 V	1 V	1 V
I_d	4 mA	4 mA	14 mA	14 mA

2.1.2 Device Modeling

Because the device model of foundry does not cover drain bias at 1 V, device modeling of 1 V drain bias is fitted at the desired gate bias of -0.6 V and -0.35 V. For simplicity, only small signal model [7] is fitted, rather than complete non-linear model.

Fig. 2.7 shows the small-signal model of the transistor including extrinsic components and intrinsic components. By the small signal measurement result, the value of each component can be estimated initially. Each value is then tuned to fit *S*-parameters of model to the measurement result. The detailed step by step model parameter extraction can be found in [8].

Table 2.2 shows the parameter values of the small signal models, including gate bias at -0.6 V and -0.35 V. Fig. 2.8-2.9 show the comparisons of modeled and measured *S*-parameter and maximum gain from 1 to 110 GHz of 2f50 device with V_g of -0.6 V.

Except S_{12} shows larger difference, other parameters basically fit to measured results reasonably. The discontinuity of S_{22} at high frequency, which caused by measurement variance, is ignored. Fig. 2.10-2.11 show the comparisons of modeled and measured *S*-parameter and maximum gain from 1 to 110 GHz of 2f50 device with V_g of -0.35 V. Also, except larger difference of S_{12}, the modeled results agree with measurement results.

Noisy temperatures T_i and T_{ds} of the resistors R_i and R_{ds} are included in the noise model [9]. The measured noise performance of the 2f50 device is not available during this model work. The noise model is fit to foundry noise model and estimated by the 2f100 device measurement result. The fitting results of the NF_{min} of two different bias are shown in Fig. 2.12.

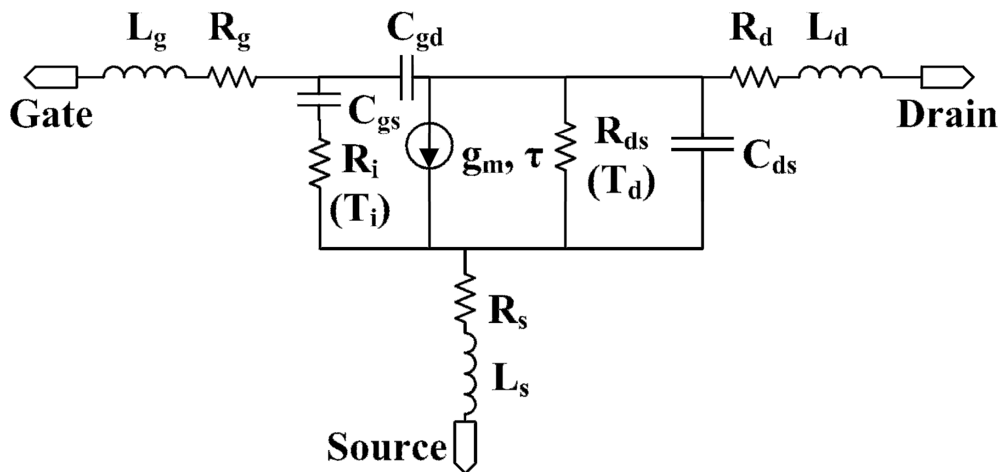
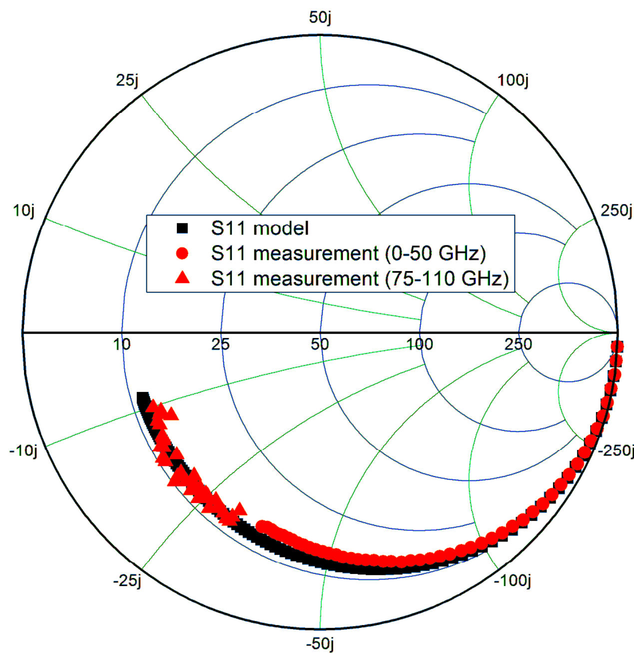


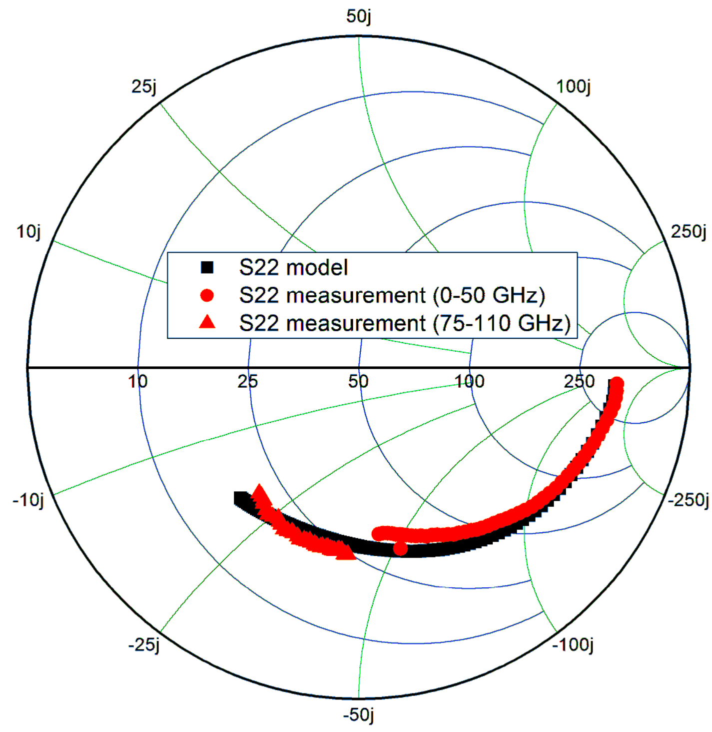
Fig. 2.7. The small signal model including extrinsic and intrinsic model.

Table 2.2. The parameters in small signal model of 2f50 device.

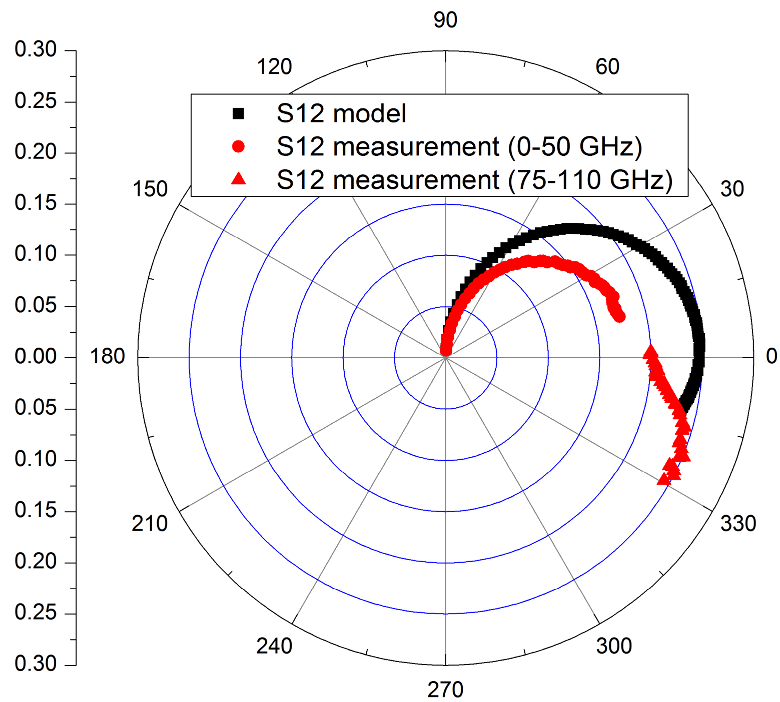
Parameter	V_g = -0.6 V	V_g = -0.35 V	Parameter	V_g = -0.6 V	V_g = -0.35 V
R_s (Ω)	2.94	2.94	g_m (mS)	38	44.4
R_g (Ω)	1.28	1.28	τ (pSec)	0.184	0.184
R_d (Ω)	2	2	R_{ds} (Ω)	335.22	289.82
L_s (pH)	1.82	1.82	R_i (Ω)	6	6
L_g (pH)	0	0	T_d (℃)	2487	10000
L_d (pH)	0	0	T_i (℃)	925	925
C_{gs} (fF)	39.1	34.6			
C_{gd} (fF)	15.9	12.9			
C_{ds} (fF)	18.6	18.6			



(a)



(b)



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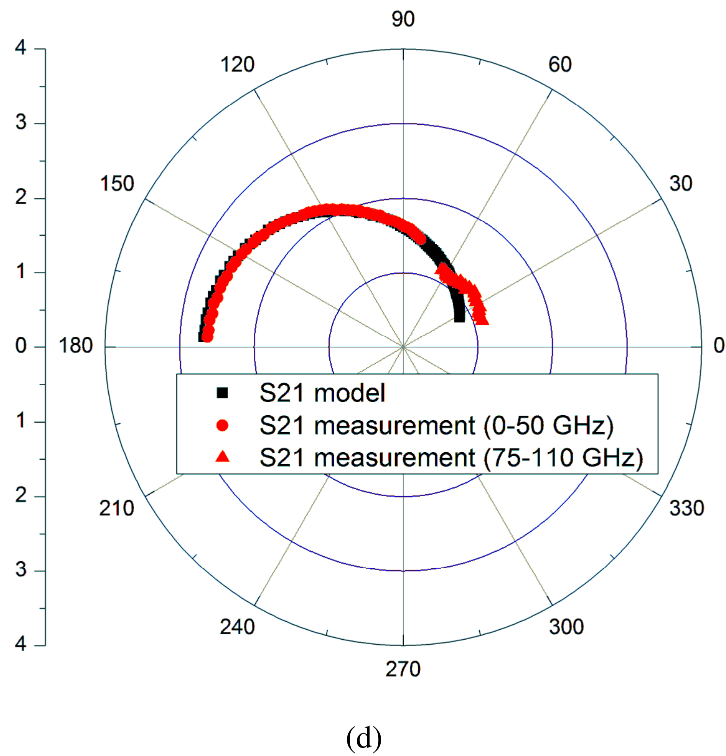


(d)

Fig. 2.8. The S-parameters from 1 to 110 GHz, (a) S_{11}, (b) S_{22}, (c) S_{12}, (d) S_{21} of 2f50 device with V_d of 1 V and V_g of -0.6 V.

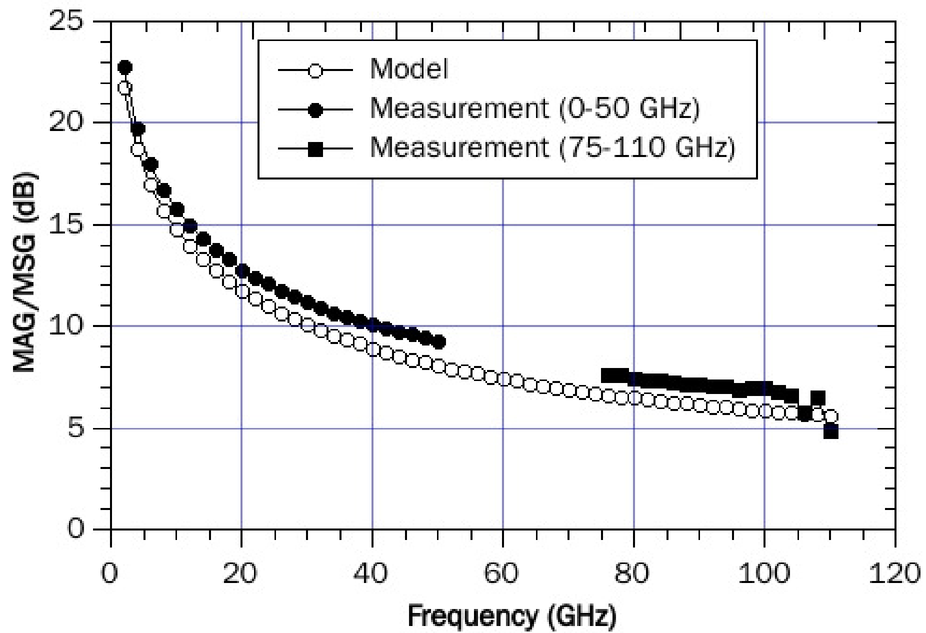
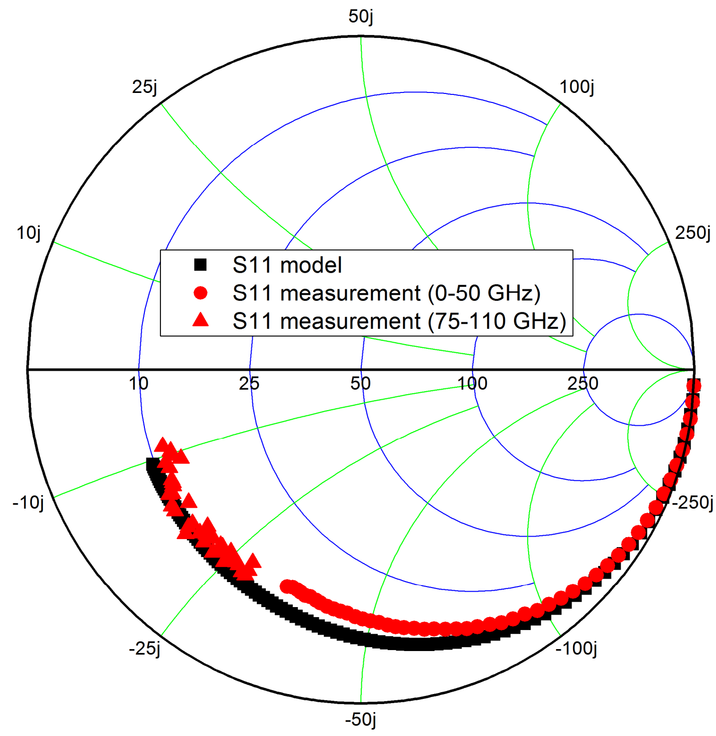
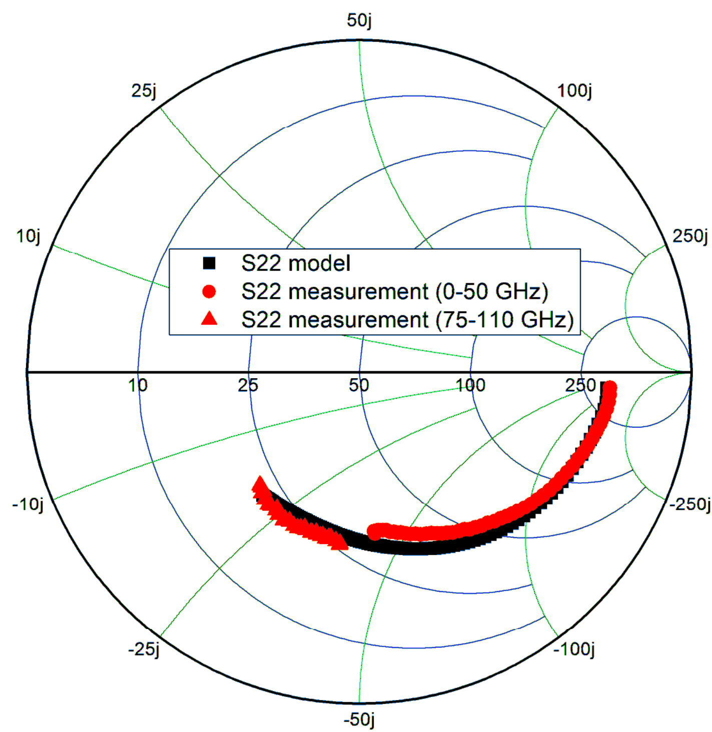


Fig. 2.9. The maximum gain of 2f50 device with V_d of 1 V and V_g of -0.6 V.



(a)



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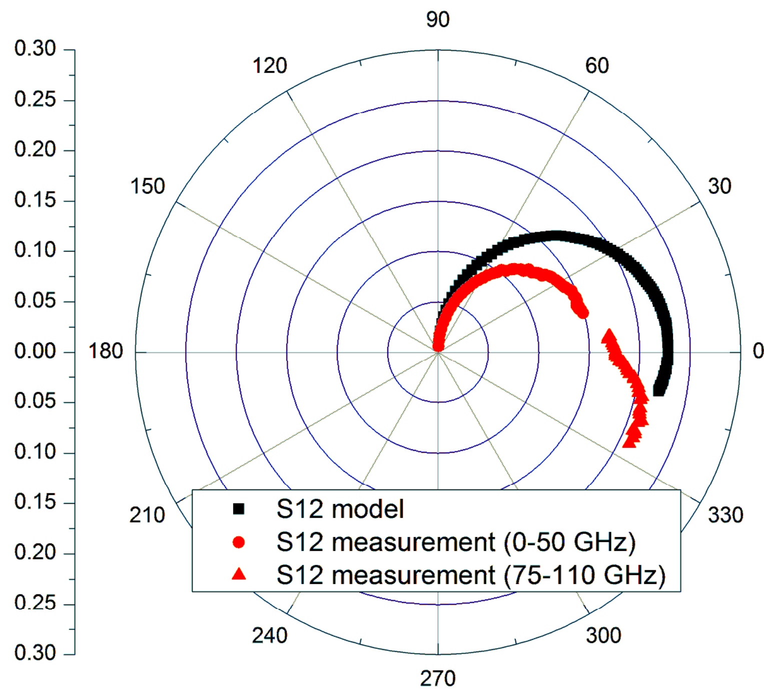

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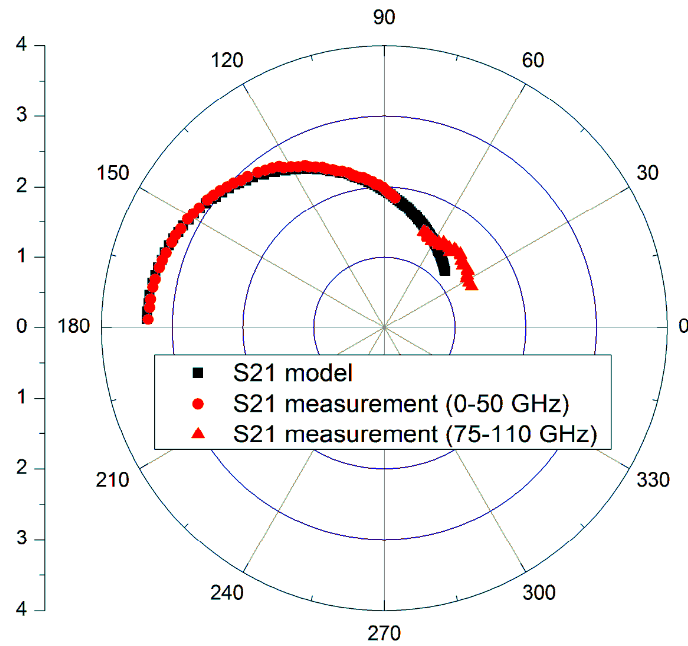


(d)

Fig. 2.10. The *S*-parameters from 1 to 110 GHz, (a) S_{11}, (b) S_{22}, (c) S_{12}, (d) S_{21} of 2f50 device with V_d of 1 V and V_g of -0.35 V.

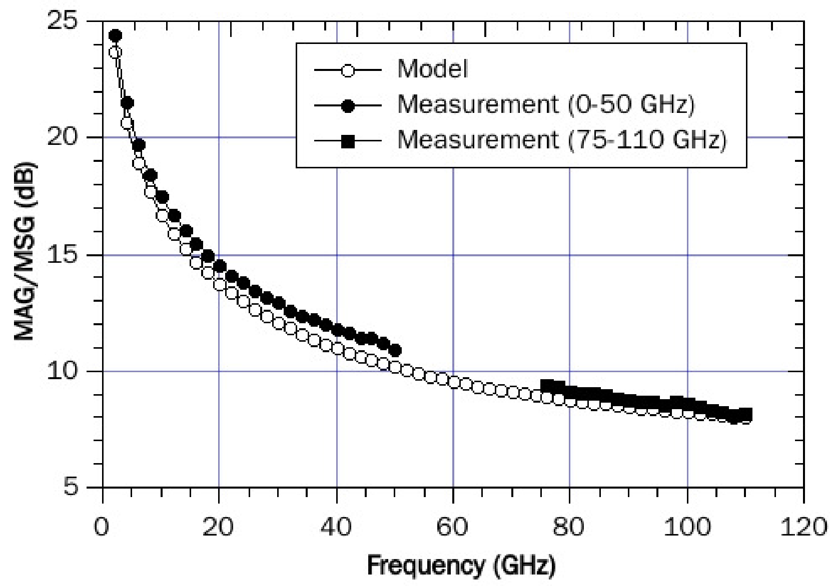


Fig. 2.11. The maximum gain of 2f50 device with V_d of 1 V and V_g of -0.35 V.

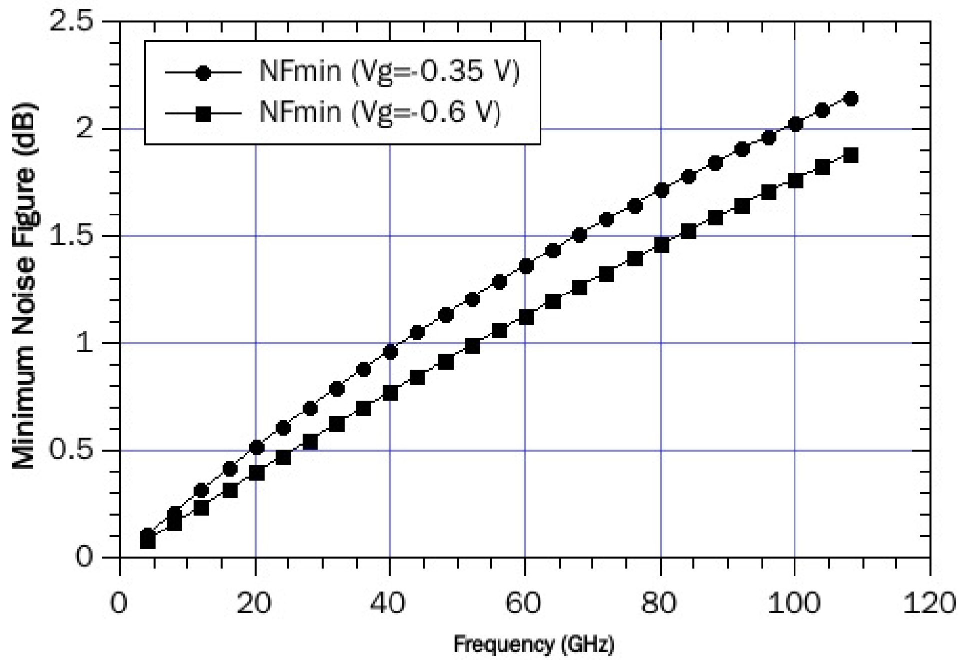
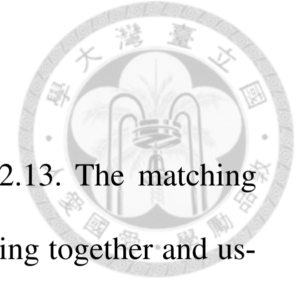


Fig. 2.12. The NF_{min} of 2f50 device model when V_d is 1 V and V_g are -0.35 V and -0.6 V, respectively.

2.1.3 Circuit Design



The overall schematic of the E-band LNA is shown in Fig. 2.13. The matching networks are realized by using microstrip line with M1-M2 connecting together and using backside metal as reference ground. Source of the transistors are directly short to ground through back side via. In the 50 μm substrate of this process, back side via shows about 6 pH inductances acted as source degeneration inductances. Along with the loss of the matching network, the circuits can be stabilized without other special techniques.

Gate voltage is fed through a large resistor because of low current at gate bias. A short stub is included into the matching network to feed the drain current. The dc blockings implemented by metal-insulator-metal (MIM) capacitor are also considered.

On-chip bypass provides a good RF short at the end of short stubs. The basic schematic of the bypass circuit is shown in Fig. 2.14. The bypass is composed of a 0.19 pF capacitor as in-band bypass. Out-band bypass is provided by a 0.4 pF and a 1.5 pF capacitors with 10 Ω resistors to ground. Top view of structure of EM simulation is shown in Fig. 2.15. Larger capacitor with size 100 μm × 100 μm is added if layout space is allowed. The simulated reflection coefficient of the bypass circuit is shown in Fig. 2.16. The reflection coefficient close to RF short near 60 to 80 GHz. Also, the S_{21} is shown in Fig. 2.17, it provides an RF short circuit starting from 20 GHz. The simulation results of S-parameters are shown in Fig. 2.18, and the noise figure is shown in Fig. 2.19.

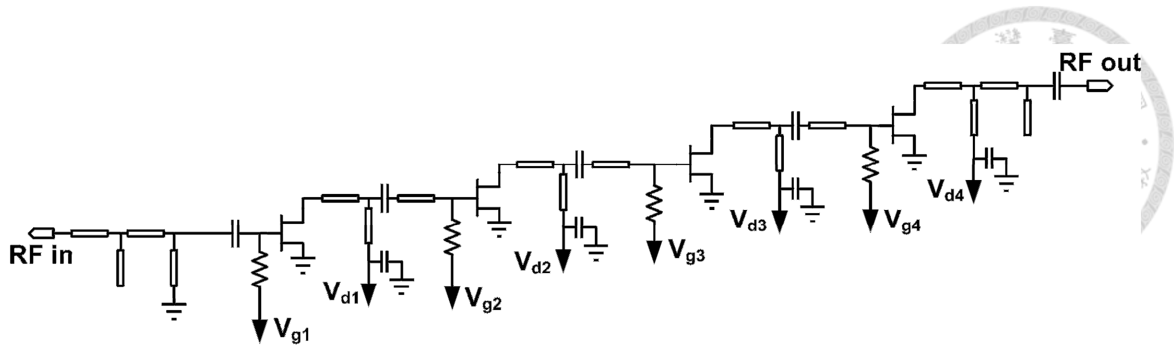


Fig. 2.13. Schematic of the E-band LNA.

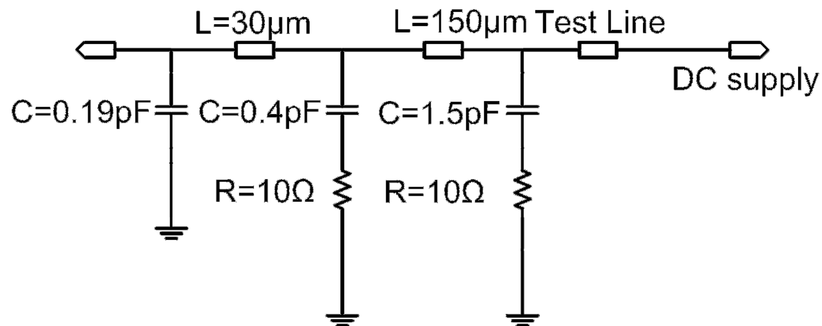


Fig. 2.14. Schematic of the bypass circuit.

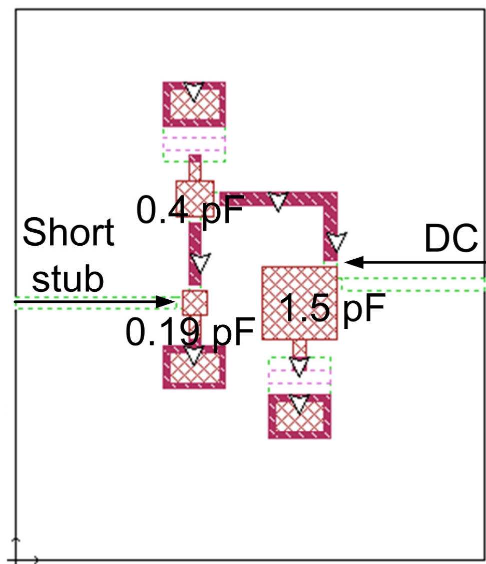


Fig. 2.15. The bypass structure of the matching network between 3rd and 4th stages in EM simulation.

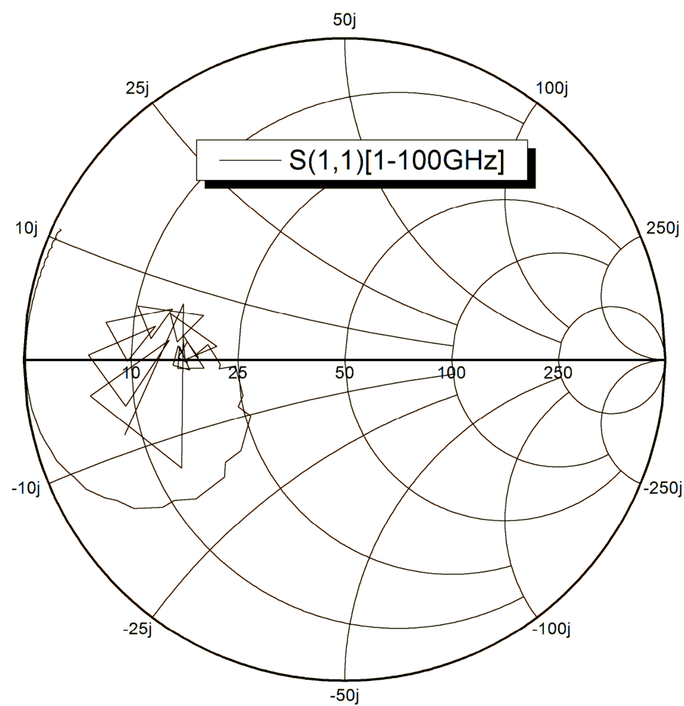


Fig. 2.16. Reflection coefficients of the bypass circuit with test line.

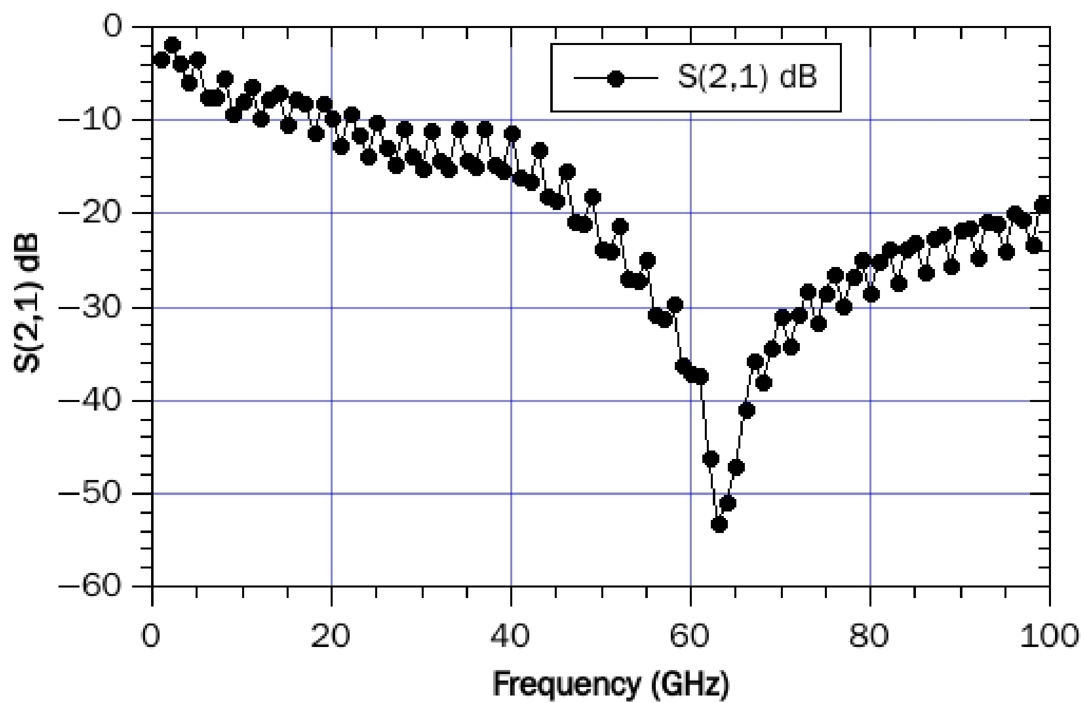


Fig. 2.17. S_{21} of the bypass circuit, simulated with testline.

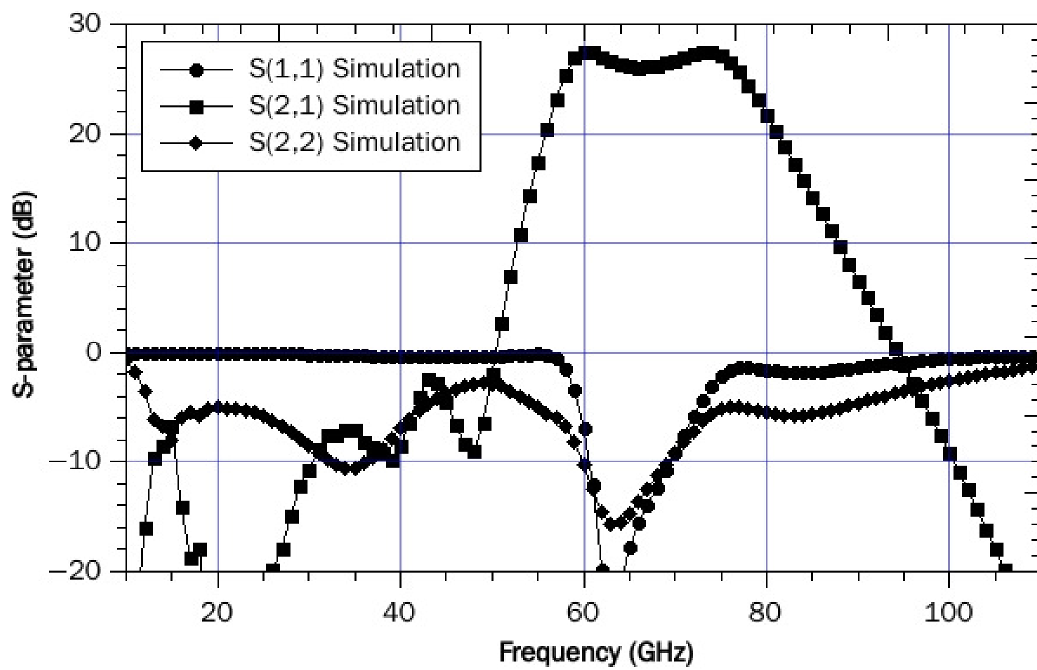


Fig. 2.18. Simulation result of the *S*-parameters.

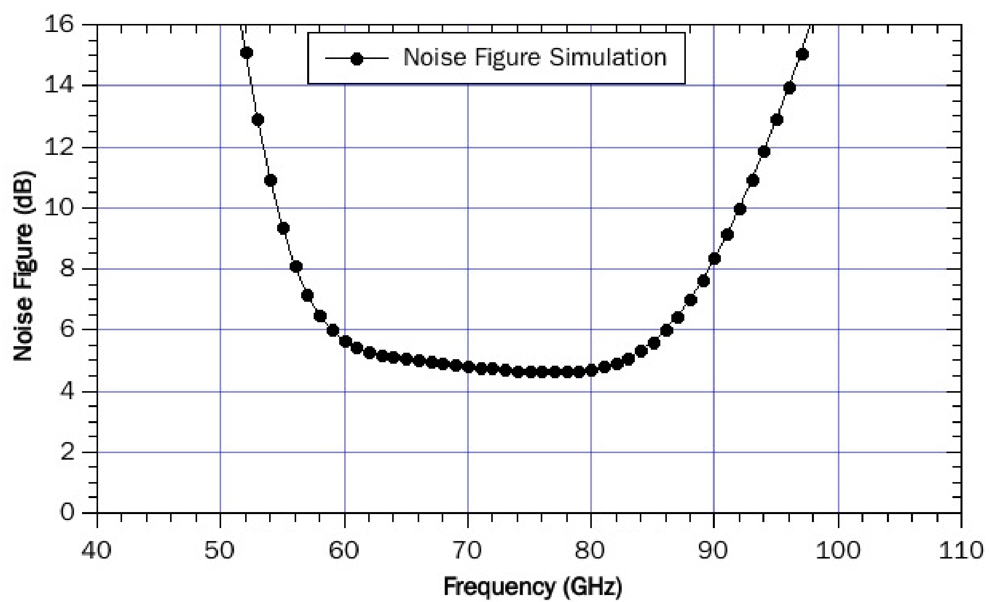
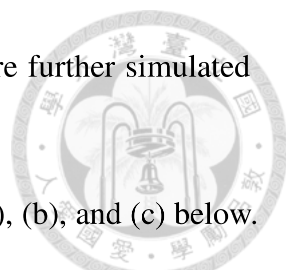
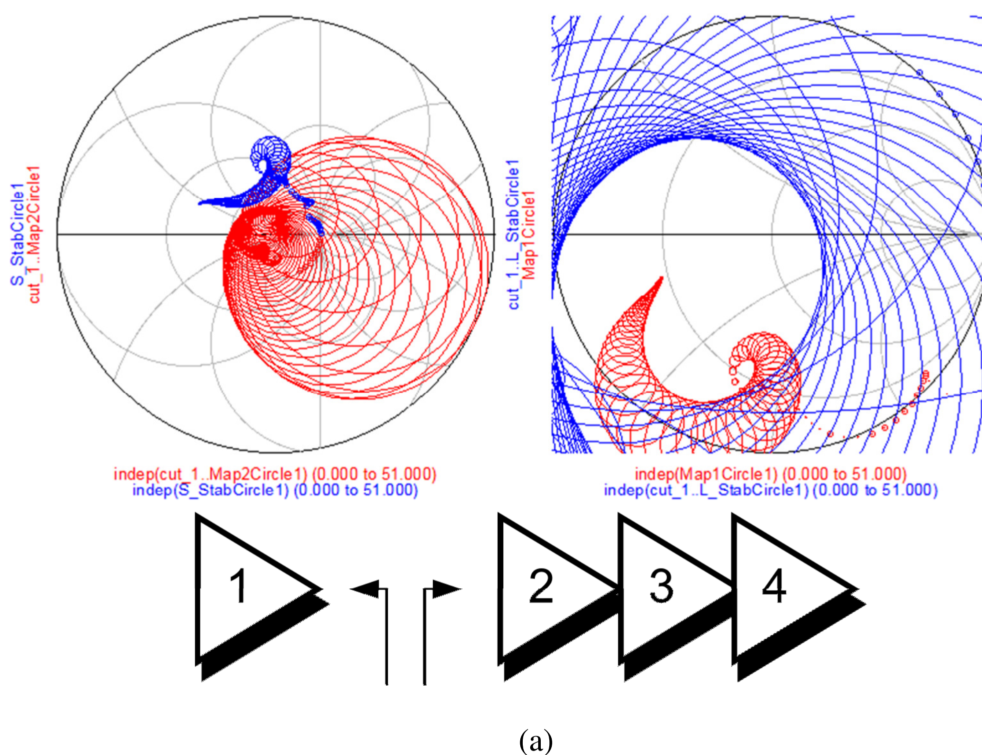


Fig. 2.19. Simulation result of the noise figure.

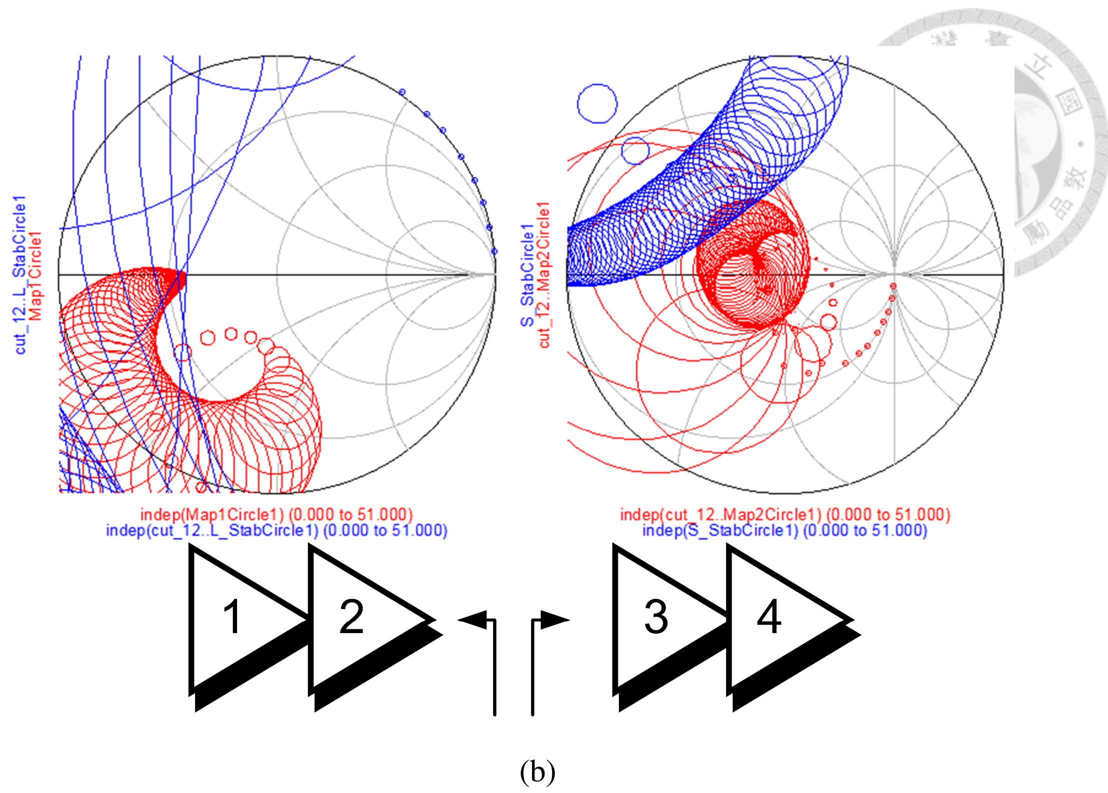


Bypass circuits, blocking capacitors, and matching networks are further simulated and optimized by Sonnet EM solver [16].

The simulations of interstage stability are shown in Fig. 2.20 (a), (b), and (c) below. Swept from 0 to 110 GHz, each plot is checked carefully that two circles do not intersect with each other at the same frequency. Fig. 2.21 shows the final layout of the E-band LNA with size $2 \times 1\ \text{mm}^2$.



(a)



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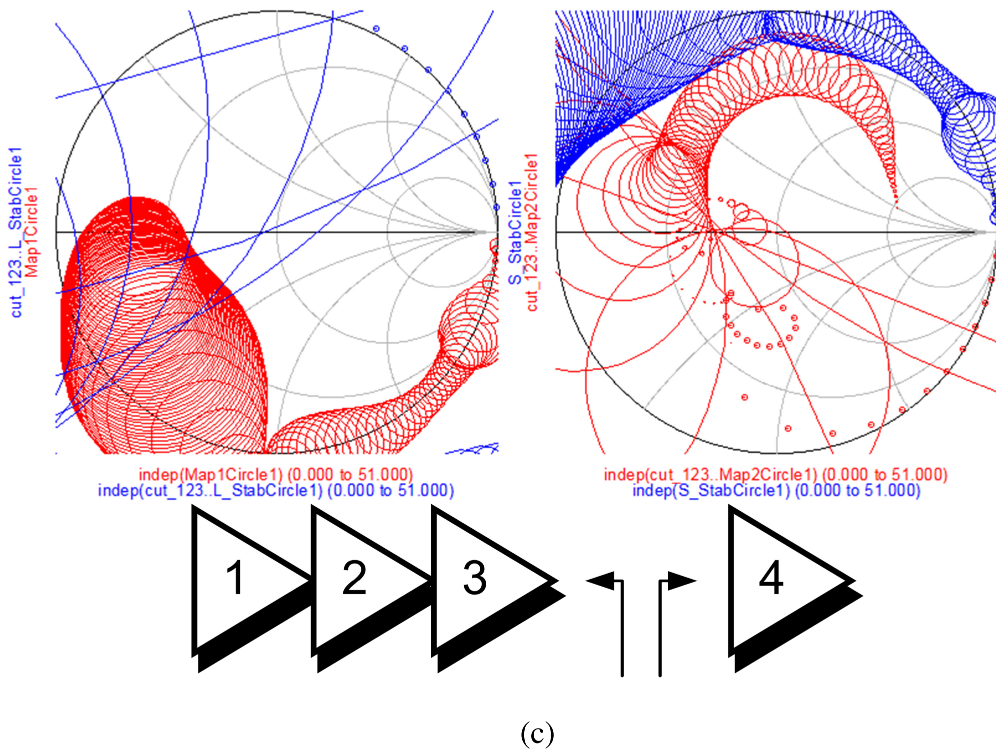


(c)

Fig. 2.20. The interstage stability of (a) the 1st stage with last 3 stages, (b) the first 2 stages with last 2 stages, and (c) the first 3 stages and last stage.

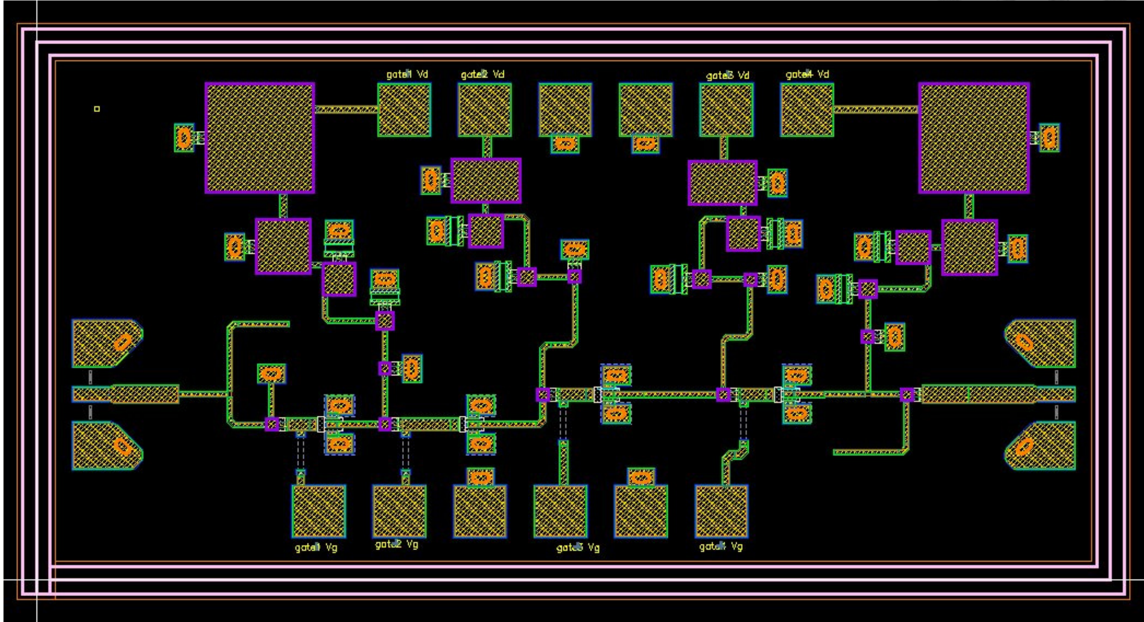


Fig. 2.21. Layout of the E-band LNA.

2.2 Experimental Results

The chip photo mounted on PCB with size of 2 × 1 mm^2 is shown in Fig. 2.22. Small signal data is measured via on-wafer probing, with bond wire to dc pad to supply dc power. Each stage is biased same at the voltage and current as described in Table 2.1. The circuit consumes 44 mW dc powers.

The *S*-parameters are measured from 10 to 110 GHz by Agilent E7350A vector network analyzer. Fig. 2.23 shows the *S*-parameters simulation and measurement results under the bias condition listed in Table 2.1. Measured gain is 1-2 dB higher than simulated gain, which is caused by the slight difference in g_m between model and device. The average small signal gain is 28 dB from 62 to 77 GHz. Input and output return loss is better than 10 dB from 63 to 72 GHz. Reverse isolation is better than 40 dB over the measured frequency.

The noise figure is measured by Agilent N8975 noise figure analyzer with K88 down converter module. The measurement is performed only from 75 to 90 GHz due to our instrumentation constraints. Simulated and measured noises are shown in Fig. 2.24. The E-band LNA exhibits a minimum noise figure of 3 dB at 80 GHz, and average 4.5 dB noise figure across the measured frequency band. The measured noise agrees with simulation reasonably at low frequency, and about 1 – 2 dB better at high frequency.

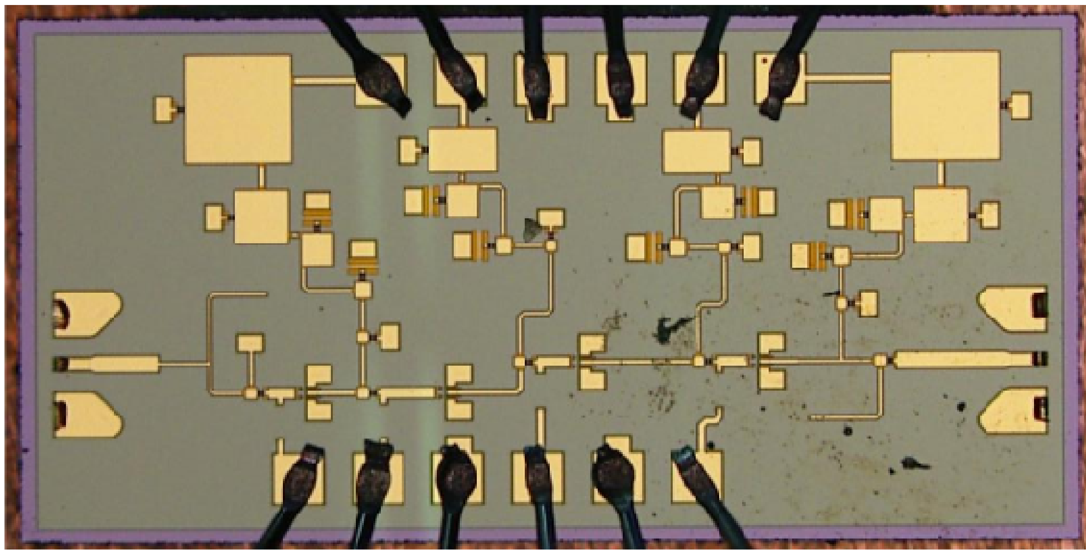
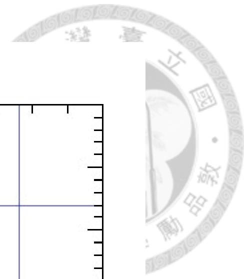


Fig. 2.22. Chip photo of the E-band LNA.



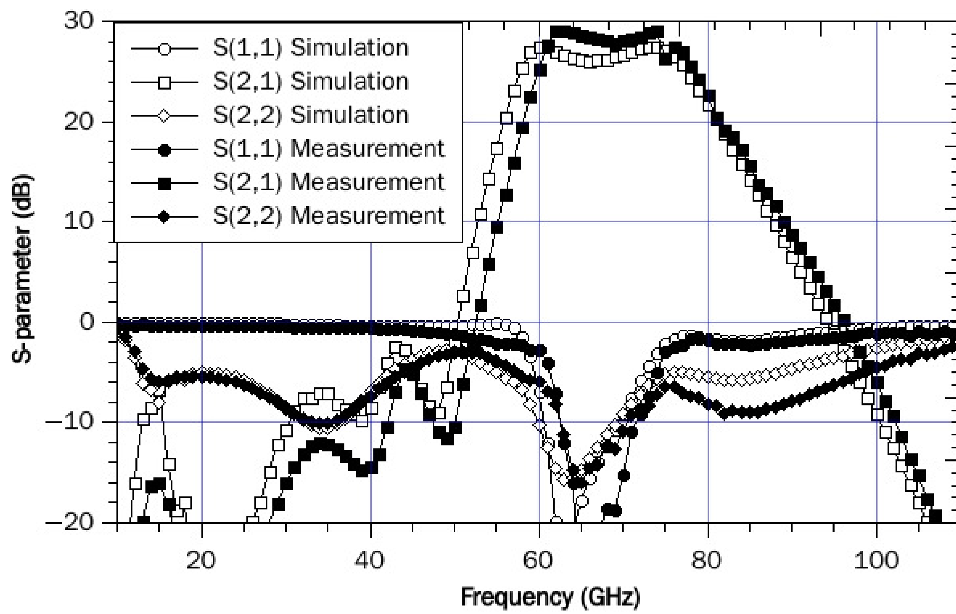


Fig. 2.23. The simulated and measured *S*-parameter from 10-110 GHz of the E-band LNA.

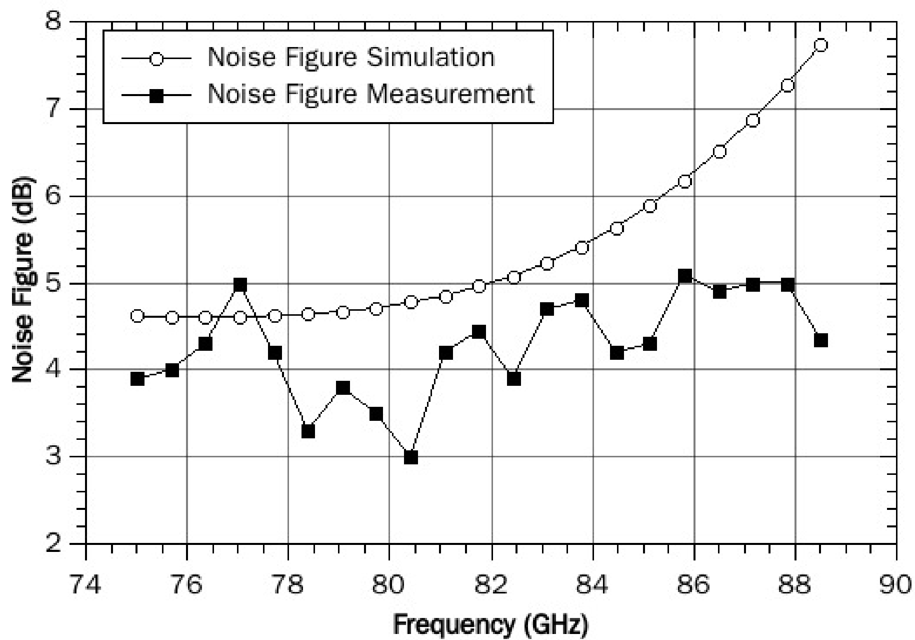


Fig. 2.24. Simulated and measured noise figure from 75-90 GHz of the E-band LNA at 297 K ambient temperature.

2.3 Summary

The performance of LNA can be assessed by the FOM [18] related to gain-bandwidth product (GBP), noise figure and dc consumption. The definition of FOM and GBP are shown below:

$$FOM = \frac{GBP[\mathrm{GHz}]}{(NF_{mag} - 1) \times P_{dc}[\mathrm{mW}]} \tag{2.1}$$

$$GBP = S_{21,mag} \times Bandwidth[\mathrm{GHz}] \tag{2.2}$$

where $S_{21,\mathrm{mag}}$, NF_{mag} are the magnitudes of small signal gain and the noise figure, respectively, and P_{dc} is the overall dc power consumption in milliwatt. This E-band LNA exhibits an FOM of 180.9 (GHz/mW).

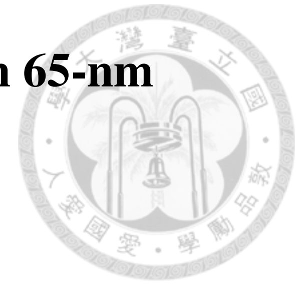
Table 2.3 summarizes the performance of this LNA and recent published LNAs from 60 to 110 GHz. Ref. [10] and [12] show better FOM due to their process advantages in InP HEMT and GaAs mHEMT process. Ref. [15] is a GaAs mHEMT based LNA, but it consumes higher dc power. Ref. [16] is also a GaAs 0.1-μm pHEMT LNA published recently, and it shows very high power consumption compared to this work. This LNA demonstrates highest gain at low E-band with low dc consumption compared to other LNAs. Although the noise figure is inferior to those of InP HEMT or mHEMT LNAs, it is sufficient to be used as gain stages in the E-band radio telescope system.

Table 2.3. Comparison of this work and previously reported LNAs

Ref.	Technology	BW (GHz)	BW (%)	Gain (dB)	P_{dc} (mW)	Noise Figure (dB)	Chip Area (mm^2)	FOM
[10] 2009	35-nm InP HEMT	70-92	27	26	16.8	3.1	2.1 × 0.8	500.4
[11] 2010	80-nm InP HEMT	68-110	42	18	12	3.5	0.55 × 0.75	178.3
[12] 2008	70-nm GaAs mHEMT	70-105	40	25	35	2.7*	2.8 × 1.8	366.8
[13] 2005	ABCS 0.2-µm InAs/AlSb HEMT	85-102	18	18	6	3.9	1.75 × 0.7	122.9
[14] 2006	ABCS 0.2-µm InAs/AlSb HEMT	65-105	47	5.6	2	2.5	1.1 × 1.1	93.3
[15] 2012	0.1-µm GaAs mHEMT	60-90	40	19	56	2.5	3.5 × 1	54.7
[16] 2012	0.1-µm GaAs pHEMT	68-88	25.6	20	262	4.1	-	4.9
This work	0.1-µm GaAs pHEMT	60-77	25	29.3	44	4.5	2 × 1	180.9

*: simulation result

Chapter 3 Design of an W-band Tripler in 65-nm CMOS process



A wideband frequency multiplier can be used in broadband signal source. In this work, a W-band wideband tripler is designed and fabricated and measured using CMOS 65-nm process provided by Taiwan Semiconductor Manufacturing Company (TSMC).

3.1 Circuit Design of the W-band Tripler

3.1.1 Structure of Frequency Multiplier

Fig. 3.1 shows the typical topology of a frequency multiplier. The non-linear device is used to generate harmonic frequency. The output load of the non-linear device should match to optimum load of the desired frequency, which can be determined by load pull at the frequency. The input matching should achieve conjugate matching at fundamental frequency and a good reflector at harmonic frequency.

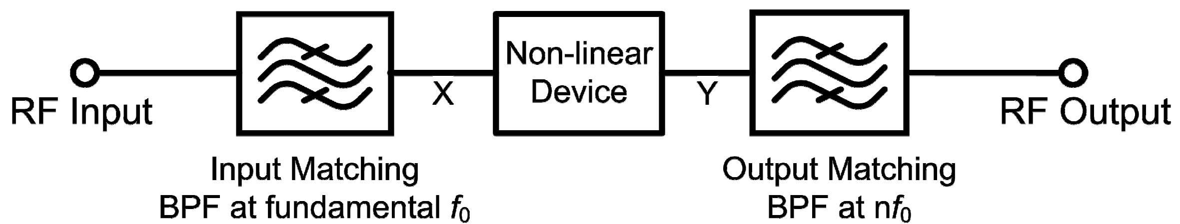


Fig. 3.1. Topology of the typical frequency multiplier.

The non-linear device is usually a transistor bias at pinch-off region [19] or a passive device such as diode [20]-[21]. We can express the output as a polynomial of the input:

$$y = A_0 + A_1 x + A_2 x^2 + A_3 x^3 \tag{3.1}$$

Without losing generality, we represent input signal as a sine signal:

$$x(t) = V\cos(\omega t) \tag{3.2}$$

The output of the non-linear device is:

$$\begin{aligned} y(t) &= A_0 V + A_1 V\cos(\omega t) + A_2 V^2\cos^2(\omega t) + A_3 V^3\cos^3(\omega t) + H.O.T \\ &= A_0 V + \frac{1}{2}A_2 V^2 + (A_1 V + \frac{3}{4}A_3 V^3)\cos(\omega t) + \frac{1}{2}A_2 V^2\cos(2\omega t) \\ &+ \frac{1}{4}A_3 V^3\cos(3\omega t) + H.O.T \end{aligned} \tag{3.3}$$

The output signal is a combination of fundamental and harmonic signals. By passing the output signal through a filter on desired frequency, the whole structure is a frequency multiplier. In the design of tripler, the third harmonic frequency is the desired frequency.

Rejection of other harmonic is one necessary attribute in multiplier design. Some designs add filters at output to suppress the harmonic signal. However, the filter occupies more chip area and adds additional insertion loss to the multiplier [22]. In this design, differential structure [23] and transformers are used to suppress harmonic signal.

With differential structure, input signal first splits into two paths in opposite phase, and each feeds into a tripler stage. The outputs of triplers then combine together in opposite phase. Since the even harmonic signals are in-phase, they cancel each other at combining stage.

To split and combine signal in opposite phase, balun or transformers can be used [24]. Transformer is chosen in this design for the following reasons. Firstly, its input/output can be designed to desired impedance rather than 50 Ω in balun. Because of this flexibility, chip size using transformer is usually more compact than using balun

since the latter requires additional matching circuit. Second, transformer provides a path to ground in low frequency, thus naturally increasing the harmonic rejection. Compare to other frequency multiplier, this design eliminates the need of additional filters to increase the harmonic rejection. Finally, in differential structure, the virtual RF ground enables biasing at the center point of the symmetry transformer coil. No additional short stub or λ/4 stub in matching circuit is needed, and chip size can be further minimized.

3.1.2 Design of W-band Tripler

The schematic of this tripler is shown in Fig. 3.2. The single-ended input signal is divided into differential signal by transformers. The differential signals are then passed to a buffer stage and a tripler stage, generating the desired third harmonic signal. Output signal is produced by combining the differential signal with transformer, cancelling the even harmonic signal.

The size of the tripler devices is 32 fingers with total width 96 μm. Fig. 3.3 shows the plot of third harmonic output power under different voltage bias. In order to maximize the output power of third harmonic signals, device bias of V_d and V_g are 1.0 V and 0.5 V, respectively. Rather than bias at pinch-off region, the bias close to saturation can achieve larger saturated power when input power is large. The drawback is consuming more dc power. Due to the effect of load impedance to the output power of transistors [25], the load pull simulation is adopted to find optimal load of third harmonic. The result of load pull is shown in Fig. 3.4. In ideal devices simulation, under high input power, the device in load pull shows better output power than that of the conjugated matched. Also, the load pull results from 20-25 GHz input are close to same impedance,

indicating that if presenting constant impedance across 20-25 GHz to the tripler output, the tripler can achieve wideband performance.

A buffer stage using a common source transistor is added to compensate the conversion loss of the tripler. The buffer is also biased at V_d of 1.0 V and V_g of 0.5 V, which provides enough transconductance g_m with low drain current. Because of higher gain at low frequency, the buffer is connected before the tripler. The larger signal from buffer also drives tripler stage more non-linear, increasing the conversion efficiency. A 30-Ω resistor is added at the gate of buffer stage to stabilize the buffer transistor.

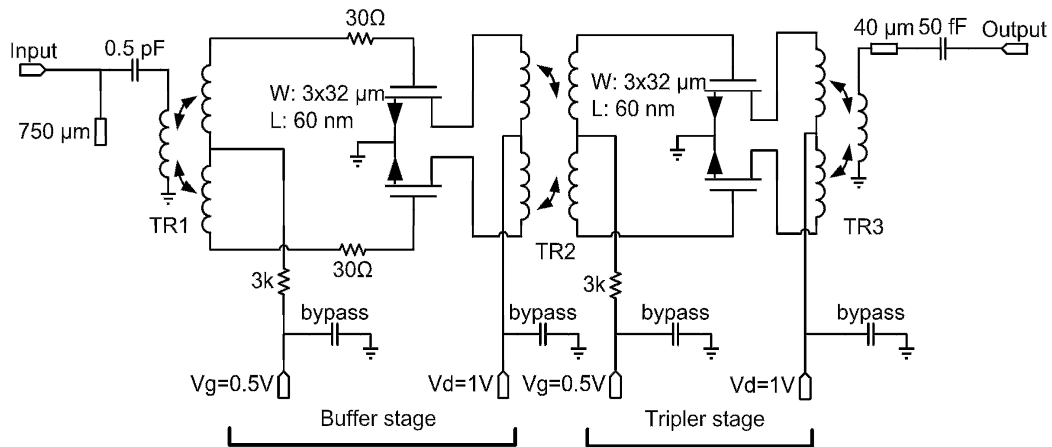
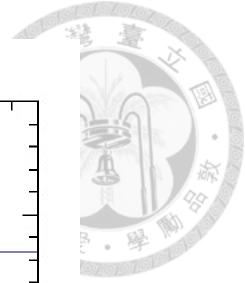


Fig. 3.2. Schematic of the complete W-band tripler.



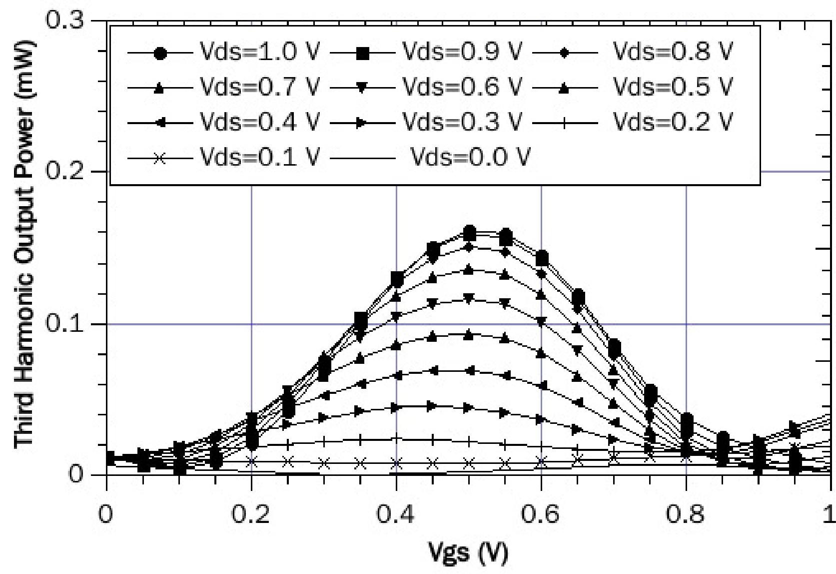


Fig. 3.3. Sweep third harmonic output power with device size 3 × 32 μm under different voltage bias.

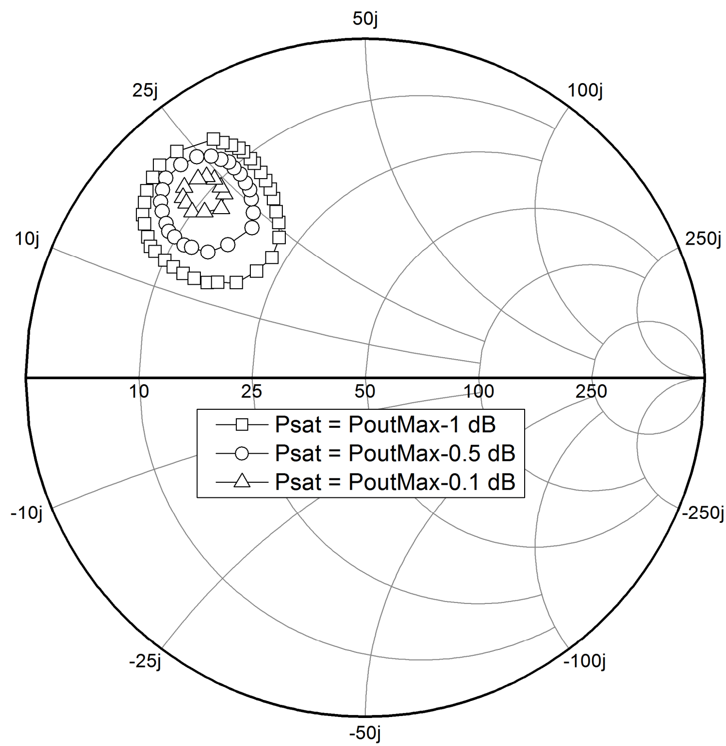


Fig. 3.4. Result of load pull on third harmonic output with device size 3 × 32 μm. Each circle means the loadsthat generate constant third harmonic output power. From inside out: 0.1dB, 0.5 dB 1 dB lower then simulated maximum output power

3.1.3 Transformers Design

In this design, three transformers TR1, TR2, and TR3 are used to achieve impedance matching between stages. TR1 and TR3 also serve as signal splitter and signal combiner. All three transformers are first simulated using ideal inductors with practical mutual inductance and coupling factor. The TR2 is chosen that transfers conjugate matching of buffer stage output to the input impedance of tripler. TR1 and TR3 are selected that transfers impedances to a value that is easy match to 50 Ω. Taking output transformer TR3 as example, Fig. 3.5 shows the third harmonic load pull result at 75 GHz and the impedance transformation of the ideal transformer. The transformer converts the load pull impedance to impedance that is easy to match to 50 Ω.

Based on the result, more accurate EM simulation is carried out using Sonnet EM software. The transformer coils are made of top two metal layers with line width and line spacing of both 4 μm. Ground metal is slotted to decrease insertion loss. The inductance value is achieved by adjusting the size of transformer and the number of turns. The geometry of each transformer is adjusted subtly considering the parasitic effect. Fig. 3.6 shows the three-dimension view of three transformers in simulator, and the simplified topology of each transformer. Table 3.1 summarizes the characteristics, including inductance, Q factor, and actual turn number of these transformers after EM simulation.

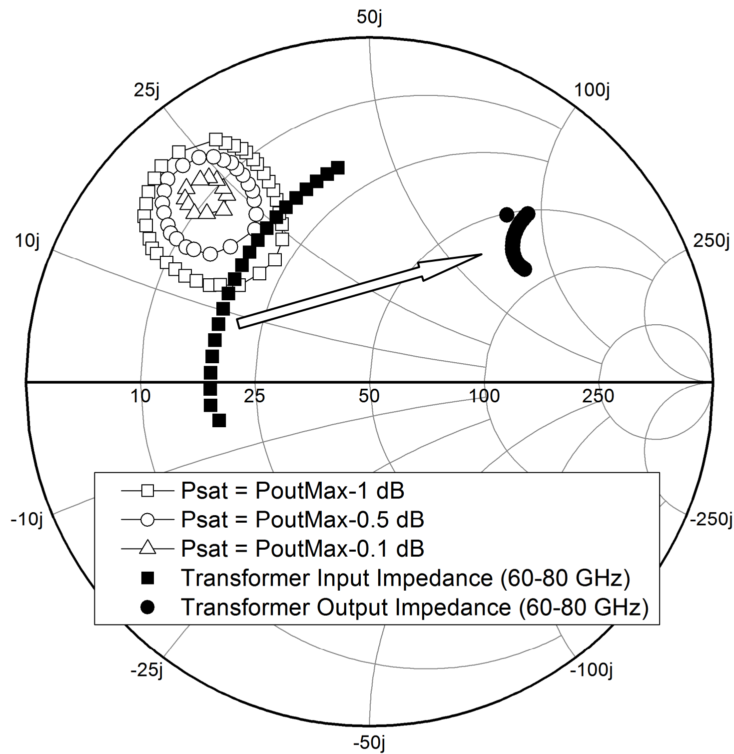
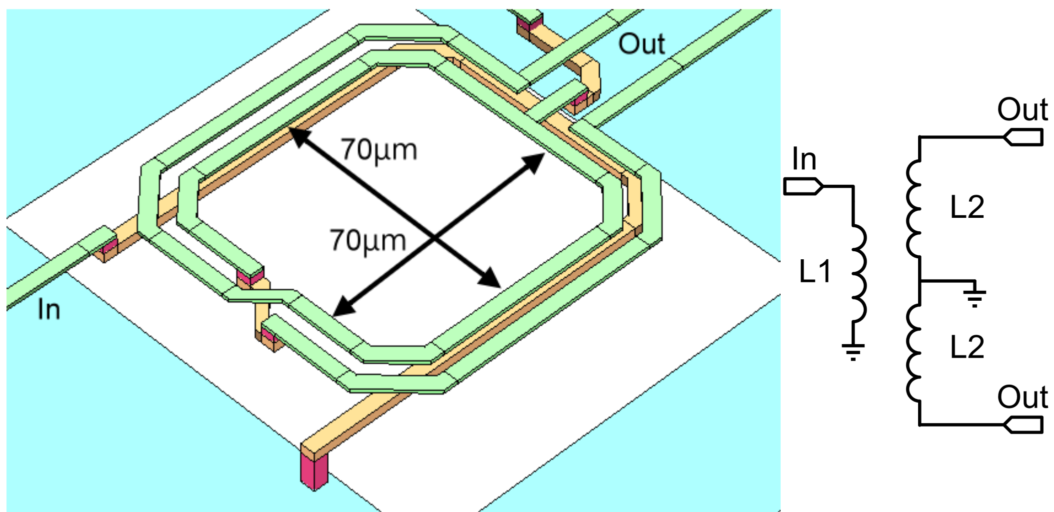
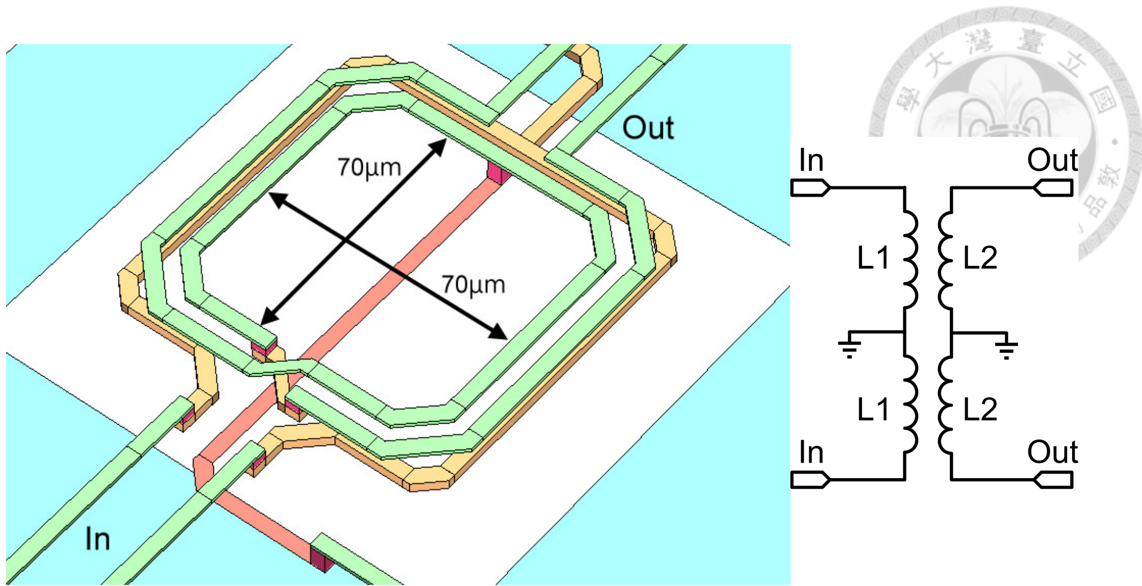


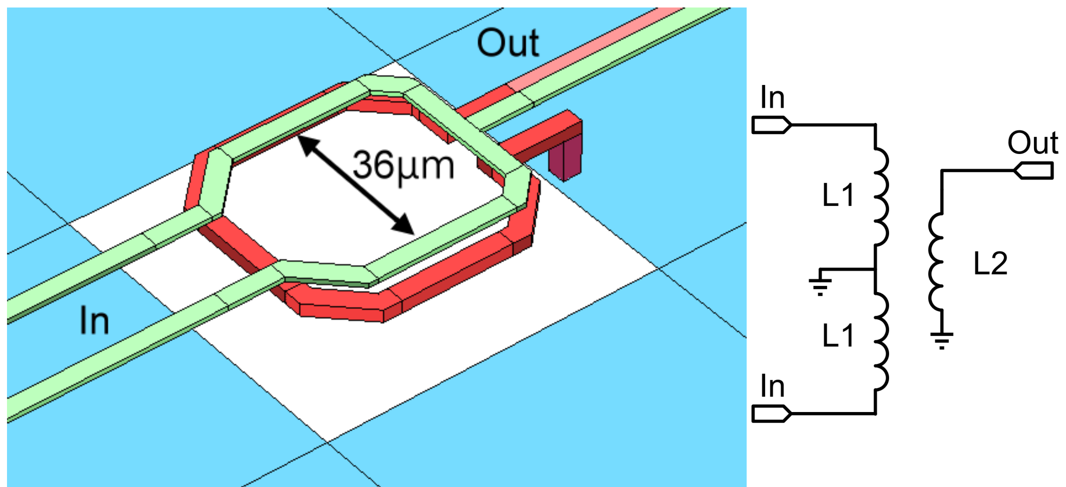
Fig. 3.5. Third harmonic load pull result and the input/output impedance of the transformer TR3. The input impedance is matching the load pull result impedance, and the output impedance of the transformer is easy to match to 50 Ω.



(a)



(b)



(c)

Fig. 3.6. Three-dimensional illustrations and simplified equivalent circuits of the transformers: (a) TR1, (b) TR2, and (c) TR3.

Table 3.1. Simulated characteristics of transformers

	L1(pH)	Q1	Actual Turn Number	L2(pH)	Q2	Actual Turn Number
TR1	240	8.3	1	280	8.4	2
TR2	240	6.5	1	504	3	2
TR3	65	7.8	1	104	10	1

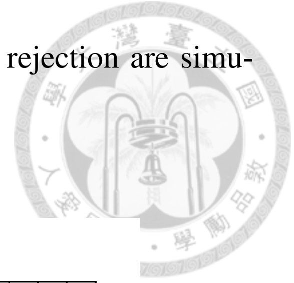
3.1.4 Full Circuit Simulation

Since the transformers have transferred the impedance for easy matching, the rest matching work is simple. The input matching is done by an open stub and dc blocking capacitor implemented by metal-insulator-metal (MIM). Output matching is made of a short transmission line and a small series capacitor implemented by top two layers metal.

All the dc voltage is biased through the virtual ground point of the transformer. Though the virtual ground provides isolation of RF noise in dc bias network, on-chip bypass capacitors are added for stability concern. The drain bypass is composed of a 1.3 pF capacitors as in-band bypass, which is simulated along with transformer. A 2.5 pF MIM capacitor and a 25 pF MOSCAP are used as out-band bypass.

The simulation results of conversion gain versus input power of 20 GHz and 25 GHz are shown in Fig. 3.7 and Fig. 3.8. The conversion gain shows peak value at input power is -5 dBm. Fig. 3.9 shows the simulated conversion gain versus input frequency with input power of -5 dBm. The simulated peak conversion gain is 1.7 dB, with 3-dB

bandwidth from 20 to 28 GHz. Fundamental and second harmonic rejection are simulated and illustrated in Fig. 3.10.



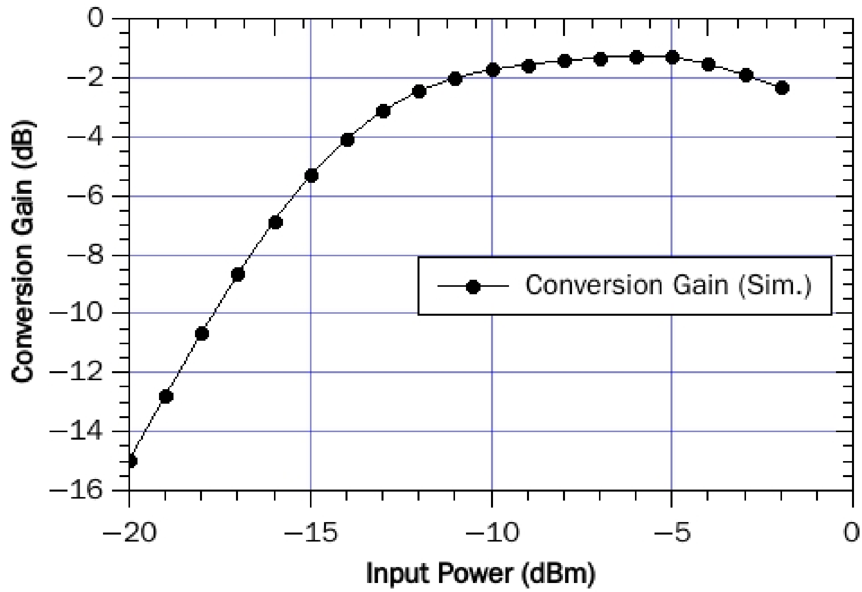


Fig. 3.7. Simulated conversion gain versus input power at input frequency of 20 GHz.

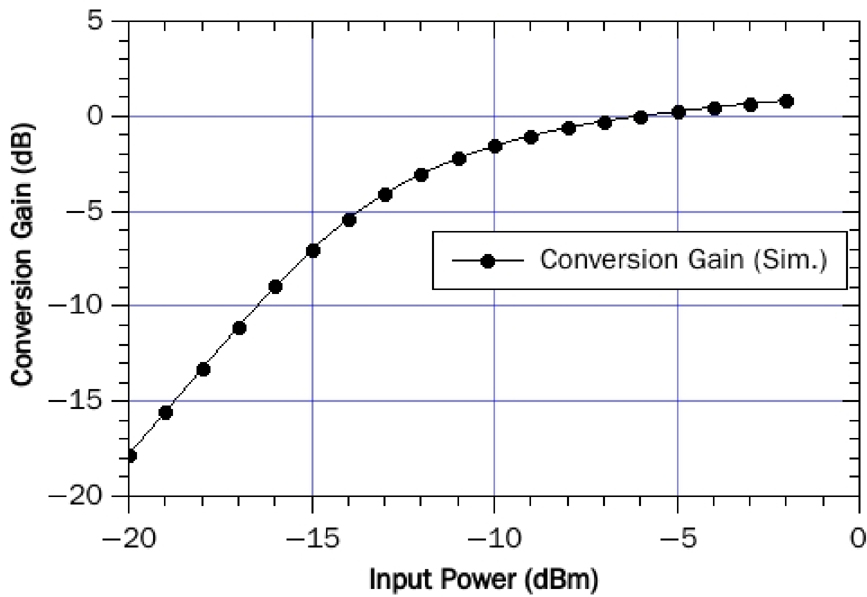
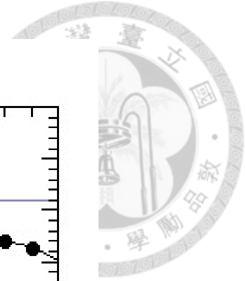


Fig. 3.8. Simulated conversion gain versus input power at input frequency of 25 GHz.



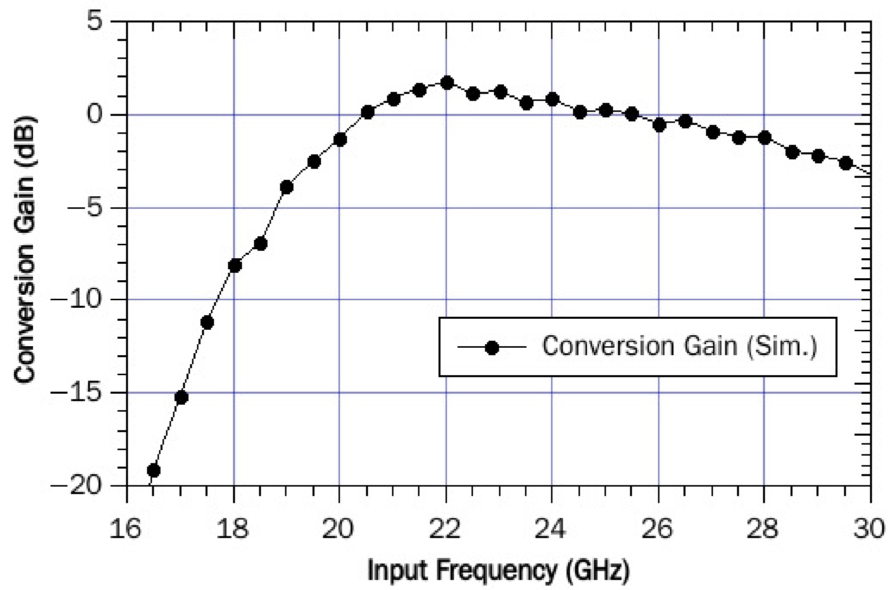


Fig. 3.9. Simulated conversion gain versus input frequency with input power of -5 dBm.

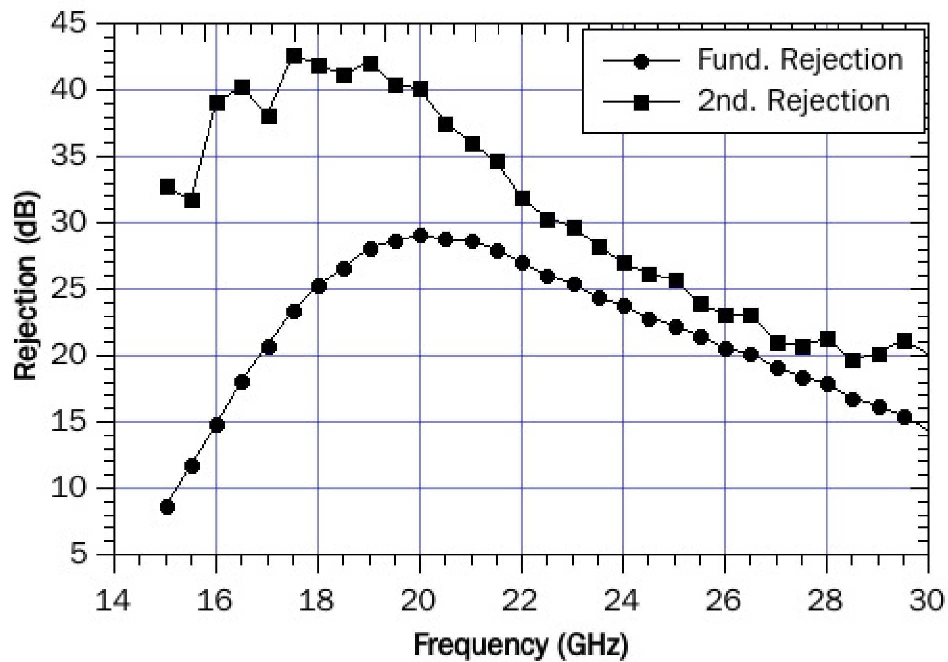


Fig. 3.10. Simulated fundamental and second harmonic rejection versus input frequency with input power of -5 dBm.

The circuit is designed in TSMC CMOS 65-nm process. The layout of the W-band tripler is shown in Fig. 3.11. Including the pad, total size of the tripler is 0.905 × 0.5 mm^2. Pad size is 80 × 80 μm^2 due to the limitation of system package requirement. Chip size can be further minimized if using standard 50 × 50 μm^2 pad. The transformers and capacitors are simulated and verified by Sonnet EM solver [17]. The small-signal inter-stage stability is checked between buffer stage and tripler stage, and the result is shown in Fig. 3.12. To further verify the stability, transient simulation is simulated with 25 GHz, -5 dBm input signal. The frequency domain output signal is transformed from time domain by fast Fourier transform. The result is shown in Fig. 3.13, which shows no oscillations except the desired output signal and its harmonic.

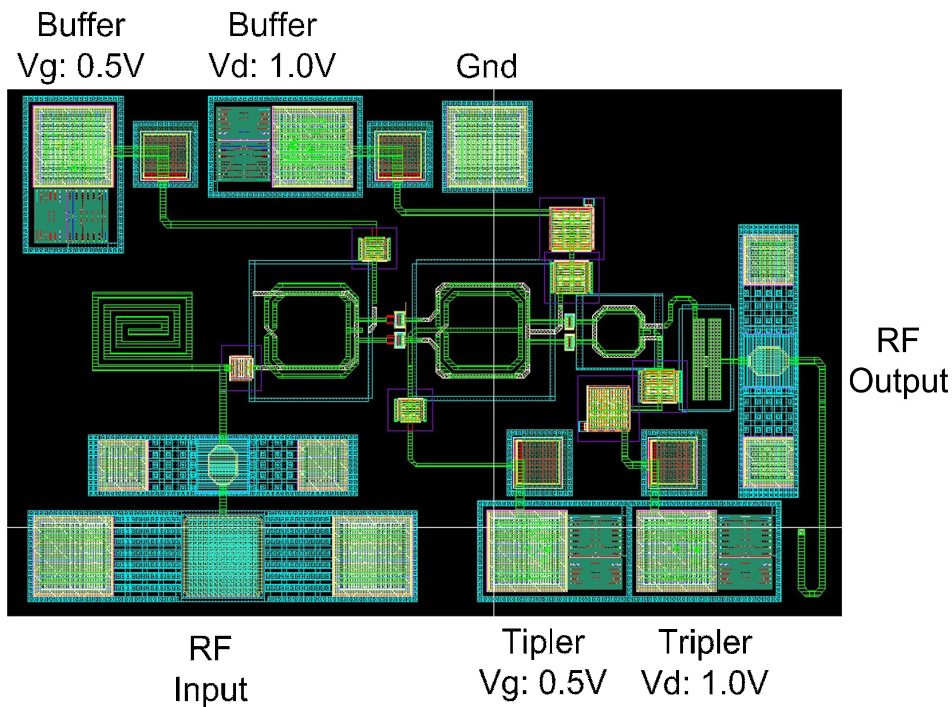


Fig. 3.11. Layout of the W-band tripler.

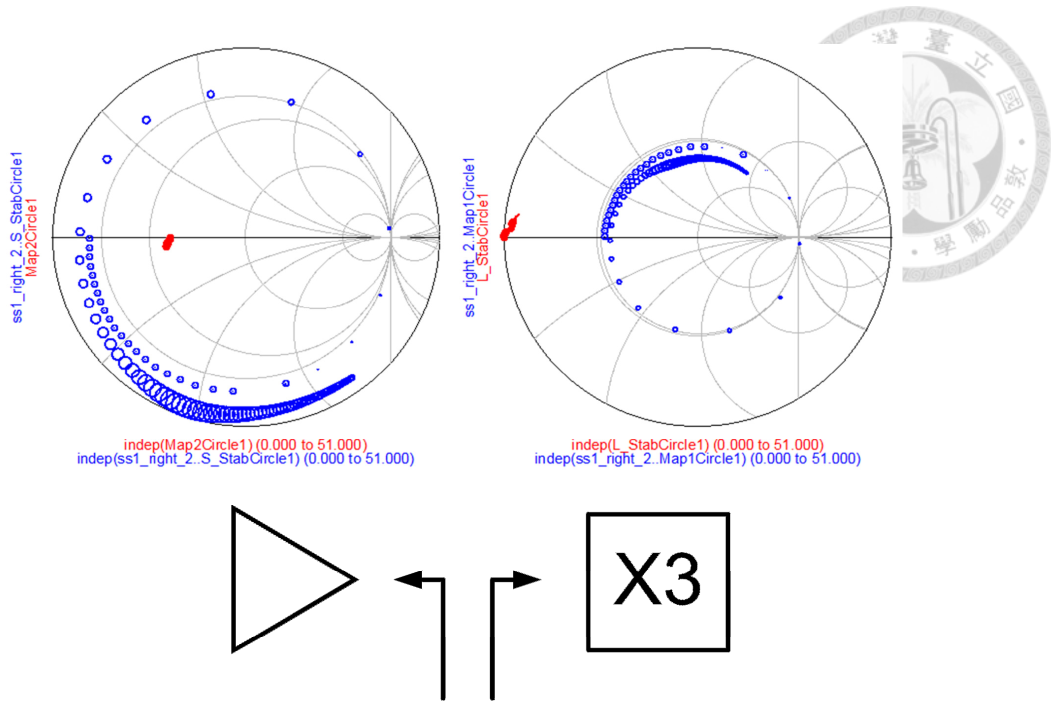


Fig. 3.12. The interstage stability between the buffer and the tripler.

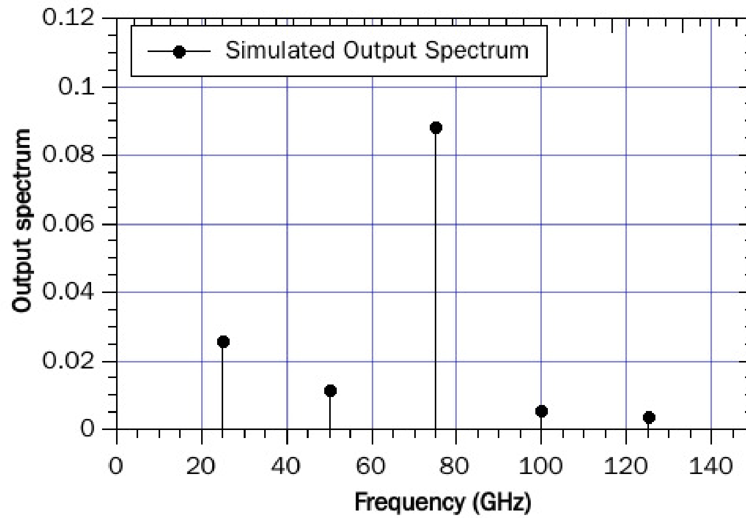


Fig. 3.13. Simulated output spectrum with input signal of 25 GHz, -5 dBm input power. The frequency domain spectrum is generated by applying fast Fourier transform on transient simulation time-domain output.

3.2 Experiment Results

3.2.1 Measurement Setup

This chip is measured via on-wafer probing, with bond wire to dc pad to supply dc power. The chip photo is shown in Fig. 3.14. To measure performance of fundamental rejection, second harmonic rejection and output signal, different equipments are applied. Agilent E8267D vector signal generator is used to generate the input signal around 15 to 30 GHz. The output signal is measured by Agilent E4448A spectrum analyzer and Agilent E4419B power meter. The following Table 3.2 shows the accessories along with the spectrum analyzer and power meter.

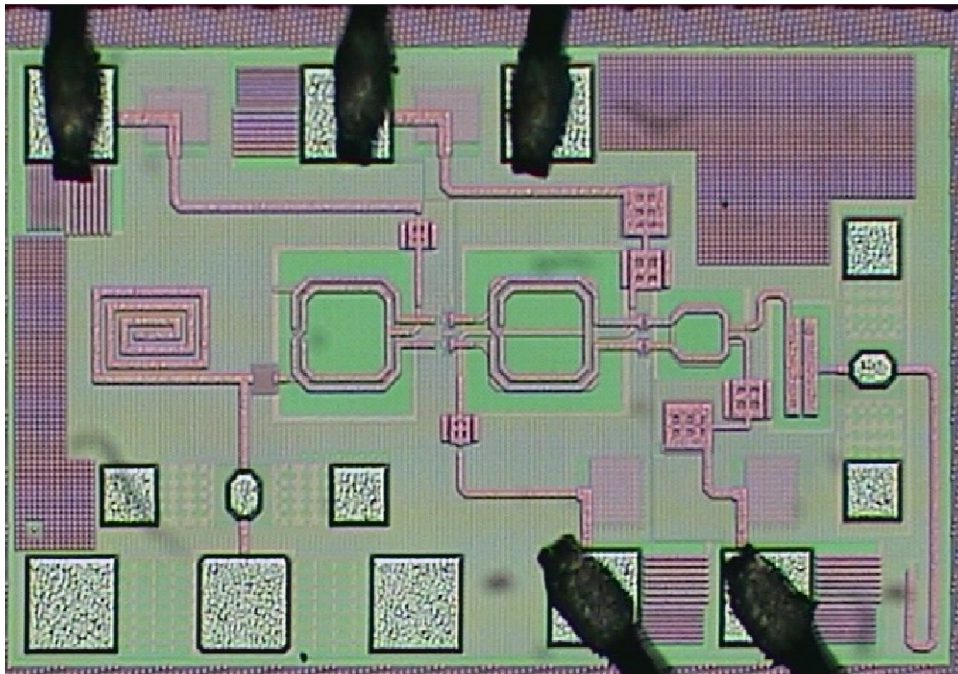


Fig. 3.14. Chip photograph of the tripler with chip size of $0.905 \times 0.5\ mm^2$.

Table 3.2. List of measurement equipments

	0-50 GHz	**V-band Signal (50-75 GHz)**	**W-band Signal (75-110 GHz)**
Measured data	Fundamental Rejection Second Harmonic Rejection	Third harmonic output signal	Third harmonic output signal
Spectrum analyzer	-	11974V preselected millimeter mixer	1197W W-band Mixer
Power meter	-	V8486A V-band power sensor	W8486A W-band power sensor

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3.2.2 Measurement Result

The supply voltage and gate voltage is set to 1 V and 0.5 V like in simulation. The drain current of buffer stage and tripler stage are both 30 mA, together consuming 60 mW quiescent power. When the input power increases to 0 dBm, the dynamic current of tripler and buffer will increase to 90 and 40 mA, respectively.

Fig. 3.15-3.16 show the simulated and measured result of output power versus input power at input frequency of 20 and 25 GHz. Saturated output power can achieve -2.5 dBm with 20 GHz, -4 dBm input signal. The simulated and measured conversion gains versus input power are shown in Fig. 3.17-3.18. The conversion gain is higher than simulation at 20 GHz. At input power of -5 dBm, the tripler shows best conversion gain. Fig. 3.19 is the screenshot of measured spectrum at input power of -5 dBm, input

frequency of 26 GHz. After adding the loss of -69.9 dB, the output power of the tripler at 78 GHz is -5.32 dBm.

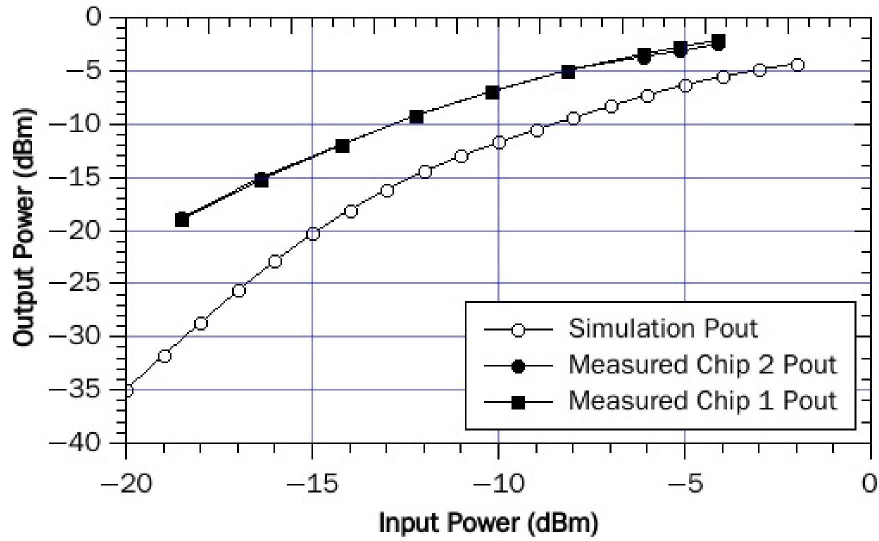


Fig. 3.15. Simulated and measured output power versus input power of the W-band tripler at input frequency of 20 GHz.

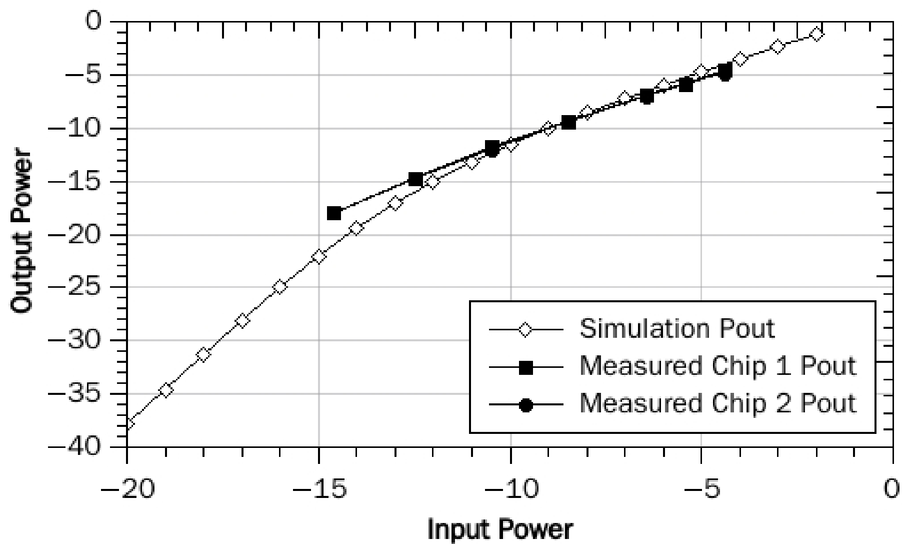


Fig. 3.16. Simulated and measured output power versus input power of the W-band tripler at input frequency of 25 GHz. Output power with input power lower than -15 dBm is beyond the sensitivity limitation of power meter.

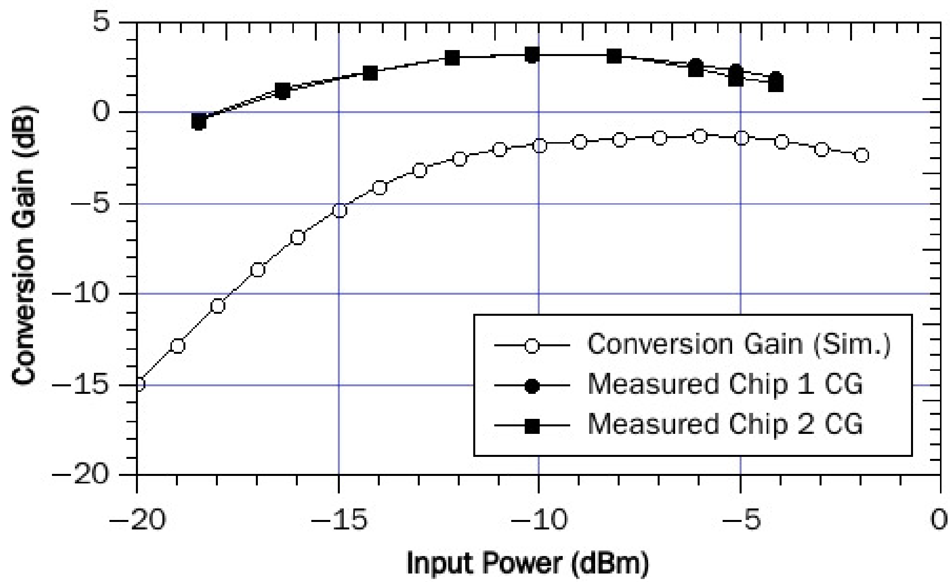


Fig. 3.17. Simulated and measured conversion gain versus input power of the W-band tripler at input frequency of 20 GHz.

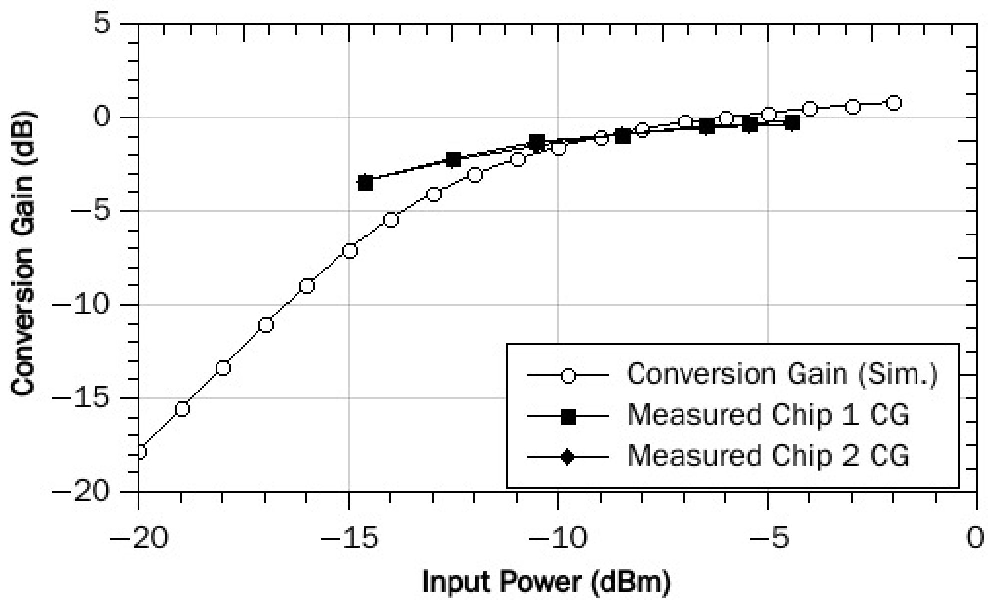


Fig. 3.18. Simulated and measured conversion gain versus input power of the W-band tripler at input frequency of 25 GHz.

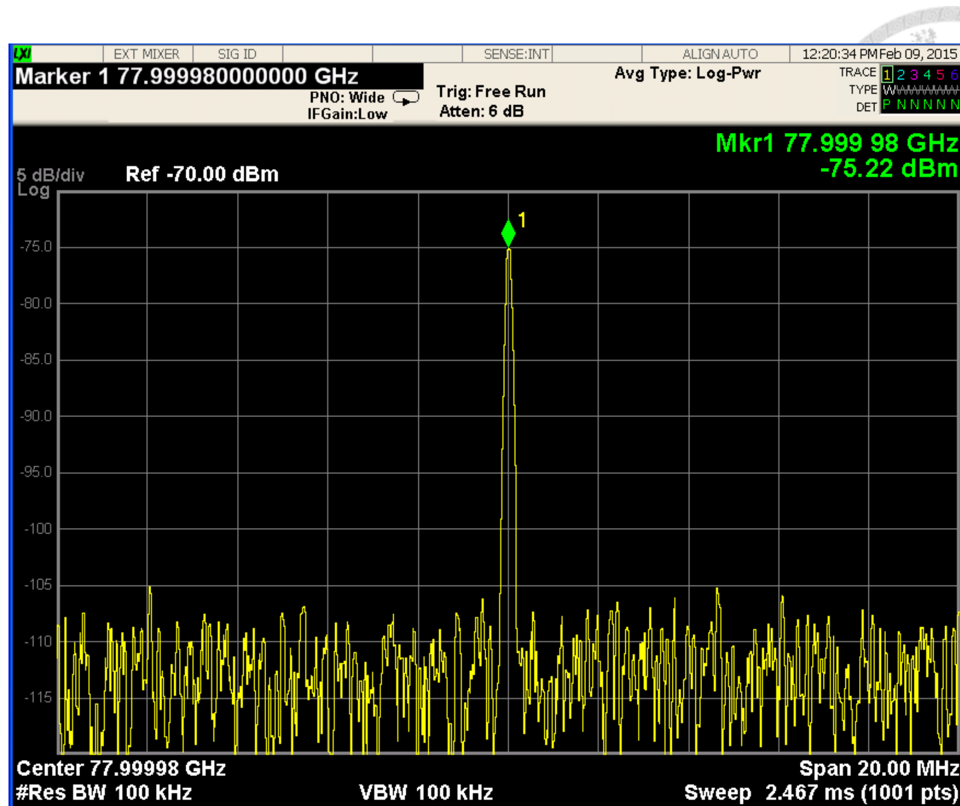
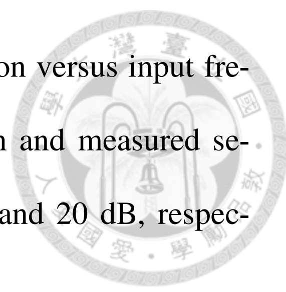


Fig. 3.19. Spectrum screenshot of tripler output at input frequency of 26 GHz, input power of -5 dBm.

The measurement results of conversion gain versus frequency at input power of -5 dBm is shown in Fig. 3.20. The conversion gain extends to lower frequency compared to simulation with peak conversion of 1.3 dB near 20-21 GHz. The 3-dB bandwidth of conversion gain ranges from input frequency of 19 to 26 GHz, or 31 % fractional bandwidth.

The reason that conversion gain shifted to lower frequency is because of the slight inaccuracy in simulation. In the EM simulation of transformers, ground metal is simulated by “planar resistor”, which sacrifices the accuracy of parasitic capacitance between metal layers a little. Fig. 3.21 shows the re-simulation result after adding 15 fF capacitors to ground beside the transformer EM simulation. The re-simulation agrees with measurement.

The measured fundamental signal and second harmonic rejection versus input frequency is shown in Fig. 3.22-3.23 Measured fundamental rejection and measured second harmonic rejection in measured range are larger than 25 dB and 20 dB, respectively.



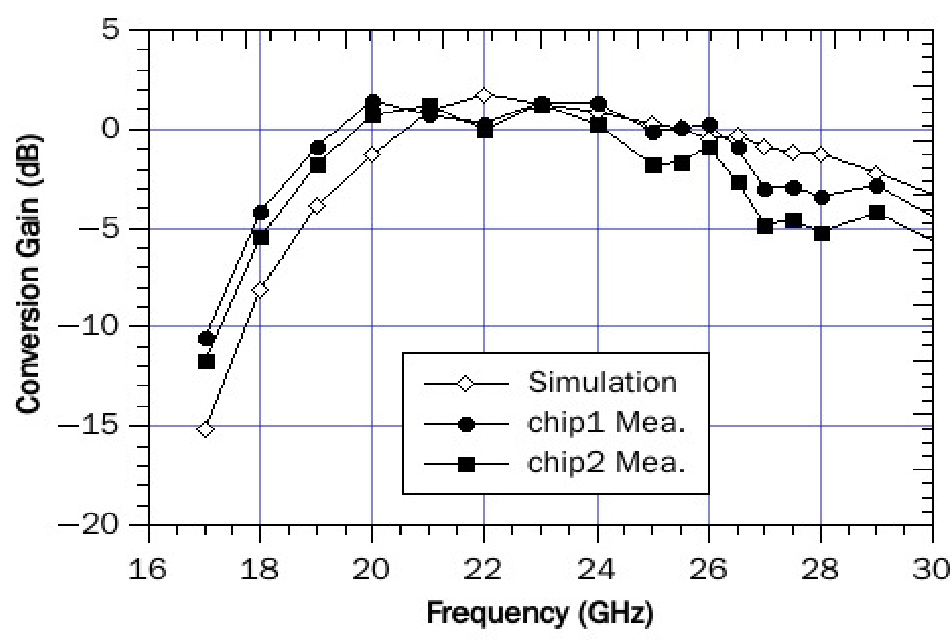


Fig. 3.20. Simulated and measured conversion gain versus input frequency of the W-band tripler at input power of -5 dBm.

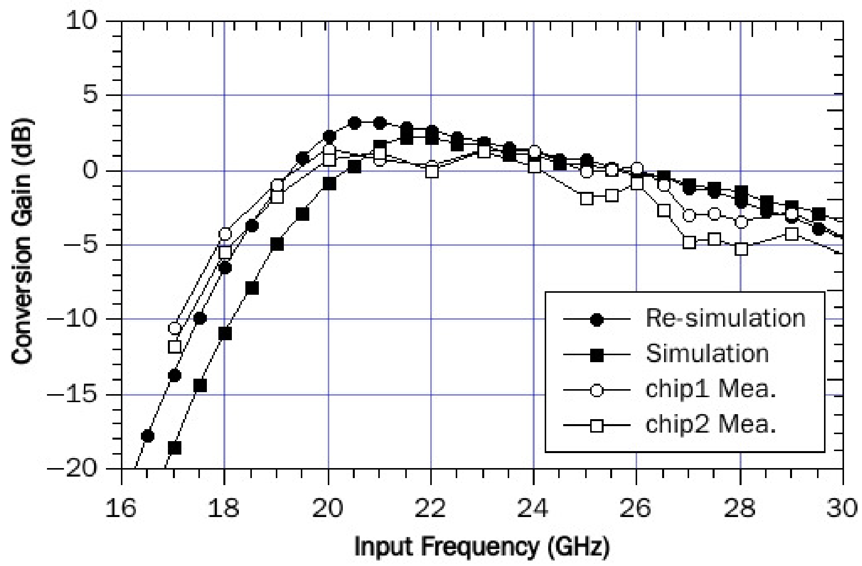


Fig. 3.21. Measurement, simulation and re-simulation of conversion gain versus input frequency of the W-band tripler at input power of -5 dBm.

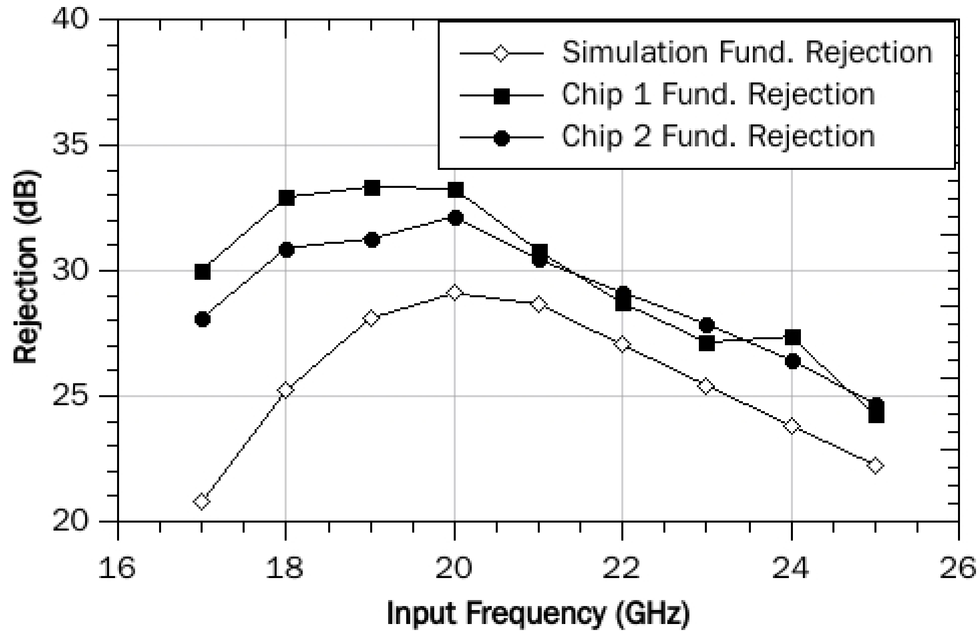


Fig. 3.22. Simulated and measured fundamental rejection of the tripler versus input frequency at input power of -5 dBm.

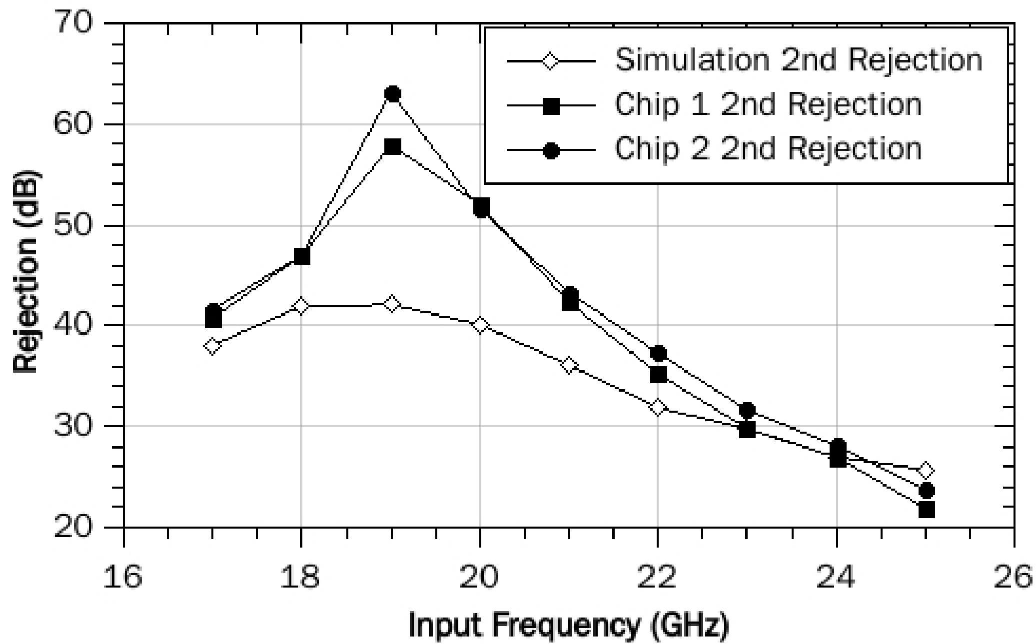


Fig. 3.23. Simulated and measured second harmonic rejection of the tripler versus input frequency at input power of -5 dBm.

3.3 Summary

In this chapter, a broadband tripler with W-band output frequency is designed and measured. Table 3.3 summarizes the performances of the published frequency multiplier with output frequency at W-band. Using active device biased at pinch-off region, though consumes more power, this tripler shows 1.3 dB conversion gain, which is largest except [26]. However, the dc power consumption is only one quarter of [26], and better to other active type multiplier. The differential structure and rejection of transformers together achieves 20 dB rejections without any supplementary filter. Take advantage of broadband characteristic of transformers, this tripler has 3-dB bandwidth of 31.3 percent, which is the best among other CMOS multiplier works. This tripler achieves wide

working range, good conversion gain, harmonic rejection and low dc consumption simultaneously.

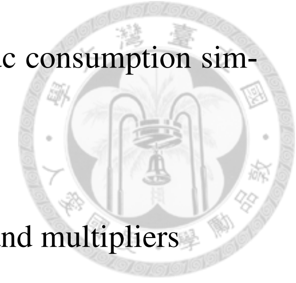


Table 3.3. Comparison of this work and other published W-band multipliers

	Technology	**Type**	**Output BW (3-dB BW)**	**CG/ Reject (dB)**	**P_{sat}/P_{in} (dBm)**	**P_{dc} (mW)**	**V_d (V)**	**Size (mm^2)**
[26] 2007	0.1-µm HEMT	X6	78-104 (28.6 %)	6/25	7/4	286	2	8
[27] 2010	0.15-µm mHEMT	X6	72-114 (45.2%)	>-17.9/40	-3.4/14.5	120	-	3.3
[28] 2012	0.18-µm SiGe BiCMOS	X3	80-100 (22 %)	-10.5/20	-10.5/0	75	2.5	-
[29] 2012	65-nm CMOS	X4	75-110 (-)	-24.3/30*	-14.3/10	16	1.5	0.342
[30] 2012	65-nm CMOS	X9	88-99.5 (12.2%)	-5.7/>31	8.5/13	438	2.4	0.45
[31] 2014	0.13-µm SiGe BiCMOS	X3	36-83 (79 %**)	0/10	-10/18	362	2.4	0.52
[32] 2014	65-nm CMOS	Injection Lock (X10)	77.8-78.9 (1.4%)	-/59(spur)	>8.8/-	265	1.8	0.53
This work	65-nm CMOS	X3	57-78 (31.3%)	1.3/>20	-2.5/-4	60	1	0.45

*: Simulation result.
**: Bandwidth of rejection larger than 10 dB.

Chapter 4 Evaluation of a V-band transmitter module using CMOS integrated circuits in LTCC package

4.1 Introduction

In this chapter, we demonstrate a 60 GHz system-in-package (SIP) super heterodyne transmitter in the National Network Communication Program. All the works including system planning, component design, unit testing, and system integration are proposed by research team of Graduate Institute of Communication Engineering of National Taiwan University. The thorough system architecture of the transceiver is shown in Fig. 4.1. In this demonstration, the transmitter chain circuits include T1 – T5 are integrated and measured. Whole transmitter chips are designed and fabricated using 65-nm CMOS process provided by TSMC. The contribution in this chapter is the evaluation of V-band transmitter system module packaged in LTCC.

The proposed super heterodyne transmitter shows small-signal gain of 28 ± 1 dB and saturation power larger than 7 dBm from 57 GHz to 66 GHz. The measured output power 1-dB compression power (OP_{1dB}) is 3 dBm. The transmitter demonstrate the ability to utilize 802.11ad unlicensed band on high data rate transmission.

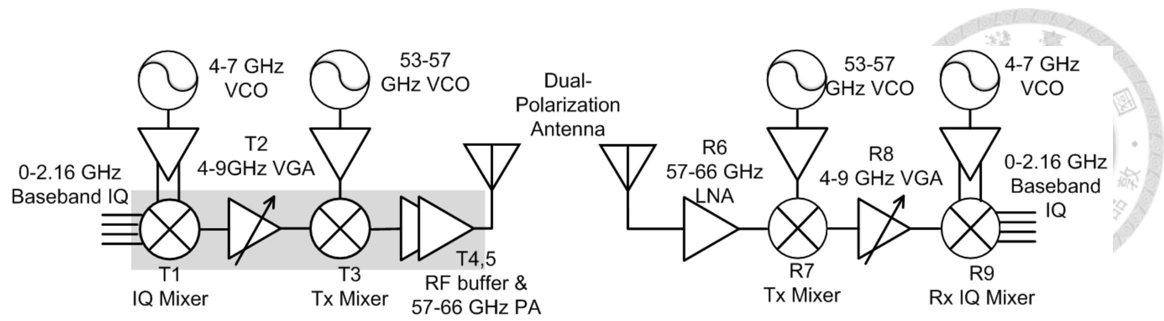


Fig. 4.1. Transceiver architecture of the National Network Communication Program.

4.2 Transmitter Architecture

The transceiver is composed of eight identical structures shown in Fig. 4.1. A pair of transceiver shares a dual-polarization antenna, fully utilizing four V-band unlicensed bands on different polarization to achieve eight channels high speed parallel communication. Super heterodyne topology is used as the transceiver architecture. Baseband signal first convert to intermediate frequency (IF), and then converting to V-band RF frequency. Fig. 4.2 shows the frequency planning of baseband, intermediate, and RF frequency. This architecture can greatly enhance the ability of channel selectivity compared to traditional heterodyne architecture.

The transmitter chain is made of an IO mixer, IF variable-gain amplifier (VGA), heterodyne mixer, RF buffer amplifier, and RF power amplifier. The output power of transmitter is set at 15 dBm based on 1 meter free-space loss of 68 dB and data rate requirement. Gain of each component is estimated by other published circuits using 65-nm CMOS. Fig. 4.3 shows the link budget of each component of transmitter chain. Fig. 4.4 shows other requirement of each component. Linear output power is set larger than planned output power to ensure linear operation.

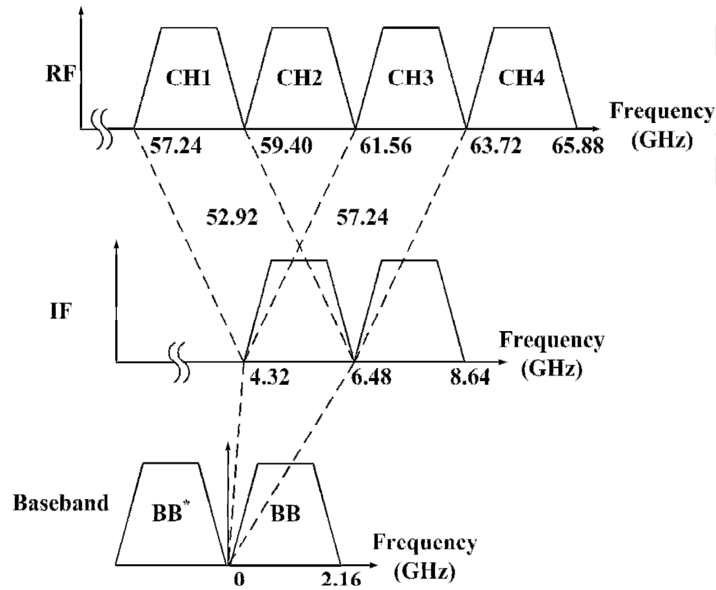


Fig. 4.2. Frequency planning and spectrum utilization.

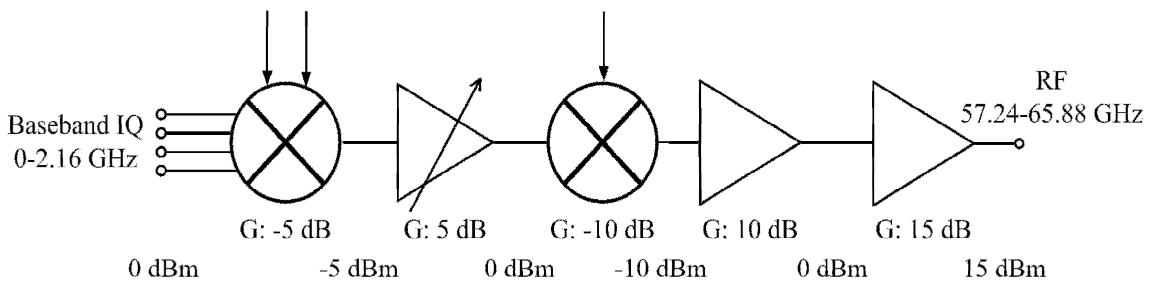


Fig. 4.3. The gain budget of the V-band transmitter.

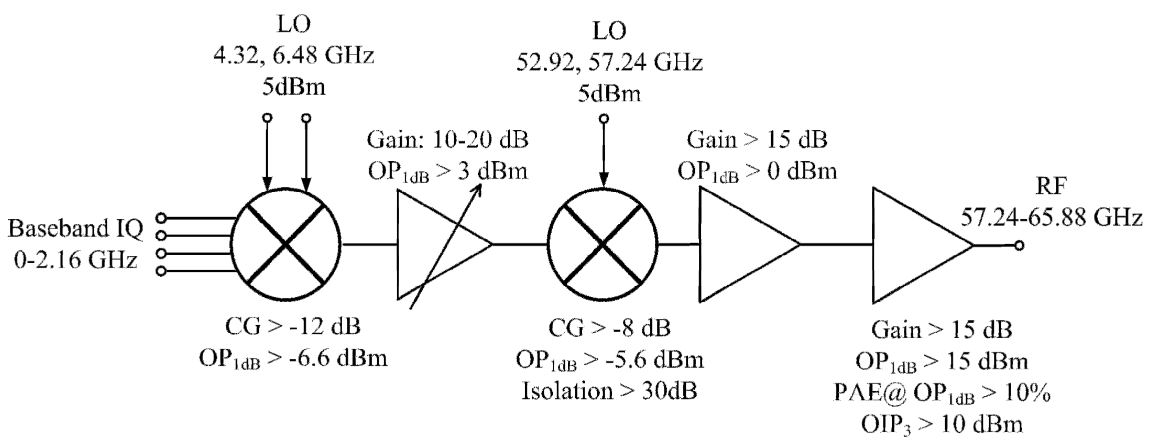


Fig. 4.4. Specification of the building block in V-band transmitter.

4.3 Description of Circuit Components

All circuit components are designed and fabricated using 65-nm CMOS process provided by TSMC foundry service [33]. All the EM simulation on capacitors, inductors, bypass circuits, and matching circuits are simulated by Sonnet EM solver [16]. The overall circuit including transistors and passive components are combined in Advanced Design System (ADS) [34]. The flip-chip component, dual-polarization antenna are simulated using the High Frequency Structure Simulator (HFSS) [35].

4.3.1 First Stage Mixer and Variable Gain Amplifier

Fig. 4.5 shows the layout of first stage mixer and variable gain amplifier with chip size of 1.1×0.95 mm^2. The first stage IQ mixer and variable gain amplifier are contributed by Mr. Po-Hang Chiang and Mrs. Li-Yin Tseng, respectively. Circuit schematic of IQ mixer is shown in Fig. 4.6. LO signal first passes polyphase filter to generate quaduature signal. The IQ IF signal is then mixed with quadrature signal in two gilbert cells. This topology gains the advantage of improvement on RF image signal rejection.

The schematic of VGA is shown Fig. 4.7. It consists of two stages common source topology. Matching circuit and dc feed is realized by capacitors and inductors. To stabilize the circuit, source degeneration inductors and RC feedback are added. Attenuation cell is realized by M_2 and M_3, which is controlled by V_{tune}. In high gain mode operation V_{tune} is set to 0 V, so M_2 and M_3 are turned off and made no influence to RF signal. Increasing V_{tune} provides a path short to ground, and thus attenuates the RF signal. The detail of design consideration and measurement result can be found in [36].

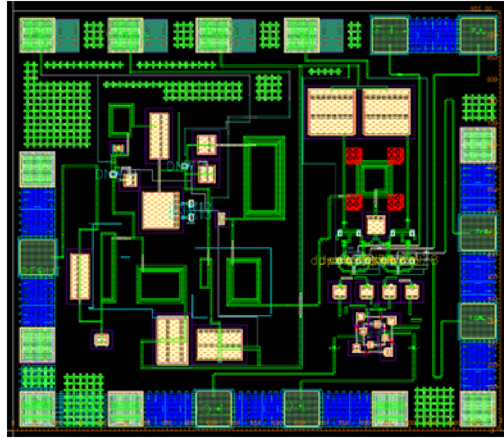


Fig. 4.5. Layout of IQ mixer (right) and variable gain amplifier (left). Chip size is 1.1 × 0.95 mm^2.

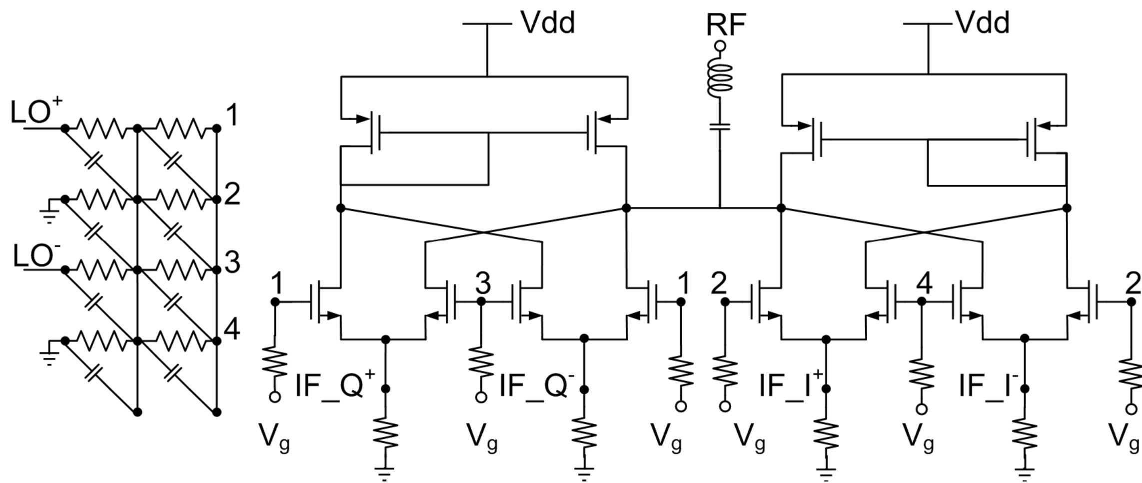


Fig. 4.6. Schematic of the IQ mixer.

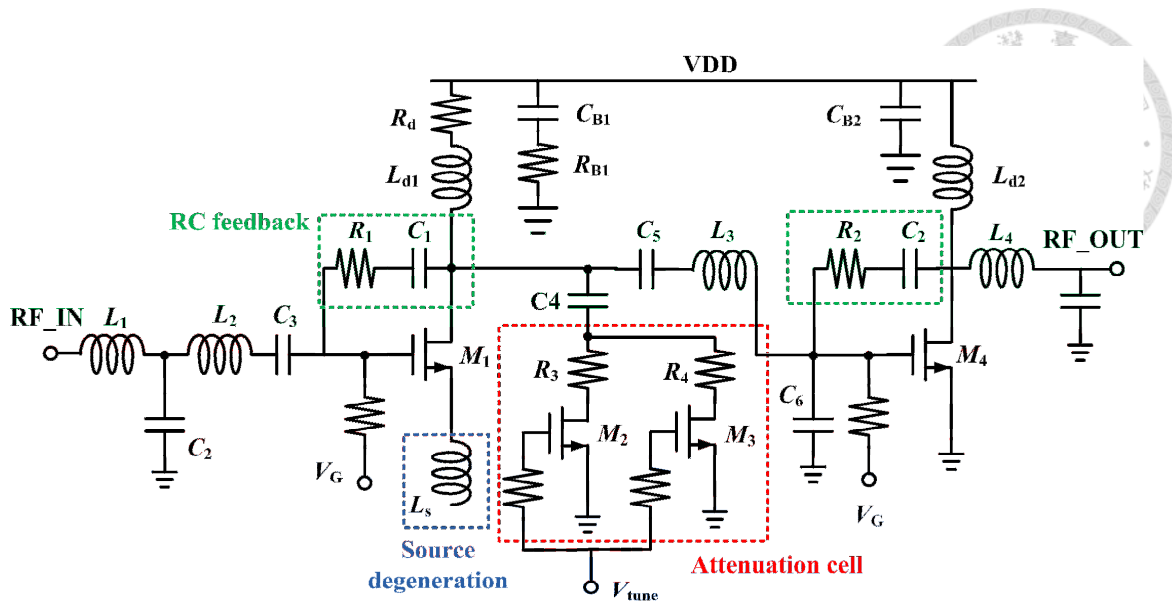


Fig. 4.7. Schematic of the variable gain amplifier.

The mixer-VGA is measured under IF frequency at 1 GHz with IF power -7 dBm. With 4.32 GHz LO frequency, the measured result of mixer-VGA shows conversion gain of near 8 dB at 10 dBm LO power. Measured result is 5 dB larger than simulated result as shown in Fig. 4.8. The conversion gain versus IF power is measured under IF frequency, LO frequency, LO power at 1 GHz, 4.32 GHz, 5 dBm, respectively. It is found measured conversion gain is also about 5 dB larger than simulated result. The measurement result is shown in Fig. 4.9.

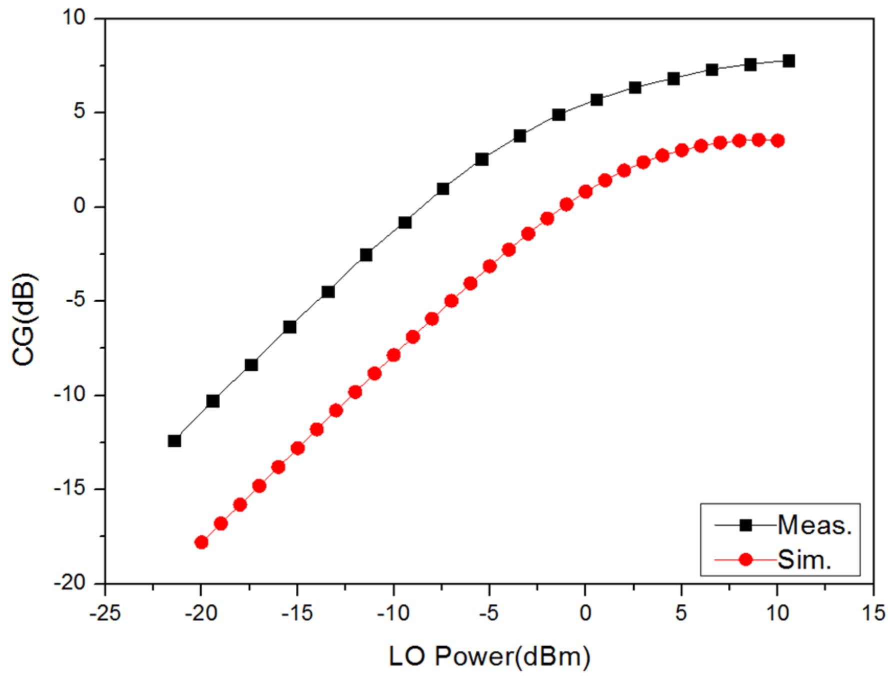


Fig. 4.8. Measured conversion gain of chip mixer-VGA versus LO power. The IF frequency, IF power, LO frequency are 1 GHz, -7 dBm, 4.32 GHz, respectively.

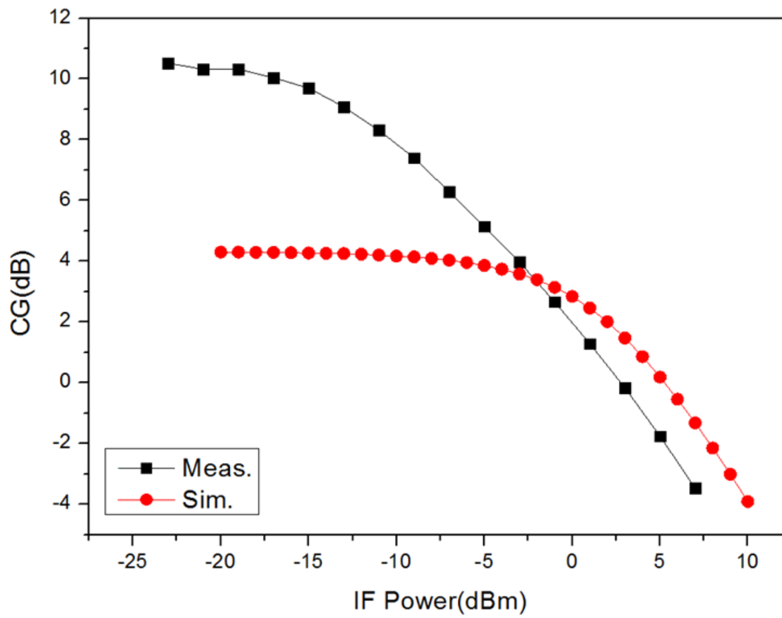


Fig. 4.9. Measured conversion gain of chip mixer-VGA versus IF power. The IF frequency, LO frequency, LO power are 1 GHz, 4.32 GHz, 5 dBm, respectively.

4.3.2 Second Stage Mixer, Buffer Amplifier, and Power Amplifier

The second chip contains second stage mixer, V-band buffer amplifier and V-band power amplifier. The layout of the second chip is shown in Fig. 4.10 with chip size of 1.92×0.92 mm^2. The second stage mixer and power amplifier are contributed by Professor Kun-You Lin and his students Yao-Chia Yang and Guan-Wei Chen. The buffer amplifier is contributed by Yuan-Hung Hsiao.

Fig. 4.11-4.13 show the schematic of proposed mixer, buffer amplifier and power amplifier. The modified Gilbert-cell topology [37] is adopted in this mixer. The mixer is measured by on-wafer probing and bonding wire to feed dc. The detail of measurement results can be found in [38].

The buffer amplifier consists of conventional three stages common source topology. Fig. 4.14 presents the simulated and measured *S*-parameters of the buffer amplifier. It shows small signal gain over 18 dB across V-band. The saturated power is 6 dBm with linear outpour power 2 dBm.

The power amplifier consists of two stages of cascode devices, allowing higher voltage swing compare to common source device. Two diode-connected MOS are the adaptive bias circuits. Since the performance of the adaptive bias in this power amplifier has not yet been verified, the adaptive bias circuit is not used in this measurement. To achieve high output power, two way direct combine is used at output stage. Fig. 4.15 shows the simulated and measured small signal gain of the power amplifier.

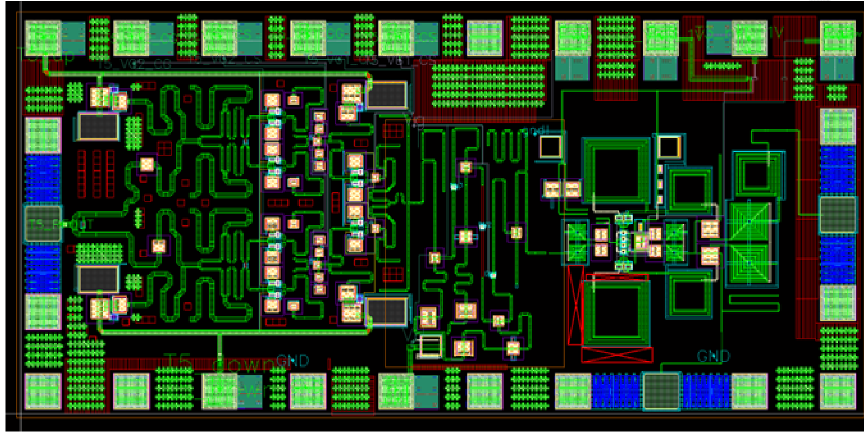


Fig. 4.10. Layout of 2nd stage mixer (right), buffer amplifier (middle), and power amplifier (left) with the size of $1.92 \times 0.92\ mm^2$.

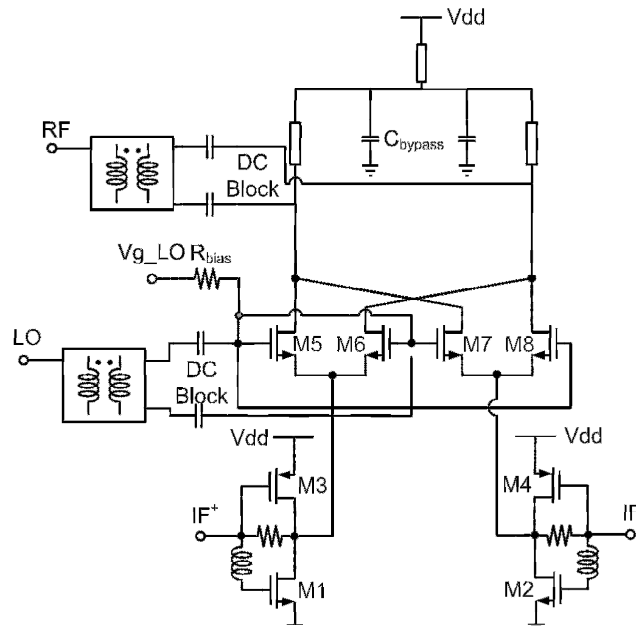


Fig. 4.11. Schematic of the V-band up-conversion mixer.

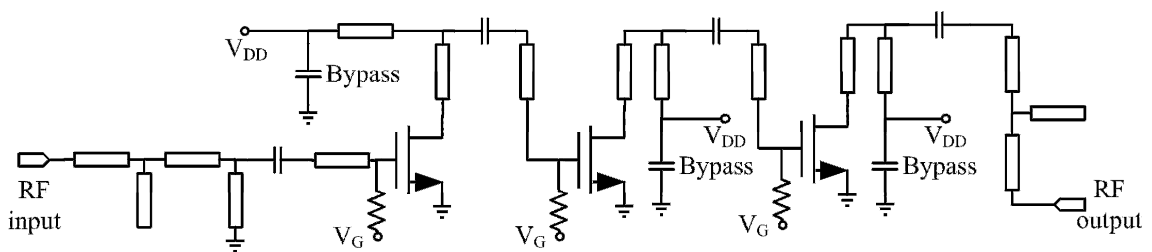


Fig. 4.12. Schematic of the buffer amplifier.

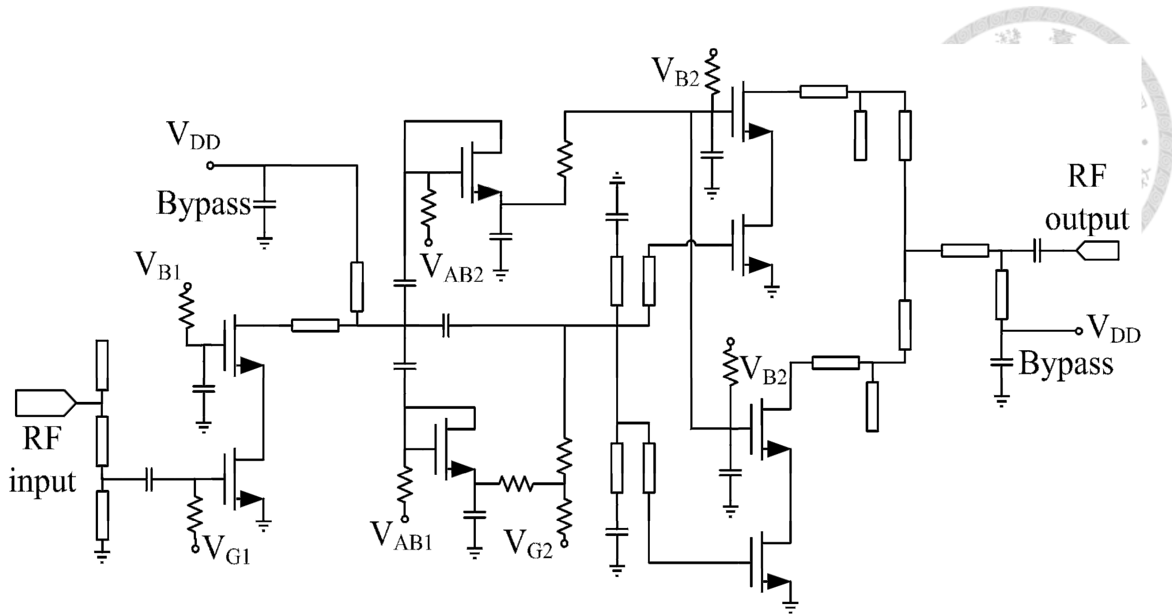


Fig. 4.13. Schematic of the power amplifier.

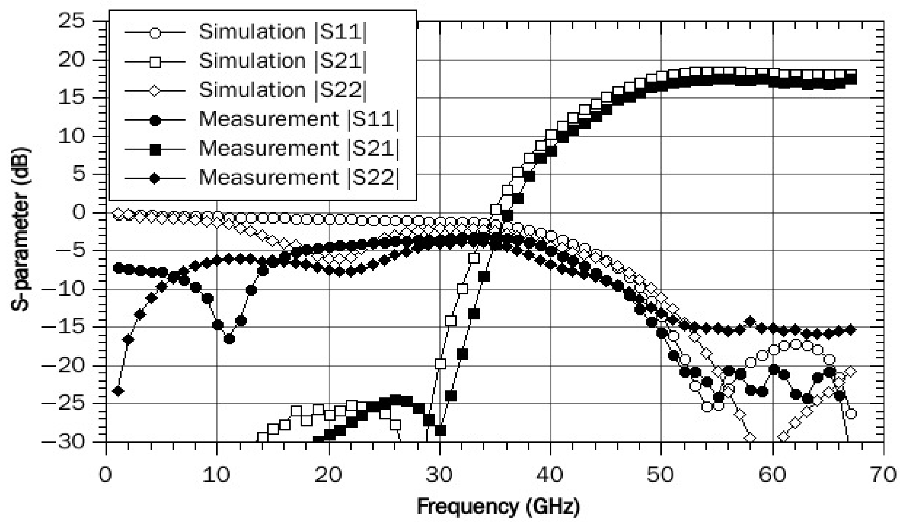


Fig. 4.14. Simulated and measured *S*-parameters of the buffer amplifier.

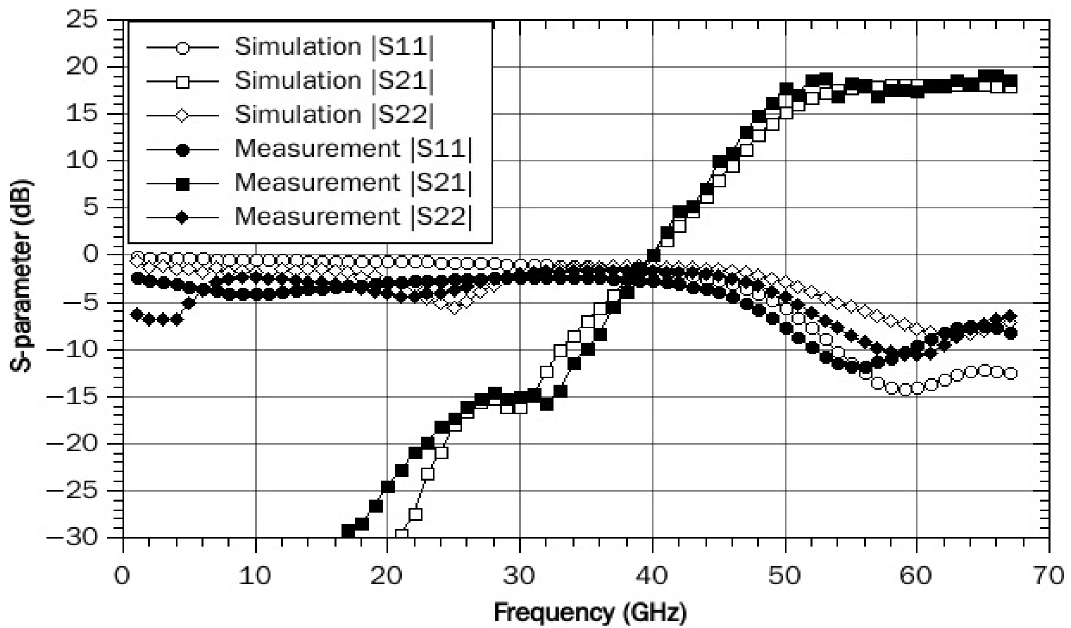


Fig. 4.15. Simulated and measured *S*-parameters of the power amplifier.

The chip is measured by on-wafer probing with wire bonding for dc supply. The LO signal is set to 52.92 GHz and 57.24 GHz with 5 dBm input power. The simulated and measured results of two LO signals are shown in Fig. 4.16-4.17. The measured conversion gain is a little lower than simulation; however it is not critical to the system performance. The conversion gain versus RF frequency is shown in Fig. 4.18.

Fig. 4.19 shows the large signal performance of the chip, mostly dominated by the power amplifier performance. The saturation power is 15 dBm with 1-dB compression point (OP_{1dB}) near 7 dBm. Detail about measurement setup and measurement results can also be found in [38].

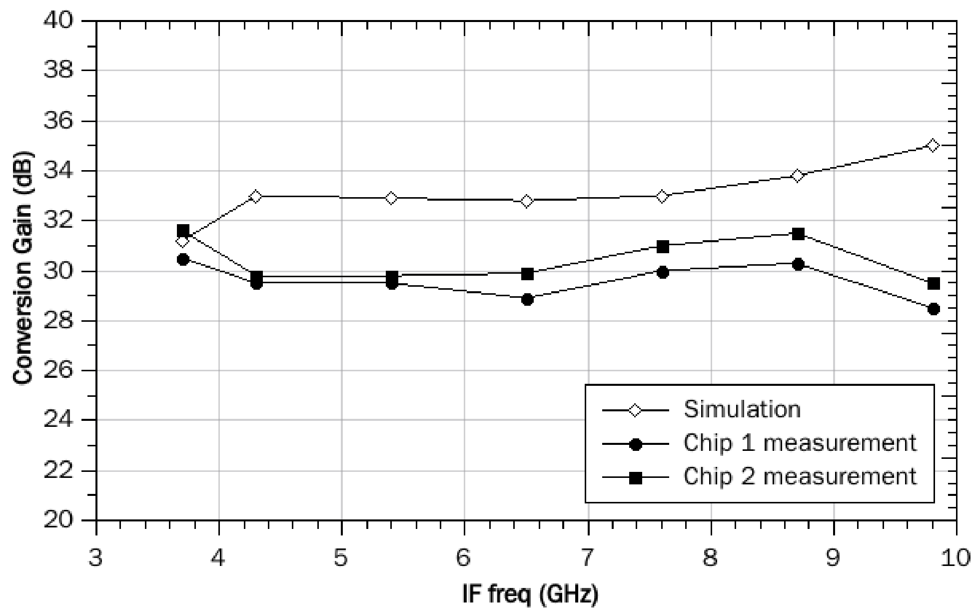


Fig. 4.16. Measured and simulated conversion gain versus IF frequency, with LO power 5 dBm at 52.92 GHz. The simulation and measurement data are taken from [38].

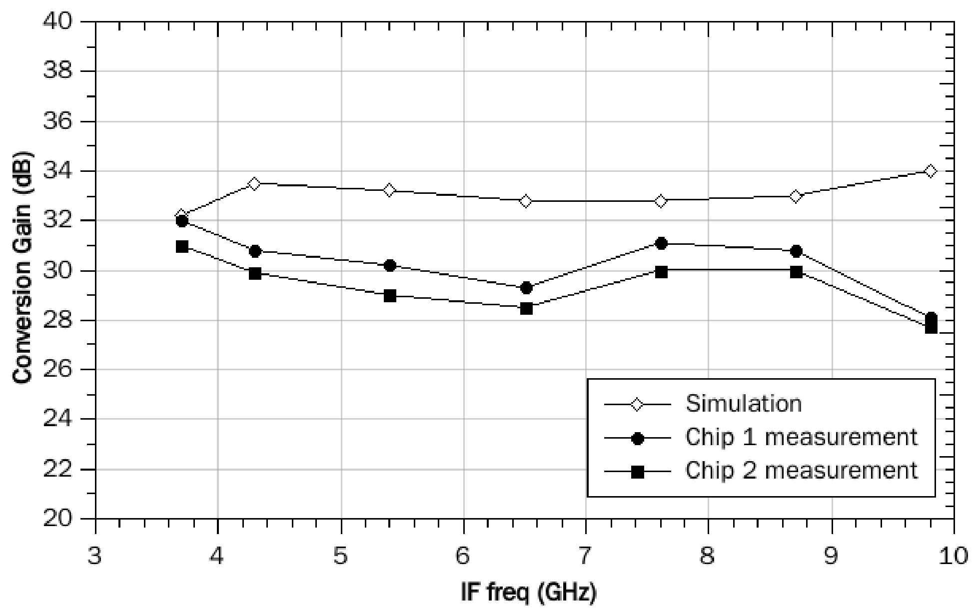


Fig. 4.17. Measured and simulated conversion gain versus IF frequency, with LO power 5 dBm at 57.24GHz. The simulation and measurement data are taken from [38].

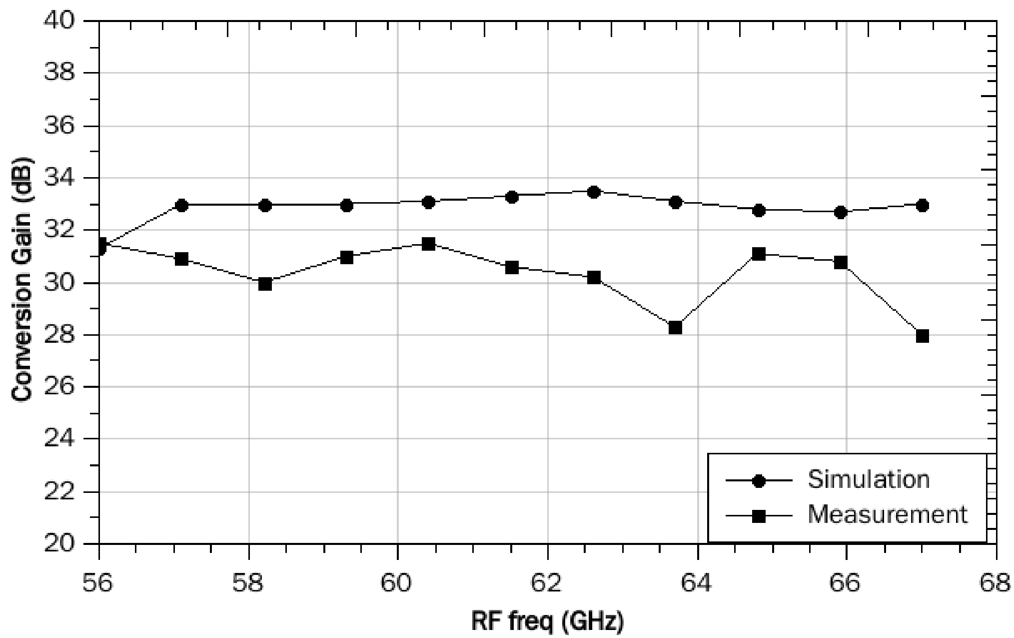


Fig. 4.18. Measured and simulated conversion gain versus RF output frequency. The simulation and measurement data are taken from [38].

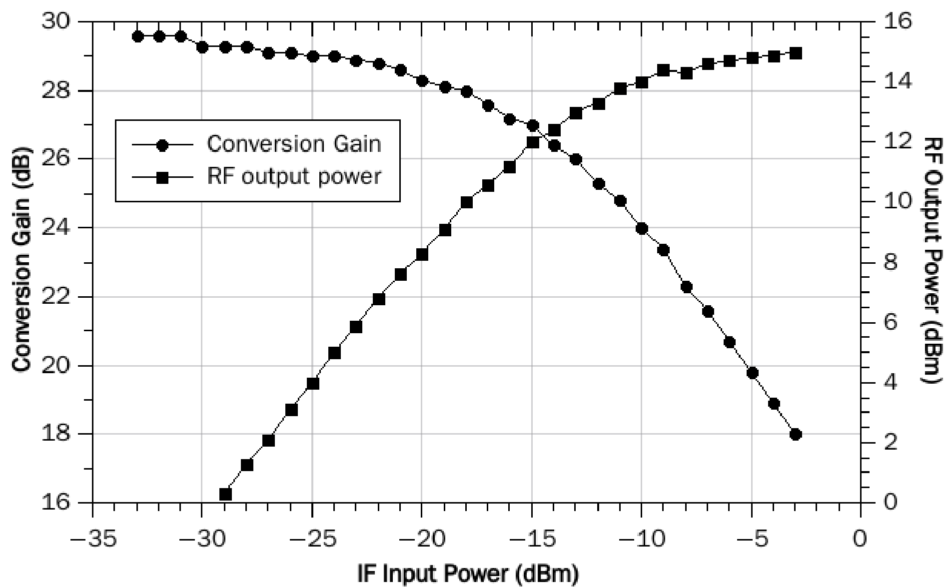


Fig. 4.19. Measured large-signal performance with IF input signal at 4.32 GHz and 5 dBm LO signal at 52.92 GHz. The simulation and measurement data are taken from [38].

4.4 Description of Low Temperature Co-Fired Ceramic (LTCC) Package and Antenna

There are various packaging processes that developed to realize passive component like antenna, power divider, inductor, etc. These passive components can integrate with multiple chips through flip-chip into single package. Such mature industrial high frequency packaging process includes low temperature co-fired ceramic package (LTCC) [39], high temperature co-fired ceramic package (HTCC) [40], and glass integrated passive device (GIPD) [41].

In this program, low temperature co-fired ceramic is chosen to be the solution of high frequency system packaging. The high temperature processes of HTCC restrict some highly conductive metal like silver, copper to be used. Because of that, LTCC shows better electrical conductivity, allowing thinner metal line and smaller packaging size than HTCC. Unlike the GIPD, LTCC technology provides high dielectric constant substrate, which makes it easier to realize a smaller size antenna on packaging. Furthermore, the high integration characteristic of LTCC meets the requirement of package size minimization in this program.

4.4.1 Description of Low Temperature Co-Fired Ceramic (LTCC) Package

The design of LTCC packaging is contributed by the Professor Ruey-Beei Wu, Porfessor Hsin-Chia Lu, and Dr. Tze-Min Shen. Each LTCC packaging contains a pair of TXs. The LTCC module is fabricated by DT Microcircuits Corporation. The through

via transition, and flip-chip compensation is simulated using the full-wave high-frequency structure simulator (HFSS) [35].

The monolithic microwave integrated circuits (MMIC) are connected to LTCC through flip-chip connection. The dc bias line, antenna, signal connect can be put densely into a single packaging. Table 4.1 shows the layers and their function of the DT LTCC process, which provides 11 metal layers for the interconnection. To reduce the voltage drop over metal line, drain bias are biased through one metal layer rather than metal wiring in one layer. Fig. 4.20 shows the layout of the transmitter LTCC module with size 9.6×9.6 mm^2. Additional metal pads are added with dc line, allowing 2 mm × 1 mm capacitors integrated in LTCC module.

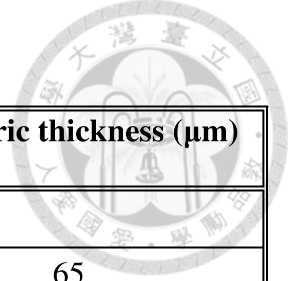


Table 4.1. Layers of the DT LTCC Process

Layer Index	**Layer Name**	**Function**	**Dielectric thickness (μm)**
01	M1	RF signal	
02	VIA1	Via 1	65
03	M2	RF Ground Plane	
04	VIA2	Via 2	50
05	M3	Power Line	
06	VIA3	Via 3	50
07	M4	Power Line	
08	VIA4	Via 4	50
09	M5	Antenna Ground Plane	
10	VIA5	Via 5	100
11	M6	0.7V Gate Power Line	
12	VIA6	Via 6	150
13	M7	NULL	
14	VIA7	Via 7	150
15	M8	1V Drain Power Line	
16	VIA8	Via 8	100
17	M9	NULL	
18	VIA9	Via 9	100
19	M10	2V Drain Power Line	
20	VIA10	Via 10	100
21	M11	NULL	

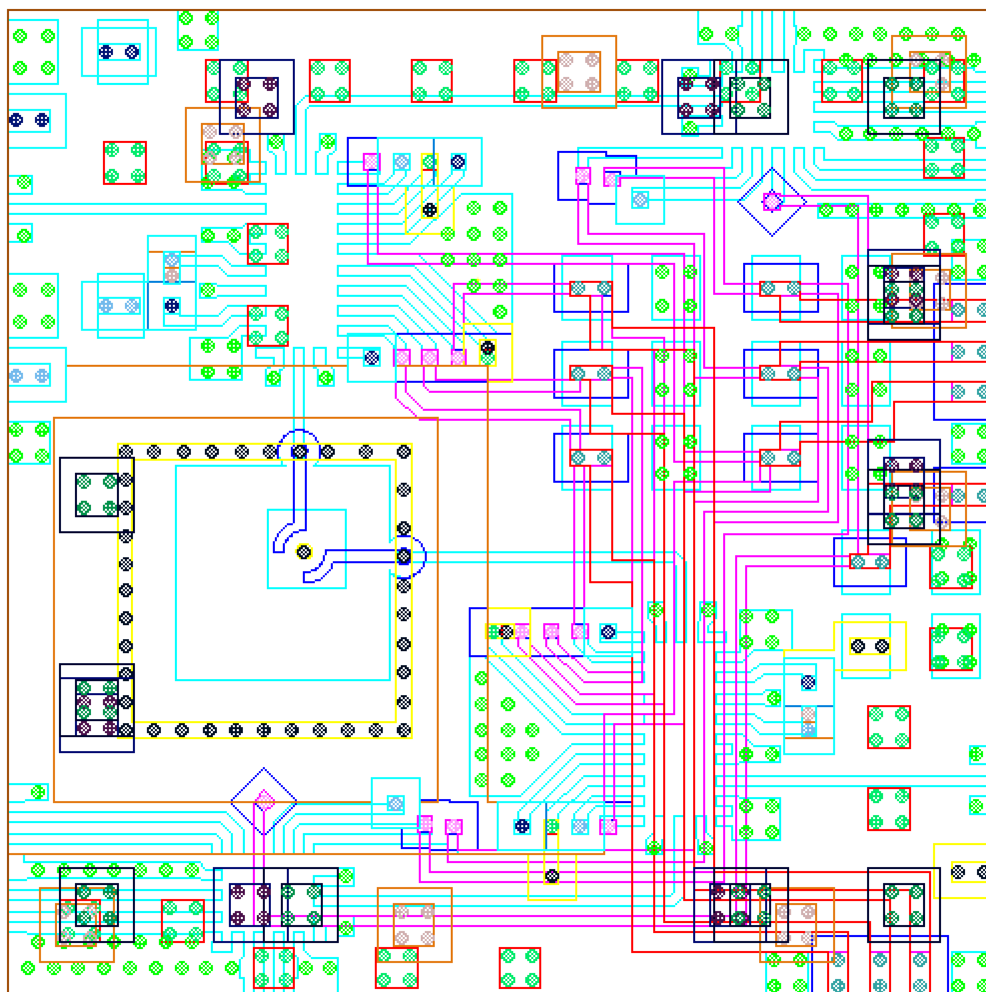


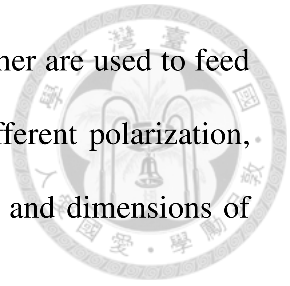
Fig. 4.20. LTCC layout of the transmitter module with size of 9.6 × 9.6 mm^2.

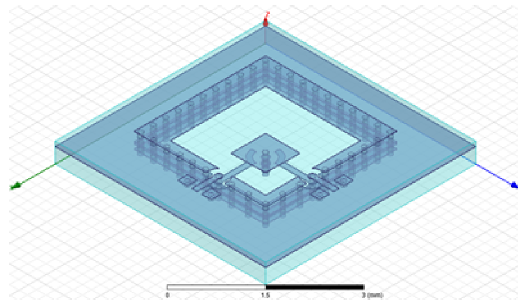
4.4.2 Description of Low Temperature Co-Fired Ceramic (LTCC) Antenna

The design of LTCC antenna is contributed by the Professor Yi-Cheng Lin, and his student Yao-Wen Hsu [42]. The top view and cross view of the antenna are shown in Fig. 4.21.

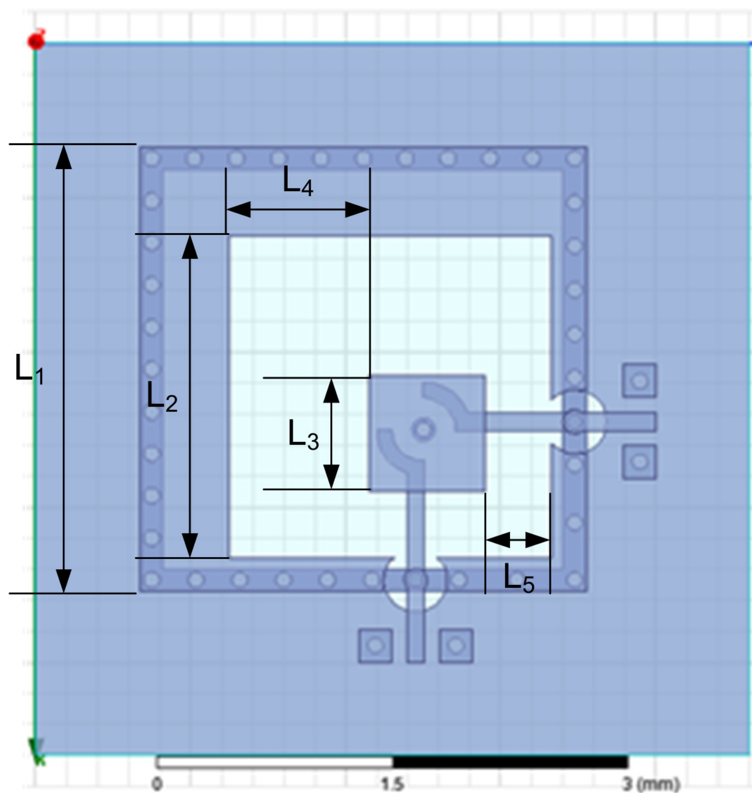
According to the project, four channels will transmit with four patch antennas with different size. The antenna demonstrates here is the antenna of the first channel from

57.5GHz to 59.5GHz. Two microstrip lines perpendicular to each other are used to feed in the patch antenna. The signals fed in from two ports emit in different polarization, allowing two signals transmit in same time. The design parameters and dimensions of the dual-polarization antenna is shown in Table 4.2.





(a)



(b)

Fig. 4.21. (a) cross view. (b) top view of the dual-polarization patch antenna.

Table 4.2. Design parameters and dimensions of the dual-polarization antenna.

Parameters	Dimensions (mm)
L1	2.875
L2	2.075
L3	0.75
L4	0.9
L5	0.425

4.5 Experiment results

4.5.1 Measurement Setup

The chips mentioned in section 4.3 are flip-chip connected to LTCC package module in section 4.4. The photograph is shown in Fig. 4.22, and the cross view is shown in Fig. 4.23. The baseband and two LO signals can be provided by RF probing on pad of LTCC. RF signals are transmitted through interconnected microstrip lines to the dual-polarization antenna.

The LTCC module is then mounted on PCB, with bond wire to dc pad on LTCC pads to supply bias. The chips and antenna are designed and implemented on the same side on LTCC module, allowing the module directly attaches on printed circuit board (PCB). Additional off-chip bypass capacitors are added on PCB bias line. The photo of PCB is shown in Fig. 4.24. DC bias condition of measurement is listed in Table 4.3. The

power consumption of component T2 is high, which may be considered to improve in future system design.

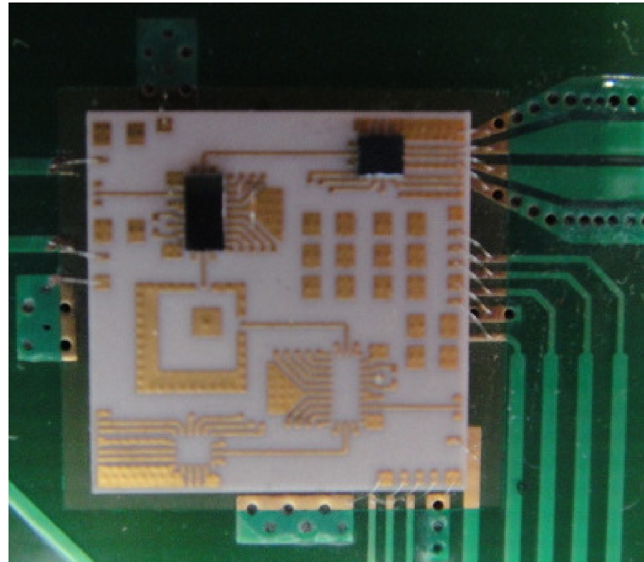


Fig. 4.22. Photograph of the LTCC with chips mounted on it, with size of 9.6 × 9.6 mm^2.

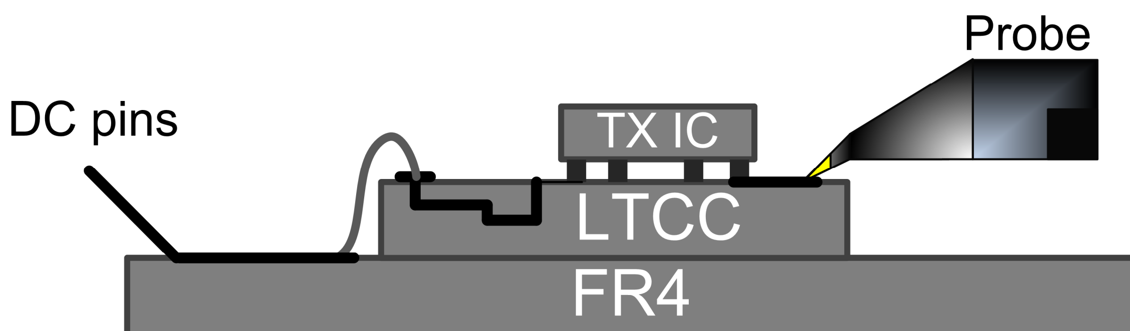


Fig. 4.23. Cross view of measurement setup of the Tx module.

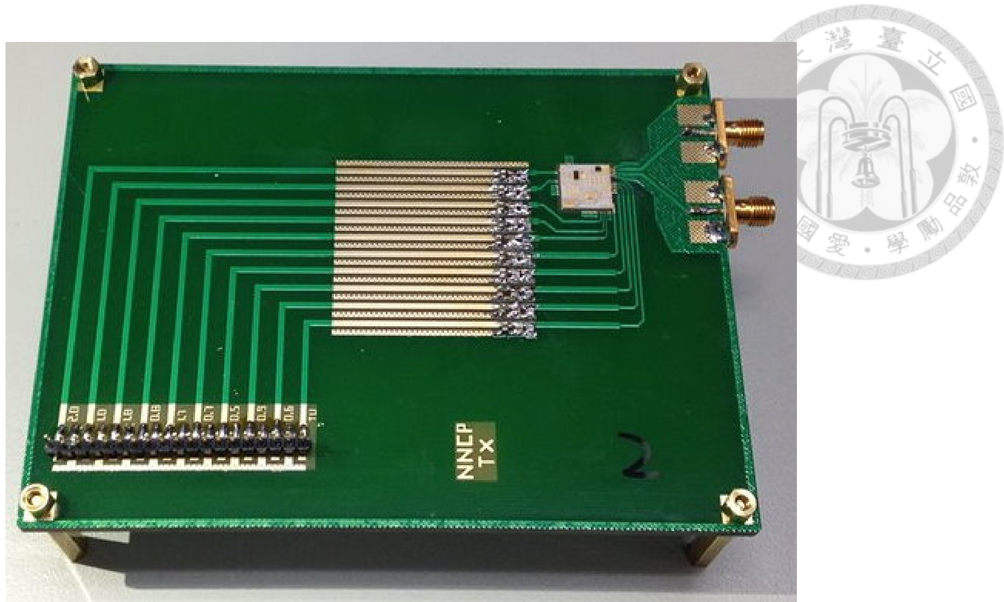


Fig. 4.24. Photograph of the PCB for dc supplying, bypass, and IF SMA connector with size of 13.5 × 10 cm^2.

Table 4.3. DC condition of the Tx component

Component	Drain Current (mA)	DC consumption (mW)
T1 IQ Mixer	5	5
T2 VGA	69	69
T3 Second Stage Mixer	7	7
T4 Buffer Amplifier	44	44
T5 Power Amplifier	297	594

When measuring conversion gain, baseband signal is generated by Tektronix 7122B arbitrary waveform generator, and fed through SMA connectors. For simplicity, we only feed I^+ and I^- channels and leave Q^+ and Q^- channels open. This only affects the performance of the image rejection but not the conversion gain. The LO signals are generated by Agilent E8267D vector signal generator and Agilent E8257D analog signal

generator. First LO signal passes through a balun realized by rat-race coupler on FR4 PCB as shown in Fig. 4.25 to generate differential LO signals, and then fed into LTCC with GSSG probe. Second LO signal is directly fed by GSG probing. The RF signal output is measured by Agilent E4448A spectrum analyzer with Agilent 11974V preselected millimeter mixer.

The measurement setup for transmitter large signal performance is similar to the above setting, except that baseband signal is replaced by Agilent E8247C signal generator and feeds only I^+ channel. The measurement setup of conversion gain and large signal performance are shown in Fig. 4.26-4.27.

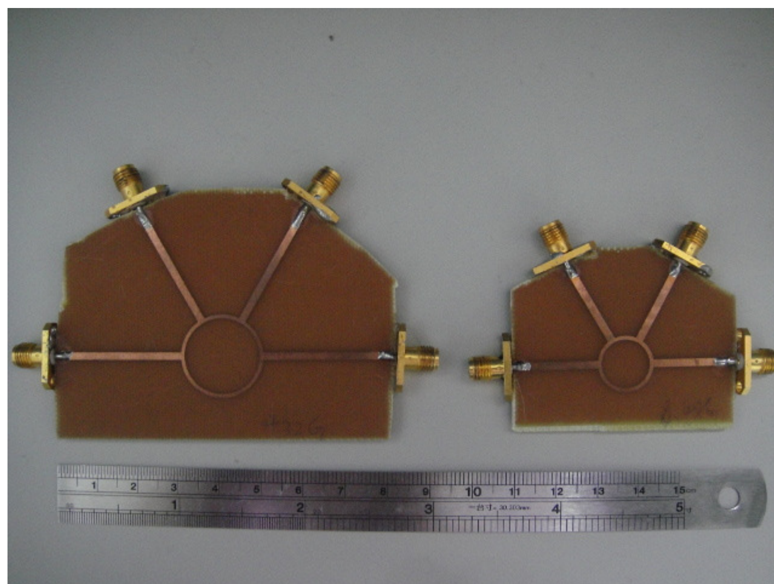


Fig. 4.25. Photograph of the PCB baluns of 4.32 GHz (left) and 6.48 GHz (right).

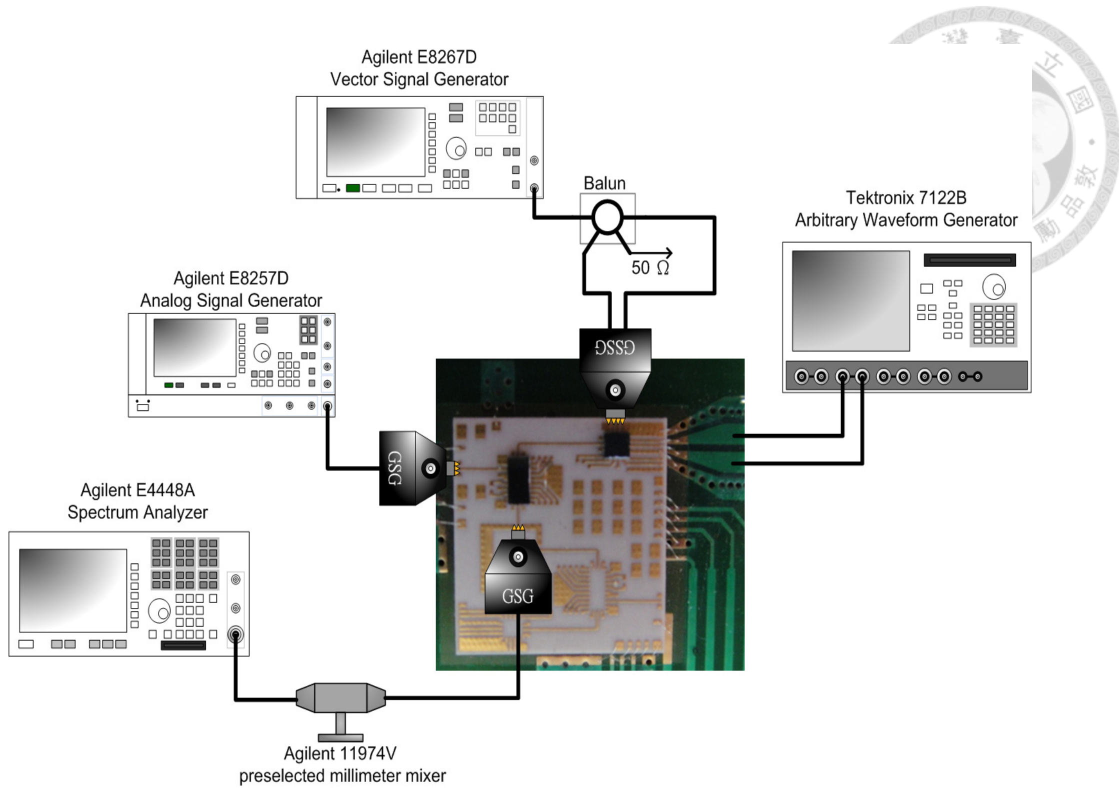


Fig. 4.26. The TX measurement environment setup of conversion gain.

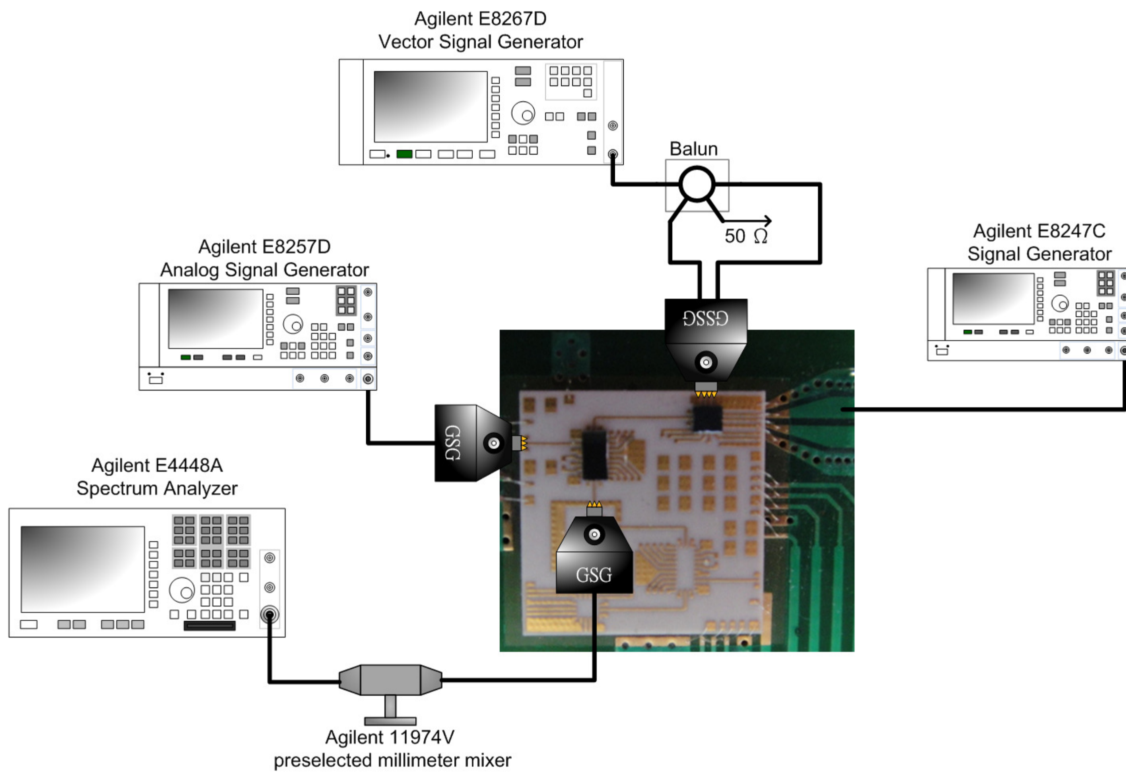


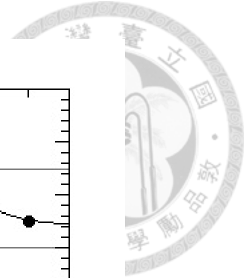
Fig. 4.27. The TX measurement environment setup of large-signal response.

4.5.2 Measurement Results

Fig. 4.28 presents the measured transmitter conversion gain over one channel (57.24 GHz - 59.40 GHz). The measured transmitter gain is about 28 ± 1 dB over IF frequency from 0 to 2.16 GHz. The simulated result is about 2 dB higher than measured result. The first LO power is set at 5 dBm and second LO power is set at 7 dBm. Considering the loss of cables and balun, the power feeds into transmitter are both near 0 dBm.

Fig. 4.29 - 4.32 illustrate the USB large signal performance at various IF frequency, from 100 MHz, 200 MHz, 500 MHz to 1 GHz. The power of two LO signals are set equal to value mention above. The transmitter shows saturation power of 7 dBm and OP_{1dB} larger than 3 dBm.

There are two issues in this measurement. Firstly, the IF input of first mixer is not quaduature signal. The image terms in first chip output will reduce the saturated power of the transmitter. Secondly, measured by probing on antenna may cause additional loss. However, the measurement proves the functionality of the transmitter system integration in LTCC module.



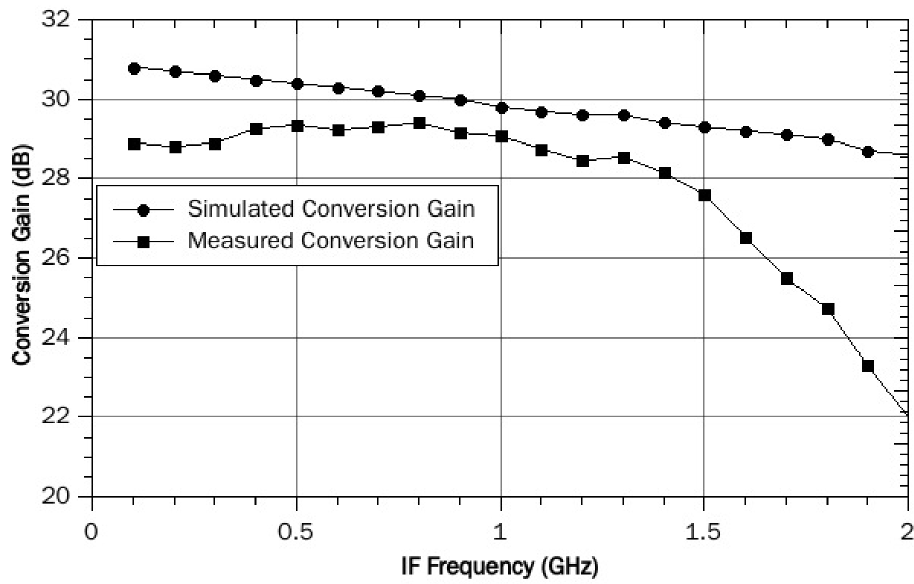


Fig. 4.28. Measured conversion gain versus IF frequency. The first LO and second LO are at 4.32 GHz, 53 GHz, respectively.

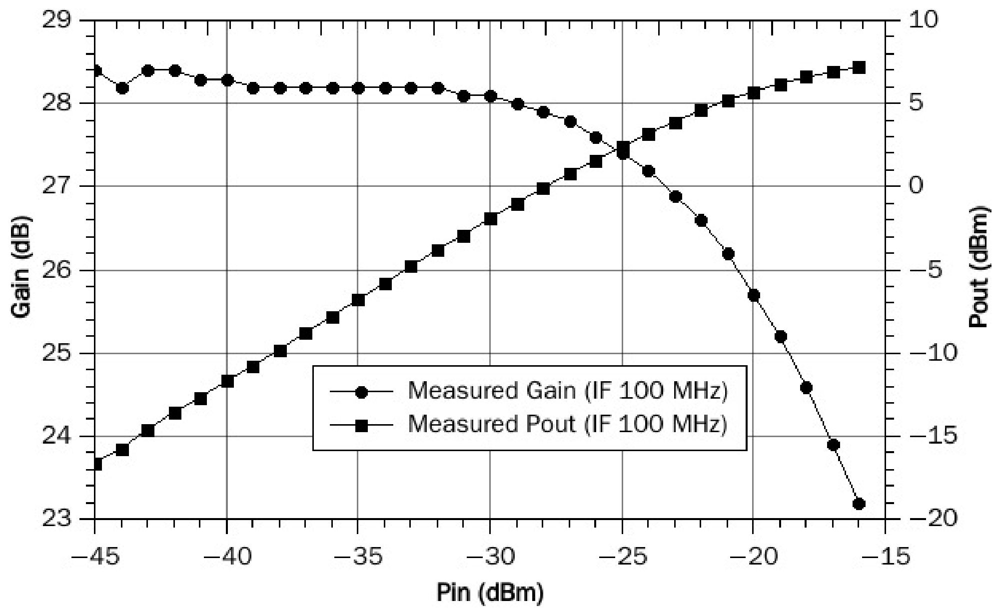


Fig. 4.29. Measured conversion gain, output power versus input power of the transmitter. The first LO, second LO, and IF are at 4.32 GHz, 53 GHz, and 100 MHz, respectively.

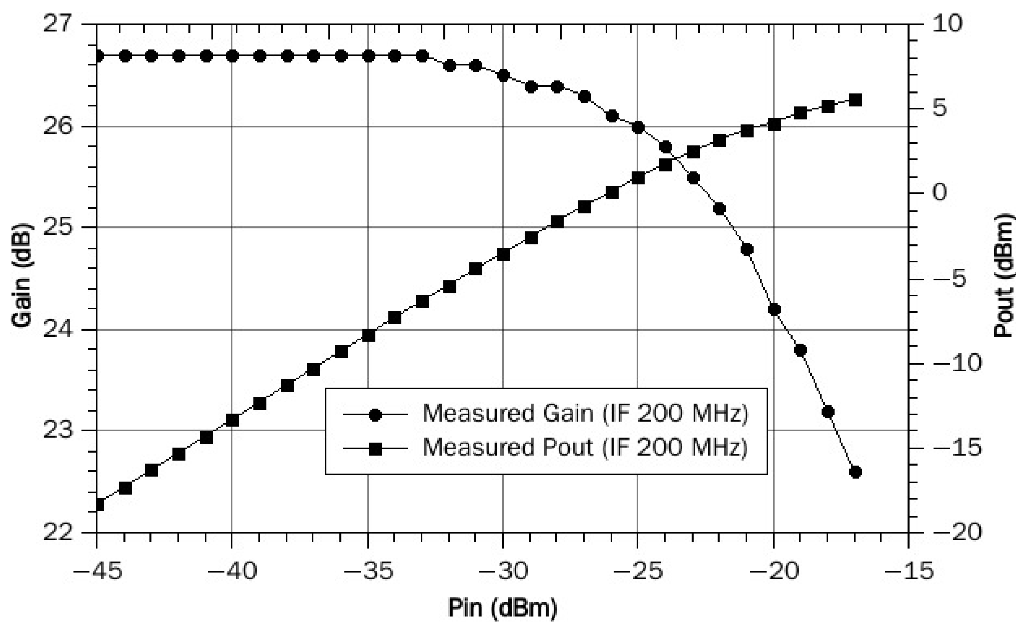


Fig. 4.30. Measured conversion gain, output power versus input power of the transmitter. The first LO, second LO, and IF are at 4.32 GHz, 53 GHz, and 200 MHz, respectively.

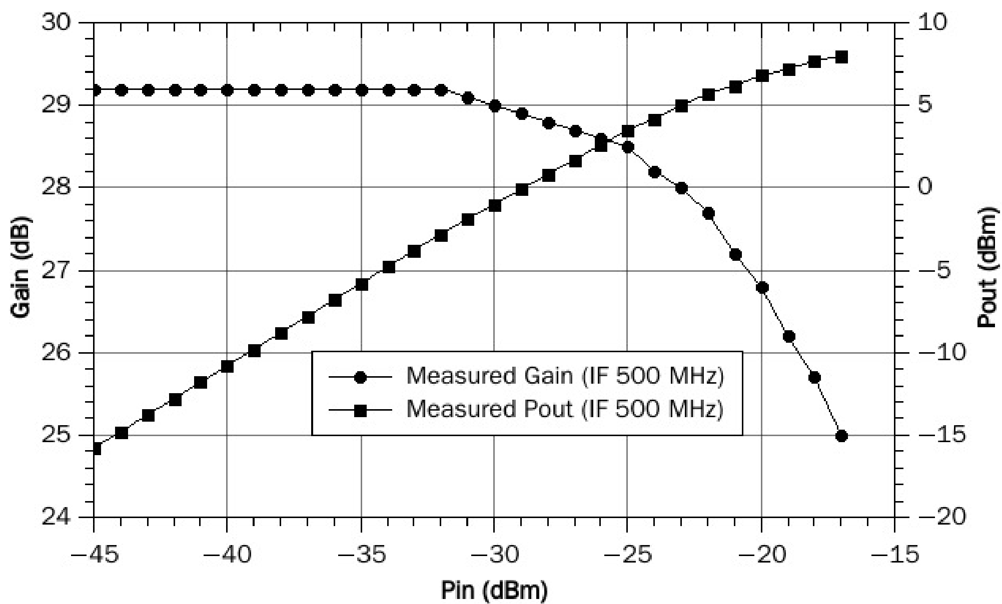


Fig. 4.31. Measured conversion gain, output power versus input power of the transmitter. The first LO, second LO, and IF are at 4.32 GHz, 53 GHz, and 500 MHz, respectively.

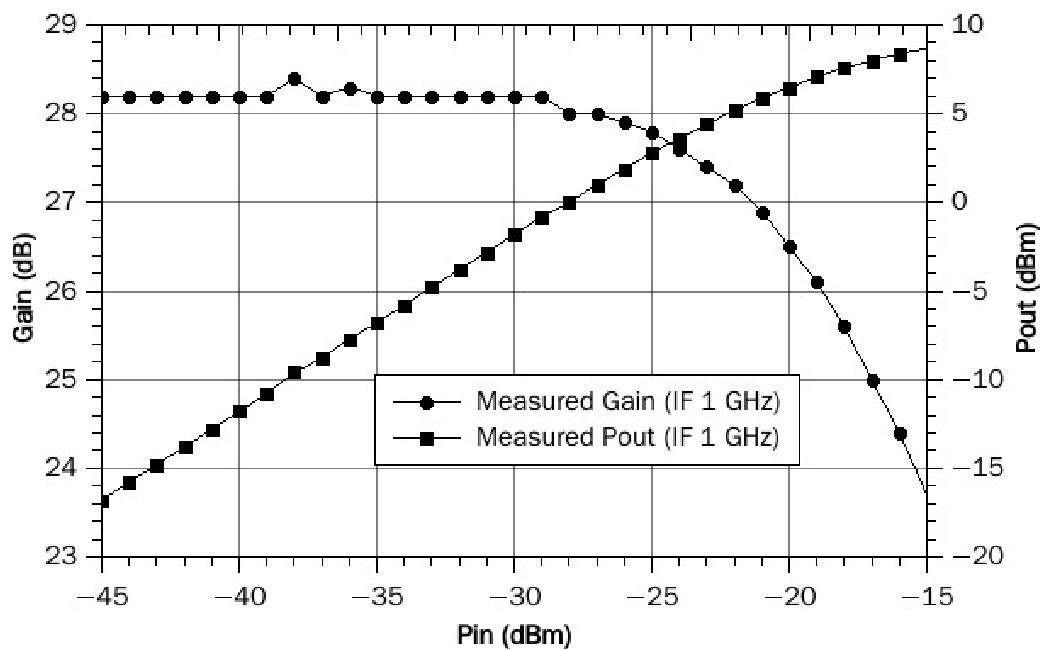


Fig. 4.32. Measured conversion gain, output power versus input power of the transmitter. The first LO, second LO, and IF are at 4.32 GHz, 53 GHz, and 1 GHz, respectively.

4.6 Summary

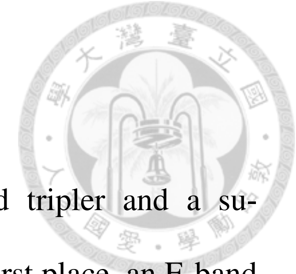
In this chapter, a V-band super-heterodyne transmitter fully integrated in a single package is presented. The V-band super-heterodyne transmitter shows conversion gain 28 ± 1 dB and saturation power larger than 7 dBm across one channel, from 57.24 GHz to 59.40 GHz. The linear output power is over 3 dBm. Table 4.4 summaries the performance of the proposed V-band transmitter and previous published works. The proposed V-band transmitter shows highest small signal gain compared to other works in CMOS technology. Though at the cost of large power consumption, the transmitter also shows high saturated output power and linear output power.

Table 4.4. Comparison of this work and other published V-band transmitter

Ref	**[44]**	**[45]**	**[46]**	**[47]**	**[48]**	**This Work**
Topology	Super heterodyne	Direct conversion + LO multiplier	Direct conversion	heterodyne with sub-harmonic mixer	Super Heterodyne	Super Heterodyne
System Package	Integrated circuit	Integrated circuit	Integrated circuit	Integrated circuit	Integrated circuit	Package in LTCC
Process	0.12-μm SiGe BiCMOS	0.15-μm GaAs mHEMT	0.13-μm CMOS	90-nm CMOS	65-nm CMOS	65-nm CMOS
Freq(GHz)	51-65	1.25-2.75 → 54-61	0.5 →57-65	0.1-20→57-62	53-62	0-2.16→57.24-66.56
Gain(dB)	35	5.2	-	13.1	20	28 ± 1
LO Power(dBm)	-	-3	4	-	-	0
OP_{1dB} (dBm)	9-13.5	0	4	-1.3	6	>3
P_{SAT} (dBm)	15	3.7±1.5	5±1.5	4.6	11	>7
Image Rejection (dB)	-	-	-	-	25-28	-
LO Rejection (dB)	>20	-	>27	-	20	
Area (mm^2)	6.5 × 6.75	5.7 × 5	8.4	1.2*	4.06	3.83
Power Consumption (mW)	3800-6400	820	-	113	590	719

*: including frequency synthesizer

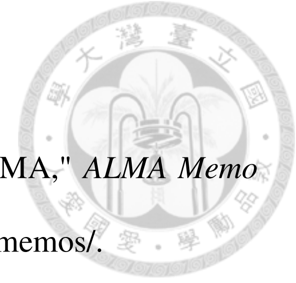
Chapter 5 Conclusions



In this thesis, an E-band low noise amplifier, a broadband tripler and a super-heterodyne transmitter on LTCC package are presented. In the first place, an E-band low noise amplifier using 0.1-μm pHEMT technology is designed, fabricated and measured. This LNA exhibits very high gain from 60 to 77 GHz with relative low power consumption. It shows the potential of pHEMT devices in the radio astronomy and other millimeter wave applications.

Secondly, a W-band tripler fabricated in TSMC advanced 65-nm CMOS process is designed and measured. Using the differential topology and compact transformer matching, the tripler achieves wide working range, good conversion gain and low power consumption. The measured results majorly agree with the simulation except unexpectedly better harmonic rejection, which makes this tripler more competitive to other published multiplier.

Facing the demand in short range communication, a V-band super-heterodyne transmitter is demonstrated. The whole system is packaged in LTCC package, along with the dc bias network and antenna. This work exhibits the advantages of LTCC in high frequency application. The transmitter shows highest gain performance compared to other reported V-band transmitter realized in CMOS technology.



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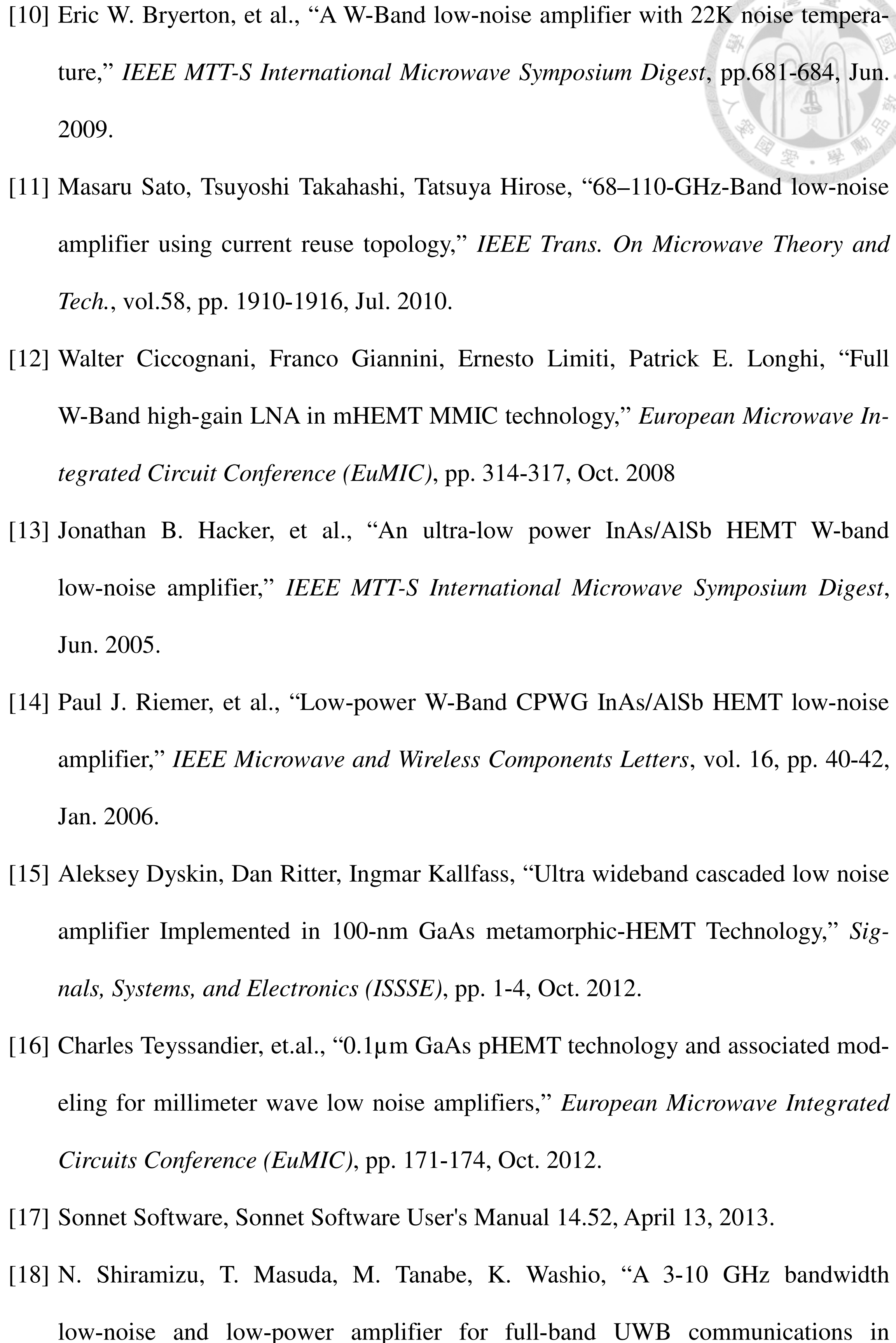

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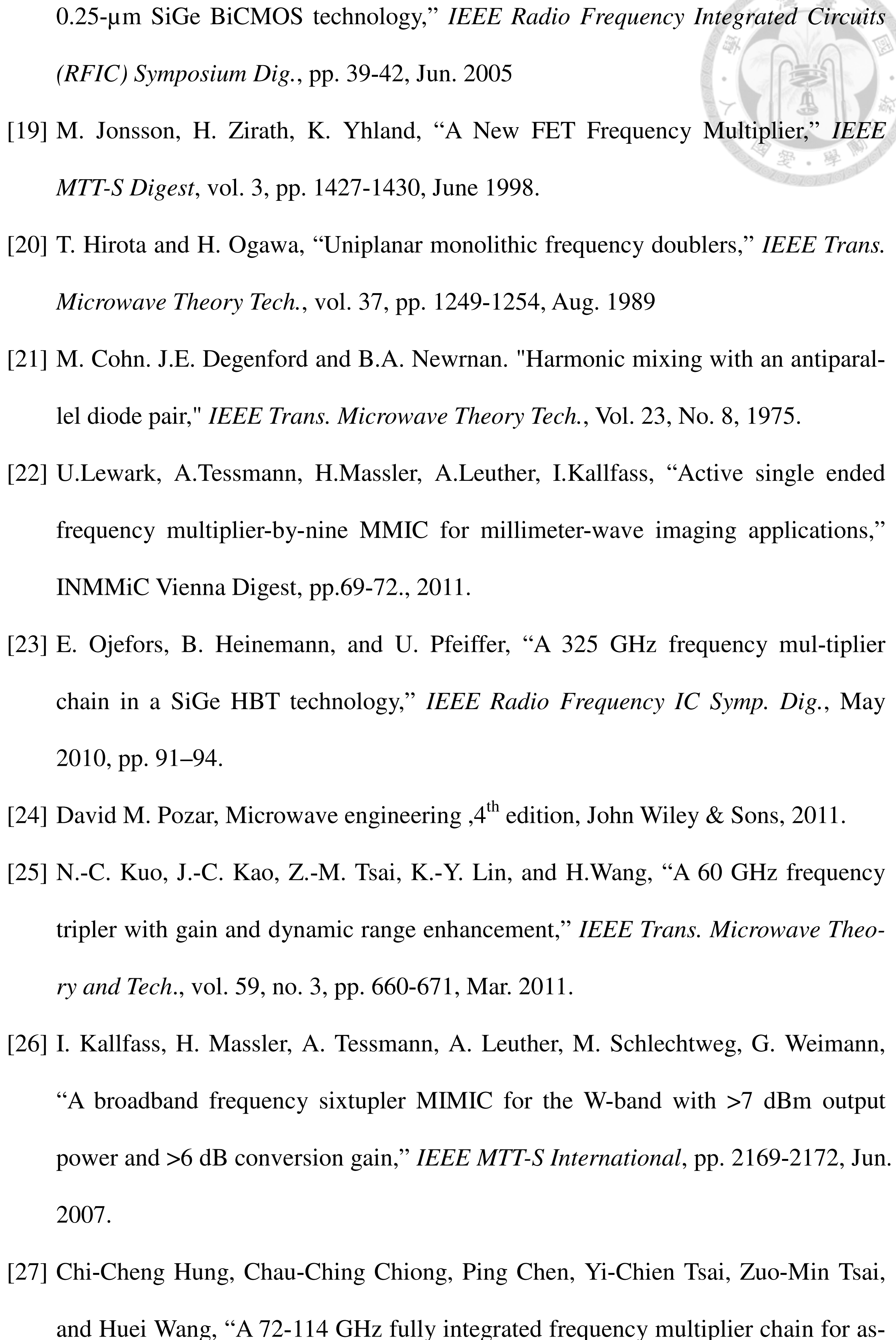

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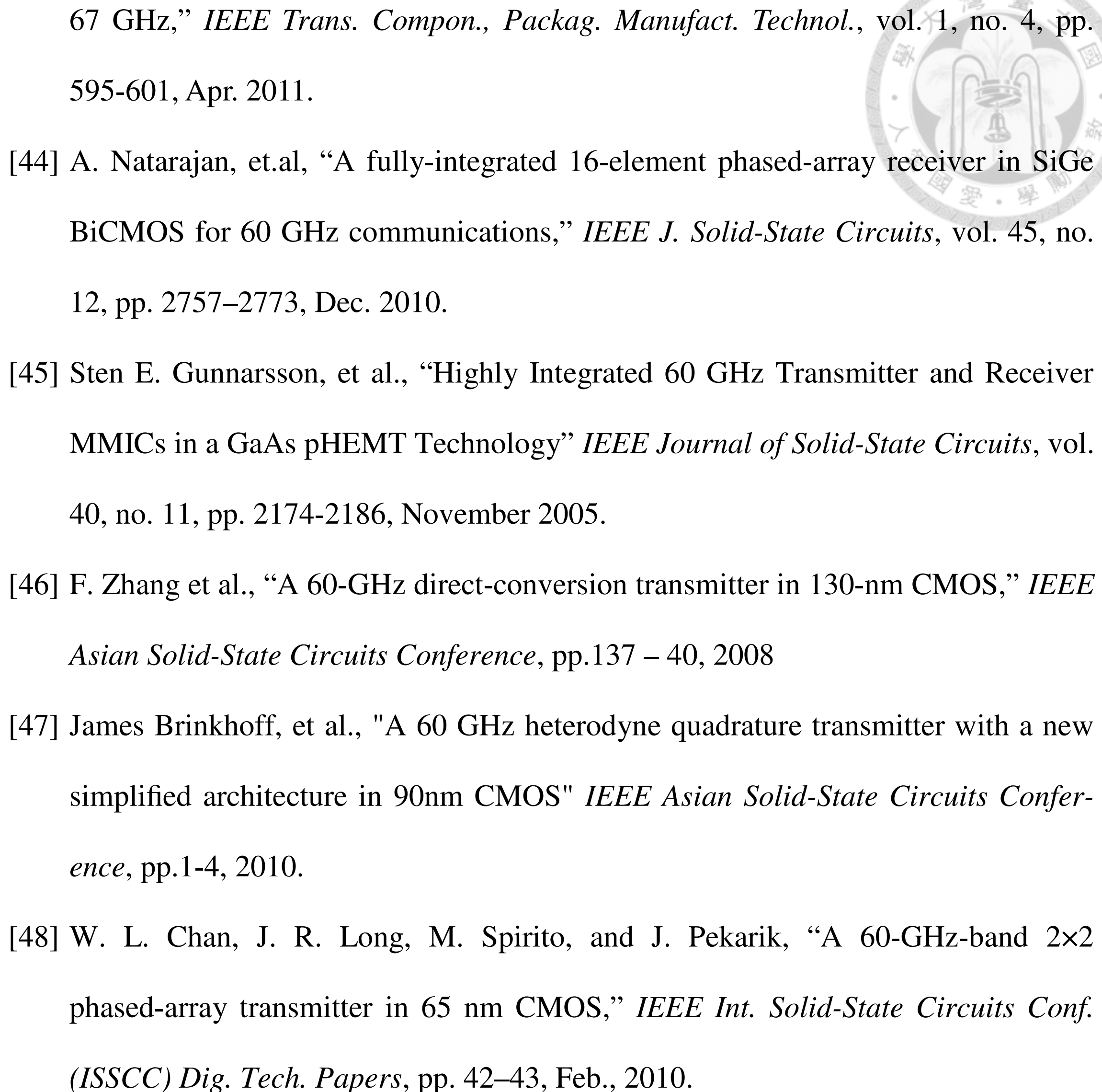

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