國立臺灣大學理學院物理學研究所

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Master Thesis

SuperKEKB 試運轉期間之 BEAST2 偵測器中的 BGO 背景與光度監測器的設計、製造與測試

Design, Production and Testing of the BGO Background/Luminosity Monitor in BEAST2 for SuperKEKB Commissioning

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口試委員會審定書

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本論文係陳昱潭君（R01222034）在國立臺灣大學物理學系、所完成之碩士學位論文，於民國 104 年 07 月 11 日承下列考試委員審查通過及口試及格，特此證明

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_____（簽名）

張寶棣（指導教授）

張敏娟

徐靜戈

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摘要

利用 BGO 閃爍體作為偵測器的 BGO 系統在新升級的 SuperKEKB 加速器的試運轉偵測器 Beast2 中，擔任階段一的背景監控器與階段二的粒子反應亮度監控器。

在階段一，SuperKEKB 加速器初步試運轉，此時雖然沒有碰撞產生，但背景能量會慢慢上升。Beast2 的偵測器有部分會進駐，而我們的 BGO 系統在此階段可藉由能量校準的數據偵測及累加得知即時的背景能量，作為此階段的背景能量監控器。

在階段二，伴隨著高能電子及正子的碰撞，產生許多 Bha-bha 散射。由於動量守恆，在質心座標中，具有「背對背」的特性。藉由測量背對背事件的事件率，BGO 系統可以計算出粒子反應的亮度，作為此階段的亮度監控器。

我的研究主要是讀出板的設計、製造與測試，以及整個系的組裝。在這篇文章中，會特別詳細介紹讀出板從設計到最後的測試結果，以及整個系統運作的數據校準。

Abstract

The BGO system is a detector with BGO crystals. In the SuperKEKB commissioning, which is the accelerator upgraded in these years, BGO system is one of the Beast2 detectors. It will be the background monitor in the phase 1 and the luminosity monitor in the phase 2.

In the phase 1, SuperKEKB starts to work. Although there's no collision, the background energy still rises slowly. Some of the Beast2 detector will be inside the SuperKEKB. The BGO system will sum up to calculate the background energy for monitoring with the important data from the energy calibration.

In the phase 2, there're so many Bha-bha scattering after the collision between high energy electrons and positrons. In the C.M. frame, there's the so-called "back to back" property in the scattering because of the conservation of momentum. By detecting the back to back event and calculating the rate, BGO system can get the luminosity of interaction for monitoring.

My study is focused on the design, production, testing of the readout board and the building up of the whole system. In this thesis, I'll introduce more on the readout board from design to the final test and the calibration for whole system running.

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Chapter 1
Introduction

1.1 BEAST2 for Belle2 in SuperKEKB

SuperKEKB is the accelerator upgrade from KEKB which was the most important equipment in KEK (こうエネルギーかそくきけんきゅうきこう, **K**ou **E**nerugii Kasokuki **K**enkyukikou, High Energy Accelerator Institute in Japan).

KEKB is an electron-positron collider and known as a B-factory for B physics. It uses 8.0Gev electrons and 3.5GeV positrons to collide at the Y(4S)-resonance energy in order to create B and anti-B meson pairs. The Belle detectors are used to detect and record the data.

After CP violation is verified, which is the most important physics target at Belle, KEKB is upgraded to SuperKEKB. Belle, of course, becomes Belle2. The beam energies have been changed. It uses 7.0GeV electron and 4.0GeV positron to produce B and anti-B mesons. The target luminosity becomes $8 \times 10^{35} cm^{-2} s^{-1}$ which is about factor of 40 of the KEKB peak luminosity. This upgrade allows people to study B physics in a more efficient and finer way.

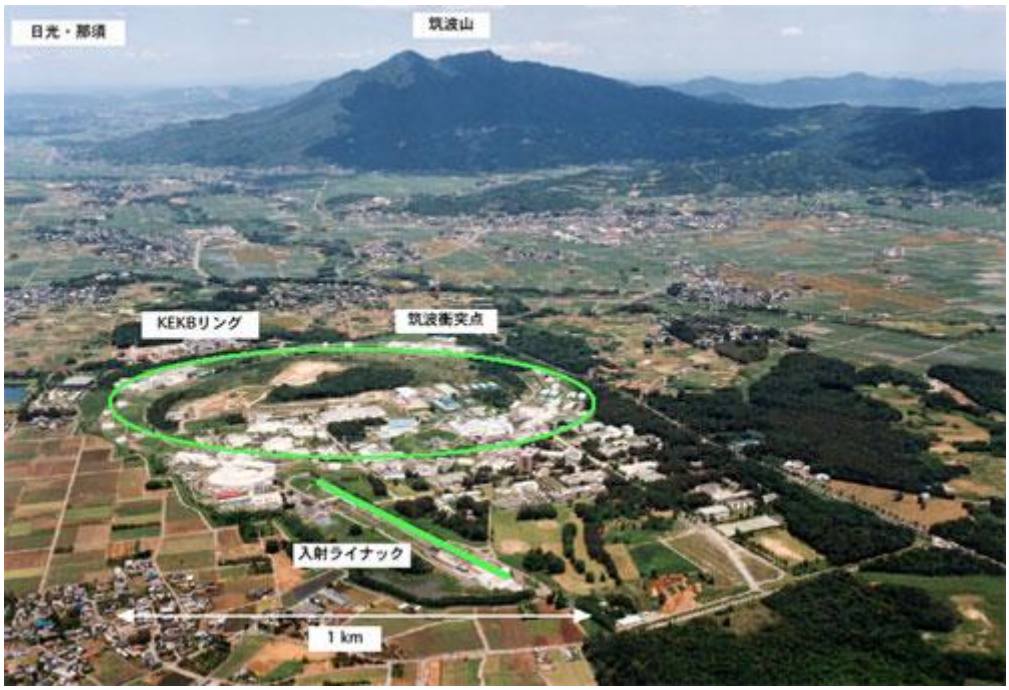


Figure 1-1 KEKB accelerator in Tsukuba City, Japan

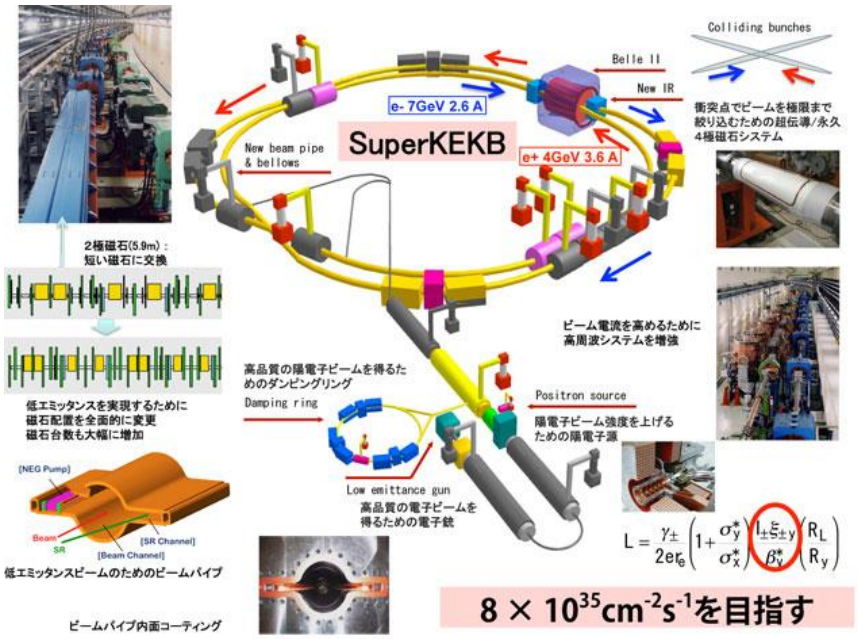


Figure 1-2 Schematic view of SuperKEKB

The BEAST2 in Belle2, as the BEAST in Belle, is a set of experiments with many detectors for SuperKEKB's commissioning. BEAST2 will gather useful information for Belle2. Most importantly, this information can protect Belle2 detector from the unstable operation of SuperKEKB during its early turn-on phase.

1.2 BGO System in BEAST2

There're several phases in BEAST2. The BGO system will be the back ground monitor in phase 1 and the luminosity monitor in phase 2. After phase 2, the BGO system will be removed from the interaction point. However, the data gotten in these two phases will be helpful for Belle2.

In phase 1, the beams will not be focused to make collisions. Hence, there's no Bha-bha scattering and no luminosity. However, the system can still provide important data by detecting the intensity of backgrounds, such as the radiative photons, ionized particles and scattering events caused by interactions between the beam and the environment, and particles in the same bunch. The BGO system can detect the noise energy and acts as a background monitor.

In phase 2, the beams will be focused to make collisions between electrons. With the known cross-section of Bha-bha scatterings, the BGO system can determine the instant luminosity by detecting the back-to-back Bha-bha events.

Chapter 2
BGO System Apparatus

2.1 Whole Architecture

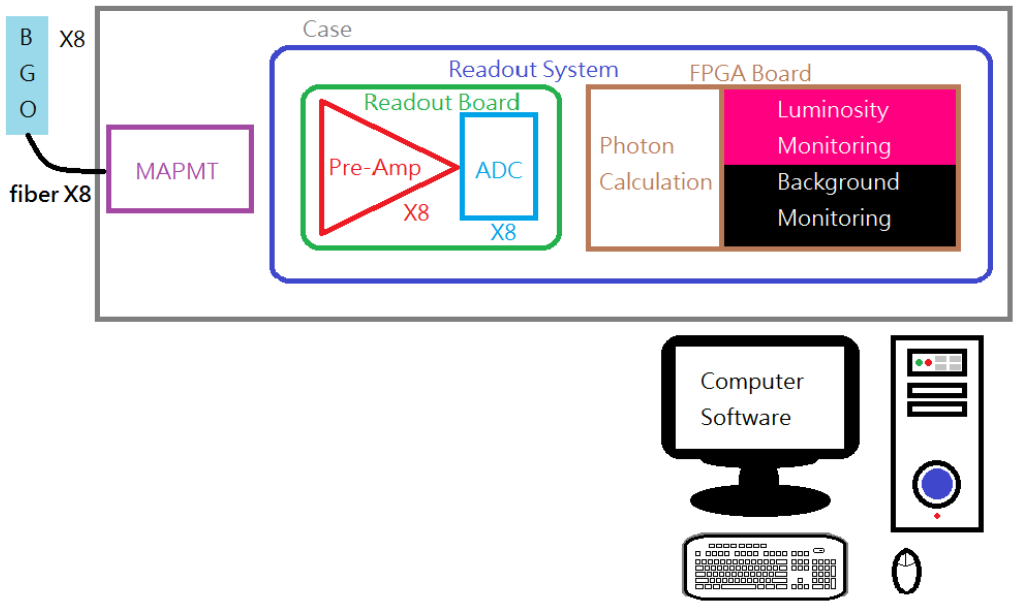


Figure 2-1 BGO system schematic

To monitor the luminosity or the background, we use BGO as the scintillator, MAPMT as the scintillation light detector, and two boards as the readout system. The two boards are a readout board (Pre-Amp and ADC) and a FPGA board.

When a high energy particle hits the BGO, it can excite the scintillator and then release the scintillation light. Some of the light will be seen by the MAPMT through the optical fiber. After that, MAPMT will change the light signal into charges and send the charge signal to the readout board. The Pre-Amp on the board will reshape, amplify, and digitize the signal and then pass it to the FPGA board. We can use different firmware codes to calculate the incident charge or to form coincidence between different input channels, and communicate with computer. Finally, we can use the software in the computer to see the final result such as the luminosity counts or the accumulated background energy.

2.2 BGO Crystals

BGO (Bismuth Germanium Oxide) is a kind of artificial crystal used widely as a scintillator in high energy (particle physics) experiments. The luminescence spectrum of BGO has a maximum at 480nm. The decay time of scintillation light is about 300ns at room temperature.

The BGO will be put in a holder to be fixed in the Beast2 structure. It also helps for the connection with fiber.

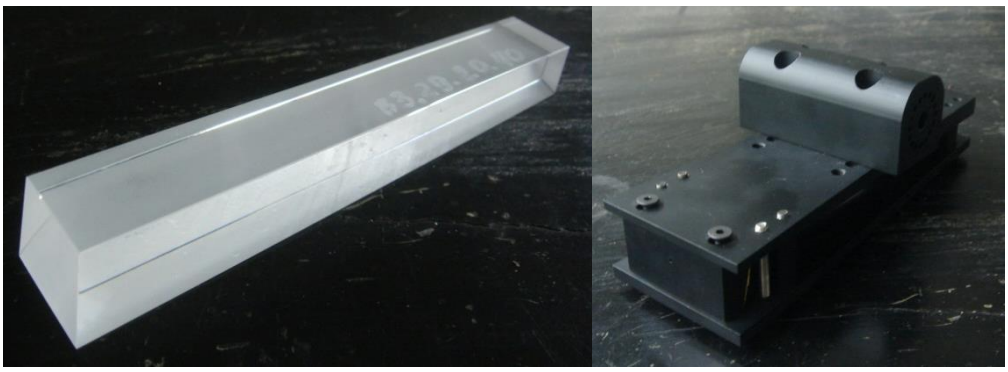


Figure 2-2 BGO crystal and its holder

2.3 Optical Fibers

In BGO system, the scintillator is close to the collision point but the others are far away. We need 37~40 meters long optical fibers to guide the scintillation light to the MAPMT. In our design, we made two bunches of fibers. In each one, there're 6 fibers in a black plastic tube for protection and light tightness. We need only 4 for each bunch. The other 2 are spare ones. For each fiber, one end will be fixed in the BGO holder with silicone and the other will be fixed in the cover of MAPMT.

We choose Eska SK-40 1mm plastic fibers for use. Its refractive index is 1.49 and its numerical aperture (NA) is 0.5. It's a kind of high NA large diameter plastic fiber. Usually, this kind of fibers is used as a photon collector but not an exact communicating media. The decay for 40m fiber is less than 6dB according to the datasheet. Some details will be explained more in chapter 5.

Figure 2-3 Fibers with plastic tube

2.4 MAPMT

MAPMT (Multi Anode Photo Multiplier Tubes) is a multi-channel PMT. We can use it to detect the photons form BGO through fibers and change it into charge signal. We use MAPMT Hamamatsu H7546B (30mm*30mm*50mm) having 64 (8*8) pixels. It can detect even single photon (quantum efficiency ~15% for the BGO emission spectrum). The gain is around$10^5 \sim 10^6$ with a typical 800V high voltage setting. Its spectral response is from 300nm~650nm which matches the BGO scintillation light well.

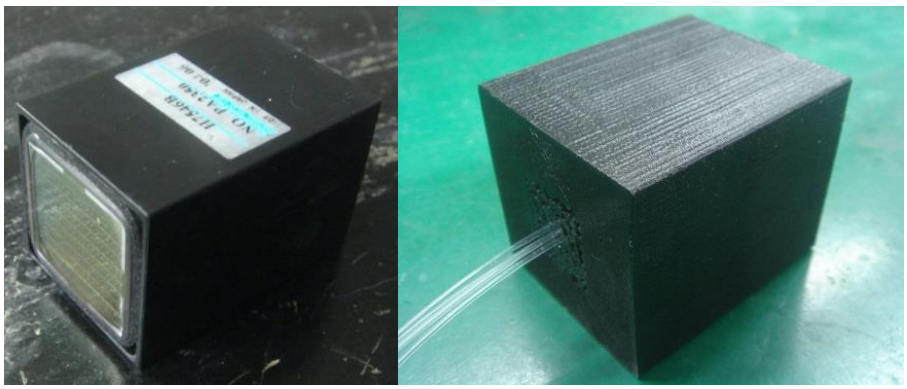


Figure 2-4 MAPMT and its cover

2.5 Readout Board

The final readout board contains 8 channels of Pre-Amp's and ADC's. The most important is the Pre-Amp circuit. For this OP-Amp circuit, the output signal will be an exponential decay pulse due to the discharging nature of the R-C circuit. There're some useful relationships.

$$V_1 = {}^{Q_1}/_{C}\,; V_2 = V_1{}' + {}^{Q_2}/_{C}$$

$$\text{Decay time conatant } \tau = \mathrm{R} \times \mathrm{C}$$

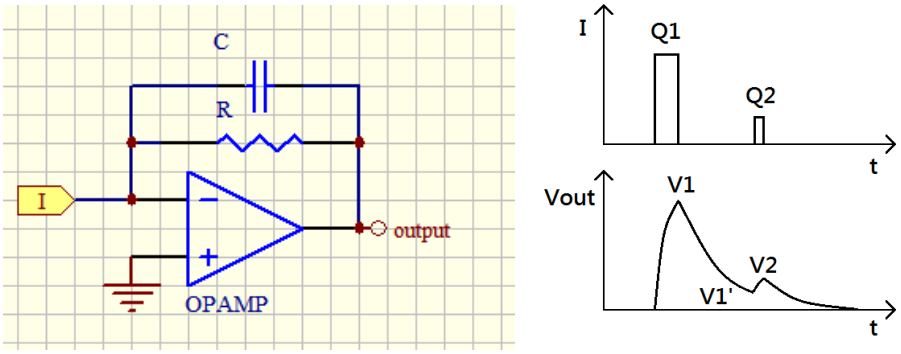


Figure 2-5 Simple schematic for Pre-Amp

After Pre-Amp, ADC converts the signal into digital one for FPGA to calculate the input charge. The design detail will be explained in the next chapter.

2.6 FPGA

FPGA (Field Programmable Gate Array) is a special kind of technology which offers programmable chip that can help us design the digital circuit easily. We choose the purchased board with Xilinx FPGA chip provided by E-elements Technologies. With it, the digitized signal can be calculated. After that, FPGA will communicate with computer and send the result to outside world.

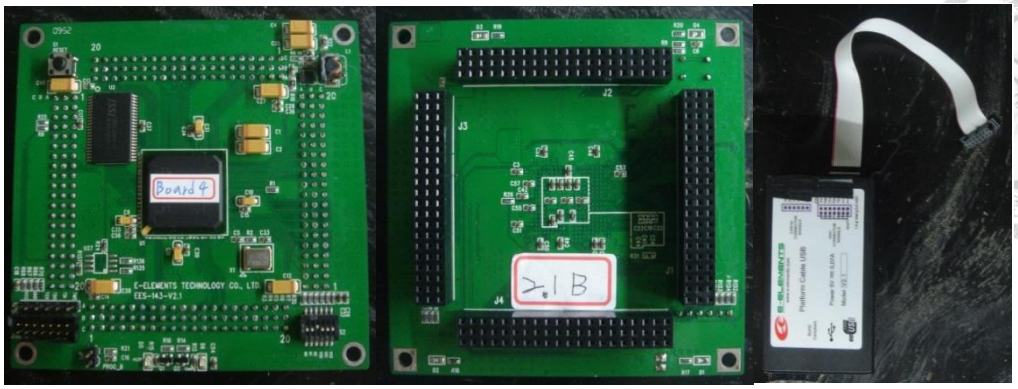


Figure 2-6 FPGA board and J-tag

FPGA is programmed by using the VHDL language and can be configured before the real operation. With the J-tag device, each code for luminosity monitoring or background monitoring can be configured in few seconds.

In the operation of background monitoring in phase 1, its function is like an energy meter, FPGA sums up all the dosage depositing in several second and show the total charge accumulated. If there's any unstable situation, we can see the unexpected result from the output to monitor the background.

In the operation of luminosity monitoring in phase 2, the back-to-back coincident signals over some pre-set threshold form the readout board will be triggered and accumulated. The final luminosity number will be determined by subtracting the random coincidence from other non-back-to-back counts, and multiplied by a conversion due to the constant ratio between the true Bha-bha event rate and the luminosity. We can use the Bha-bha event rate to monitor the luminosity.

2.7 Computer Software

To receive information from all BEAST2 detectors, the result from FPGA will be sent to the computer for BEAST2. In order to achieve the goal, some software effort is needed. The computer will communicate with FPGA in the path shown below.

FPGA (TTL) ↔ RS232 ↔ CUC(Comport-USB convertor) ↔ Computer

The computer will then get the data from FPGA and show the result in GUI (graphic user interface).

Chapter 3
Readout

3.1 Readout Structure

Readout system contains readout board and the FPGA board which are fixed and connected together. The readout board is designed and produced by me and the FPGA board is a commercial product. I'll explain more detail about the readout board in next several sections and how to pack different major components in the next chapter.

3.2 Readout Board Circuit Design

3.2.1 Readout Board

The design of readout board takes the front-end board of the neutrino telescope as a reference. The whole readout board design is shown below. It includes 8 channels as the main circuit, power part, clock part and FPGA (and RS323 also) connection part.

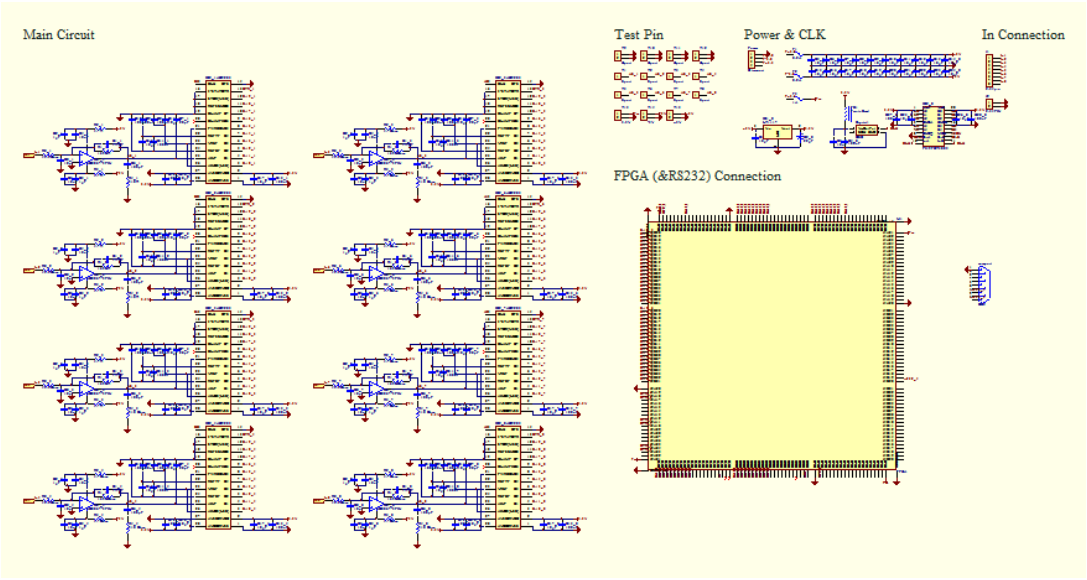


Figure 3-1 Schematic of whole readout board circuit

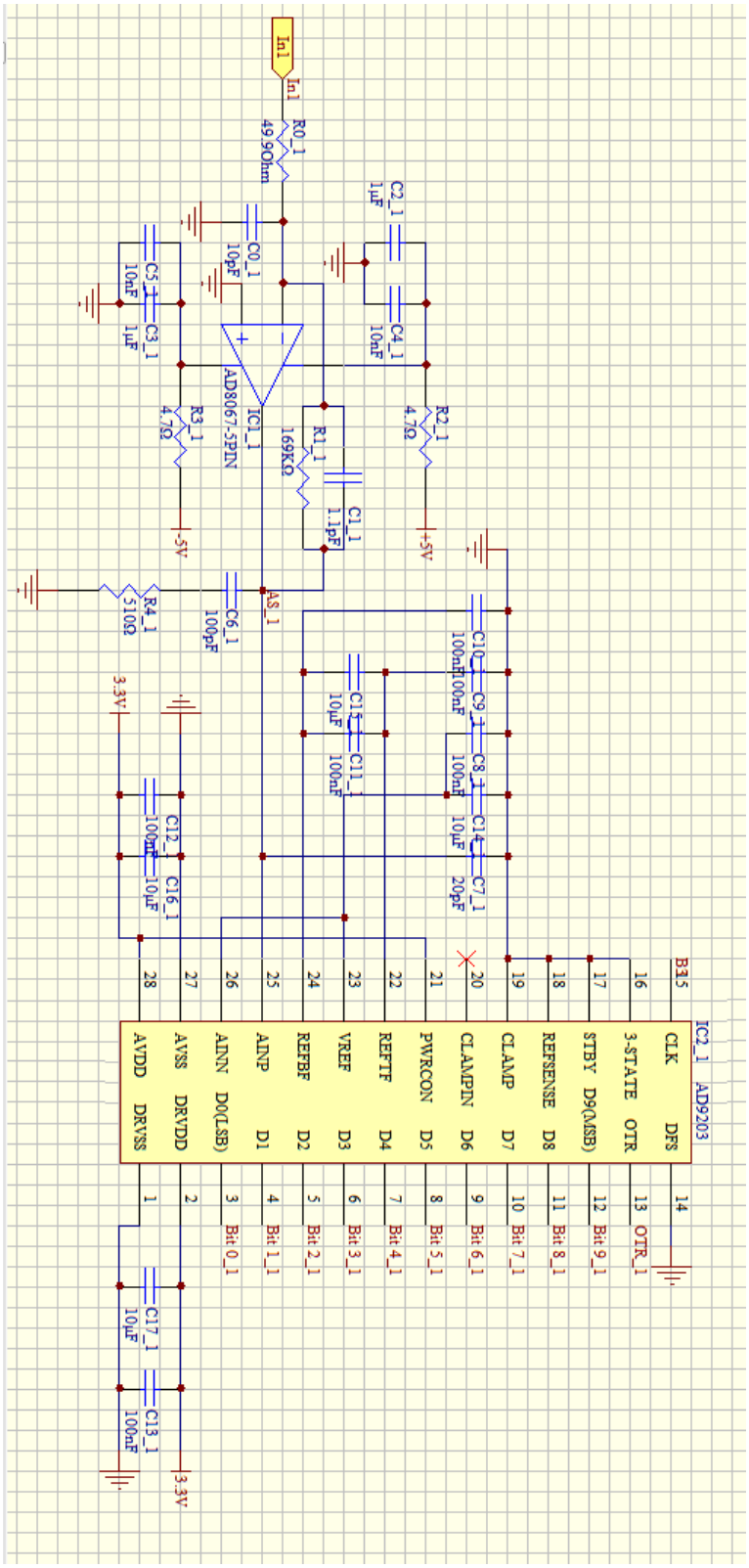


Figure 3-2 Schematic of Pre-Amp circuit

In the main circuit (all 8CH are designed in the same way), there's a Pre-Amp (pre-amplifier) in the front (before AS_X) and an ADC (analog to digital convertor) in the back. Since the charge from MAPMT for single photon is about 10~100 fC, Pre-Amp can magnify the signal to mV order and also to reshape it to longer timing. Then, ADC will convert the signal to digital one for FPGA in order to carry out all the functions we need.

The Pre-Amp circuit is based on an OP-Amp (operational amplifier) IC, an RC circuit and a pole cancellation circuit. The IC AD8067 was chosen because it has higher speed (~54MHz, 640V/μs). Considering the signal scale and sample timing, the capacitor value is chosen to be C = 1.1pF and the resistor value R = 169KΩ. Theoretically, the amplify rate =0.91mV/fC and the decay time constant = 186ns. However, these R and C will cause a pole in the Pre-Amp circuit. If the input source fit the frequency of that pole (1/187ns = 5.38MHz), there's a long time oscillation occurs to interfere the data sampling. So, we add another R (510Ω) and C (100pF) connected to ground to cancel this pole.

The ADC is made up just by an ADC IC which AD9023 is selected. By datasheet of this IC, we choose the following mode/setting for input = 2V single-ended. The other capacitances are specified in the way datasheet recommends. Clock for ADC is generated from the clock circuit.

3.2.3 The Clock Part and the Power Part

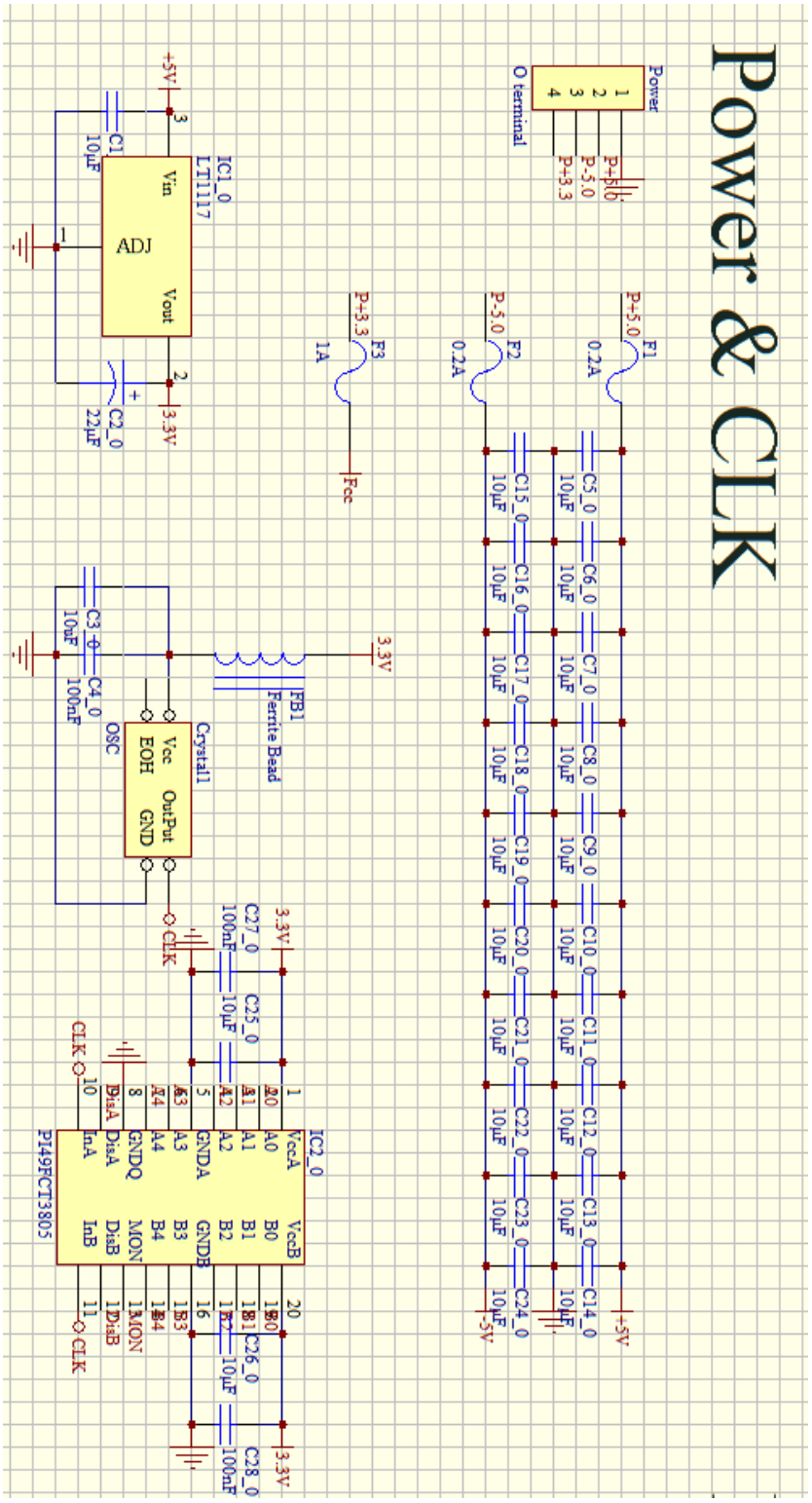


Figure 3-3 Schematic of power and clock circuit

ADC needs a clock for sampling. Also, FPGA need a clock for digital operation. Limited by the sampling rate of ADC IC, we use a 40MHz crystal to generate the clock signal. Considering the large loading for 8 ADC and also FPGA, there is a clock fan-out IC PI49FCT3805 to ease the loading. The design is followed from PI49FCT3805 datasheet.

In this readout board, there're 5 places need power inputs as shown below:

	+5V	-5V	+3.3V
Pre-Amp	V	V	
ADC			V
CLK			V
CLK fan-out			V
FPGA			V

Table 3-1 Power needed for each functional area in readout board

Although there are only 3 different power voltages, it's better to give FPGA its own power. As a result, other 3 parts needing +3.3V use the power adapted from +5V. This special +3.3V circuit design uses the normal design.

At last, there're fuses between the board and the power supply to protect the IC in the circuit.

3.2.4 FPGA and RS232 Connection

For more solid connection and easy usage, there are connections designed in the readout board. The FPGA board can be connected solidly to the readout board and has the flexibility for future changes. The connection for RS232 is also designed in the readout board.

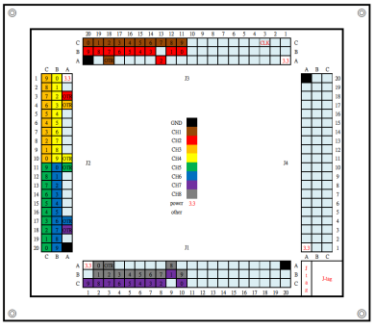


Figure 3-4 Schematic of connection between the readout board and the FPGA board

3.3 Readout Board Layout

3.3.1 Whole Layout Structure

The readout board is a 6-layered board. Only the first one and the last one can be used for components soldering. The DIP (dual in-line package) components even need to take space in all six layers. So, most of the chosen components are SMD (surface-mount devices) type in order to use the space more efficiently. There are two layers for grounding to shield the interference of power and the clock and also make the grounding more solid. The usages of each layer and the whole layout structure are shown below.

	Layer name	Main function	Second function
1	Top	signal	Power adapt, CLK generator & power strengthen
2	Internal Plane	GND	
3	Midlayer 1	power	power strengthen
4	Midlayer 2	CLK	RS232
5	Internal Plane	GND	
6	Bottom	signal	power strengthen

Table 3-2 Functional distribution in every layers

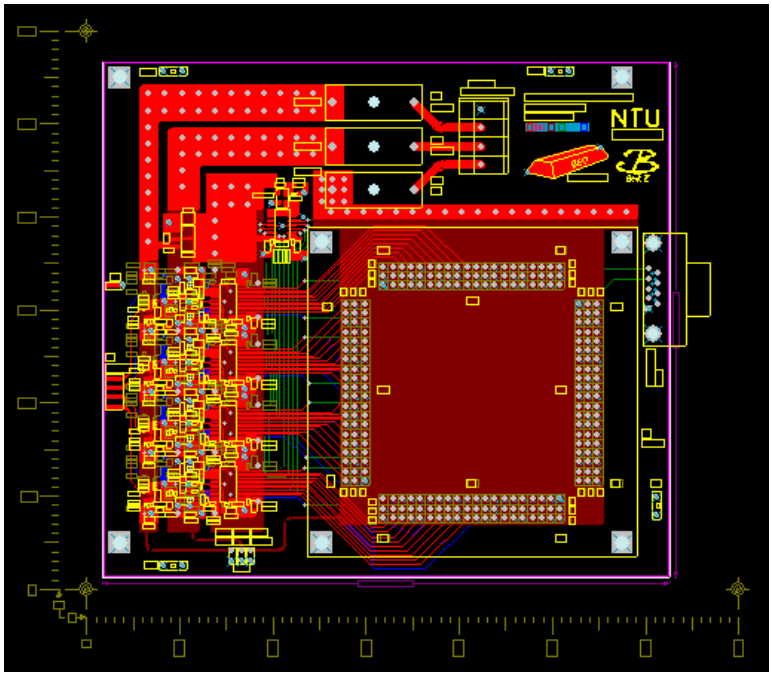


Figure 3-5 Layout of whole readout board

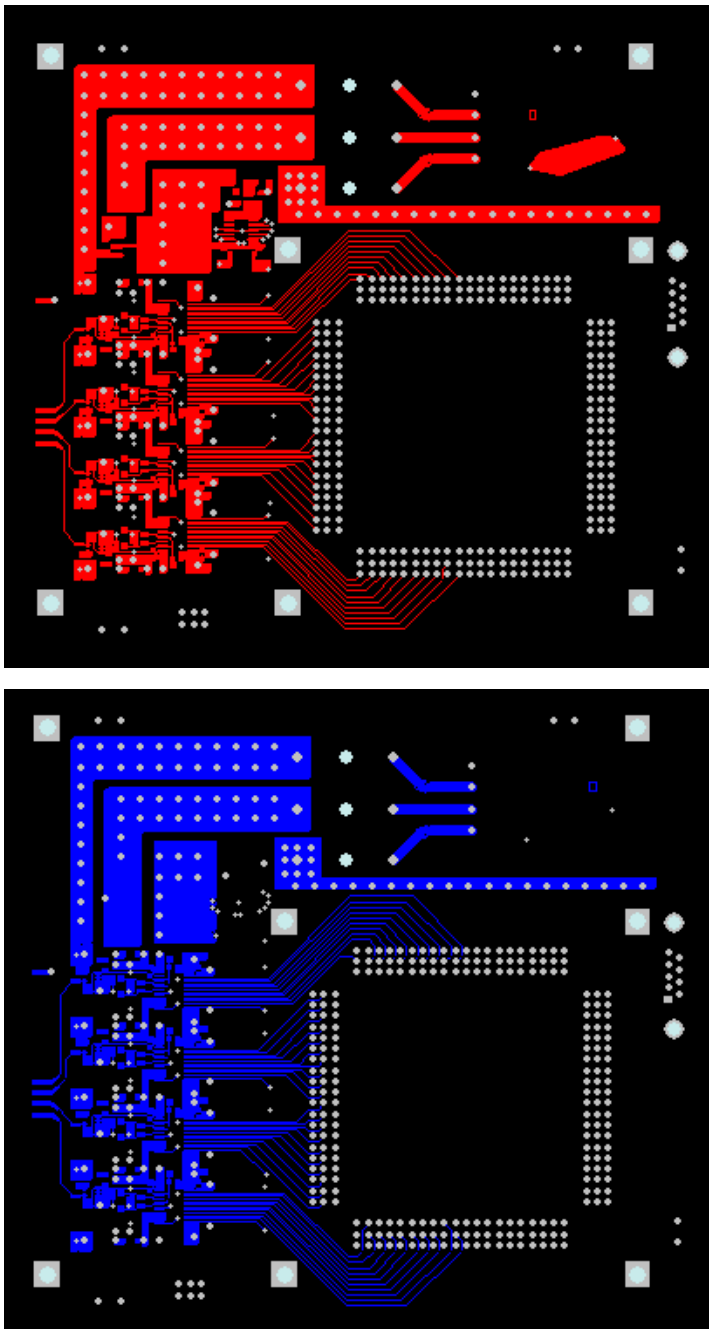


Figure 3-6 Layout of two surface layers

They looks similar. Actually, they almost have the same function excpt there's a +3.3V adapter and clock generator in the top layer (red one). On the upper side, there're more copper for power to go through in order to make the power more stable in the board. Both layers have 4 channels in the left. Then, after ADC, there're just serveral digital bits connected to the FPGA.

3.3.3 Power Layer (Midlayer 1)

These 4 large area are for +5V, -5V, +3.3V (adapted from +5V) and +3.3V (from power supply directly). There're so many holes just beyond the IC to support the power from this layer to the IC.

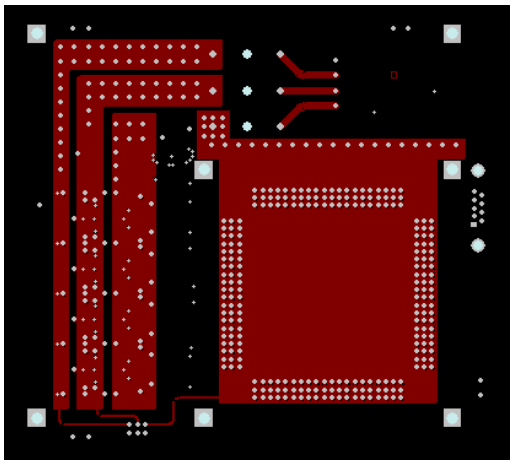


Figure 3-7 Layout of power layer

3.3.4 Clock Layer (Midlayer 2)

The clock signals from the fan-out IC are delivered in this layer. The curved design is to make sure that all channels work synchronously.

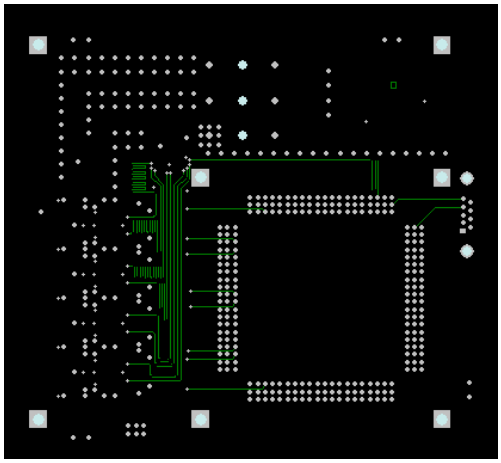


Figure 3-8 Layout of clock layer

3.3.5 Grounding Layers (Two Inter Planes)

These two layers are the same. In these pictures, there’re copper in black area. They all connected to ground.

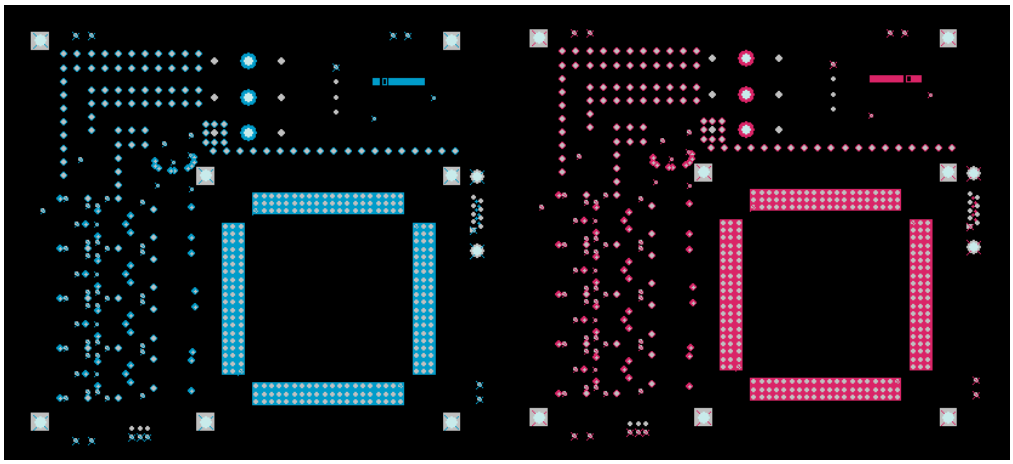


Figure 3-9 Layout of two grounding layers

3.4 Empty Board Production

After finishing the layout, the empty board is produced by JetPCB. It takes about one week to produce. It's shown below. (155mm X 141 mm)

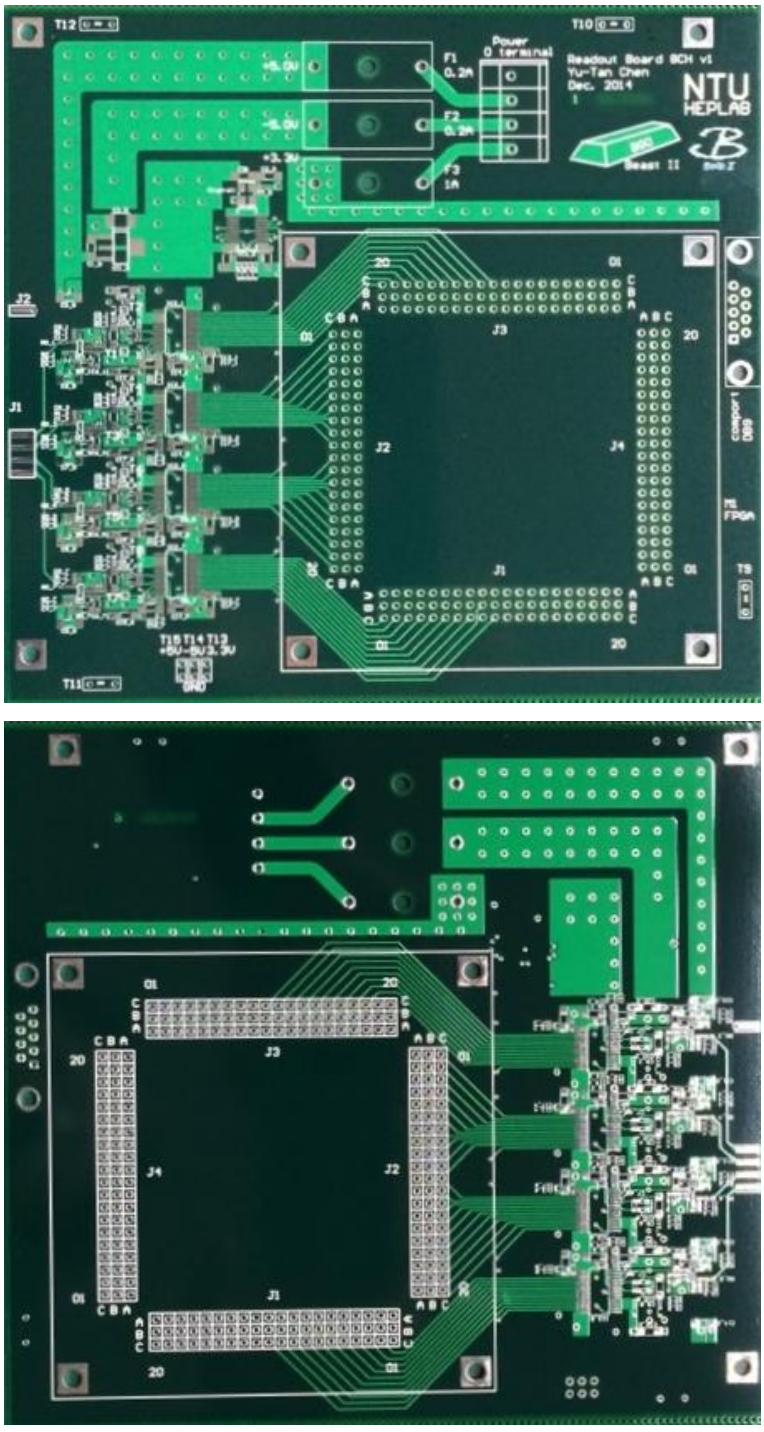


Figure 3-10 Empty readout board

3.5 Soldering Tools

Since most of the components used are SMD, there're some special tools needed.

1. Soldering iron

Unlike the normal one, there're some special shapes for magical function. The left one shown below has a notch to adsorb small amount of solder in it. When it touches the pad, it will release appropriate amount for soldering material and take out the extra one. It's useful when soldering the small pad. The right can let the solder on its blade heated and adsorbed in the line between the pad and the component.

2. Soldering paste

Though there's paste in the usual solder, the small amount of the additional one can make the solder more fluid-like when heated.

3. Isopropyl alcohol

Even though paste is useful, it should be removed after the soldering. Isopropyl alcohol is a good choice to remove it and not to harm the board.

4. Tweezers

The pad and the component are so small that the sharp tweezers is needed. Unlike the normal one, the thickness is even only 0.2mm.

Figure 3-11 Soldering tools: soldering iron, soldering paste, isopropyl alcohol, tweezers (from left to right)

3.6 Test

3.6.1 Pulse Test

The charge pulse for testing is produced by the test circuit shown below with the function generator AFG 3252.

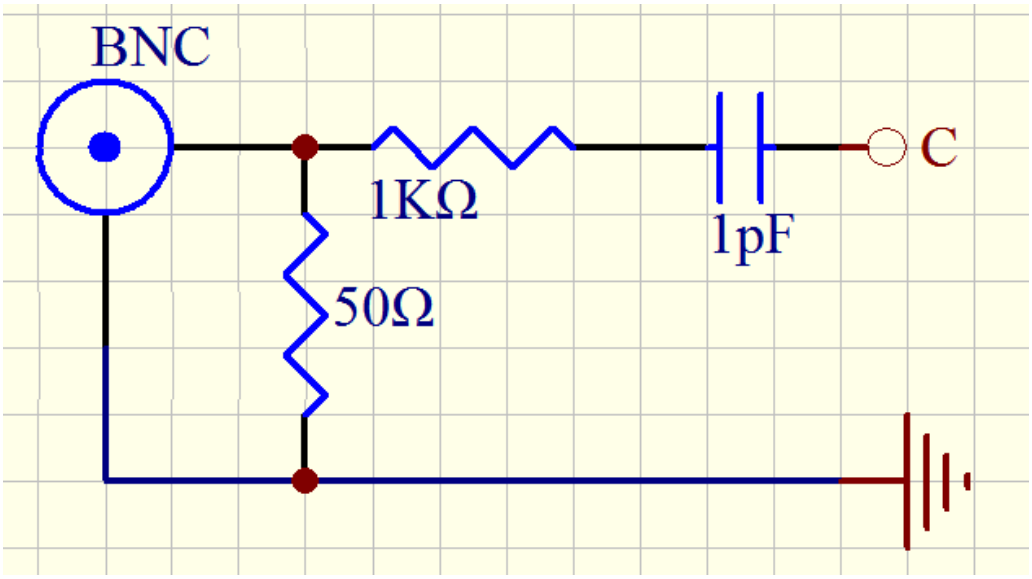


Figure 3-12 Schematic of testing circuit

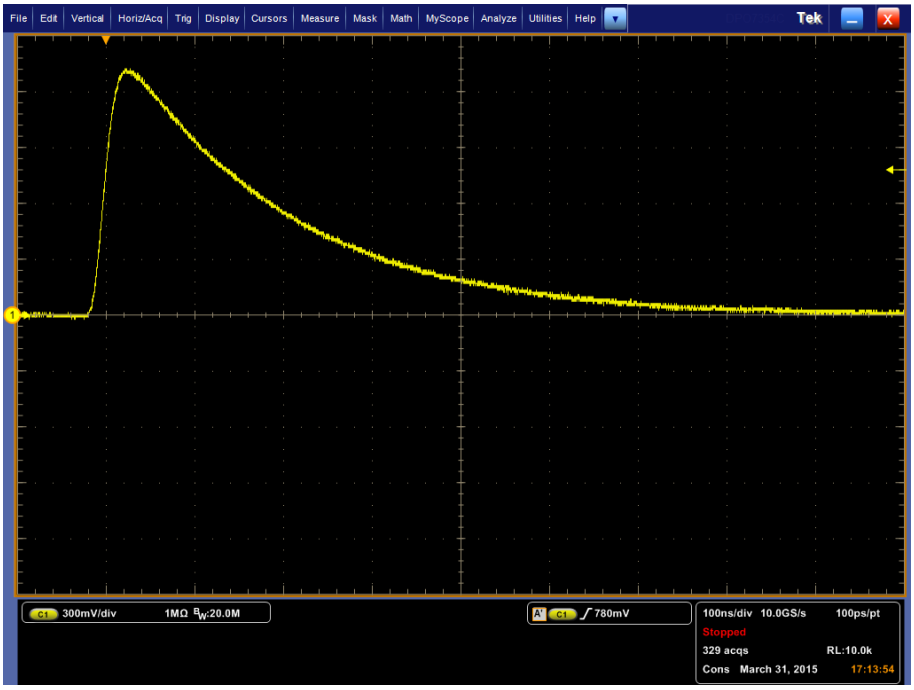
This circuit is just for producing the charge signal from the capacitance. The 50Ω resistor is used to couple the BNC cable. The 1KΩ resistor and 1pF capacitance form a high pass filter to decrease the noise in lower frequency (3dB point = 1GHz).

Standard function is a step pulse (Vpp = 1.1V, once / 3μs). Sometimes, we change the Vpp to check the linearity of the readout system.

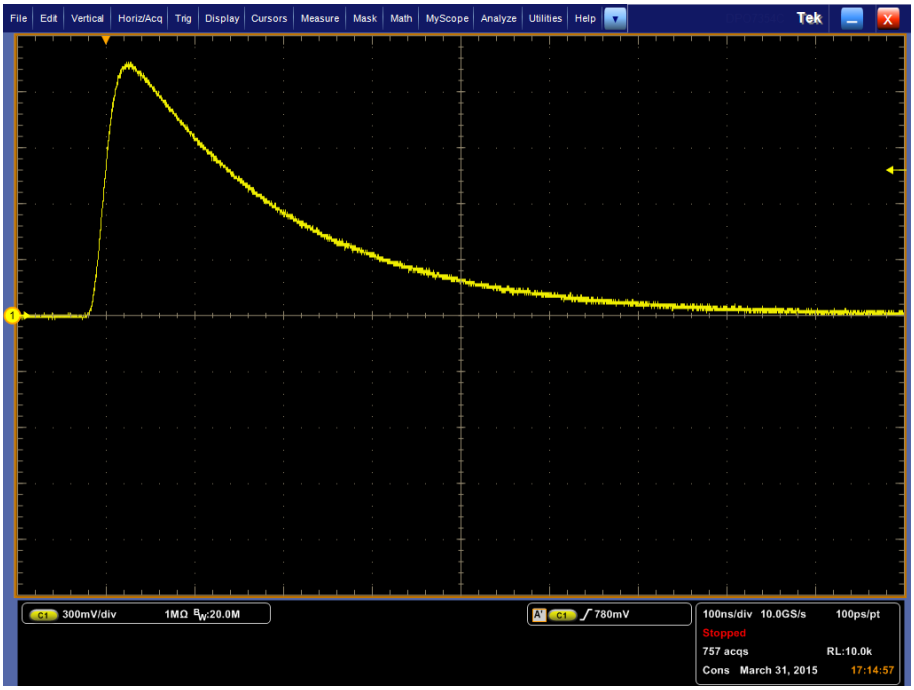
3.6.2 Pre-Amp Test

Pre-Amp function is checked by oscilloscope DPO7354. From the result below, we can see perfect exponential decay pulse in the analog output (AS_X). Its decay time constant is around 186ns.

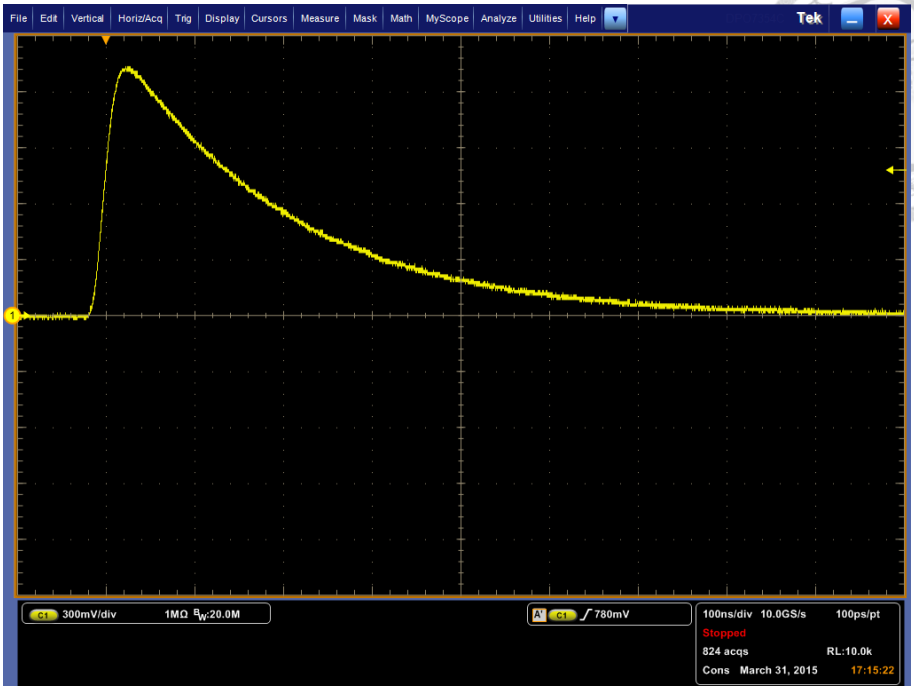
CH1



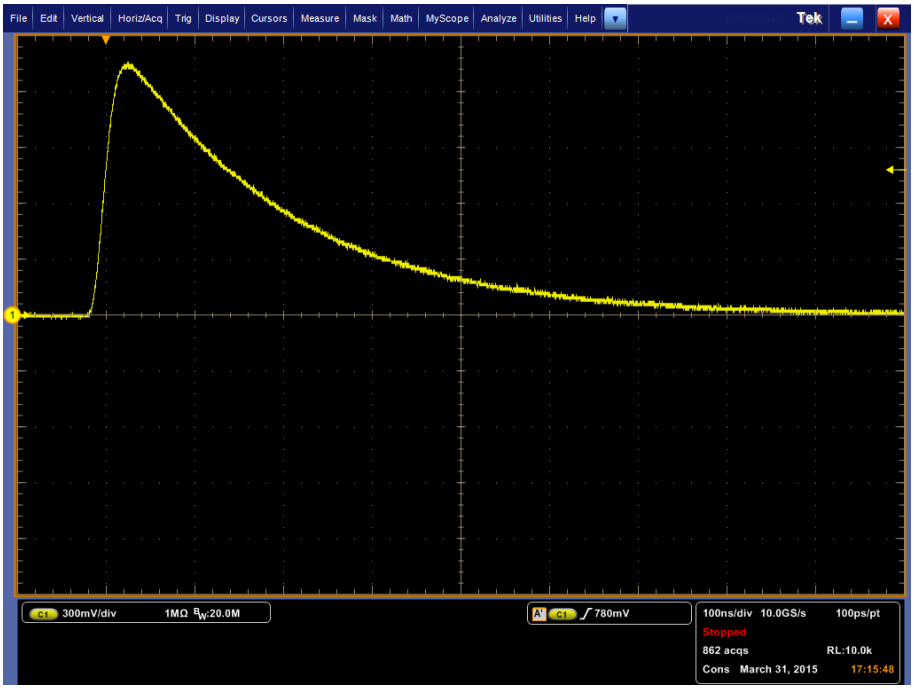
CH2



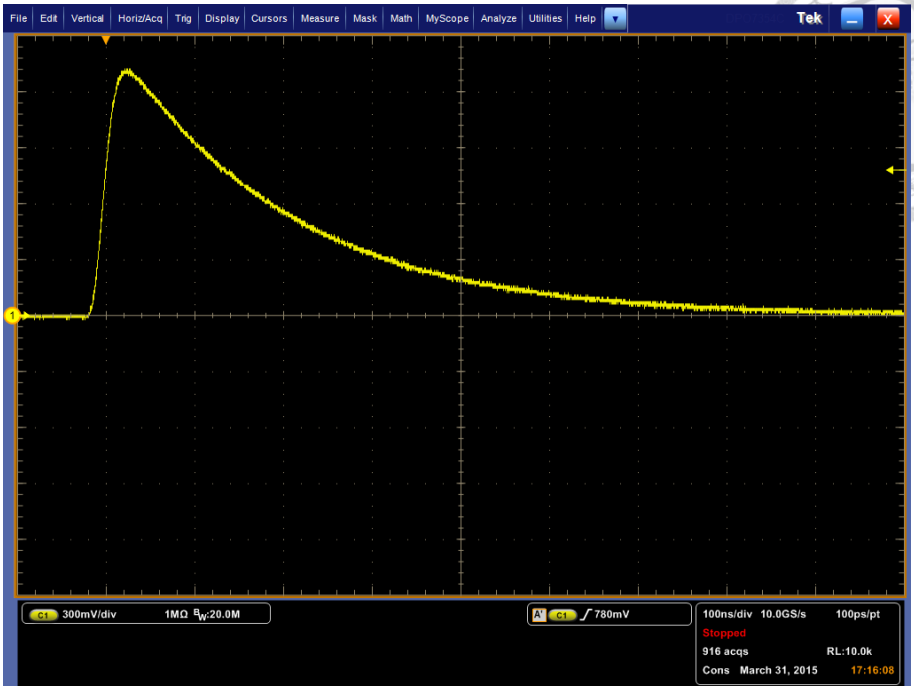
CH3


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
C1 300mV/div 1MΩ BW:20.0M
A C1 780mV
100ns/div 10.0GS/s 100ps/pt
Stopped
824 acqs RL:10.0k
Cons March 31, 2015 17:15:22

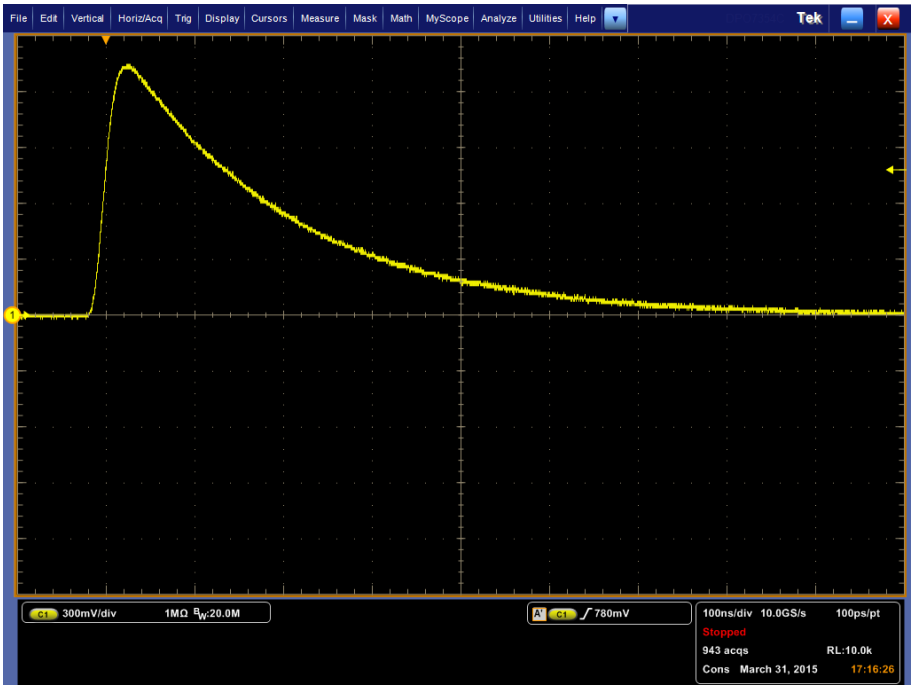
CH4


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
C1 300mV/div 1MΩ BW:20.0M
A C1 780mV
100ns/div 10.0GS/s 100ps/pt
Stopped
862 acqs RL:10.0k
Cons March 31, 2015 17:15:48

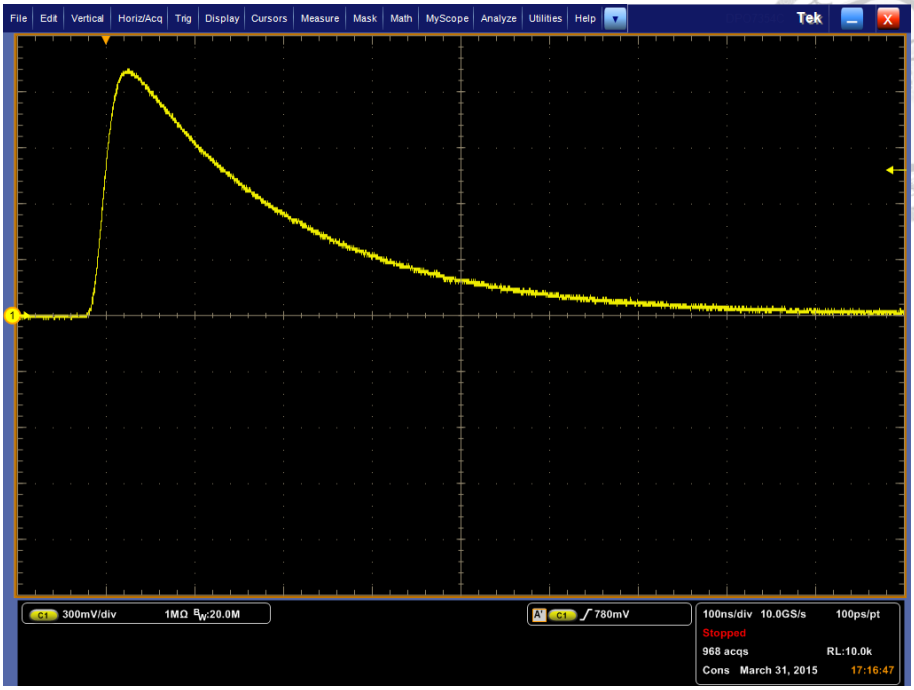
CH5


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
C1 300mV/div 1MΩ BW:20.0M
A C1 780mV
100ns/div 10.0GS/s 100ps/pt
Stopped
916 acqs RL:10.0k
Cons March 31, 2015 17:16:08

CH6


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
C1 300mV/div 1MΩ BW:20.0M
A C1 780mV
100ns/div 10.0GS/s 100ps/pt
Stopped
943 acqs RL:10.0k
Cons March 31, 2015 17:16:26

CH7



CH8

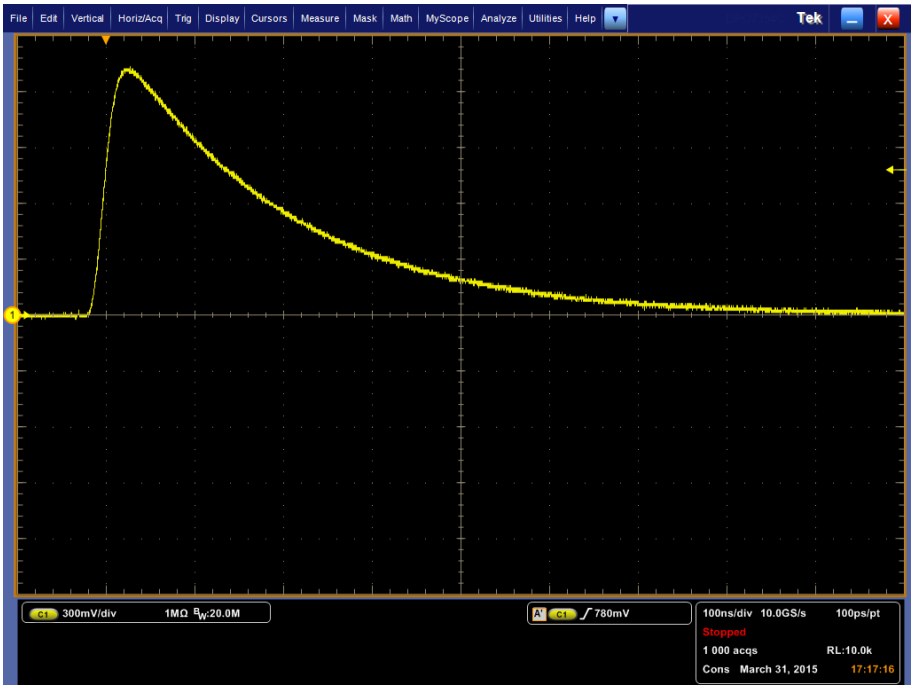
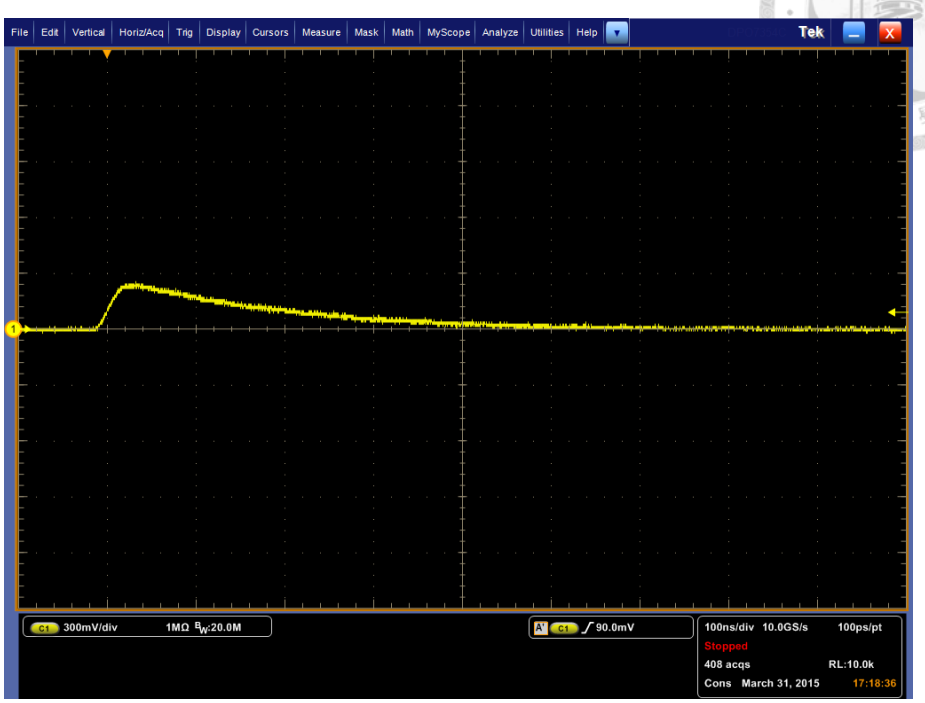


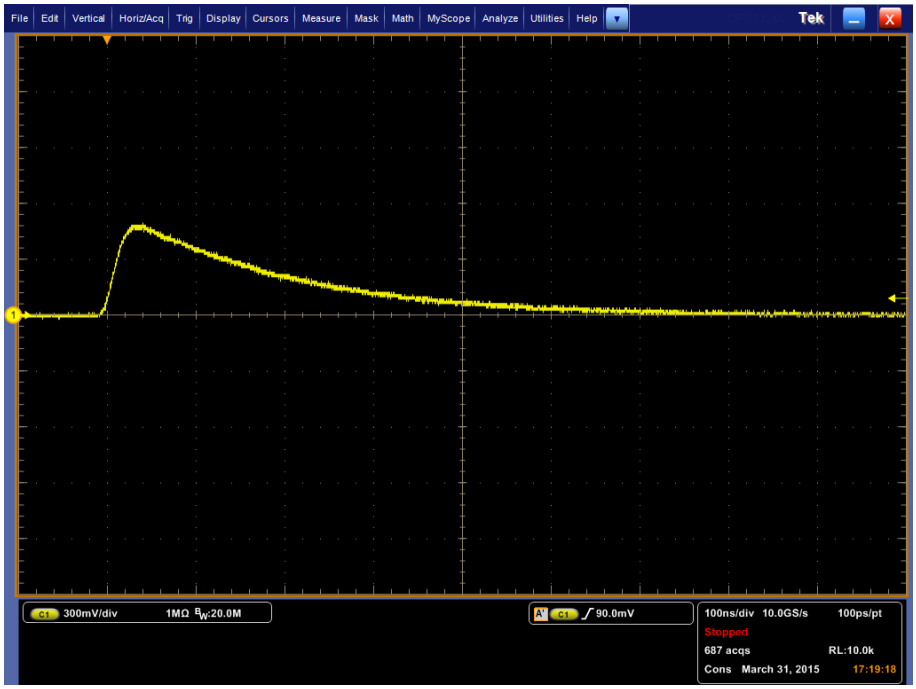
Figure 3-13 Testing result for each channels of Pre-Amp

When we change the input charge, the output also changes linearly.

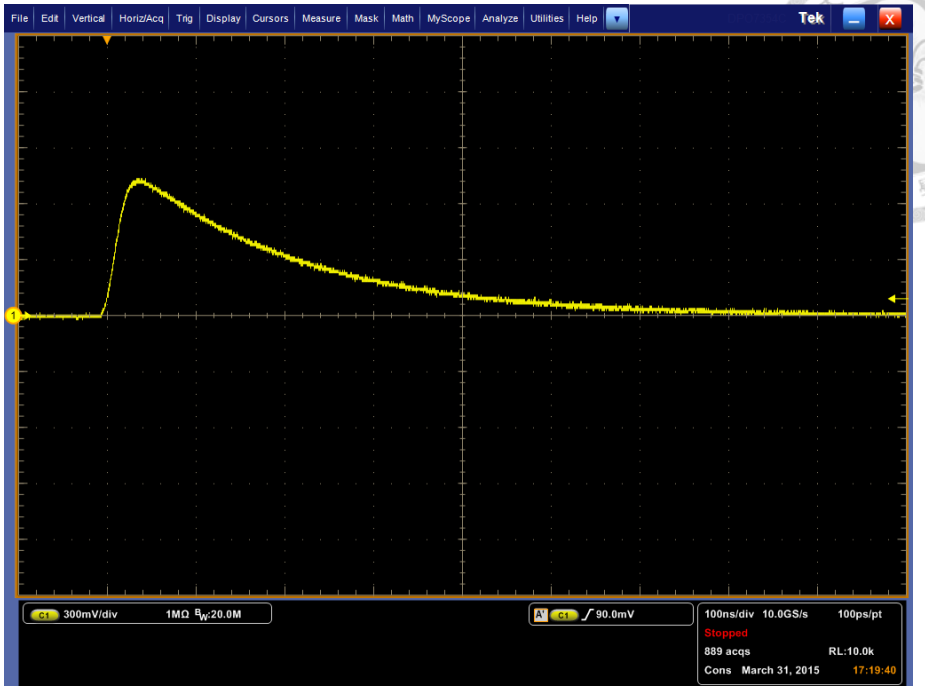
200mV



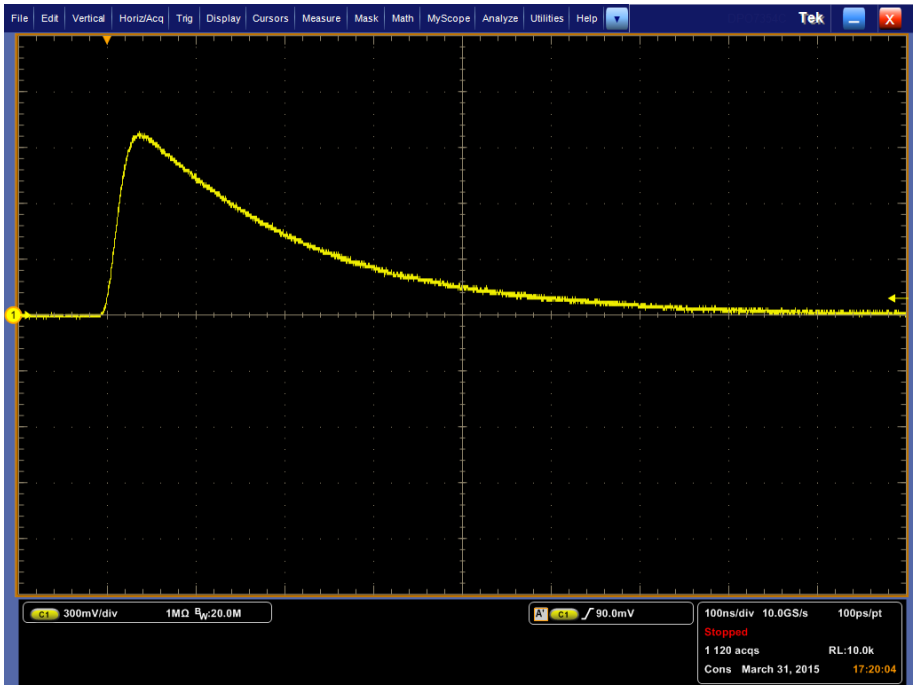
400mV



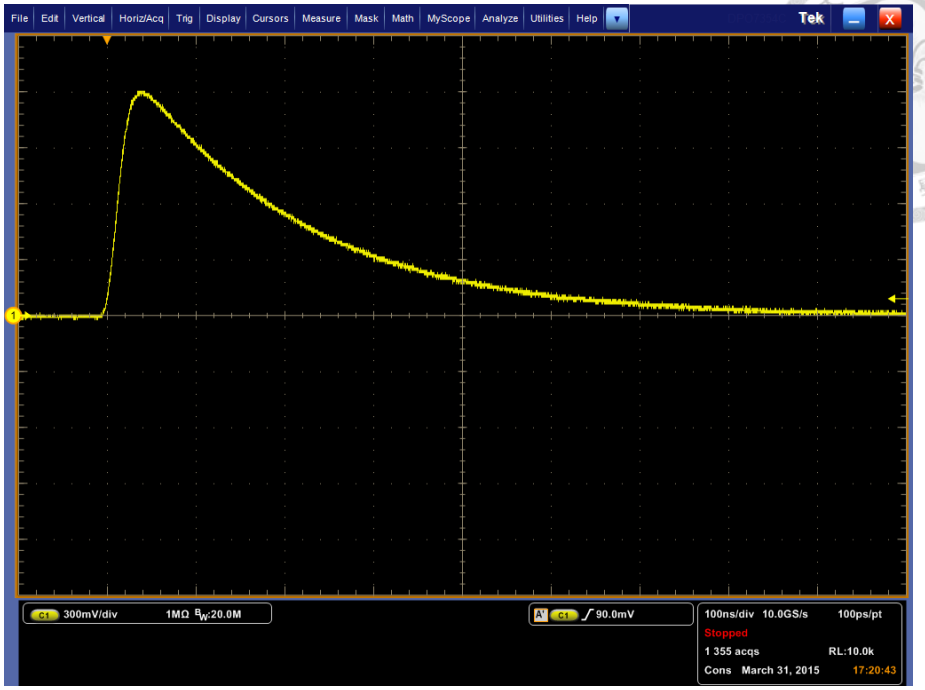
600mV


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
300mV/div 1MΩ BW:20.0M
90.0mV
100ns/div 10.0GS/s 100ps/pt
Stopped
889 acqs RL:10.0k
Cons March 31, 2015 17:19:40

800mV


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
300mV/div 1MΩ BW:20.0M
90.0mV
100ns/div 10.0GS/s 100ps/pt
Stopped
1 120 acqs RL:10.0k
Cons March 31, 2015 17:20:04

1000mV



1200mV

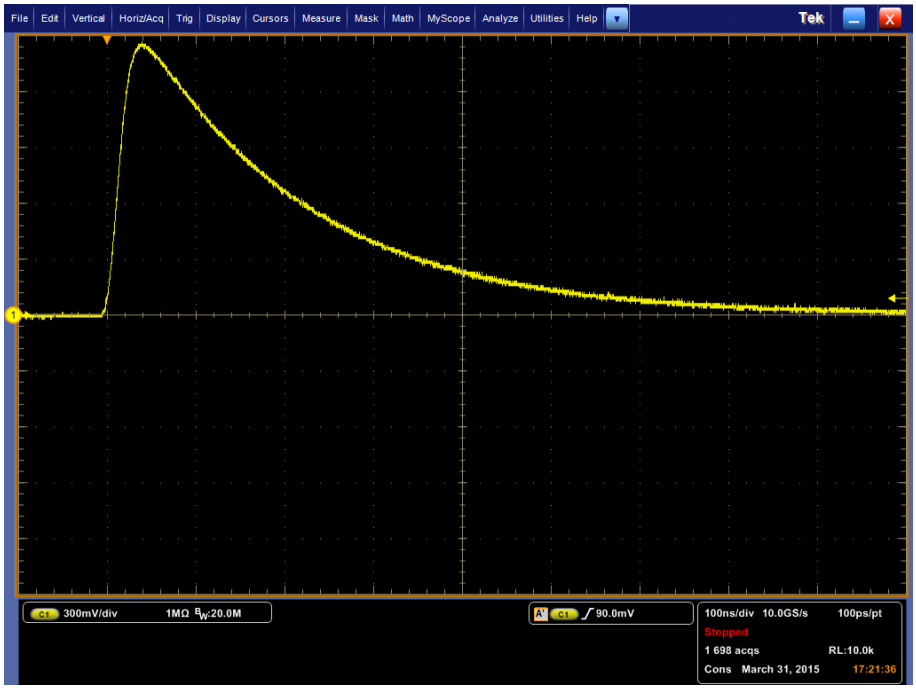


Figure 3-14 Testing result for each amplitude of pulses

3.6.3 ADC Test

ADC function is tested by Acute Logic Analyzer. The result is shown in the picture below. First 10 lines show the digital values for each bit. Then, it shows the digital bus summation value (last significant bit $=2^0$; most significant bit $=2^9$) and its diagram with time.

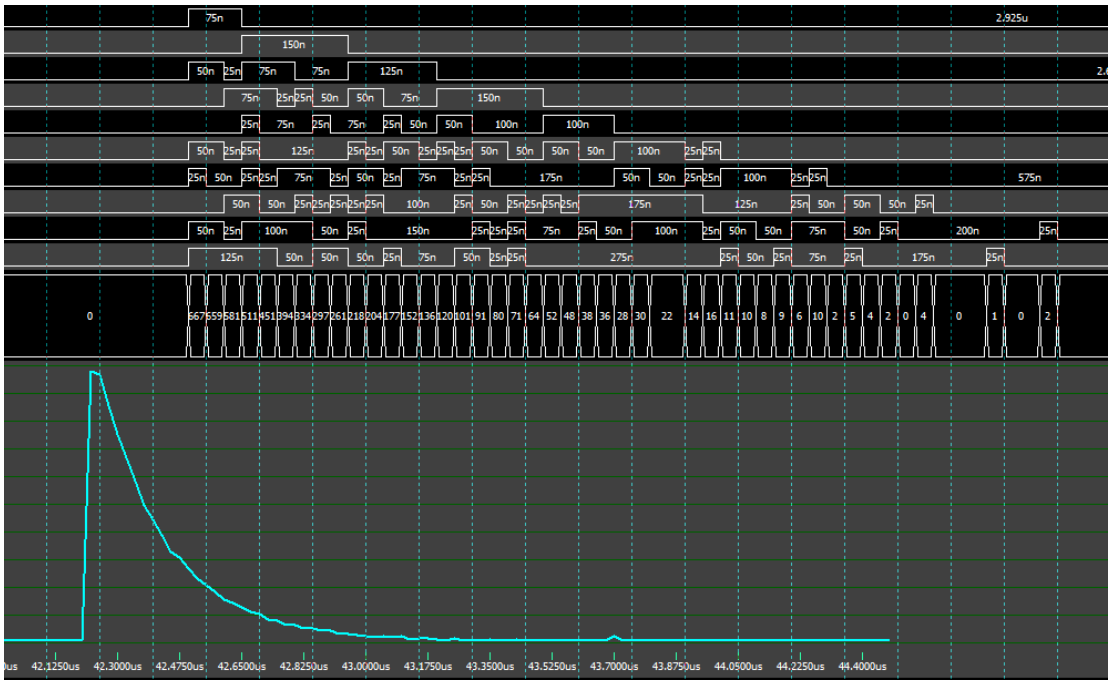


Figure 3-15 Testing result of ADC with single pulse

We can also see the long term running result. It's very clear that we can see a pulse per 3μs just as the input pulse.

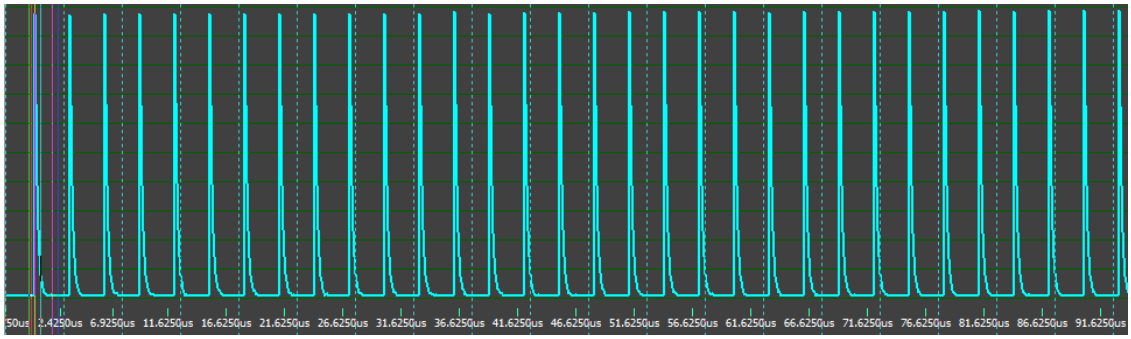


Figure 3-16 Testing result of ADC with periodical pulse

There’s almost nothing when we stop the input.

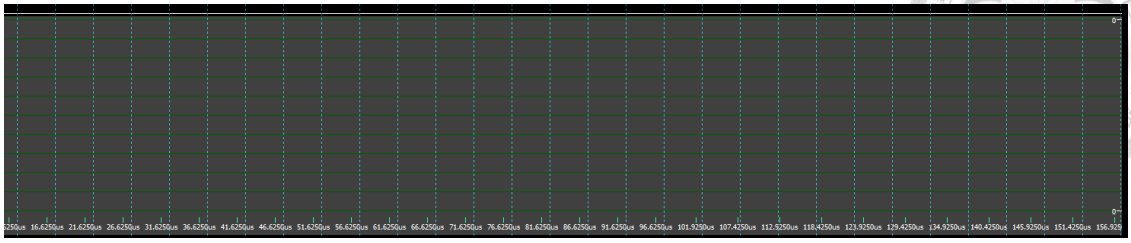


Figure 3-17 Testing result of ADC without any pulse

The same test has been carried out with all 8CH of this readout board and almost the same result is observed.

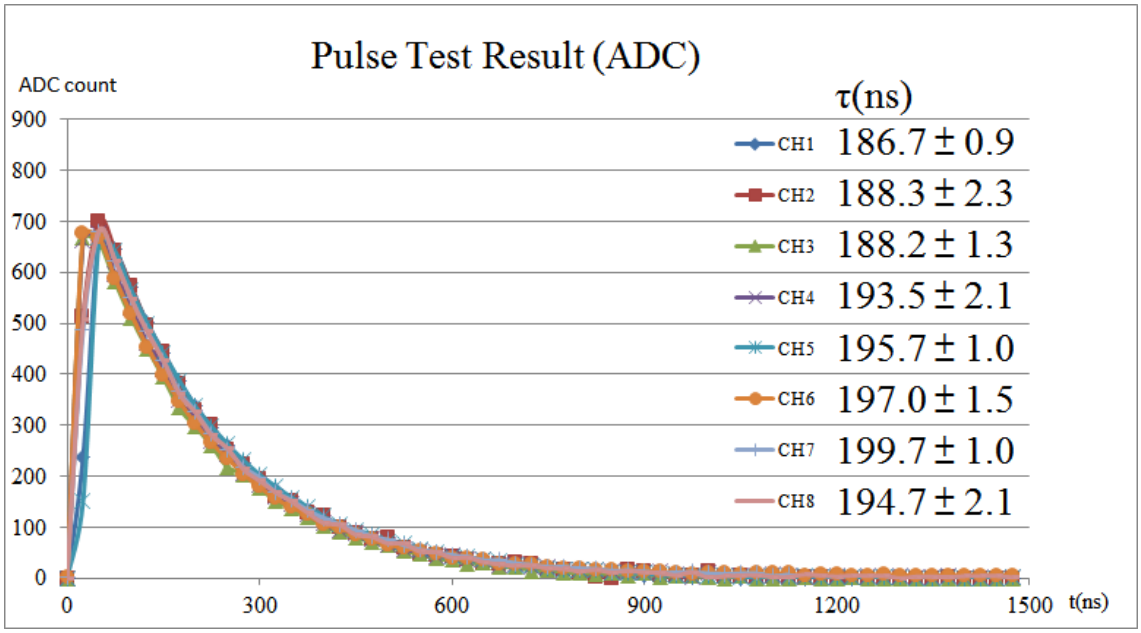


Figure 3-18 Waveform analysis

It shows that the ADC part works well and also proves that all 8 channels have very close R and C values.

3.6.4 Debugging in the Test

During testing, there’re some problems occurring which should not happen theoretically. The following are my personal experience about how to fix these problems.

(1) Pre-Amp

Once after soldering, some channels of Pre-Amp didn't work well. There was a DC shift in the Pre-Amp output. The current sometimes became larger after running for several seconds. A check on the power of the IC turns out that the problem might be a short between the by-pass capacitance for Pre-Amp power. After resoldering some channels, the DC shift situation is improved but still there are wrong pulse shapes found in some channels due to their wrong RC values.

By checking and cleaning the board again, the problem is pointing to the solder paste where with lowering the paste usage, the current increasing phenomenon is suppressed. Then, by resoldering channels (with minimum solder paste) with new components one by one, the problems are solved.

(2) ADC

The ADC IC is much easier to break because of soldering problem or over-heating. Sometimes, it just breaks without any reason. From the test experience, about 10% may not work or not work very well. However, it's also easy to fix up. Just use the heating gun (300℃) to disolder that IC and change a new one. The picture shown below is the ADC pulse test result with a broken ADC.

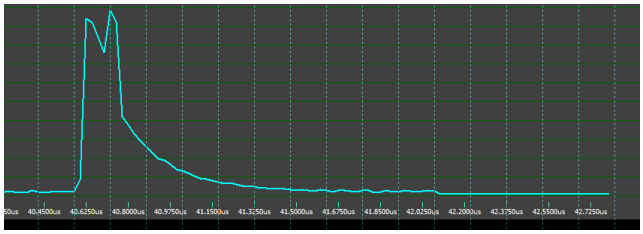


Figure 3-19 Wrong ADC result tested by LA

(3) Clock

By the datasheet of clock crystal, it should still work when the control pad is open. However, during the test, it doesn't always work. Fortunately, it can work for sure when the control pad is set on high. After shorting the control pad and +3.3V with a FB (ferrite bead), clock crystal will not stop working at all.

3.7 Result

After these mentioned tests and debugging, the readout board works as expected. The uniform time constants will be used for firmware. All channels of the readout boards have been calibrated well.

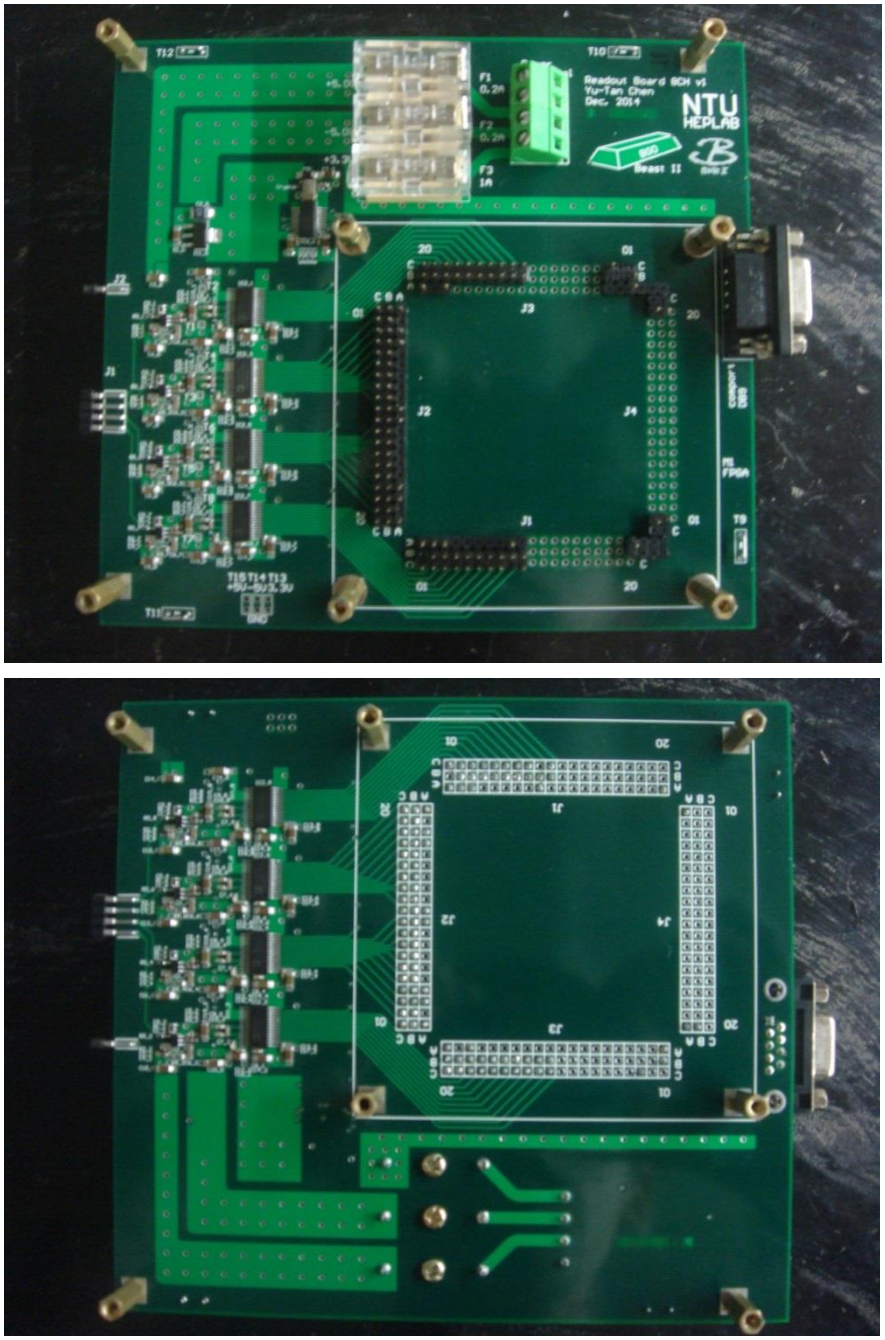


Figure 3-20 Finished readout board

Chapter 4
Packaging of BGO System

4.1 Purpose and Whole Structure

To give all system a better protection and a good electromagnetic shielding, all system (fiber not included) should be put in and fixed with a suitable metal case. For quicker and easier process, it's decided to be made by refitting into a chassis. We need to put the readout board and the MAPMT inside. Fortunately, we found a case made with iron and aluminum (W=210mm, L=292mm, H=98mm). For user-friendly, all connections are fixed on the case surface so that we can just put on the fibers and cables to run the BGO system.

Figure 4-1 Case for BGO system

In the case, there are readout boards and MAPMT. All electronic I/O and power are on the back of the case. Readout system is fixed in the case and has good connection with all connectors. The fibers are placed through the front of the case to the cover of MAPMT. The MAPMT is also fixed in the case. The output form the MAPMT will be calculated by the readout system and transferred to a DAQ computer.

In this chapter, the mechanical structure of the readout system, optical system, the I/O ports, and the power of the whole system are described.

4.2 Mechanical fixture of Readout

Readout contains the readout board and the FPGA board. The main design guideline is not only to fix their positions w.r.t. the case but also make sure their functions work well.

4.2.1 Fixing

If we treat the readout board, the FPGA board and the case as a 3-layers structure, each layer are fixed and connected with copper pillars. The holes for pillars are connected to the ground. This will ensure that they have the same and stable grounding. The readout board is designed for this FPGA board, so the two boards can be fixed very well.

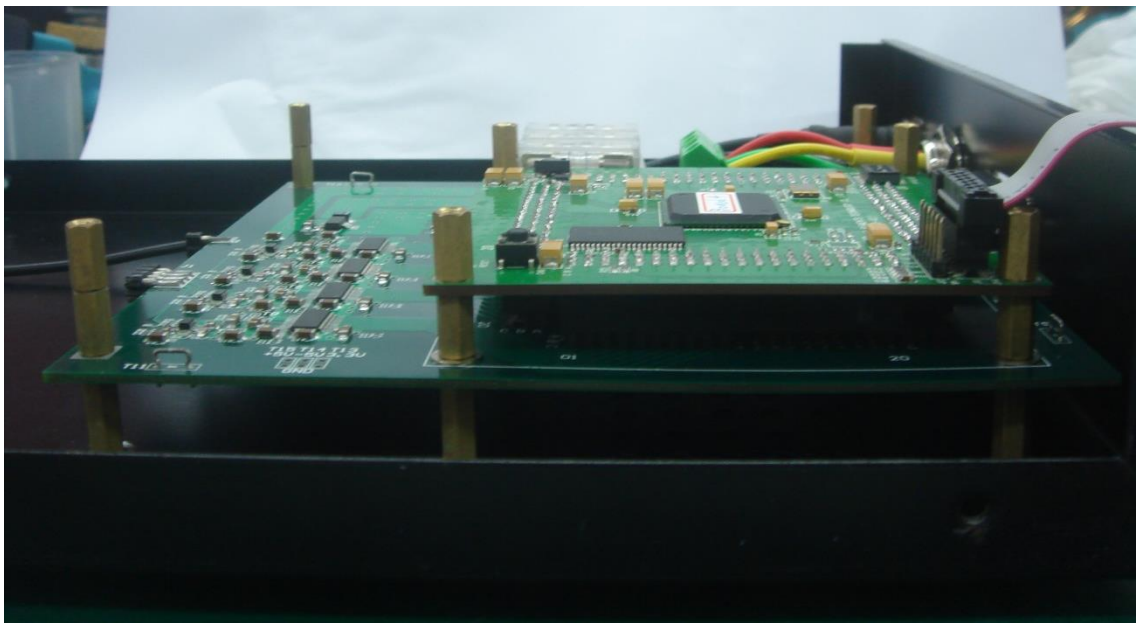


Figure 4-2 3-layers structure for fixing

4.2.2 Connections between the Two Boards

It is a delicate work to connect the readout board and the FPGA board. There are lots of pins which have to be connected tightly between the two boards. There are 88 pins for ADC output (11 pins for 1 channel), 8 pins for power (4 for GND and 4 for 3.3V to FPGA), 1 pin for clock and 2 pins for RS232 transmission. These connections achieve two goals – good electric contacts and mechanical fixation.

4.2.3 Power and I/O of Readout

For the purpose of user friendly, all I/O and power have their connectors on the case. For low voltage power, there's a terminal on the readout board. The connector is linked with an electric wire to the designated terminal. The RS232 connector is directly soldered on the readout board. A J-tag cable links between FPGA and the computer. Its flexible flat cable can do the job nicely.

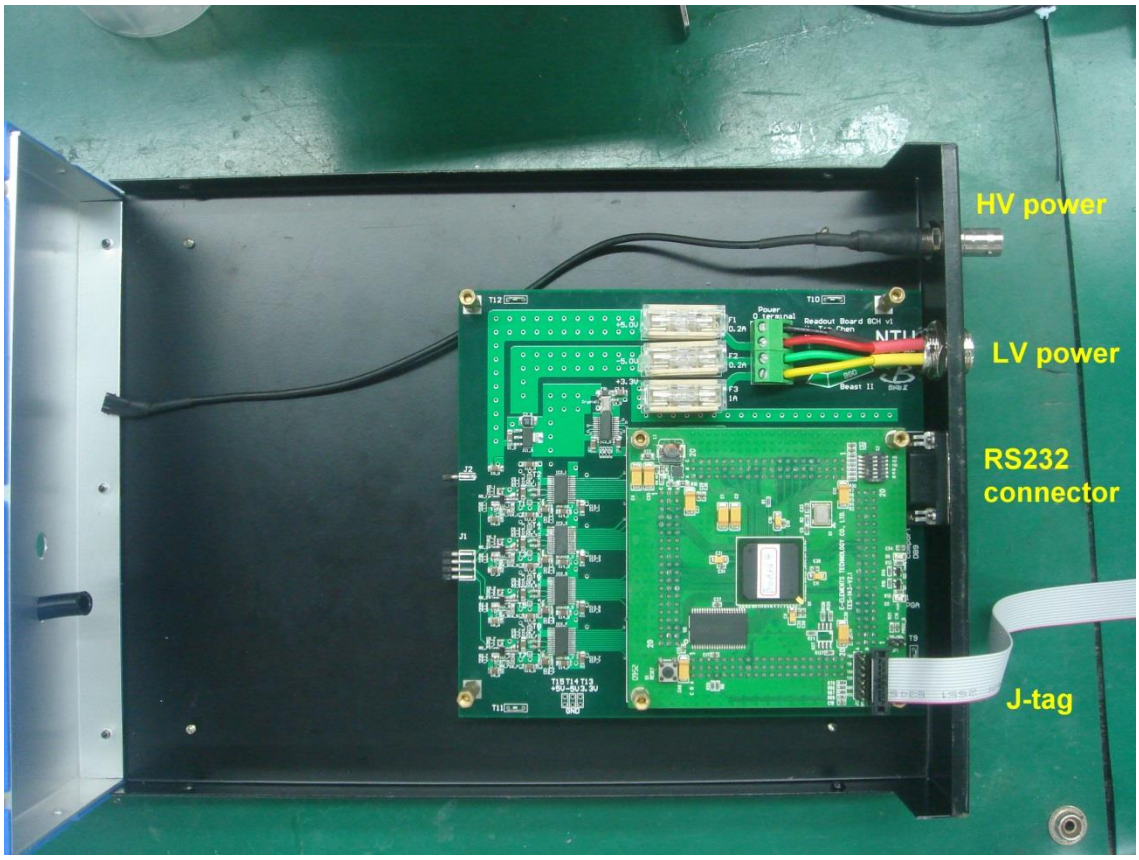


Figure 4-3 Distribution of each functional I/O and power for readout board

4.3 I/O Design and Their Cables

Except the optical part, the I/O and power connector are placed on the back of the case. There are specific cables for these connectors.

4.3.1 Connector on the Case

From the photo shown below and from left to right, the three connectors are for RS232 transmission, low voltage power supply, and high voltage power supply.

RS232 transmission uses normal RS232 D-type 9 pin PCB-use connector. It can be soldered on PCB directly and fit for the normal RS232 cable.

Low voltage power supply uses 4 in 1 power connector. It's designed to be used for the boards inside the case. There are 4 independent channels in it and has a special mechanical structure preventing wrong channel connection.

High voltage power supply uses normal SHV (save high voltage) connector. The fire pin is hidden inside to avoid causing any accident. The thicker insulating material of the SHV connector can ensure the safe supply of the applied high voltage.

Figure 4-4 Back of the case with connectors

4.3.2 Cables

The signal from FPGA is actually with 3.3V CMOS logic level which in principle can be used directly as the TTL signal. We change it into real RS232 transmission by a commercial product, i.e. a standard convertor. After that, we use another convertor to change it into USB (Universal Serial Bus), just because the USB is much more convenient in connecting to a computer. The cable is shown below.

The connector end of the low voltage cable is the standard one. It can be connected and fixed easily. The other end is the Y terminals. They can be fixed to low voltage power supply. The cable is a 4-wired cable with protection over them. It can be loaded at least 10 A for each channel. The real current for each is less than 1 A.

The high voltage cable used is the standard SHV W-W cable. The connectors on both case and high voltage power supply are M (male).

Figure 4-5 Cables for BGO system: RS232, LV power, HV power (from left to right)

4.4 Mechanical Structure of Optical Part

The connection of the optical part is shown below. The optical input, electronic output and power supply for MAPMT will be described.

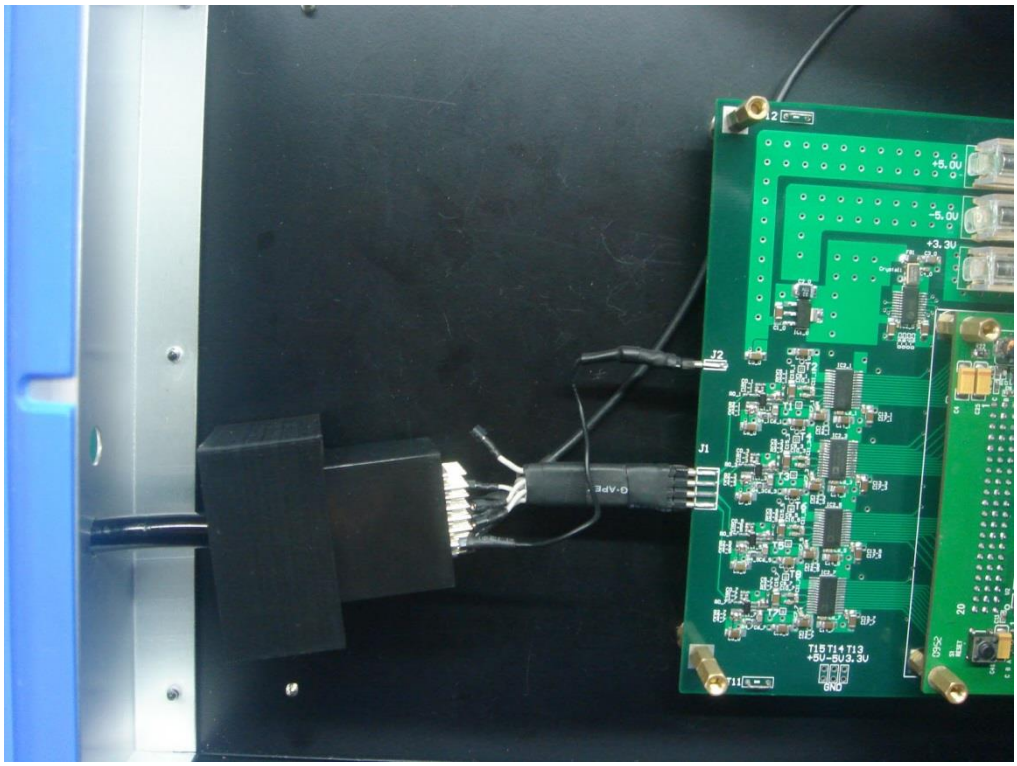


Figure 4-6 All connection with MAPMT

4.4.1 Optical Input

The most important connector is the cover for MAPMT. It's produced by 3D printer. So, we can make it well matched with the MAPMT. The fibers can be placed in the hole in the front of the cover. It helps us to locate the position of pixel that we want to use. Furthermore, the cover can provide the light tightness for MAPMT. The plastic tube around the fibers can provide the protection and prevent the optical interference for optical fibers.

4.4.2 Electronic Output

The output from MAPMT is just the charge from each pixel (output pin). Flexible wires are connected to them and we can select the pixels that we want to use. There' is also a wire connection to ground which can make the noise level low.

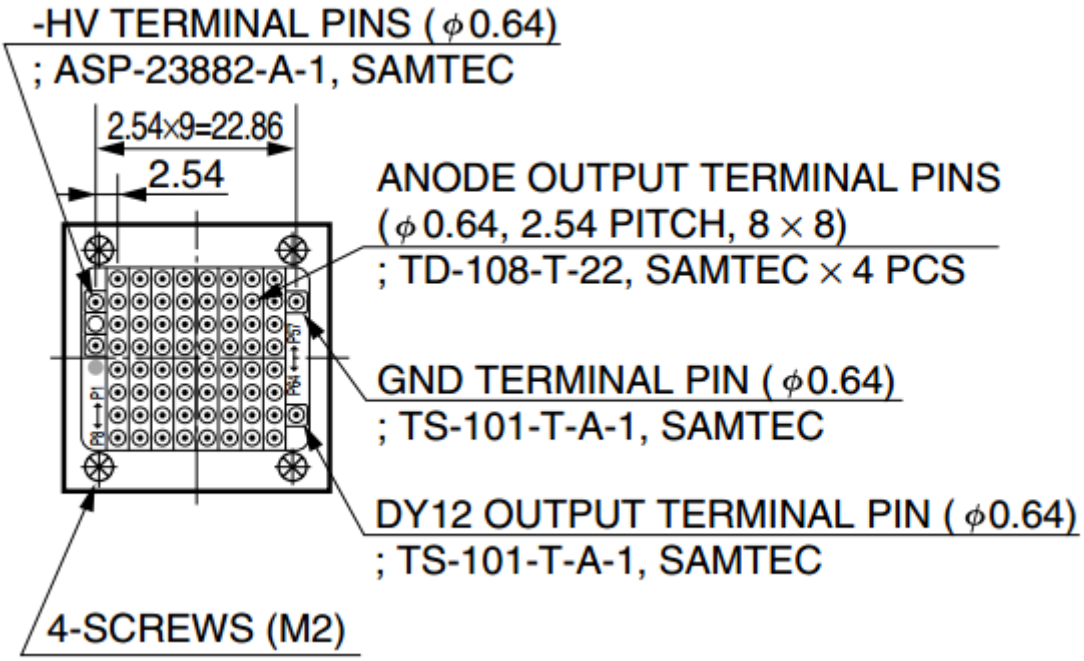


Figure 4-7 MAPMT output distribution

4.4.3 Power Supply

The high voltage power for MAPMT is configured by an input pin. A coaxial cable makes the connection between the HV pin on MAPMT and the SHV connector on the case. The coaxial cable can prevent the EM field interference between the DAQ and the MAPMT.

Chapter 5
Calibration

5.1 Purpose and Procedure

It is crucial to calibrate a system before its real operation. This chapter contains four parts which are related to the calibration procedures needed for phase 1 and phase 2 operations.

The first one is the measurement of fiber transmission loss. Although it can be found in the datasheet, we still need to know the accurate/exact value for each fiber. With this information, we can run quick tests with short fibers and estimate the performance of the BGO system with the 40meter long fibers in BEAST2.

The second one is the gain calibration for MAPMT. The gains for different pixels or at different high voltages are not the same. This is very important part in our calibration procedure. We will calibrate the MAPMT and convert the observed digital results in the unit of photo-electron which is more relevant in physics.

The third one is the background monitoring calibration for phase 1. In phase Ⅰ, we want to detect the real background value in unit of Gy/h for water equivalent material. In order to do so, we need to know the dark current value as the pedestal. We also need to find an officially calibrated strong radioactive source to calibrate our system.

Finally, the last one is the energy scale calibration and random coincidence calibration for phase 2. In phase 2, what we need to do is to separate the real events from the background. From the simulation done by Fa-hui and improved by Terry, we can set an energy threshold to form the back-to-back coincidence trigger. Therefore, it is important to know the conversion constant between photon-electron and GeV. Another thing is that we need to obtain the relationship between the random coincidence rates in back-to-back configuration and those in the non-back-to-back configuration. That calibration can only be done with non-colliding beams.

5.2 Fiber Transmission Loss

We use LED as the light source and MAPMT with oscilloscope as the detector to measure the transmission loss. We measure the voltage peak values with 40m and 3m fibers 5 times to get the average values for each fiber.

The amplitude value for 40m fiber is $479\text{mV} \pm 2.6\%$; for 3m fiber is $542\text{mV} \pm 1.0\%$. The ratio between them is $0.883 \pm 2.8\%$. The loss is $0.539\ dB/37m$. That is $14.6\ dB/km$. The data from the datasheet is $150\ dB/km$ in maximum.

5.3 MAPMT Gain Calibration

5.3.1 Working Theorem

The photon source from LED with the pulse source can be detected by MAPMT and recorded by the readout system. According to "The Single Photon Measurement by Using the Front-End Readout System of Neutrino Telescope" – NTU Master Thesis of Chih-Pao Chang, 2011, the statistical distribution can be modeled as Poisson distribution as below, where P is the possibility; C is the observed charge; G is the average gain; N is the average number of photon-electron.

$$\mathrm{P}(C) = \frac{N^{(C/G)}}{(C/G)!} e^{-N}$$

Gain is a function of high voltage for MAPMT; Number of photon-electrons is decided by the photon source and quantum efficiency of the cathode window.

5.3.2 Setting

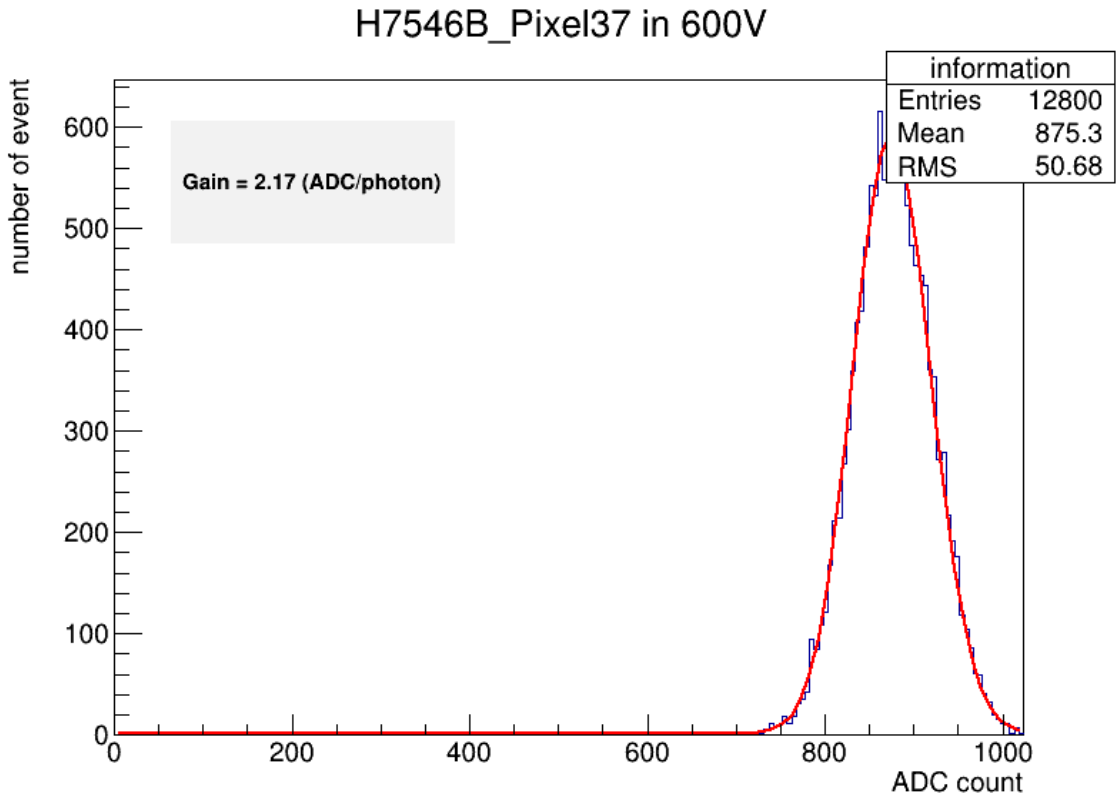
The LED (not BGO crystal) is used as the photon source forced by a step pulse (~6ns/3μs, 2.6V) to shine light on the MAPMT cathode window. We then can get the gain for each high voltage from the above mentioned fit function. After all setting is done, with one high voltage supply linked to MAPMT, there are around 6000 output waveforms from the LED test.

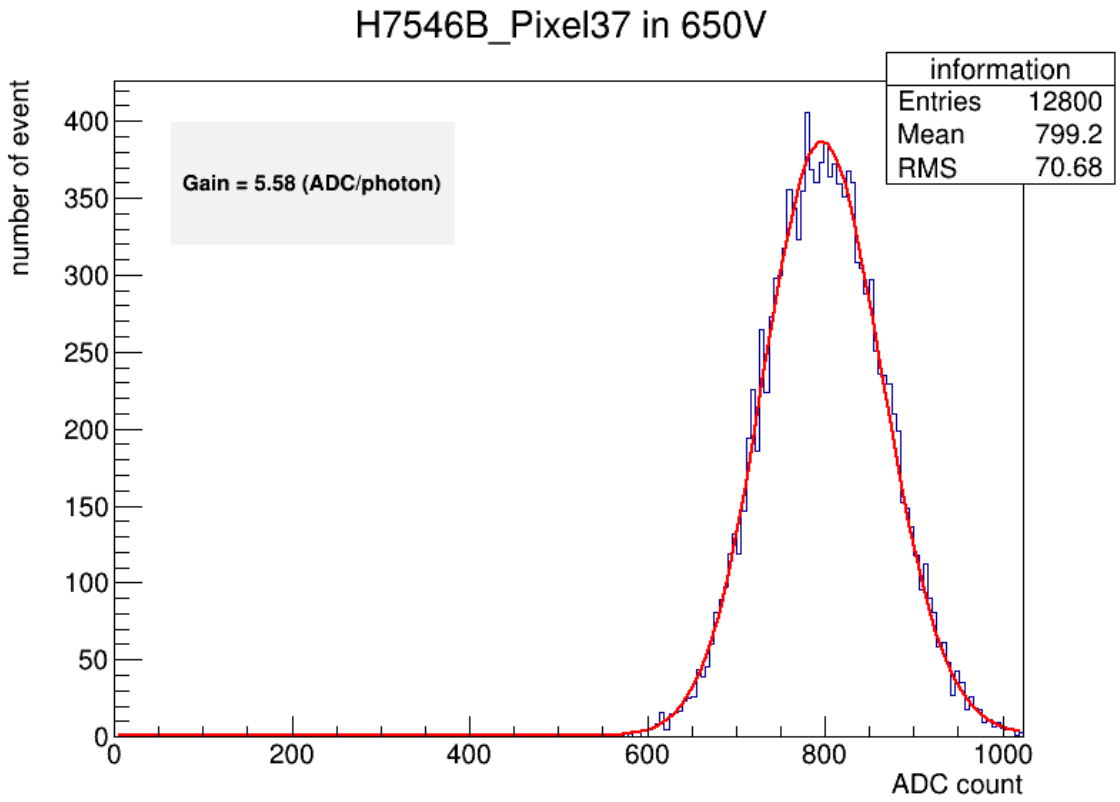
5.3.3 Statistical Software

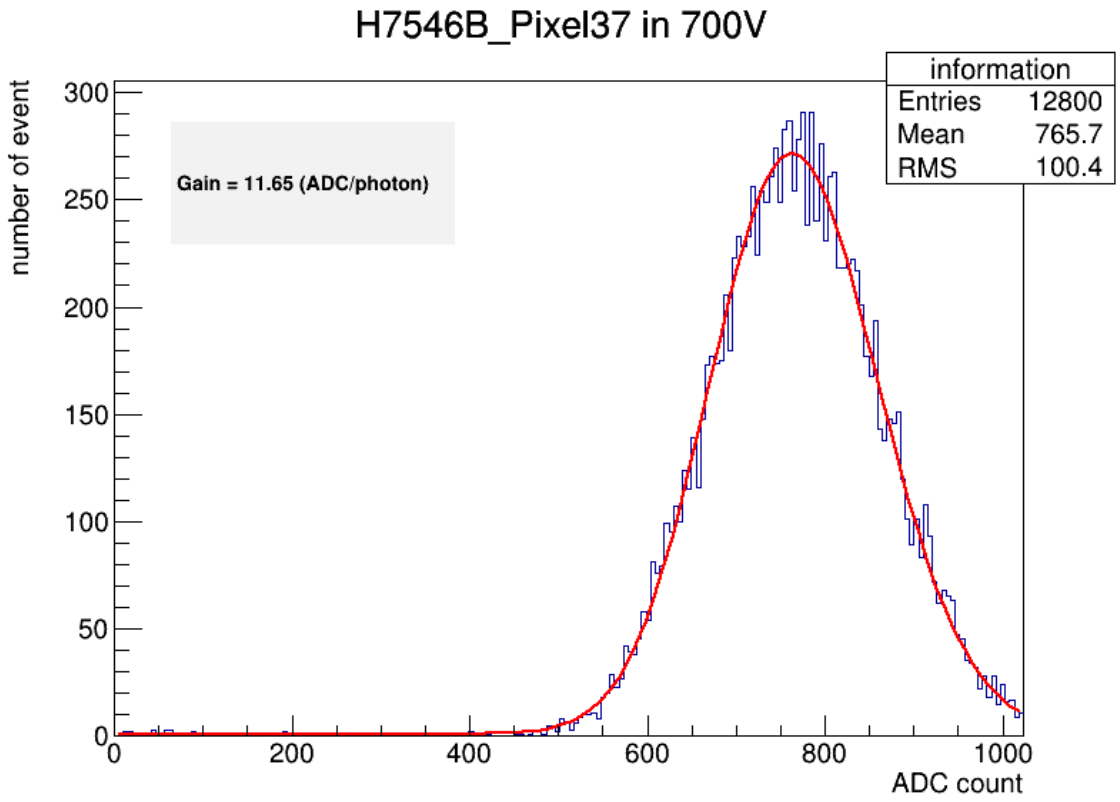
The analysis is done by some after-work. The software is written in Python and coped with Root . With it, one can calculate the charges for different pulses and make the histogram. By fitting the histograms, the gains can be determined by the above fitting model.

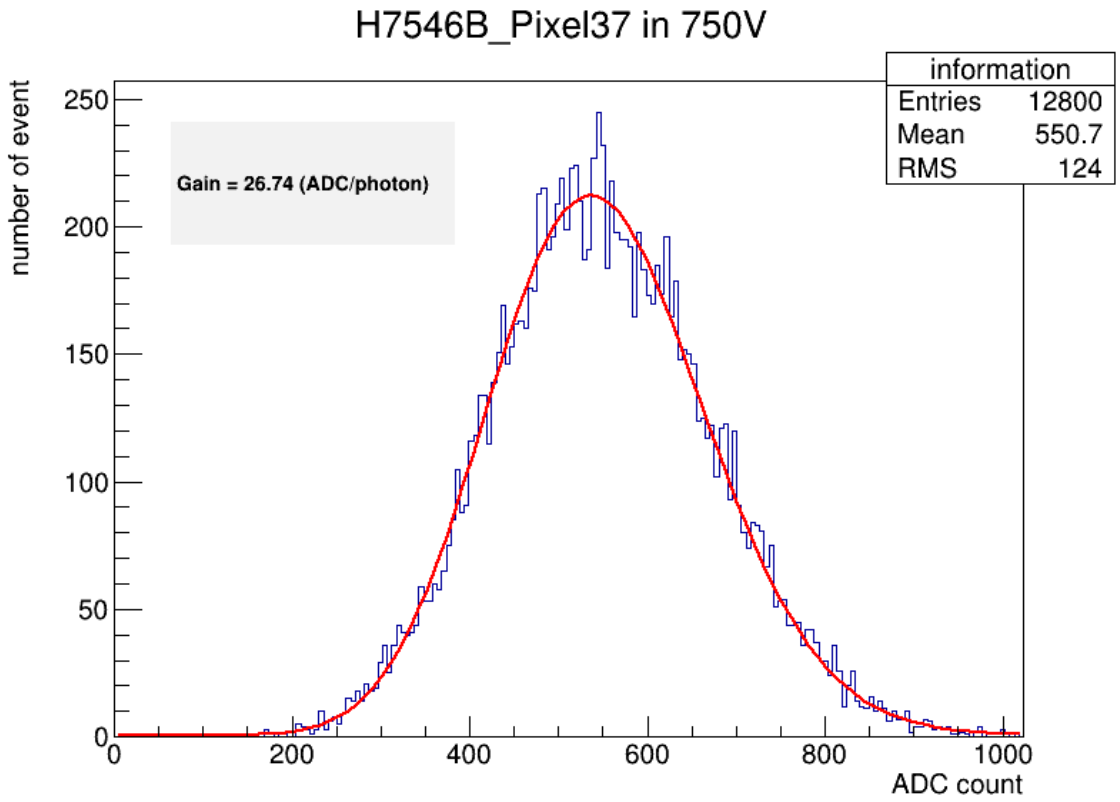
5.3.4 Result and Comparison with Datasheet

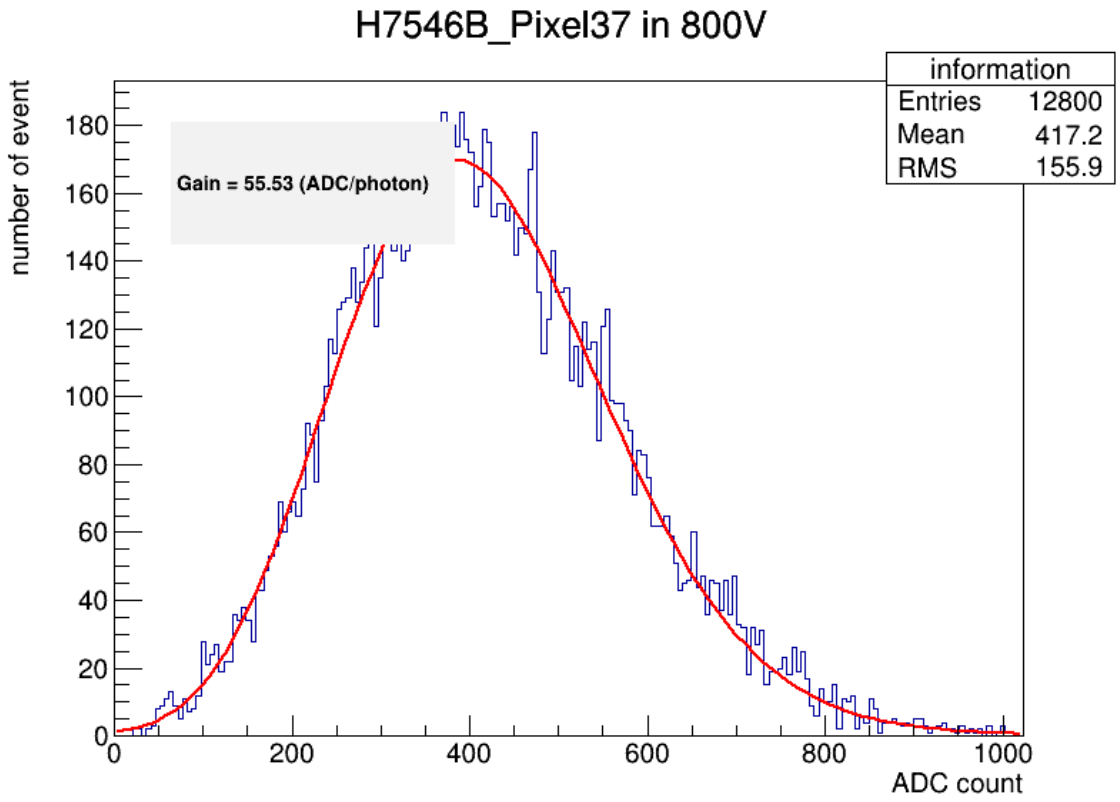
The histograms for each high voltage are shown below. The fitting is pretty good.

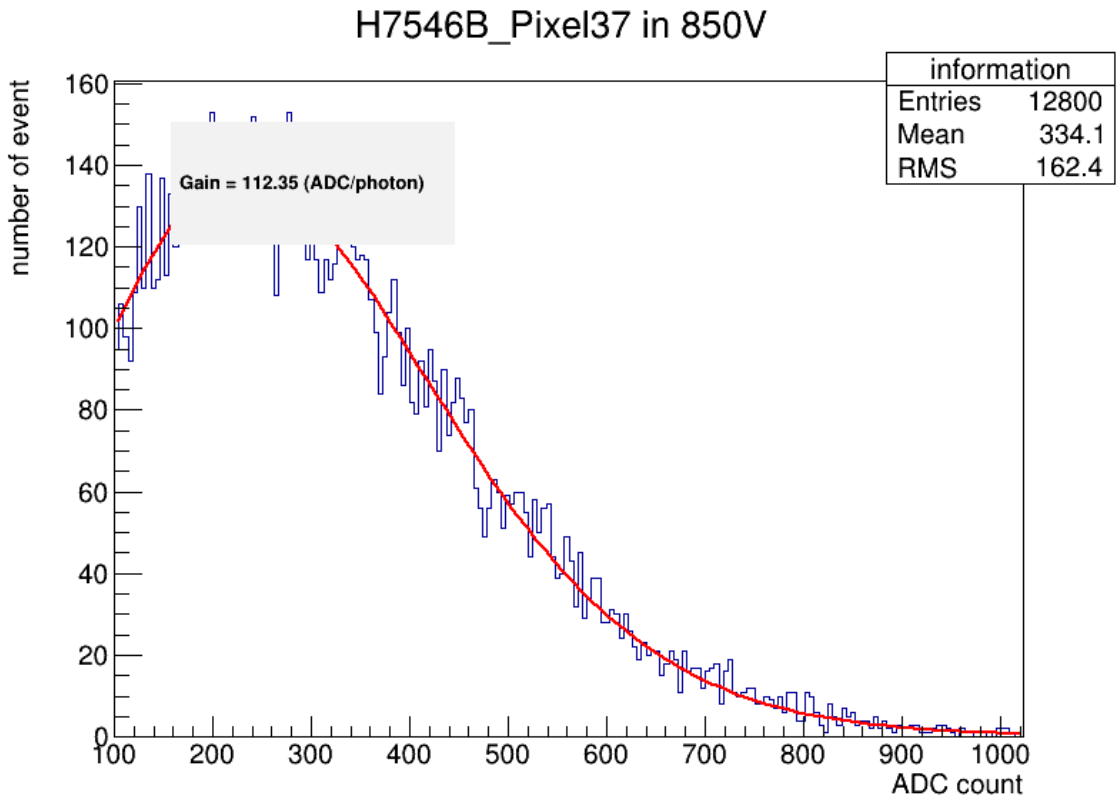



H7546B_Pixel37 in 650V
information
Entries 12800
Mean 799.2
RMS 70.68
Gain = 5.58 (ADC/photon)
number of event
ADC count
0
50
100
150
200
250
300
350
400
0
200
400
600
800
1000


H7546B_Pixel37 in 700V
information
Entries 12800
Mean 765.7
RMS 100.4
Gain = 11.65 (ADC/photon)
number of event
ADC count
0
50
100
150
200
250
300
0
200
400
600
800
1000


H7546B_Pixel37 in 750V
information
Entries 12800
Mean 550.7
RMS 124
Gain = 26.74 (ADC/photon)
number of event
ADC count
0
50
100
150
200
250
0
200
400
600
800
1000


H7546B_Pixel37 in 800V
information
Entries 12800
Mean 417.2
RMS 155.9
Gain = 55.53 (ADC/photon)
number of event
ADC count
0
20
40
60
80
100
120
140
160
180
0
200
400
600
800
1000



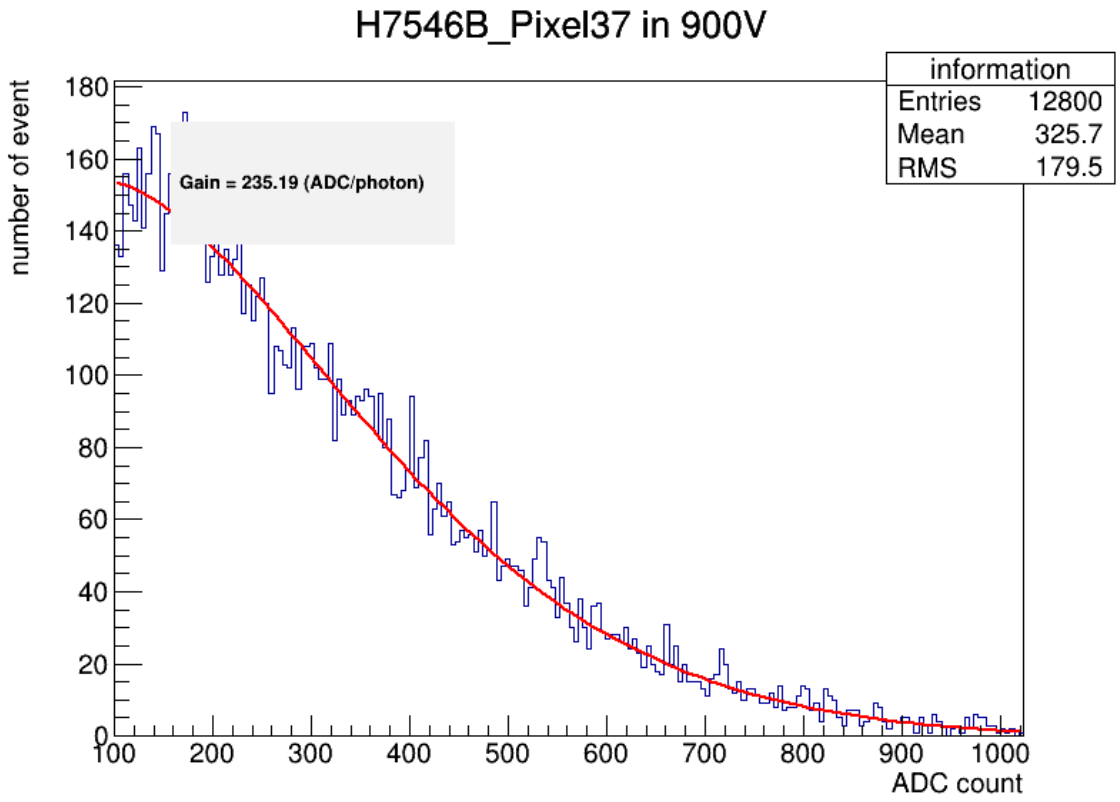
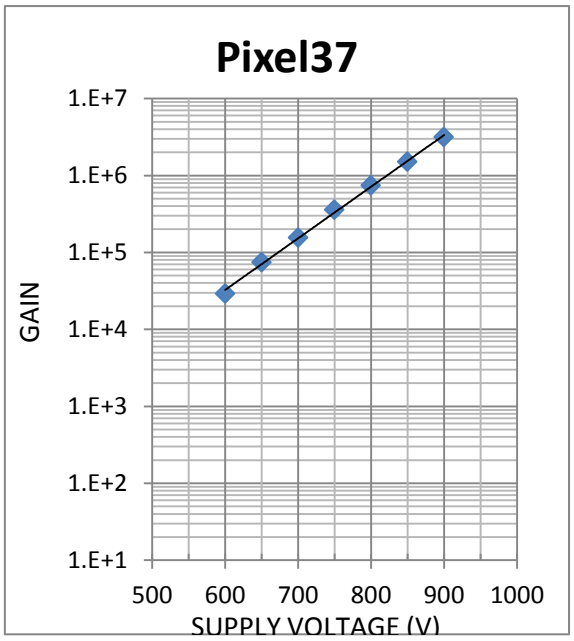


Figure 5-1 Histogram for LED events in different high voltage

From the fitting, we can get the average gains for each high voltage in ADC unit. Since the ADC is for 2V/1023 ADC count and the gain capacitance for Pre-Amp is 1.1pF, we can do some conversion.

$$ADC/_{photon} = \frac{2V}{1023} \times \frac{1.1pF}{1.6 \times 10^{-19}} \ (gain\ with\ no\ units)$$

With the conversion, we can get the gain-supply voltage diagram in half exponential scale.



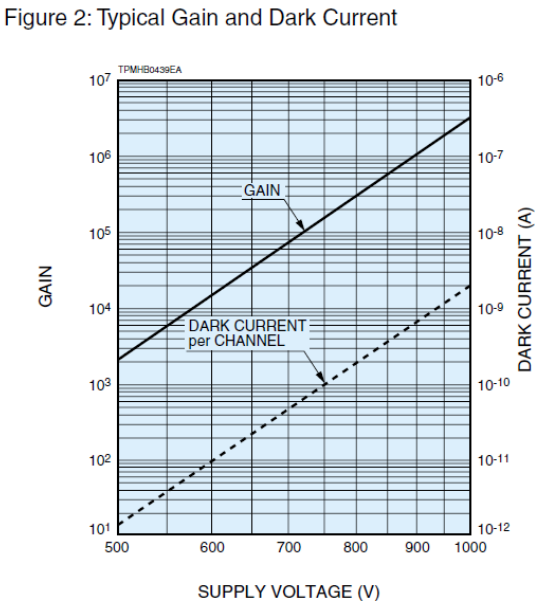


Figure 5-2 Gain calibration result versus the relationship from the datasheet

5.4 Calibration for Background Monitoring

For background monitoring, we once again use a LED driven by a function generator with fixed width to test the system performance. By varying the frequency of the generated pulses, the accumulated charges in fixed time window by our BGO system also responds linearly with respect to the frequency change.

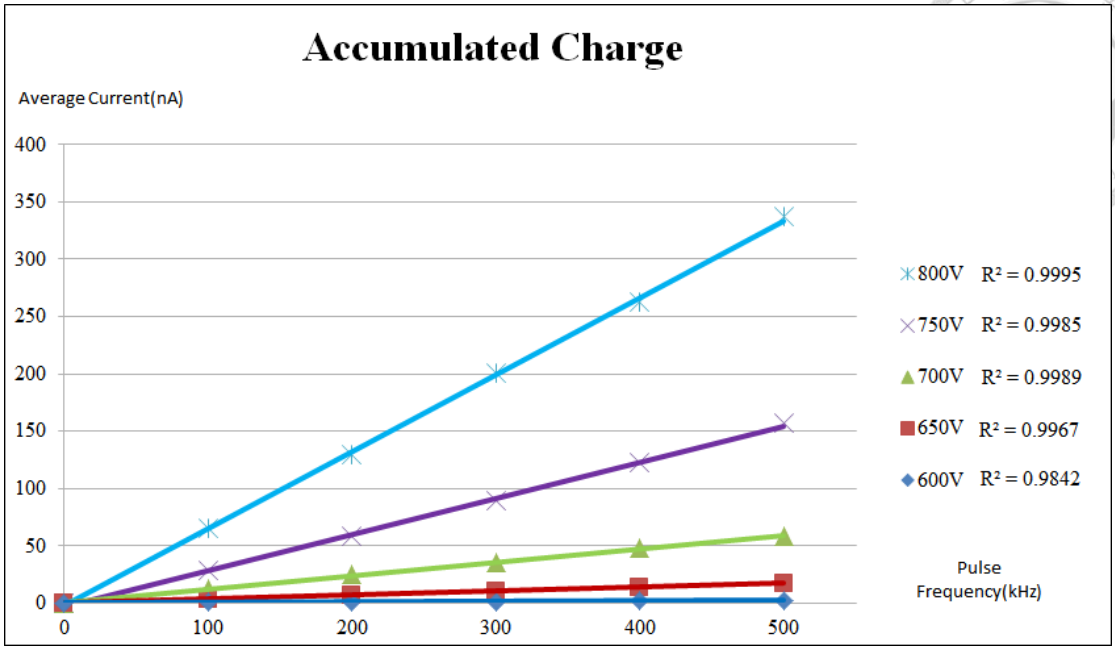
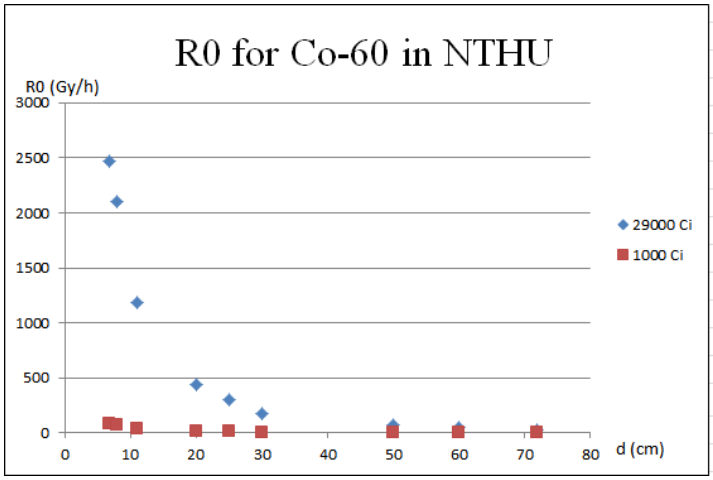


Figure 5-3 Accumulated charge versus pulse frequency

The real calibration will be carried out at NTHU. The following table shows the (expected) absorbed dose for water at different locations with respect to the Co-60 source.

We will put our crystals at different locations and swap them as a systematic check in order to calibrate our system at absolute scale. Note that the accumulated charge by dark current will be pre-determined without the source and subtracted with the source.



	(Gy/h)	(Gy/h)
distance(cm)	29000 Ci	1000 Ci
6.75	2470	87.13
8	2100	74.53
11	1180	39.66
20	440	15.34
25	300	10.43
30	180	7.49
50	70	2.4
60	50	1.64
72	30	0.9
t0	2013/1/9	2013/1/10

$R = R0 * e^{(-\lambda \Delta t)}$

Figure 5-4 Expected absorbed dose data for Co-60 in NTHU [07]

5.5 Dynamic Scale Calibration for Phase 2

5.5.1 Experimental Method

The calibration of the mapped dynamic range between p.e. and absolute energy scale. (GeV) is important for our DAQ. From a quick and rough check, we find that there are not enough photon-electrons for a ^{60}Co source with single fiber connection for transmission. Some changes are needed to get the nominal value for the real measurement and the setup will be described below.

We use a different type of MAPMT which has a much larger receiving area for each pixel. There are 25 fibers used to receive the photons from BGO for each pixel. For convenience, we choose 20 cm fibers. The source is changed from the radioactive source to cosmic rays. In short, a similar system to our BGO system is adopted in order to get the calibration data.

5.5.2 Unimproved Measurement

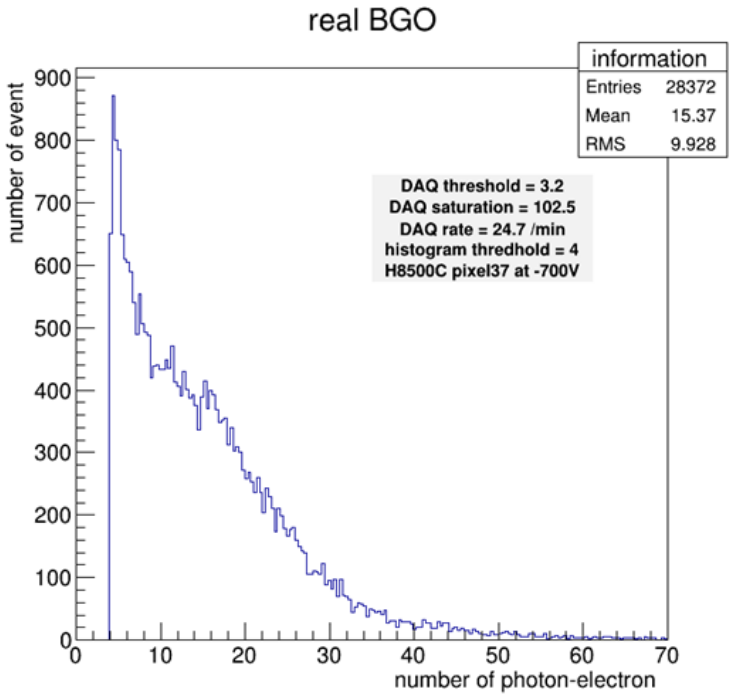


Figure 5-5 Histogram for events with BGO

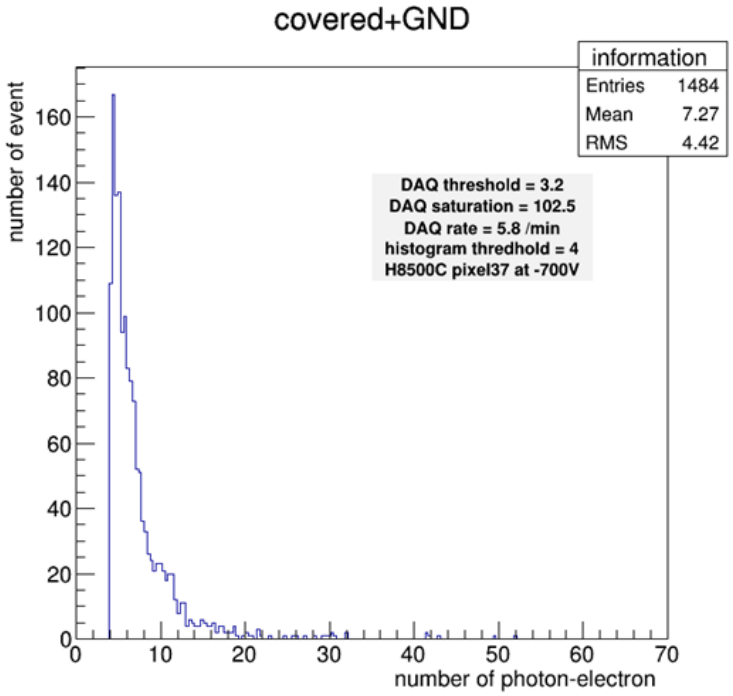


Figure 5-6 Histogram for events without BGO

We can see there's some difference between with BGO and without BGO. However, there're two problems. One is that the background signal is much higher than we think; the other is that we can't control the incidence cosmic trajectory; hence the energy deposited has a larger fluctuation.

5.5.3 Trigger System Added

To improve the experiment, we set a trigger system to solve the problems. The signals from two PMTs are also sent to the same DAQ as trigger signal. —The event will be recorded only when the cosmic ray go through three scintillators.

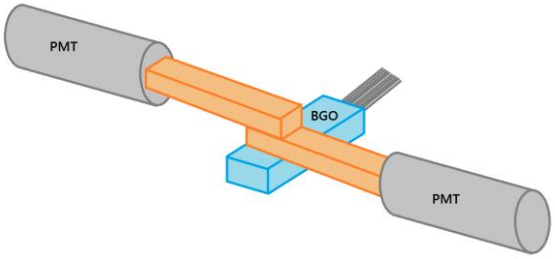


Figure 5-7 Schematic of trigger system

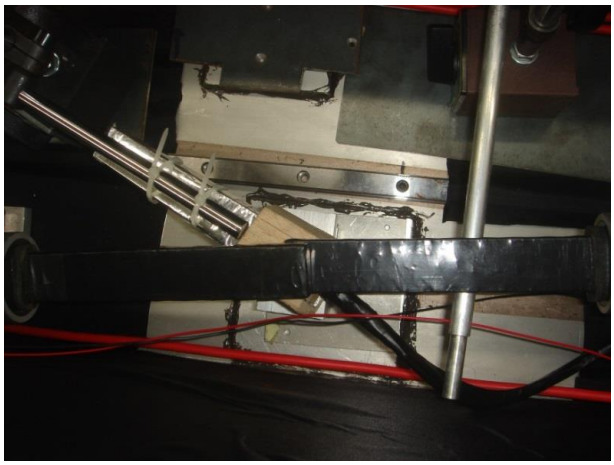


Figure 5-8 Picture of trigger system

With trigger system, the number of events without BGO is much less than the case with BGO. We successfully remove the background interference. In short, we can have a better control of the traveling distance of the cosmic rays. Then, we measure the distributions for both vertical BGO and horizontal one. The distance for these two should be different.

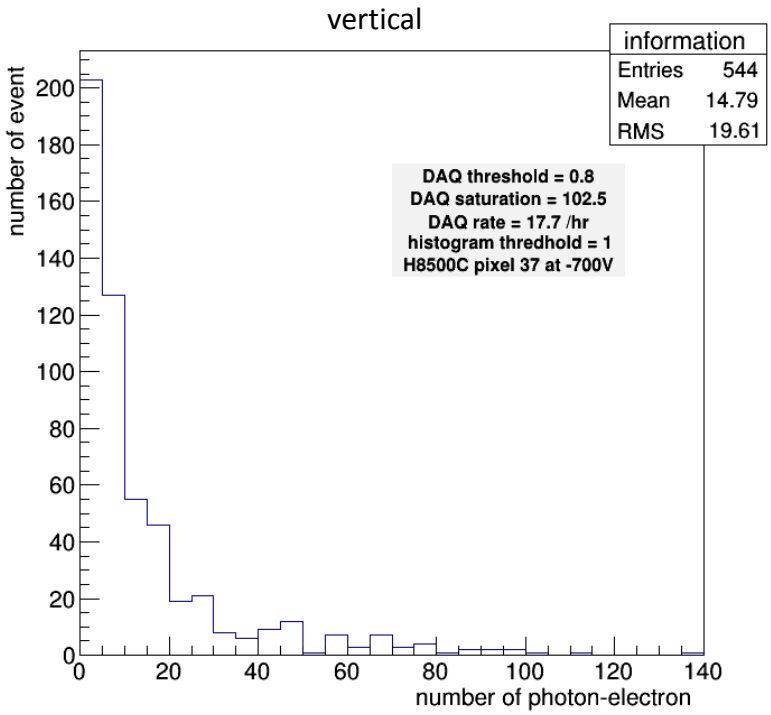


Figure 5-9 Histogram for events with vertical BGO

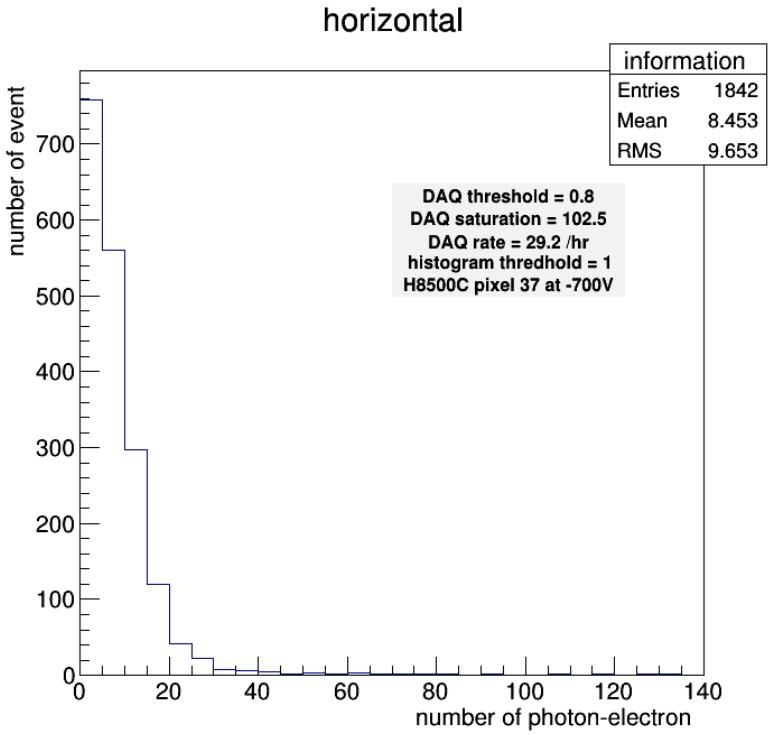


Figure 5-10 Histogram for events with horizontal BGO

Comparing the vertical case and the horizontal case, we can see that the higher photon-electron events for vertical one are much more than the other. We can roughly estimate the scale if we guess the peak in 80 photon-electrons is responded to 15cm path.

5.5.4 Result

Because the setting in calibration is a little bit different from the real case. The number of fibers is 25 times more. There's also more transmission loss for real case. We need to correct them for estimating the scale.

The minimum ionization for BGO is $8.918\ MeV/cm$[08]. So, the scale should be

$$\#\,PE/GeV\ = \frac{1000\ MeV}{8.918\ MeV/cm\ \times 15cm} \times \frac{1\ fiber}{25\ fibers} \times\ 10^{-\frac{14.6\times\frac{40m}{1000m}}{10}} \times 80\ PE$$

$= 20.9\ (PE/GeV)$.

The dynamic scale limit for our BGO system is around 70 to 110 photon-electrons, depended on the gain for different MAPMT pixel. The threshold in our simulation (done by Fa-Hui and improved by Terry) is 0.5 GeV. 10 photon-electrons is a good threshold for us. And, the Bha-bha event energy is fitted with our dynamic scale.

With this calibration data, we can make sure that we can separate the Bha-bha event from the background well. We can also find out the value for threshold.

Chapter 6
Mini-BEAST2

6.1 Purpose

To make sure the installation of all BEAST2 detectors can be done well, the leading group of BEAST2, HEPG at University of Hawaii runs a Mini-BEAST2 program. In it, part of every BEAST2 sub-system will be installed in Hawaii. Some of the detectors are prototype or a partial one. This program helps us to exercise the process of installation, and figure out unforeseeable problems in the mechanical structure and the communication of different systems.

I represented our BGO group to participate in this Mini-BEAST2 effect in late January, 2015.

6.2 Introduction to the Site

Mini-BEAST2 takes space in UH (University of Hawaii) at Manoa. The following are simple descriptions about the experimental site.

6.2.1 The Dark Room

The picture shown below is the building of Department of Physics and Astronomy. The Mini-BEAST2 is installed inside it.

Figure 6-1 Department of Physics and Astronomy

Inside the HEPG lab, there's a dark room. To achieve the darkness, there're some special designs. To avoid the light coming from the outdoor, there's rubber shield under the door, see below.

Figure 6-2 Light shield under the door

There's no any light source except the light for illumination (which can be turn off). So, the monitor and the computer are both outside the room. The signals from the BGO system are transported through a hole on the wall. A black cloth is used to cover the hole when needed.

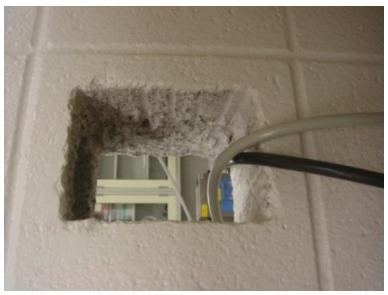


Figure 6-3 Hole between inside and outside of the dark room

There's also power source inside the dark room.

Figure 6-4 Power source in the dark room

6.2.2 Cabinet for Electronics

Lab in UH provides a cabinet for Mini-BEAST2. We can put all the detectors and power supplies in it. Because our BGO system is the first one transported to UH, there's only ours in the top section of the cabinet.

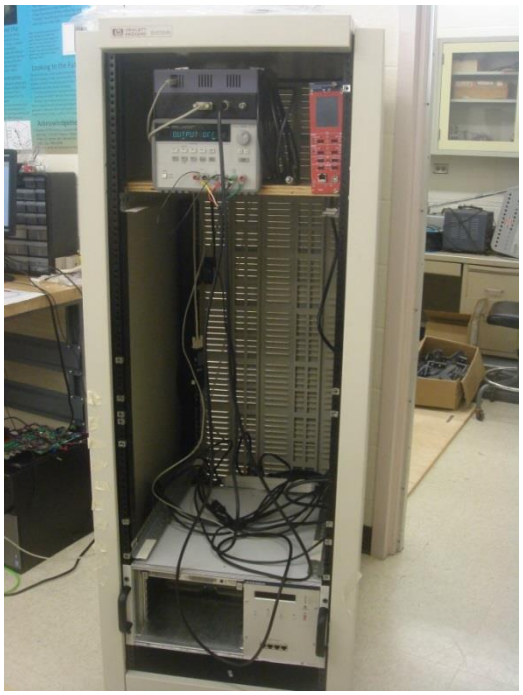


Figure 6-5 Cabinet for electronics

Figure 6-6 There're detector, high voltage power supply and low voltage power supply in the top section of the cabinet

6.2.3 Detector inside the Dark Room

The sensor part of our system should be placed in the dark room. UH team provides the mechanical structure for this Mini-BEAST2. BGO with its holder made by us can be fixed on the structure and the optical fiber can also be connected through the hole on the wall.

Figure 6-7 Mechanical structure in the dark room

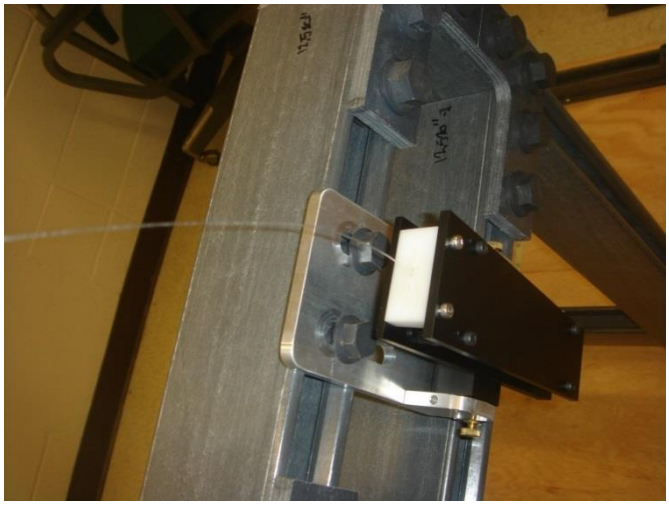


Figure 6-8 BGO crystal with its holder is fixed on the structure

6.3 BGO System in Mini-BEAST2

Two pieces of BGO crystals with supporting frames and a two-channel readout system were brought to UH for the Mini-BEAST2 operation. After some tests of each part, it can run smoothly and the UH group will do the whole Mini-BEAST2 operation with other sub-systems later.

6.3.1 Electronic Part

We first install the electronic part to make sure the system works well. With the cables that I took from NTU (note that there are different connectors and the proper connection cables might not be easy to find in Hawaii), we quickly set up the system. By using the ocilliscope and the test source board, we see the clear pulse as metioned in CH3. Then, we see it with the FPGA part. We quickly conclude that the electronics part works well.

6.3.2 Software Part

After pure hardware test, we try the software integration. We use a python code to com municate with our BGO system and get the data. Although the whole system is tested in NTU, there is still a surprise. After checking, the problem is caused by incompatibility between the code and the operating system about the “comport”. Peter, the one who works with me in UH group, add some new commends to solve this problem. Then, we can use the software to get data successfully. We design two kinds of codes. One is to get each single event’s waveform and the other is to get the accumulated charges in a fixed time period. Both functions of our DAQ work well.

6.3.3 Optical Part

With the rough result about the energy calibration, we know that we can't see the cosmic event or the low energy radiative source. So, we set a LED with a function generator as the light source. We can see the events in both readout schemes. However, we find that the light tightness problem is a little bit terrible. It also provides me a good experience for improving the light tightness.

6.4 Achievement and Contribution

We successfully set up the prototype of our BGO system. It's also an important experience for us to install the system in the real BEAST2. It also shows the compactness of our system. On the other hand, it provides us a chance to test and find out some potential problems before the real BEAST2 operation. Most importantly, by this Mini-BEAST2 integration, we can make sure that there's no major problem of our BGO system.

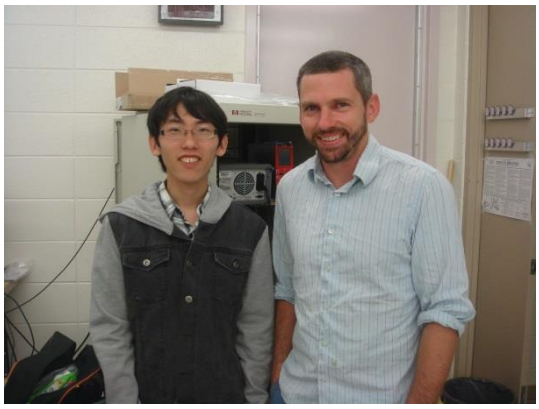


Figure 6-9 Peter, major worker with me in UH

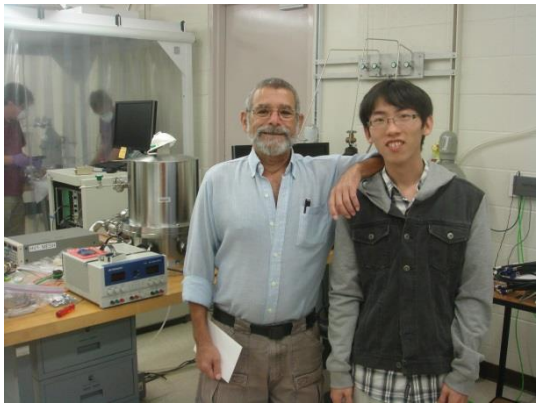


Figure 6-10 Marc, mechanic expert in UH for BEAST2

Chapter 7
Conclusion

The BGO background and luminosity monitor is made for SuperKEKB commissioning BEAST2 in phase 1 and phase 2. With the simulation result, I have finished the hardware works for BGO system. There're 8 BGO crystals as the scintillators, 40m long fibers and a DAQ for it. According to the simulation results and the calibration for the system, we get the important parameters and make sure it works well.

For phase 1, the whole system can work linearly. After the coming calibration in NTHU, we will get the absolute scale. With the scale, it can work in the phase 1 as the background monitor.

For phase 2, the scale is 20.9 photon-electrons per 1 GeV deposited in BGO. The saturation limit is around 70 to 110 photon-electrons. Energy of 0.5GeV is a good threshold to separate the Bha-bha events from background in order to count the back-to-back rate as the luminosity monitor.

The BGO system will be installed in KEK in the September of 2015. The phase 1 will start in early 2016 and phase 2 will begin to run after phase 1.

Appendix

A.1 Equipment

1. DPO 7354C - Tektronic

   4CH digital oscilloscope

2. TDS 3032B - Tektronic

   2CH digital oscilloscope

3. AFG 3252 - Tektronic

   2CH function generator

4. GPD-3303S - GWINSTEK

   3CH low voltage power

5. DT-5533m

   4CH(2+ &2-) high voltage power supply

6. Travel Logic - Acute

   36 terminals logic analyzer

7. DM-1230 - HILA

   Multimeter

A.2 Logo of Organizations

A.2.1 NTU

A.2.2 NTU HEPLAB

NTU
HEPLAB

A.2.3 BGO group

A.2.4 SuperKEKB

A.2.5 Belle2

A.2.6 Beast2 group

Bibliography

B.1 Papers and Books

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[02] “Belle2” (Official Webpage), http://belle2.kek.jp

[03] Fa-Hui Lin, “Design and Simulation of BGO Background/Luminosity Monitor in BEAST2 for SuperKEKB Commissioning”, Master Thesis (2014).

[04] Kun-Xian Huang, “Front-End Readout System of Neutrino Telescope”, Master Thesis (2007).

[05] Chih-Pao Chang, “The Single Photon Measurement by Using The Front-End Readout System of Neutrino Telescope”, Master Thesis (2011).

[06] John H. Moore, Christopher C. Davis, Michael A. Coplan **“**A Practical Guide to Design and Construction”, 2nd edition (1989).

[07] “Nuclear Science & Technology Development Center”, http://www.nstdc.nthu.edu.tw/

[08] “Particle Data Group”, http://pdg.lbl.gov/

B.2 Datasheets

[01] BGO - Amcrys

[02] SK-40 - Eska

[03] H7546B - Hamamatsu

[04] H8500 - Hamamatsu

[05] AD8067 - Analog Devices

[06] AD9203 - Analog Devices

[07] KC5032C-C3 - Kyocera

[08] PI49FCT3805 - Pericom

[09] Lt1117 - Linear Technology

[10] EDK_GKB_3S400AN/700A - E-elements Technologies

[11] DS557 - Xilinx