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應用於無線通訊之瓦級高功率密度變壓器功率結合式 LDMOS 功率放大器之研製

Research of Watt-Level High Power Density Transformer Combined LDMOS Power Amplifier for Wireless Communication

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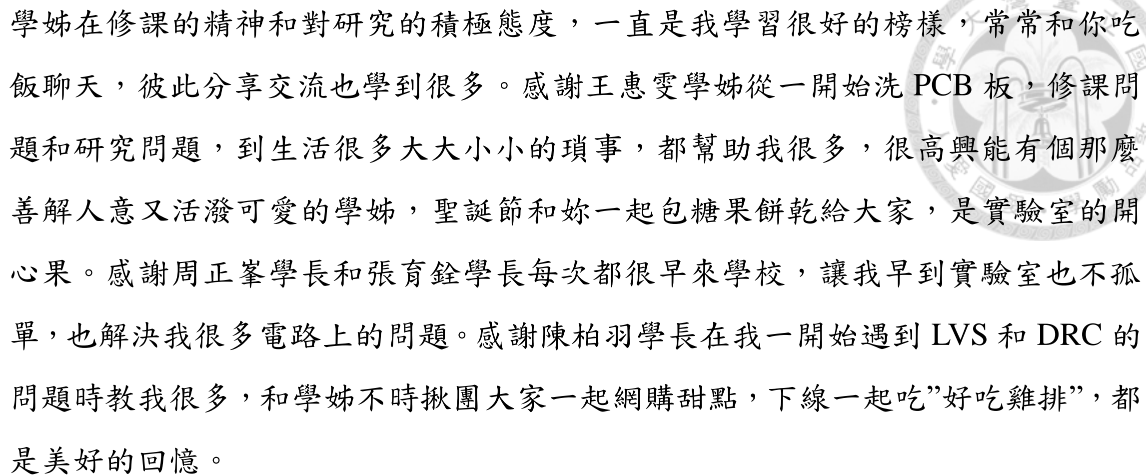

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摘要

半導體製程的演進隨著無線通訊系統的發展，以互補式金氧半場效電晶體(CMOS)實現具成本優勢的射頻電路逐漸成為市場焦點，其中功率放大器是收發機中最關鍵的電路。本論文將著重於橫向擴散金屬氧化物半導體(LDMOS)技術研製，因著高崩潰電壓，分別設計了兩顆 40 奈米製程的功率放大器。第一顆電路是以達到功率放大器之高功率密度的優點，大幅減小晶片面積以節省成本。第二顆電路為瓦級之高輸出功率的功率放大器，隨著高傳播速率和遠距離的需求，達到 3.5-GHz 頻段使用 CMOS 的製程，以提高電路整合性和降低成本。

在第三章，以 40 奈米互補式金氧半場效電晶體製程實現一個 3.5-GHz LDMOS 的變壓器功率結合式功率放大器。此運用頻段為 4G/LTE 手機通訊晶片，上傳頻寬為 80MHz，是由 3410MHz 到 3490MHz，中心頻率為 3450MHz。LDMOS 常被應用在設計給基地台使用的射頻功率放大器，原因是藉由較高的跨壓以滿足高輸出功率。為了降低晶片面積，功率放大器的功率核心使用變壓器以同時達成功率結合、阻抗匹配以及單端與差動訊號的轉換。在選擇較大的電晶體時，電晶體在柵極和漏極之間固有的電容也隨之增大，造成放大器不穩定的現象，插入一對中和電容不僅可以消除柵極和漏極之間的電容，以提高功率放大器的穩定性，同時也能達到提高增益的效果。此功率結合的功率放大器是目前此頻段附近的互補式金氧半場效電晶體最高的高功率密度，輸出功率可達到 26.5dBm 最大的輸出功率的設計，面積僅佔 0.259 平方毫米，可達到 1724mW/mm^2 的飽和輸出功率的高功率密度，以及 992.4mW/mm^2 的 OP$_{1dB}$ 輸出功率的高功率密度。

在第四章中，以 40 奈米互補式金氧半場效電晶體製程實現一個具三維結構之 3.5-GHz 瓦等級變壓器功率結合式功率放大器。為了達到近瓦等級的輸出功率，採用放射狀功率分配器及放射狀功率合成器將四路功率核心的功率結合輸出，因輸入端的分配器較不需考量損耗，走線同時具有阻抗轉換的功能以降低輸入端匹配網路的阻抗轉換比，而輸出端的合成器相對需要考量輸出功率，用最短距離的走線以降低損耗。藉由將放射狀功率分配器及合成器在電路的中央以三維結構垂直共用同一區域，突破以往二維功率結合技術的瓶頸，且可以在不用妥協和不受頻段限制的情況下同時達到電路佈局的對稱性和阻抗選擇的自由度，大幅減小功率

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分配器以及功率合成器的占用面積，達到縮小晶片面積的目的。此瓦級的三維架構功率結合的功率放大器是目前 3.5-GHz 頻段中，使用 CMOS 製程達到最高至瓦級的輸出功率，此輸出功率最高可達到 31.26 dBm。

關鍵字：功率放大器、橫向擴散金屬氧化物半導體、變壓器結合、高輸出功率、高電壓操作、高功率密度、40 奈米互補式金氧半場效電晶體製程。

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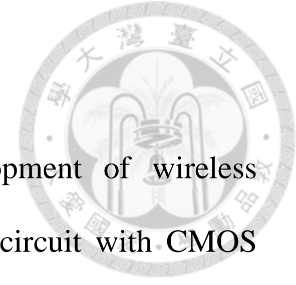

ABSTRACT

With the evolution of semiconductor process and development of wireless communication system, implementing radio frequency integrated circuit with CMOS becomes the focus point of industry market. In the transceiver design, power amplifier is the most critical and significant component. This thesis emphasizes the design and analysis of laterally diffused metal oxide semiconductor (LDMOS). Due to the high supply voltage, two LDMOS power amplifiers in 40-nm process are designed and analyzed separately. The first power amplifier design achieves high power area density to reduce the chip area and cost effective. In order to target the demand of high data rate and long distance, the second power amplifier design obtains a watt-level high output power that becomes high output power performance in 3.5-GHz band that is in CMOS process to raise circuit integrity and reduce cost.

In chapter 3, a compact 3.5-GHz transformer combined power amplifier with LDMOS transistors is designed in 40-nm CMOS process. This frequency band can be applied in 4G/LTE mobile devices, where has 80MHz bandwidth for uploading from 3410MHz to 3490MHz with the central frequency of 3450MHz. LDMOS is usually used in the design of RF power amplifiers in the base station since the high breakdown voltage provides high output power. In order to reduce the chip size, the power cells of power amplifier use transformer to do power combining, impedance matching and single-to-differential ended simultaneously. Larger device selection will bring larger gate-to-drain capacitance and it will make power amplifier instable. The neutralization capacitor can degrade the gate-to-drain capacitance, and effectively increase the stability and gain for power amplifier design. This power amplifier is the highest power density about the frequency bands in the recent power amplifiers of CMOS process. The

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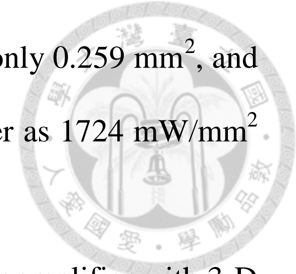

output power can reach the highest performance as 26.5 dBm with only 0.259 mm^2, and achieves in the highest power area density of saturated output power as 1724 mW/mm^2 and the highest power area density of OP_{1dB} as 992.4 mW/mm^2.

In chapter 4, a 3.5-GHz watt-level transformer combined power amplifier with 3-D architecture implements in 40-nm CMOS process. For watt-level output power design, 4-ways power combining is realized by the shortest path for the radial power combiner and longer path for the radial power splitter. The long path of input splitter can also reduce the impedance transform ratio of input matching network. By sharing the same area vertically in 3-D architecture, the occupied area of radial power combiner and power splitter can be minimized significantly. This technique breaks the bottle neck of the conventional 2-D power-combined techniques that achieves the symmetry of circuit layout and flexibility of impedance transformation without compromising and limiting in various conditions of different frequency bands. This watt-level 3-D architecture transformer-combined power amplifier achieves the highest output power in CMOS process among the recent published 3.5-GHz band power amplifiers. The maximum output power can be achieved in 31.26 dBm of high output power performance.

Index Terms – Power amplifier, LDMOS, Transformer combining, High power, High operating voltage, High power area density, 40-nm CMOS process.

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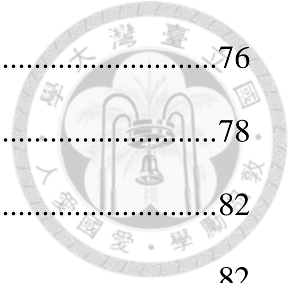

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Chapter 1 Introduction

1.1 Background and Motivation

According to the rapid development of deep-submicrometer CMOS technology, the high operating frequency of CMOS technology has propelled their applications into radio frequency and microwave systems. The massive requirement of commercial wireless communication makes CMOS technology become a desirable choice for low manufacturing cost and integration capability. The applications in CMOS process are high yield and convenience with integrating with digital and analog circuit designs.

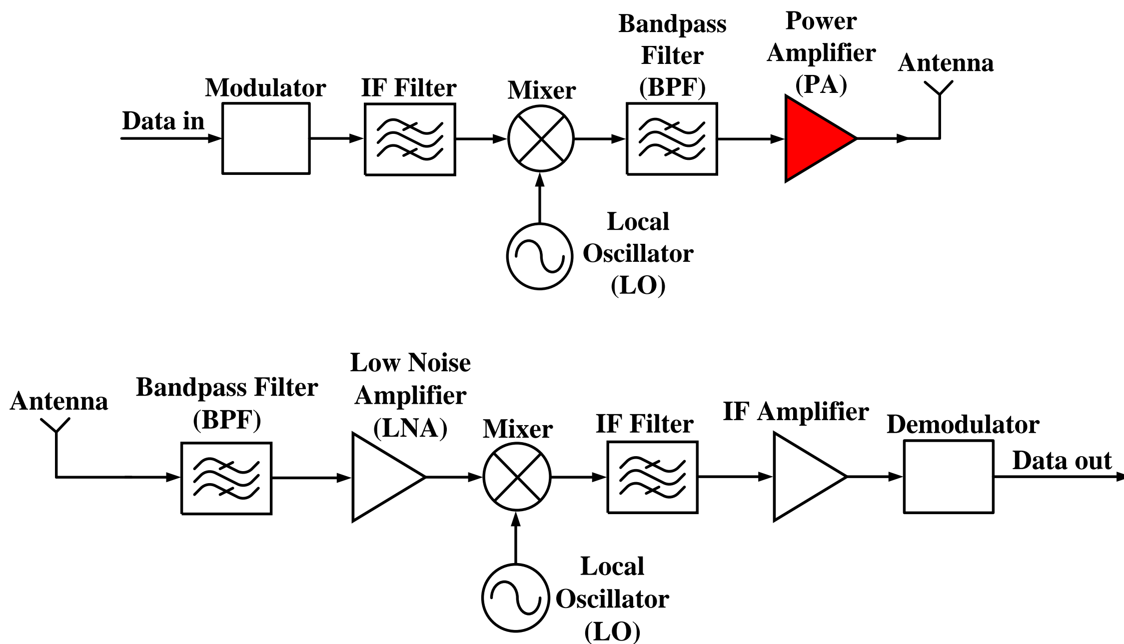

Figure 1.1 Block diagram of wireless communication system

Simple block diagrams of transceiver and receiver sides in a wireless communication system is illustrated and shown as in Figure 1.1. Power amplifier is used for amplifying RF signal to the antenna which becomes one of the most important components in a transmitter. The output power is a dominate issue in the power amplifier design consideration since the high output signal delivers to the antenna will

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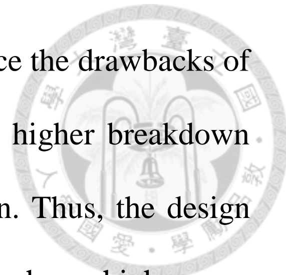
provide the longer communication distance and higher data rate. Since the drawbacks of low breakdown voltage and lossy substrate in CMOS process, the higher breakdown voltage of LDMOS device is induced for high output power design. Thus, the design topic of this thesis is high output power in a compact area which reaches a high power area density, and a large number of power combining cells achieve in a watt-level output power performance.



Band	UL (MHz)	DL (MHz)	Simp. BW (MHz)	Total BW (MHz)	Mode	Notes
1	1920 - 1980	2110 - 2170	60	120	FDD	EMEA, Japan
2	1850 - 1910	1930 - 1990	60	120	FDD	Quad band GSM
3	1710 - 1785	1805 - 1880	75	150	FDD	Quad band GSM. DCS 1800
4	1710 - 1755	2110 - 2155	45	90	FDD	AWS
5	824 - 849	869 - 894	25	50	FDD	Quad band GSM
6	830 - 840	875 - 885	10	20	FDD	Not applicable to 3GPP
7	2500 - 2570	2620 - 2690	70	140	FDD	EMEA
8	880 - 915	925 - 960	35	70	FDD	Quad band GSM. GSM 900
9	1749.9 - 1784.9	1844.9 - 1879.9	35	70	FDD	1700 MHz. Japan
10	1710 - 1770	2110 - 2170	60	120	FDD	Extended AWS
11	1427.9 - 1452.9	1475.9 - 1500.9	25	50	FDD	1.5 GHz Lower, Japan
12	698 - 716	728 - 746	18	36	FDD	Lower 700 MHz, C Spire+USCC-LTE
	N/A	716 - 722	6	6	DL only	Originally Ch.55 for QCOM mDTV venture - MediaFLO. Spectrum was sold to AT&T.
13	777 - 787	746 - 756	10	20	FDD	Upper 700 MHz, VzW-LTE
14	788 - 798	758 - 768	10	20	FDD	US FCC Public Safety
15	1900 - 1920	2600 - 2620	20	40	FDD	
16	2010 - 2025	2585 - 2600	15	30	FDD	
17	704 - 716	734 - 746	12	24	FDD	AT&T-LTE
18	815 - 830	860 - 875	15	30	FDD	Japan 800 MHz Lower
19	830 - 845	875 - 890	15	30	FDD	Japan 800 MHz Upper
20	832 - 862	791 - 821	30	60	FDD	800 MHz EMEA
21	1447.9 - 1462.9	1495.9 - 1510.9	15	30	FDD	1.5 GHz Upper, Japan
22	3410 - 3490	3510 -3590	80	160	FDD	3.5G
24	1626.5 - 1660.5	1525 - 1559	34	68	FDD	
25	1850 - 1915	1930 - 1995	65	130	FDD	AWS-G. Sprint LTE within this band
	1915 - 1920	1995 - 2000	5	10	FDD	AWS-H, will be auctioned by Feb. 2015.
26	814 - 849	859 - 894	35	70	FDD	Sprint / Nextel iDen
27	807 - 824	852 - 869	17	34	FDD	Lower 850 MHz
28	703 - 748	758 - 803	45	90	FDD	700 MHz APAC
	2000 - 2020	2180 - 2200	20	40	FDD	Dish Network to deploy LTE-A by 2016.
33	1900 - 1920		20		TDD	
34	2010 - 2025		15		TDD	China Mobile (CM) TD-SCDMA
35	1850 - 1910		60		TDD	
36	1930 - 1990		60		TDD	
37	1910 - 1930		20		TDD	
38	2570 - 2620		50		TDD	European - TD-LTE
39	1880 - 1920		40		TDD	CM TD-SCDMA
40	2300 - 2400		100		TDD	CM TD-LTE
41	2496 - 2690		194		TDD	TDD 2.5 GHz
42	3400 - 3600		200		TDD	TDD 3.5 GHz
43	3600 - 3800		200		TDD	TDD 3.6 GHz
44	703 - 803		100		TDD	700 MHz APAC

Figure 1.2 Global frequency band for 4G/LTE (long-term evaluation) development [56]

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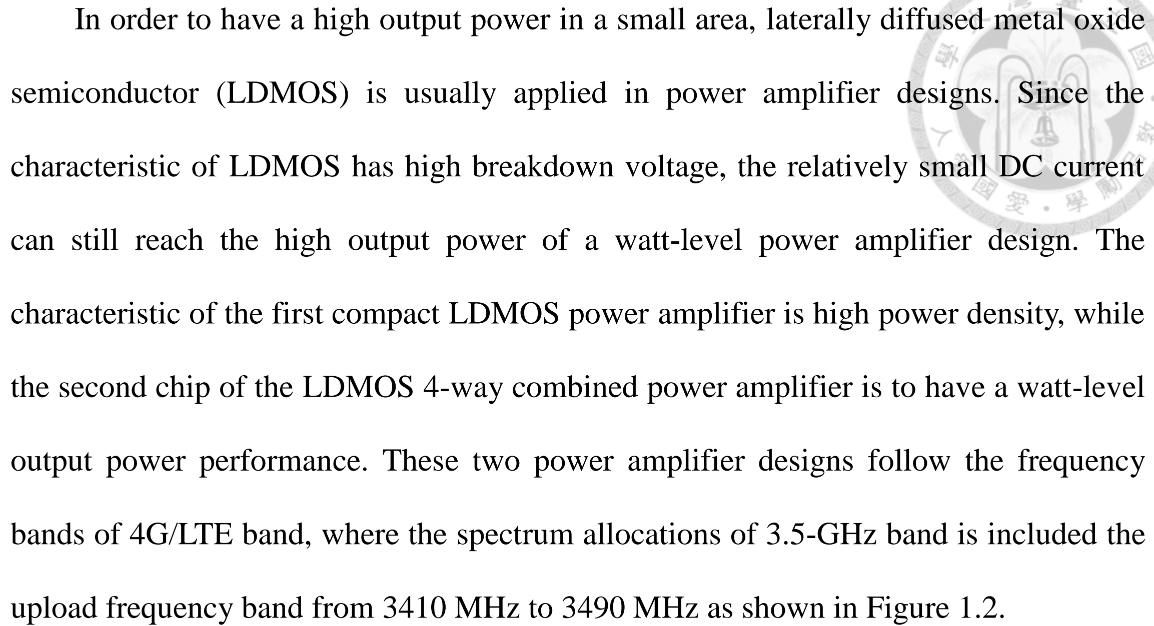

In order to have a high output power in a small area, laterally diffused metal oxide semiconductor (LDMOS) is usually applied in power amplifier designs. Since the characteristic of LDMOS has high breakdown voltage, the relatively small DC current can still reach the high output power of a watt-level power amplifier design. The characteristic of the first compact LDMOS power amplifier is high power density, while the second chip of the LDMOS 4-way combined power amplifier is to have a watt-level output power performance. These two power amplifier designs follow the frequency bands of 4G/LTE band, where the spectrum allocations of 3.5-GHz band is included the upload frequency band from 3410 MHz to 3490 MHz as shown in Figure 1.2.

1.2 Literature Surveys

The literature surveys include compact PAs and watt-level PAs in 3.5-GHz band for the application of 4G/LTE.

1.2.1 High Power Area Density PAs

A huge market in the mobile devices rapidly grows in the 21st century, and the high data rate in a thin device becomes a trend of this market. Due to the high yield and low cost, CMOS process becomes very popular for designers. This power amplifier has high breakdown voltage device of LDMOS that helps with designing low frequency band in an advance process of 40-nm CMOS technology. The power device can provide a high output power in only one power cell; as a result, it does not require many combinations to reach high output power in a certain chip area. In Table 1-1, there are recent published power amplifiers in the frequency bands that are close to 3.5 GHz and are fabricated in CMOS process. In order to identify this feature of this LDMOS device can

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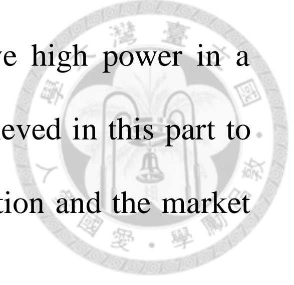

be a good model for power amplifier design, the target is to have high power in a compact chip area. Hence, the high power area density will be achieved in this part to proof the characteristic of this power device for low-cost consideration and the market trends.

Table 1-1 Previously Reported CMOS PAs in the Relevant Bands

Ref.	[4] 2011 JSSC	[23] 2009 APMC	[24] 2010 TMTT	[25] 2015 ISSCC	[26] 2009 JSSC	[27] 2012 JSSC
Process	0.18 µm CMOS	0.13 µm CMOS	90 nm CMOS	65 nm CMOS	90nm CMOS	0.18 µm CMOS
f_o (GHz)	2.5	2.5	2.5	2-6	2.3~2.7	2.4
Class/Stage	AB/2	AB/2	AB/1	AB/2	AB/2	AB/2
Vdd (V)	3.3	3.3	3.3	1.8/3.3	3.3	3.3/3.2
P_{sat} (dBm)	31	25.5	32	22.4	30.1	34
PAE(%)	34.8	32	48	28.4	33	34.9
OP_{1dB} (dBm)	28	21.4	29.5	20.7	27.7	31.5
Gain (dB) per stage	15.65	15.5	18	11.8 ±0.4	14	11
$Area_{core}$*/ $Area_{power\ stage}$** (mm^2)	1.57/ 1.09	2.52/ 1.92	1.95/ 1.95	0.75/ 0.7	3.57/ 2.59	3.045/ 1.825
$P_{sat}PAD_{core}$#/$PAD_{power\ stage}$## (mW/ mm^2)	801/ 1154.7	140.8/ 185	812.8/ 812.8	231/ 248.2	286.6/ 395	824.9/ 1376
OP_{1dB} $PAD_{core}$$/$PAD_{power\ stage}$$$ (mW/ mm^2)	401.9/ 578.9	54.8/ 72	457.1 / 457.1	86.08/ 167.8	164.9/ 227.4	463.9/ 774

*chip area without pad ** power stage area from chip photo #$P_{sat}/Area_{core}$

##$P_{sat}/Area_{power\ stage}$ $$OP_{1dB}/Area_{core}$ $$ $OP_{1dB}/Area_{power\ stage}$

1.2.2 Watt-Level PAs

Due to the demands of the market in wireless communication, a watt-level design of power amplifiers can satisfy with the requirement of long distance and high data rate. In the recent reported power amplifiers of watt-level design that shows in Table 1-2, the high supply voltages are used for increasing the breakdown voltage of the power

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amplifier. The stacked topology is induced for high supply voltage such that 8V and 12 V in [31], and 15V in [32]. In the paper of [33], the Doherty design technique provides good linearity as postponing the P_{1dB} and makes it close to the peak PAE. It also uses 5V for its supply voltage. The reason of using high breakdown voltage for a watt-level design is to reduce the current in each power cell. The previously reported power amplifiers in the frequency band of 3.5 GHz do not have CMOS process. As a result, the advanced process in 40-nm CMOS technology with the high breakdown voltage device of LDMOS transistor is worth to try in this frequency band.

Table 1-2 Previously Reported PAs in 3.5-GHz and the Relevant Bands

Ref.	Process	f_o (GHz)	P_{sat} (dBm)	Peak PAE (%)	OP_{1dB} (dBm)	Gain (dB)
[31] 2012 MWCL	2 μm GaAs HBT-HEMT	3.5-6.5	27	38	26.4	13.5
[31] 2012 MWCL	0.5 μm GaAs HBT-HEMT	3.5-6.5	29.4	27.2	29.1	11
[32] 2007 IMS	2 μm GaAs HBT	4.5-5.8	29	38	26	13.1
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	28	35	22	14
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	30.5	31	21	26.5
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	30	31	23.5	18
[34] 2003 RFICS	SiGe HBT	5	30	27	26	21

1.3 Contributions

This thesis presents two LDMOS power amplifiers that are fabricated in 40-nm CMOS process for 4G/LTE band in the mobile applications.

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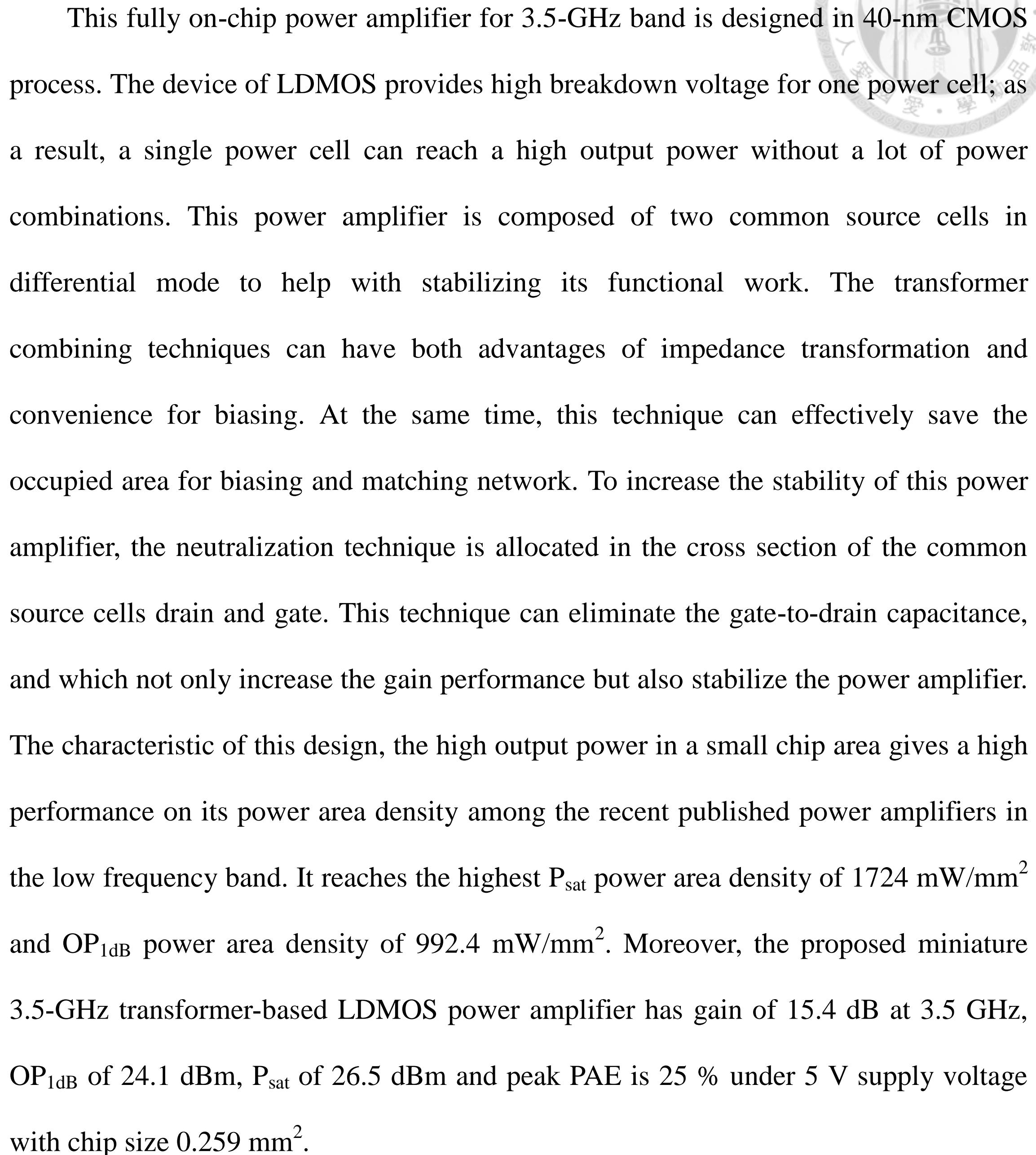
1.3.1 High Power Area Density PAs



This fully on-chip power amplifier for 3.5-GHz band is designed in 40-nm CMOS process. The device of LDMOS provides high breakdown voltage for one power cell; as a result, a single power cell can reach a high output power without a lot of power combinations. This power amplifier is composed of two common source cells in differential mode to help with stabilizing its functional work. The transformer combining techniques can have both advantages of impedance transformation and convenience for biasing. At the same time, this technique can effectively save the occupied area for biasing and matching network. To increase the stability of this power amplifier, the neutralization technique is allocated in the cross section of the common source cells drain and gate. This technique can eliminate the gate-to-drain capacitance, and which not only increase the gain performance but also stabilize the power amplifier. The characteristic of this design, the high output power in a small chip area gives a high performance on its power area density among the recent published power amplifiers in the low frequency band. It reaches the highest P_{sat} power area density of 1724 mW/mm^2 and OP_{1dB} power area density of 992.4 mW/mm^2. Moreover, the proposed miniature 3.5-GHz transformer-based LDMOS power amplifier has gain of 15.4 dB at 3.5 GHz, OP_{1dB} of 24.1 dBm, P_{sat} of 26.5 dBm and peak PAE is 25 % under 5 V supply voltage with chip size 0.259 mm^2.

1.3.2 Watt-Level PAs

This 3.5-GHz band watt-level power amplifier is fully on-chip that is fabricated in 40-nm CMOS process. Applying the radial-combining technique, the high power devices of LDMOS are spreading out in the four corners of a square. The technique

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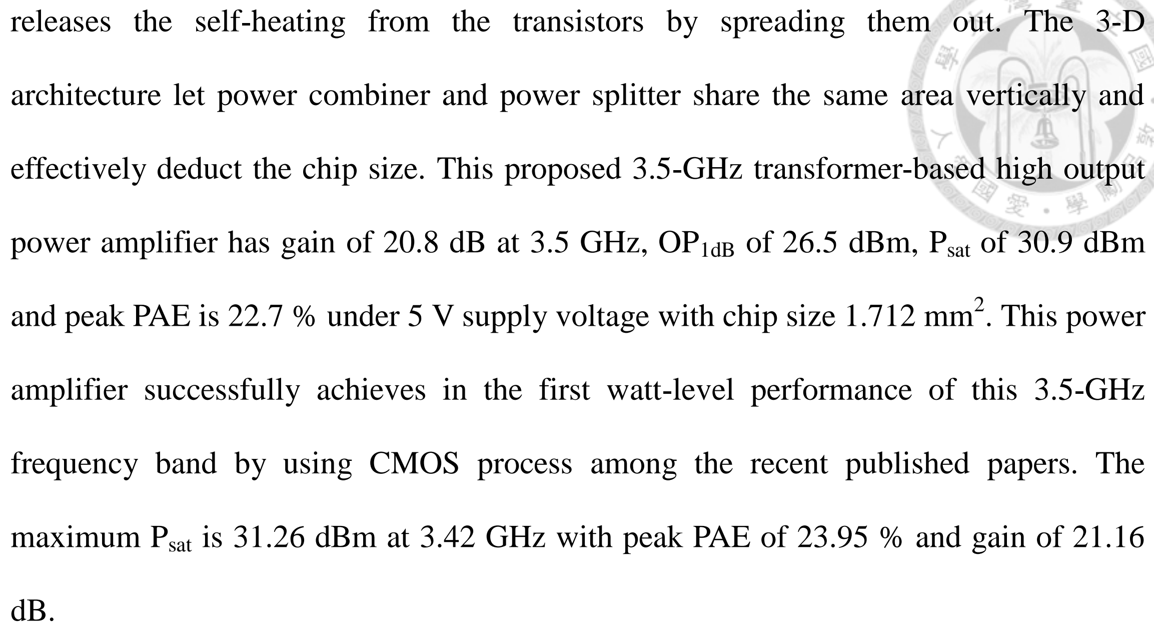

releases the self-heating from the transistors by spreading them out. The 3-D architecture let power combiner and power splitter share the same area vertically and effectively deduct the chip size. This proposed 3.5-GHz transformer-based high output power amplifier has gain of 20.8 dB at 3.5 GHz, OP_{1dB} of 26.5 dBm, P_{sat} of 30.9 dBm and peak PAE is 22.7 % under 5 V supply voltage with chip size 1.712 mm^2. This power amplifier successfully achieves in the first watt-level performance of this 3.5-GHz frequency band by using CMOS process among the recent published papers. The maximum P_{sat} is 31.26 dBm at 3.42 GHz with peak PAE of 23.95 % and gain of 21.16 dB.

1.4 Thesis Organization

The organization of this thesis is described as follows. Chapter 2 illustrates the main design challenges and techniques of transformer-combined power amplifier and the watt-level RF power amplifier in CMOS technology. A simple design of a full-integrated LDMOS power amplifier in 40-nm CMOS process is firstly introduced in Chapter 3, which applies transformer-combined techniques for area efficiency and organizes the stability techniques for circuit solutions. Chapter 4 is the main topic of this thesis for a watt-level full-integrated LDMOS power amplifier design which has four-way combined that is based on the design from Chapter 3. From the theoretical challenges of a high output power design in CMOS process to the practical issues of self-heating that happen in the measurement results that all becomes the experiences of the process of designing a high output power amplifier. All in all, Chapter 5 is concluded the successful three power amplifier designs and how these effectively work on the high power density to save the chip area and have low-cost to complete this thesis.

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Chapter 2 Watt-Level RF Power Amplifier in CMOS Technology

2.1 Challenges in RF Power Amplifier CMOS Technology

Fabricating standard CMOS technology not only has the advantage of low cost and high yield, but also being easy to integrate with another digital/analog circuit. Along with the evolution of CMOS process, many CMOS RF circuit was reported and can be comparable with III-V semiconductors in the last decade. However, some challenges in RF power amplifier design still exist, especially a fully integrate power amplifier. Scaling CMOS process let high-frequency circuit can be realized, degrades the breakdown voltage of transistors and limits the output power. A simple example in below is to illustrate this problem. Figure 2.1 is a simplified schematic of a power amplifier, the output power delivered by amplifier through output matching network to load.

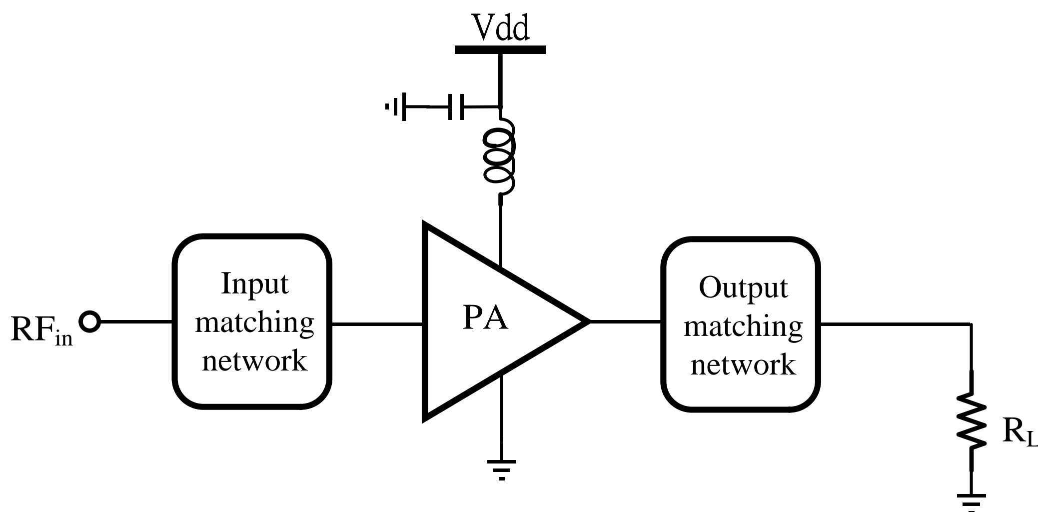

Figure 2.1 The simplified schematic of a power amplifier

The required peak-to-peak voltage (V_{pp}) can be calculated to deliver 1 watt RF power to a 50-Ω load.

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$$P_{out} = \frac{V_{pp}^{\ 2}}{8R_L} \tag{2.1}$$

$$1W = \frac{V_{pp}^{\ 2}}{8 \times 50} => V_{pp} = 20V \tag{2.2}$$

Assume that the supply voltage (V_{dd}) of a transistor is 1.8 V in the case of CMOS 180-nm technology, and the output voltage can swing from 0 to 2 V_{dd}, the load resistance present to the transistor can be calculated as in below:

$$1W = \frac{(1.8 \times 2)^2}{8 \times R_L} => R_L \approx 1.6\Omega \tag{2.3}$$

For LDMOS, assume that the supply voltage (V_{dd}) of a transistor is 5 V, and the output voltage can swing from 0 to 2 V_{dd}, the load resistance present to the transistor can be calculated as in below:

$$1W = \frac{(5 \times 2)^2}{8 \times R_L} => R_L \approx 12.5\Omega \tag{2.4}$$

Low load resistance needs to combine many transistors to achieve, and the high output impedance transform ratio will cause output matching network more complex and lossy.

In spite of the low operating voltage, another disadvantage of CMOS technology is the high loss in passive environment. Firstly, silicon substrate has higher conductivity than III-V semiconductor substrate that leads to high loss at high frequency. Secondly, CMOS technology uses multi-layer metal for inter-connection, but most of them are thin-film metals which have high parasitic resistance, high loss and low current density limit the characteristics. From the above two reasons make the power amplifier difficult to design a low loss power combiner and high impedance transform ratio matching network in CMOS.

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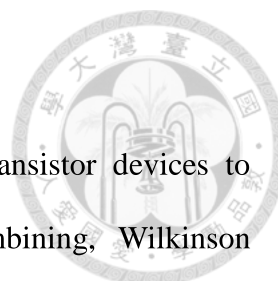
2.2 Power Combining Techniques



Power combining techniques are used for combining the transistor devices to achieve a high output power. The introduction of direct combining, Wilkinson combining, and transformer combining are listed in below. Especially, the advantage of transformer combining can save the occupied area and have impedance transformation at the same time.

2.2.1 Direct Combining

The simplest and the most efficient way to combine multiple transistors is direct combine as shown in Figure 2.2, output current from each way is summed and delivers to the load. Even though the combination will take area, the optimal output impedance drops rapidly when the numbers of combined transistor increase. The increased impedance ratio leads to a complex and lossy matching network. Moreover, increasing the metal width and combiner size can solve the problems of huge DC current from massive transistors combining. The layout asymmetry increases which results loss and phase imbalance on combiner and decreases the combination efficiency.

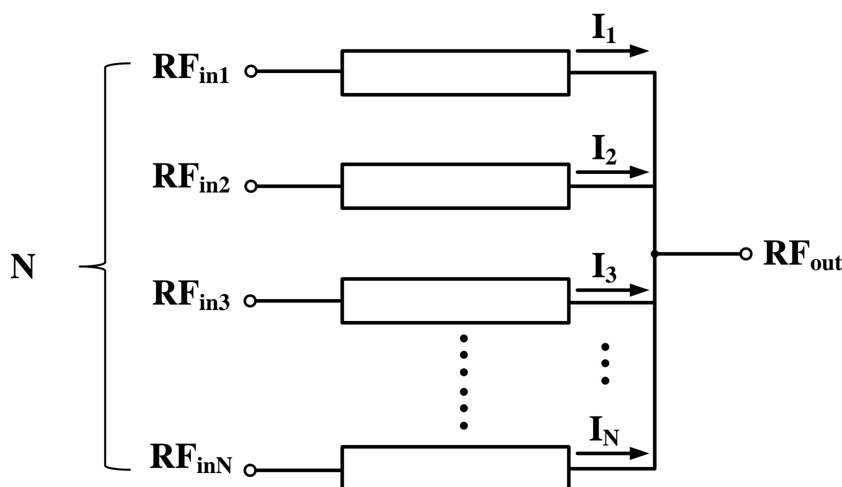


Figure 2.2 N-ways direct combining structure

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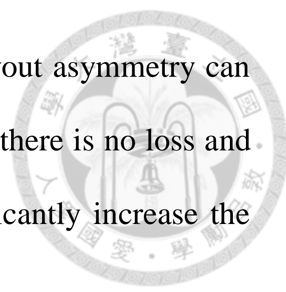

By using binary direct combining structure, the problem of layout asymmetry can be solved as shown in Figure 2.3. Since the fully symmetric layout, there is no loss and phase imbalance but the drawback is the longer metal lines significantly increase the combiner size and insertion loss.

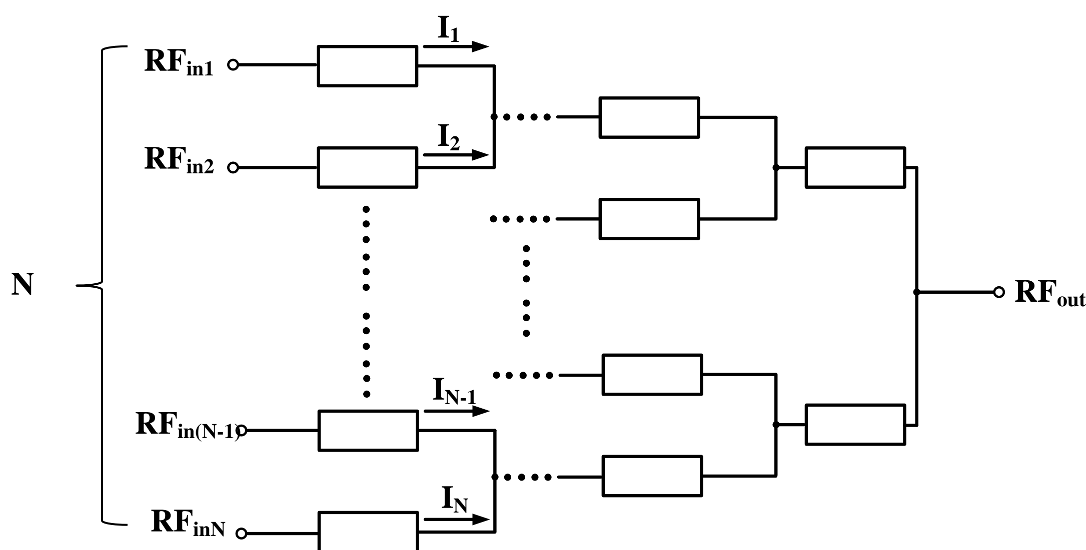

Figure 2.3 N-ways binary direct combining structure

2.2.2 Wilkinson Combining

An N-ways Wilkinson power combiner can provide in-phase power combination by full symmetric structure as shown in Figure 2.4. Between any two input ports of Wilkinson power amplifier has theoretically perfect isolation by quarter wavelength transmission line and isolation resistors. Perfect port-to-port isolation indicates when some ways of power cell fall, other power cells will not be affected and the whole amplifier can still work fine with deducted gain and output power. Since Wilkinson power combiners require quarter wavelength lines with high characteristic impedance, an N-ways Wilkinson combiner needs N quarter wavelength lines which take lots of area. The high characteristic impedance makes it difficult to realize in CMOS process.

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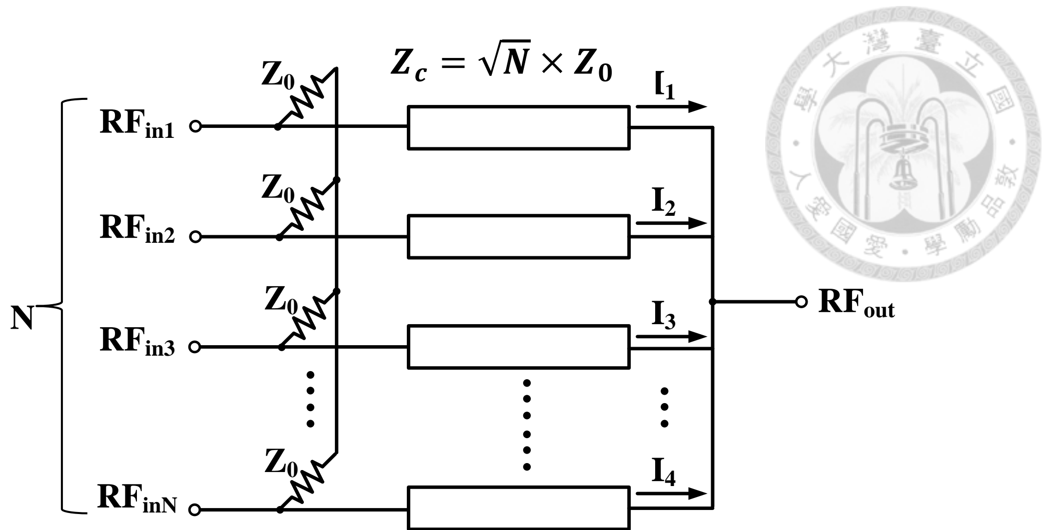

Figure 2.4 N-ways Wilkinson combining structure

The N-ways binary Wilkinson combiner is introduced to solve the high characteristic impedance problem of transmission line and planarize the previous structure. In Figure 2.5, the N-ways binary Wilkinson combiner is full symmetric and planar structure. Instead of $\sqrt{N}Z_0$, the impedance of the transmission lines is only$\sqrt{2}Z_0$. Even though the power amplifier using Wilkinson power combining structure has been successfully published in 90 nm process [1]; the area efficiency is much lower as number of combined ways increased in the quarter wavelength lines of Wilkinson combiner.

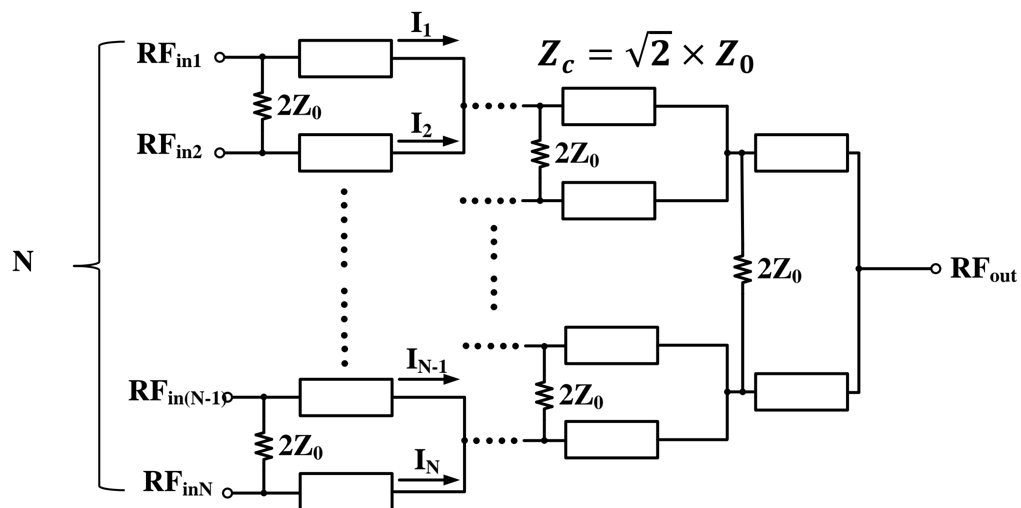

Figure 2.5 N-ways binary Wilkinson combining structure

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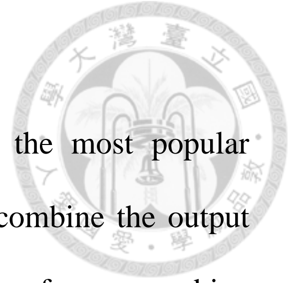

2.2.3 Transformer Combining

In the recent years, Transformer power combiner becomes the most popular combining technique. Since the characteristics of transformer can combine the output power and achieve impedance transformation, the techniques of transformer combine can make chip size more compact and enhance power density in the millimeter wave. There are many power amplifiers have been publish with varies transformer-based combining configuration [2]-[10]. Most of them use push-pull amplifier to be the power cell, and the functional work of the push-pull configuration is two transistors operating 180 degree out of phase as shown in the simple schematic in Figure 2.6.

The signal is split into two anti-phase paths by using a balun or transformer, and the signal is merged at the output according to the same technique. The abundant profits of this technique provides in power amplifier designs is in below. Without reducing the reliability of each transistor, the output voltage swing is double. The virtual ground created by differential characteristic which not only makes it strongly against parasitic inductance or capacitance from the bond wires and off-chip components and but also reduces the bypass capacitance and chock inductance at DC supply nodes. Also, it leads to a good cancellation of even harmonics that improves the linearity of the RF circuit [9]. All of above shows the transformer combining becomes an up-to-date solution for power amplifier designs.

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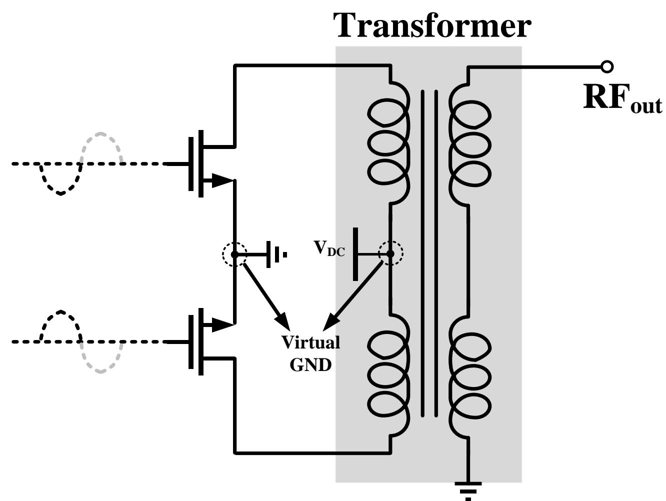

Figure 2.6 Push-pull amplifier using transformer combining technique

2.3 Circuit Solution for High Supply Voltage

2.3.1 High-Breakdown Device

High output power has high voltage swing on the load side. As the supply voltage increases higher, the swing range on each device will be expanded and the output power will have enhancement. The most intuitive way than any other methods is using high-breakdown device. LDMOS is the modified CMOS process for high power applications in nowadays. LDMOS has advantages of high breakdown voltage, high ruggedness and high thermal stability. There are several LDMOS power amplifiers have been reported [11]-[13], [28], [29].

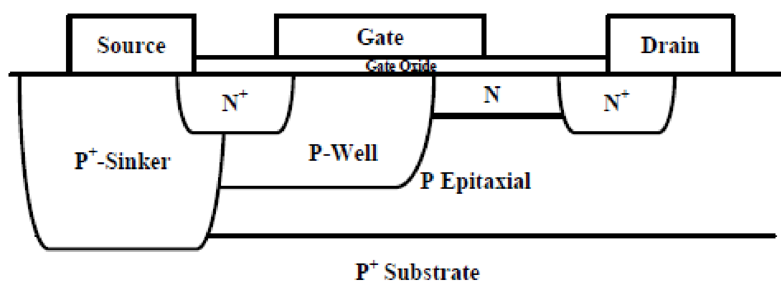

Figure 2.7 Conventional LDMOS device

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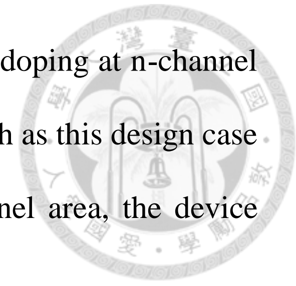

In Figure 2.7, LDMOS device uses the lower concentration of doping at n-channel between gate and drain to achieve the higher breakdown voltage such as this design case 5 V. Since the lower concentration of the electrons in the n-channel area, the device requires higher voltage to make it breakdown.

2.3.2 Cascode Configuration

The simple schematic of cascade topology is shown in Figure 2.8. The power amplifier in cascode configuration has advantage of high gain and high supply voltage than common-source (CS) or common-gate (CG) amplifier because it contains two stages which are cascaded by CS and CG amplifiers. However, cascode configuration has a disadvantage in high power operation. In the CG configuration, there must be AC ground at gate of M_2. It leads the V_{gs} swing of M_2 is equal to the voltage swing at node X which is the amplified signal from RF input, and the V_{gs} swing of M_2 large than swing of M_1. The unequal distribution of the output swing can be observed on two transistors. The output swing is small and can be ignored in small-signal operation. But in large-signal operation, the CG transistor over the breakdown voltage may happen due to the unequal distribution of the output swing. The thick-oxides transistor can be used to enhance the breakdown voltage of CG transistor by considering the reliability. However, the think-oxides transistor has defects of low gain, high parasitic capacitance which deducts the benefit.

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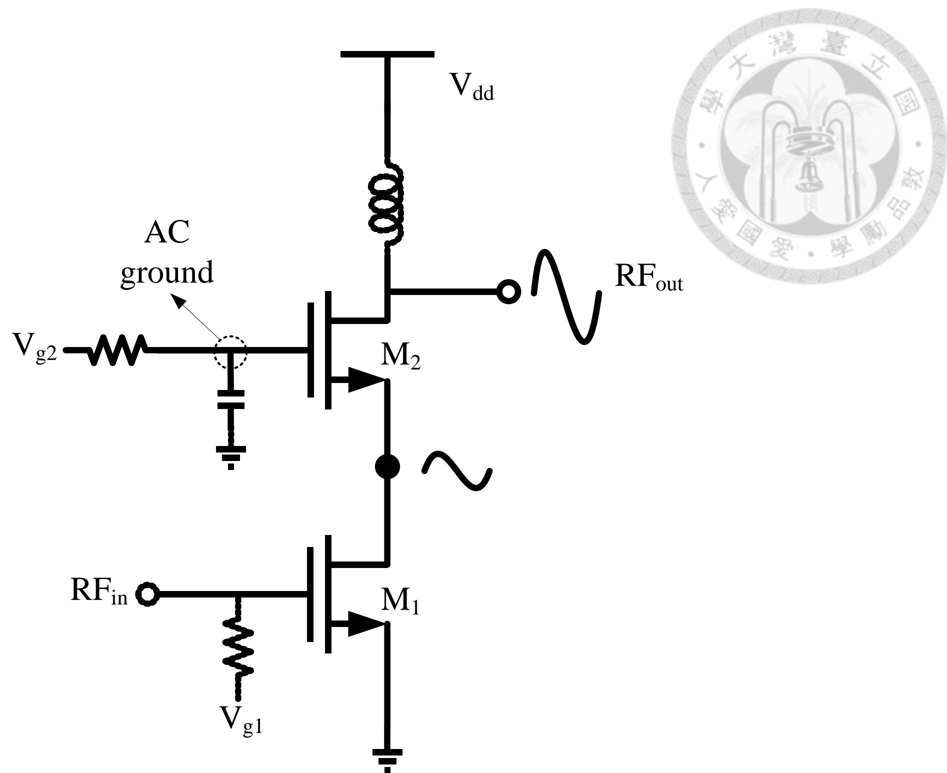

Figure 2.8 Cascode configuration

2.3.3 Stacked Device Structure

The power amplifier design in stack device structure is to solve the problem of unequal distribution of output swing. The simple schematic of stacked amplifier is shown in Figure 2.9. Each gate of the stacked transistors (M_2 to M_n) is not an AC ground, and has some voltage swing. If each transistor is identical with same DC condition and same V_{gs} swing, the output swing of each transistor can be summed up to the output node with no transistors over the breakdown voltage. The gate voltage swing can be generated by input transformer [13], by driver amplifiers [14], by feedback [15] or by parasitic component on each transistor. There are several CMOS power amplifiers use stacked configuration have been published, [13]-[17].

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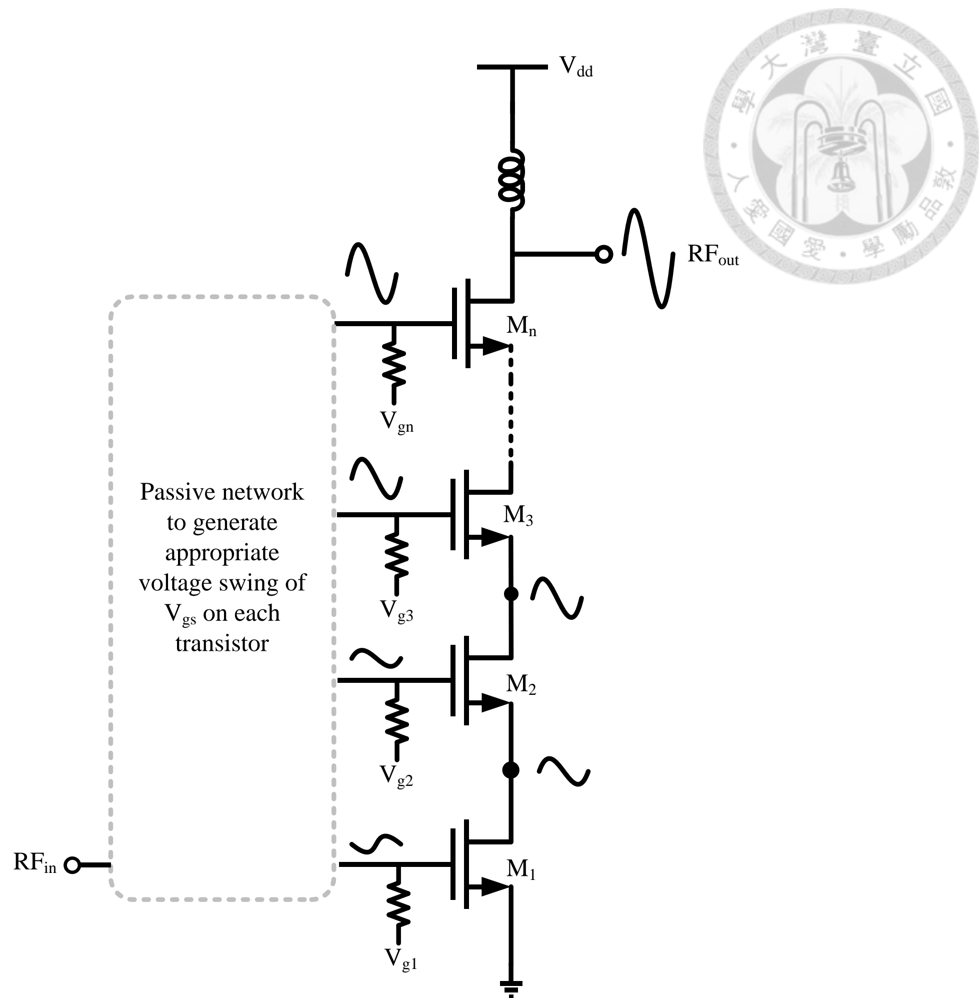

Figure 2.9 Stacked device structure

2.4 Transformer-Based Power Combining Techniques

2.4.1 Series-Combining Transformer (Voltage Mode)

Series-combining transformer (SCT) is also called voltage-combining transformer as shown in Fig. 2.10. Since the series structure of the secondary coils combines N ways of identical RF signal source by magnetic coupling at primary side, and sums up the voltage swings to load by the secondary coils to achieve high output power. Assuming that each transformer cell is identical and ideal, and then the output voltage and current swing can be expressed as:

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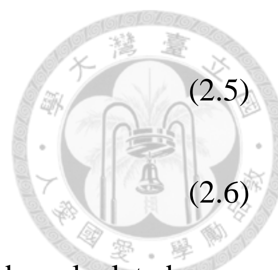

$$\mathrm{I_L} = I_s = \frac{1}{n} \times I_p \tag{2.5}$$

$$\mathrm{V_L} = \mathrm{N} \times \mathrm{V}_s = N \times n \times \mathrm{V}_p \tag{2.6}$$

Apply (2.3) here, the load impedance and load power dissipation can be calculated as:

$$\mathrm{R_L} = \frac{\mathrm{V_L}}{I_\mathrm{L}} = \mathrm{N} \times \frac{V_s}{I_s} => N \times n^2 \times \frac{V_p}{I_p} = N \times n^2 \times R_{in} \tag{2.7}$$

$$\mathrm{P_L} = \frac{1}{2}\frac{V_\mathrm{L}^2}{R_\mathrm{L}} = V_\mathrm{L} \times \mathrm{I_L} => \mathrm{N} \times n \times V_\mathrm{p} \times \frac{1}{n} \times I_\mathrm{p} = \mathrm{N} \times V_\mathrm{p} \times I_\mathrm{p} \tag{2.8}$$

The series-combining transformer can be a combiner and a matching network which has transform ratio $\mathrm{N} \times n^2$ as shown in (2.7). Applying this characteristics of this transformer combining technique, many works have been published in [9]-[10], and even in a watt-level power amplifier design.

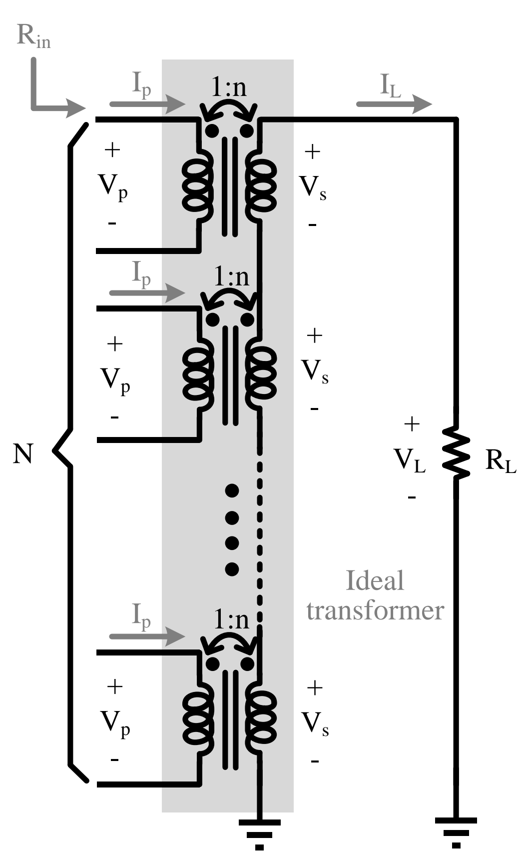

Figure 2.10 Schematic diagram of series combining transformer

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2.4.2 Parallel-Combining Transformer (Current Mode)

Two types of the parallel-combining transformer (PCT) which can also be called as current-combining are shown in Figure 2.11. The two different schematic diagrams in Fig. 2.11(a) and Fig. 2.11(b) has equivalent model. Regarded I_{load} as the superposition of the current flowing on the secondary side, the relationship between output voltage and current can be expressed as:

$$\mathrm{V_L} = \mathrm{V}_s = n \times \mathrm{V}_p \tag{2.9}$$

$$\mathrm{I_L} = \mathrm{N} \times \mathrm{I}_s = \frac{M}{n} \times \mathrm{I}_p \tag{2.10}$$

Apply (2.3) here, the load impedance and load power dissipation can be calculated as:

$$\mathrm{R_L} = \frac{\mathrm{V_L}}{I_L} = \frac{1}{M} \times \frac{V_s}{I_s} => \frac{n^2}{M} \times \frac{V_p}{I_p} = \frac{n^2}{M} \times R_{in} \tag{2.11}$$

$$\mathrm{P_L} = \frac{1}{2}\frac{V_{\mathrm{L}}{}^2}{R_{\mathrm{L}}} = V_{\mathrm{L}} \times \mathrm{I_L} => n \times V_{\mathrm{p}} \times \frac{M}{n} \times I_{\mathrm{p}} = M \times V_{\mathrm{p}} \times I_{\mathrm{p}} \tag{2.12}$$

The parallel-combining transformer can be a combiner and a matching network which has transform ratio $\frac{n^2}{M}$ as shown in (2.11). Applying this characteristic of this transformer combining technique, such as published in [8].

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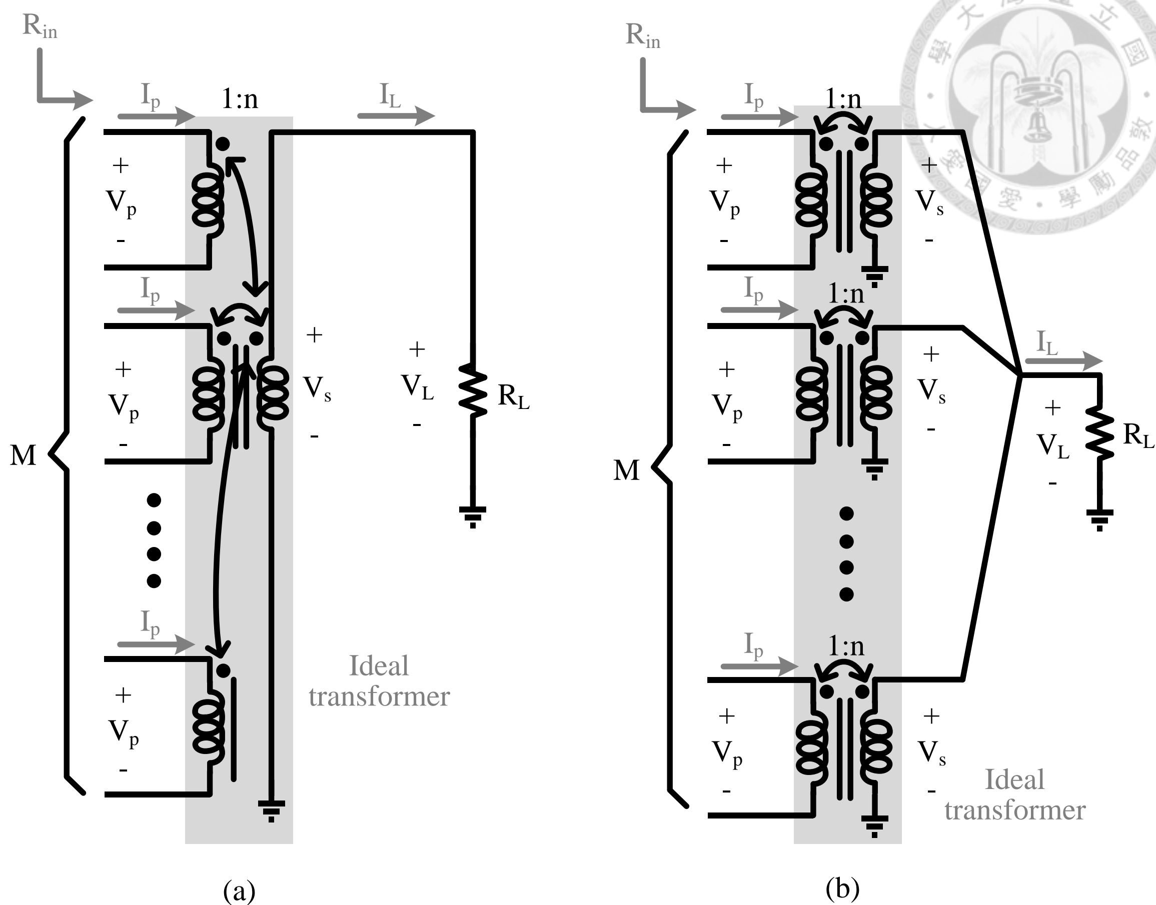

Figure 2.11 Schematic diagram of parallel combining transformer

2.4.3 Parallel-Series Combining Transformer (Current-Voltage Mode)

Both of series-combining transformer and parallel-combining transformer are suffered with the unity of impedance transformation. Series-combining transformer can only transform the impedance to relatively high impedance, so the maximum number of combined cell will be limited by optimal load of device and the load impedance of usually 50 ohm. Parallel-combining transformer can only transform the impedance to relatively low impedance. Although this transformer combination can use large turn ratio to match higher impedance, it will occupy a large area and have poor power transfer efficiency. Concerned about the design flexibility, the parallel-series combining

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transformer is applied. Parallel-series combining transformer takes the advantage of a hybrid structure of PCT and SCT.

Parallel-series combining transformer (PSCT) is shown in Figure 2.12, the output voltage is summed up by SCT and the output current is summed by PCT such that

$$V_L = N \times V_s = N \times n \times V_p \tag{2.13}$$

$$I_L = M \times I_s = \frac{M}{n} \times I_p \tag{2.14}$$

Apply (2.3) here, the load impedance can be calculated as:

$$R_L = \frac{V_L}{I_L} = \frac{N \times V_s}{M \times I_s} => \frac{N \times n^2}{M} \times \frac{V_p}{I_p} = \frac{N}{M} \times n^2 \times R_{in} \tag{2.15}$$

$$P_L = \frac{1}{2}\frac{V_L{}^2}{R_L} = V_L \times I_L => N \times n \times V_p \times \frac{M}{n} \times I_p = N \times M \times V_p \times I_p \tag{2.16}$$

The parallel-series combining transformer has more flexibility in impedance transformation than SCT and PCT as shown in the calculation of (2.13). Table 2-1 provides the summary of the three types of transformer-based combining techniques.

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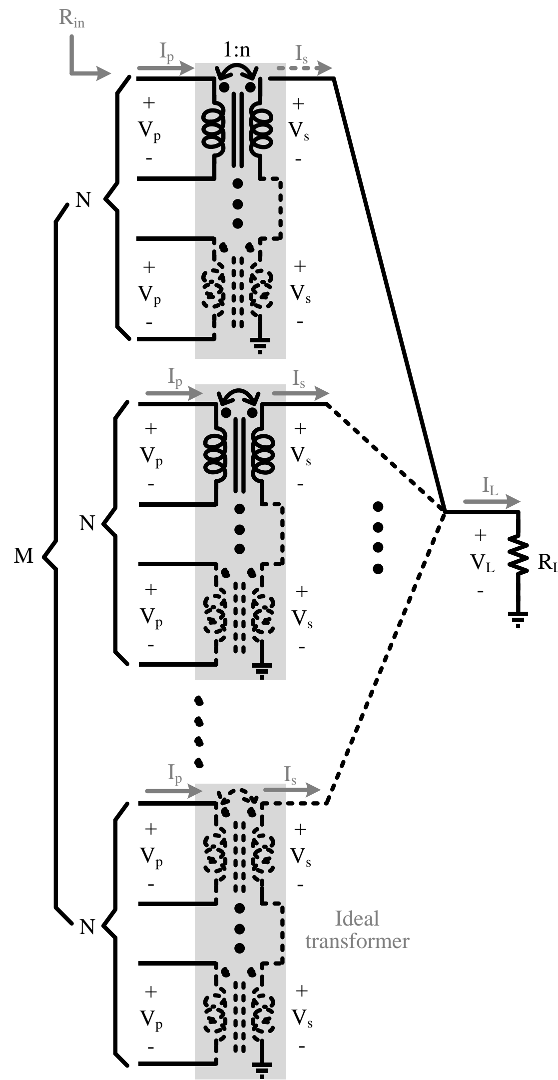

Figure 2.12 Schematic diagram of parallel-series combining transformer

Table 2-1 Summary of Different Transformer-Based Power Combining Techniques [54]

	V_L	I_L	R_L	P_L	Ways of combining
Series combining (Voltage mode)	$N \times n \times V_p$	$\frac{1}{n} \times I_p$	$N \times n^2 \times R_{in}$	$N \times V_p \times I_p$	N
Parallel combining (Current mode)	$n \times V_p$	$\frac{M}{n} \times I_p$	$\frac{n^2}{M} \times R_{in}$	$M \times V_p \times I_p$	M
Parallel-series combining (Current-voltage mode)	$N \times n \times V_p$	$\frac{M}{n} \times I_p$	$\frac{N}{M} \times n^2 \times R_{in}$	$N \times M \times V_p \times I_p$	N×M

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Chapter 3 A Compact 3.5-GHz Fully-Integrated LDMOS Power Amplifier

3.1 Circuit Design

3.1.1 Bias and Device Selection

The main target of power amplifier design is to reach the most output power without sacrificing efficiency. The bias voltage is selected in Class-AB for better performance on efficiency. The DC-IV curve and g_m curve versus different bias voltages are shown in Figure 3.1 and Figure 3.3, which demonstrate the bias selection. g_m curve shows the transistor starts turn-on at V_{gs}=0.4V, and the peak value of gm is at V_{gs}=1.6V. By the comparison between V_{gs}=1.6V and V_{gs}=1.2V, the one with 1.2V wins the selection due to its high g_m value and low quiescent current.

For the further design consideration, the four-way radial-combined power amplifier architecture can assemble 4 differential power amplifier units and each power amplifier unit composed of 2 power amplifier cells. In other words, each power amplifier cell should deliver 80 mW (~19 dBm) and 2 power amplifier cells deliver 158 mW (~22 dBm). The optimal load of each power cell for 28 dBm can be calculated as:

$$P_{out} = \frac{V_p{}^2}{2 \times R_{opt}} = \frac{(V_{dd} - V_{knee})^2}{2 \times R_{opt}} \tag{3.1}$$

$$R_{opt} = \frac{(5-1.5)^2}{2 \times 0.158} \approx 38.76\Omega \tag{3.2}$$

where V_{knee} is the knee voltage of 1.5 V as shown in Figure 3.1.Then, the device size can be determined as W/L = 2×(10×32)μm / 0.54μm according to the detailed analysis of Figure 3.4 and Table 3-1 in below.

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The MSG/MAG curve of a transistor with 10 μm width and different finger numbers at the V_{DD} =5V and V_{gs} =1.2V is shown in Figure 3.2. The MSG/MAG curves show the ideal of maximum gain without additional passive loss margin, and the gain of the target frequency at 3.5 GHz is lower than all transitional points among MSG/MAG curve. As sweeping the finger numbers from 8 fingers to 32 fingers, the output power of 1-dB compression increases from 14.26 dBm to 19.94 dBm and the saturated power increases from 15.1 dBm to 20.11 dBm. However, the PAE at output power of 1-dB compression only increases 1.23% from 43.48 % to 44.71 % and the peak PAE only decreases 1.56% from 50.24 % to 48.68 %. This appearance shows that the selection of large transistor size can provide high output power without sacrificing efficiency. As the result, the gate width of 10 μm with 32 fingers is selected. The quiescent current of a single common source is 38.7 mA and the quiescent current of one-way power cell is 155 mA.

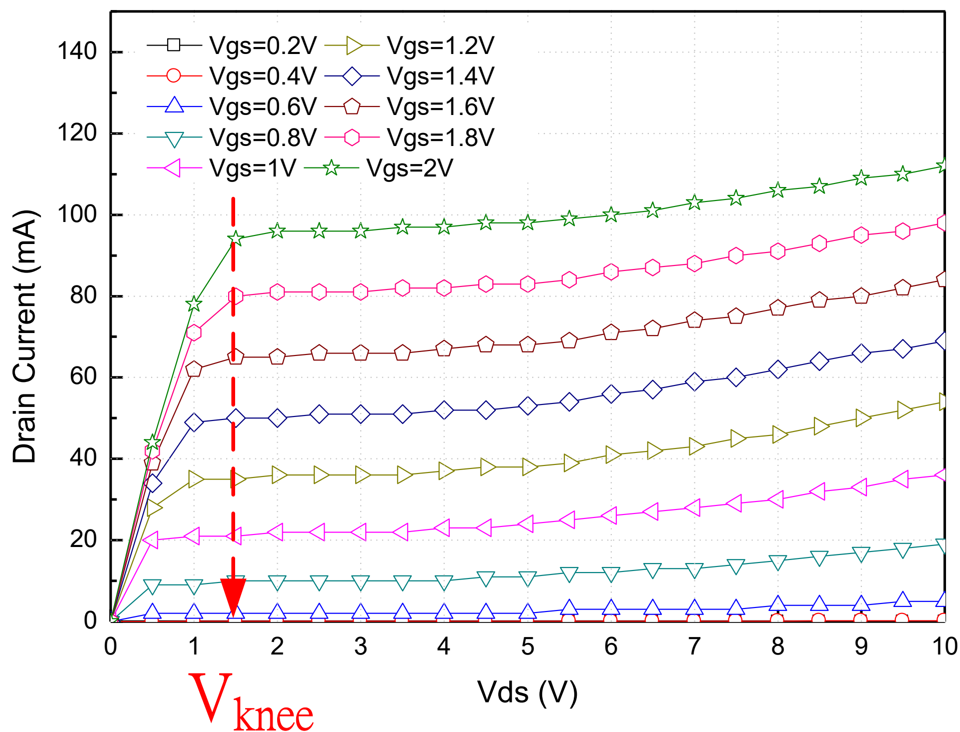

Figure 3.1 DC-IV curve of common source with width of 10-μm and finger of 32

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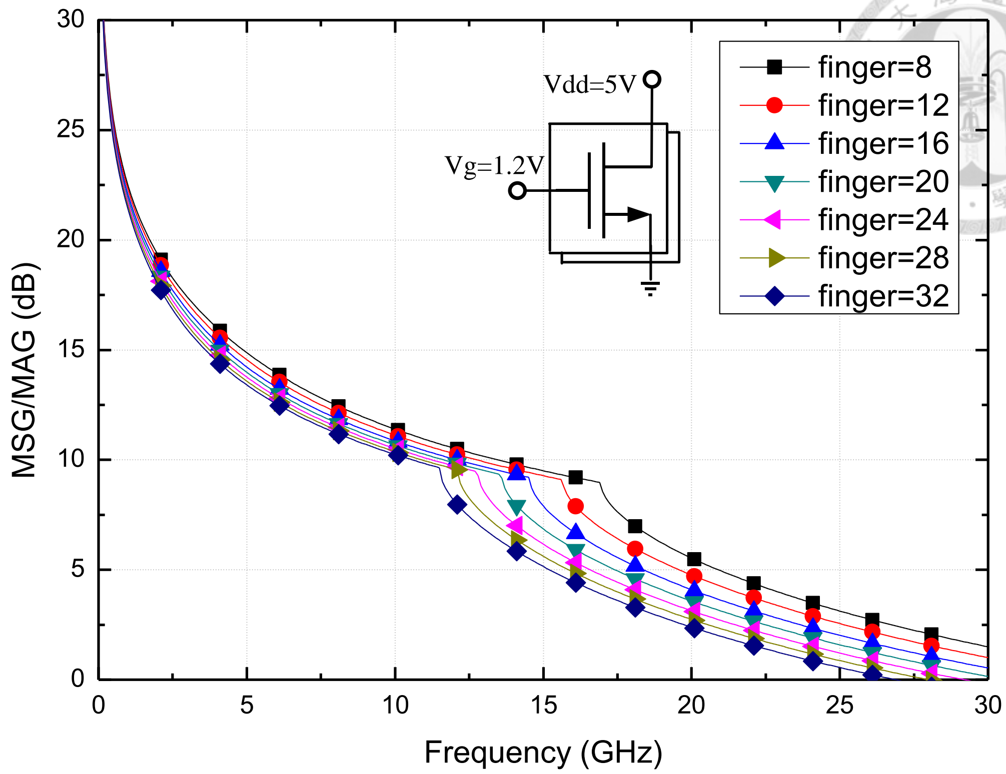

Figure 3.2 MSG/MAG curves with 10-μm width and different numbers of finger

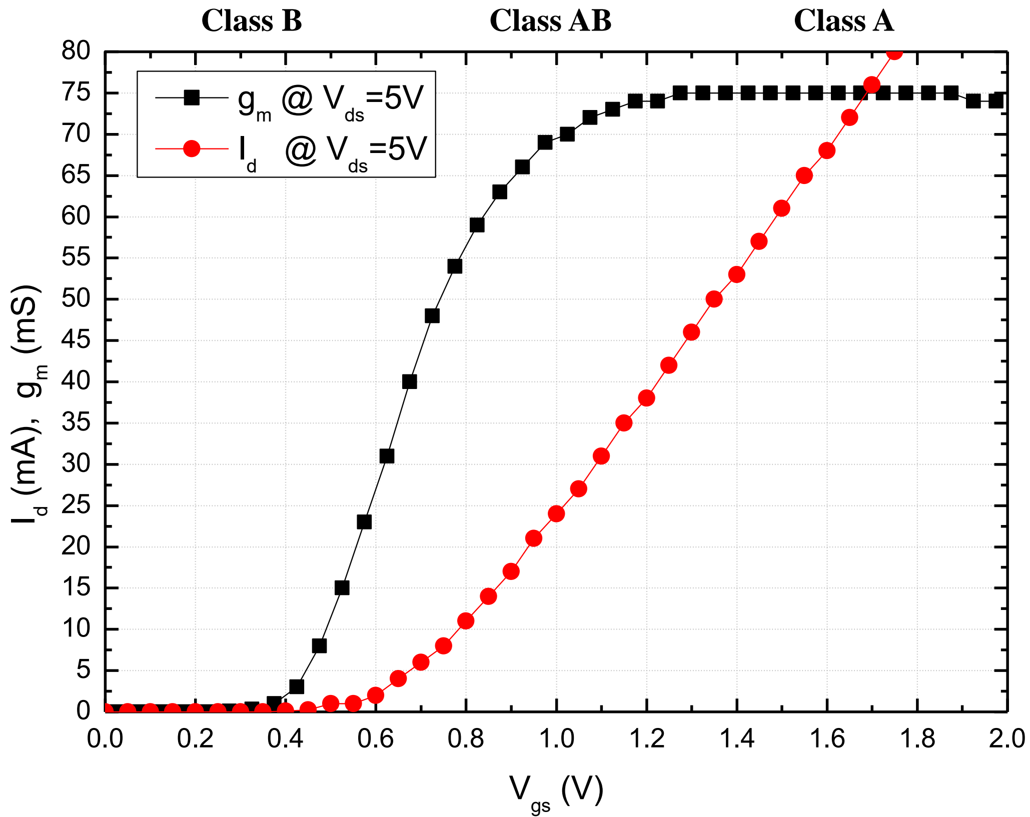

Figure 3.3 I_d and g_m curve with width of 10-μm and finger of 32 when V_{ds}=5V

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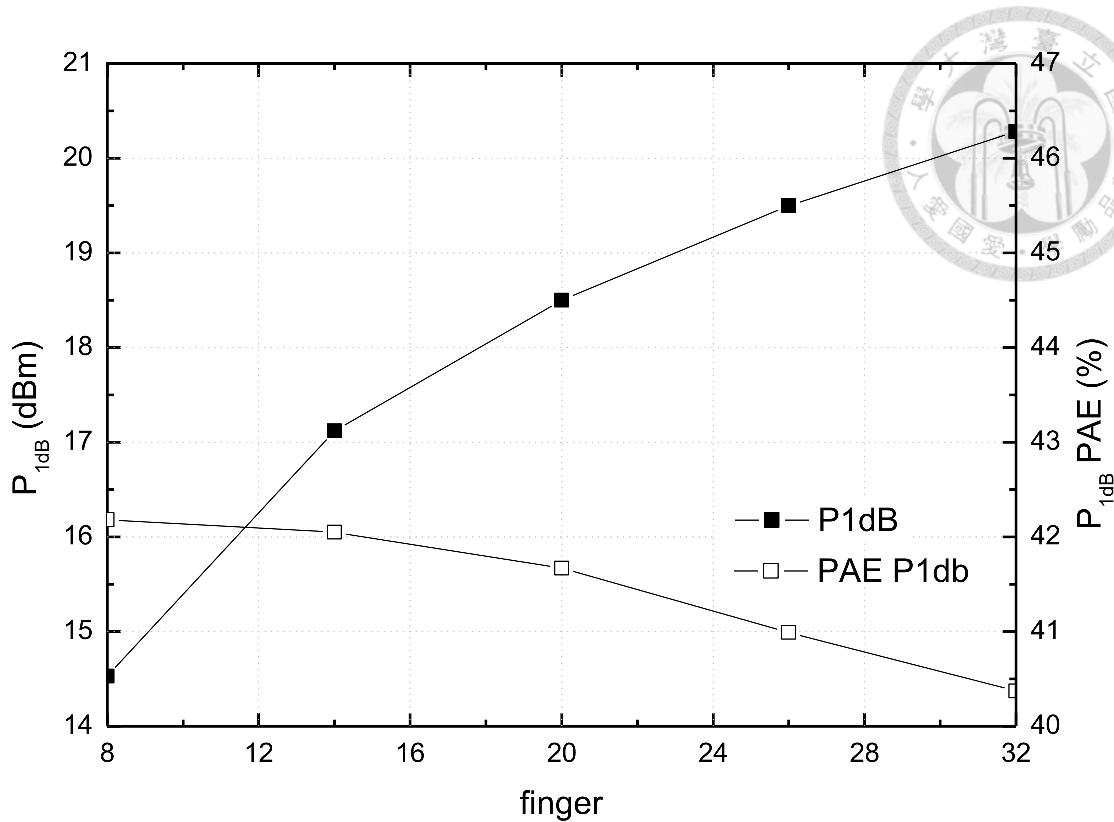

Figure 3.4 P_{1dB} and P_{1dB} PAE according to different finger numbers

Table 3-1 Device Selection with Output Impedance which is the Closest to 50-Ω Load

# of NMOS	PAE (%)	P_{1dB} (dBm)	Input Impedance (Ω)	Output Impedance (Ω)
1	44.98	19.96	7.76-36.83j	79.179+38.748j
2	43.41	22.80	2.94-17.71j	37.552+24.678j
3	42.25	24.43	2.53-11.88j	28.937+13.637j
4	40.59	25.54	1.58-9.06j	19.662+10.576j

Table 3-2 The Comparison between (10μm×32)×2 and (10μm×16)×4

Transistor Sizes	PAE_{max} (%)	Impedance (Ω)	Pout (dBm)	Impedance (Ω)
(10μm×32)×2	43.74	38.933+27.351j	22.80	37.655+20.340j
(10μm×16)×4	42.33	37.047+21.556j	22.97	38.772+17.847j

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Table 3-1 shows the two units of gate width 10 μm and 32 fingers have the closest impedance to the 50-Ω load. Table 3-2 compares the two units of gate width 10 μm and 32 fingers with the four units of gate width 10 μm and 16 fingers. In both sizes the impedances and the performance of the maximum output power and maximum PAE are similar in the load-pull simulation. Although the 16 fingers one has slightly higher gain in the operated point, in Figure 3.2 the MSG/MAG curves show that the turning point of 32 fingers has closer to the operated frequency than the 16 fingers one within the same gate width of 10 μm. As the result, the transistor size for a power cell is chosen as (10 μm × 32 fingers) ×2.

3.1.2 Transformer and Power Cell Design

The transformer model as shown in Figure 3.5 is used in order to design a transformer. A transformer is composed by two inductors which coupled with each other by magnetic field. When a time-variant current I_1 flow in the primary inductor, it generates magnetic flux through the secondary inductor, promote the secondary inductor generates some voltage, and vice versa. The relationship between voltage and current in the transformer can be expressed as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.3}$$

In (3.3), L_1 is the primary inductor, L_2 is the secondary inductor, R1 is the parasitic resistor in primary inductor, R_2 is the parasitic resistor in secondary inductor, and M is the mutual inductance which defined as

$$M = k \cdot \sqrt{(L_1 \cdot L_2)} \tag{3.4}$$

In (3.4), k is the coupling coefficient. The mutual inductance can also be calculated by Z_{ij} in N-port network, the equation is

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$$M = \frac{\mathrm{Im}(Z_{ij})}{\omega}, \text{ when } i \neq j \tag{3.5}$$

The parameter n is the turn ratio between primary and secondary windings which is defined as

$$n = \sqrt{\frac{L_2}{L_1}} \approx \frac{I_1}{I_2} \approx \frac{V_2}{V_1} \tag{3.6}$$

The lossy inductors of the transformer are modeled by the equivalent series resistors R_1 and R_2. The series resistors R_1 and R_2 can be calculated by the primary and secondary inductors L_1 and L_2 with their quality factors, which are

$$R_1 = \frac{\omega L_1}{Q_1} \tag{3.7}$$

$$R_2 = \frac{\omega L_2}{Q_2} \tag{3.8}$$

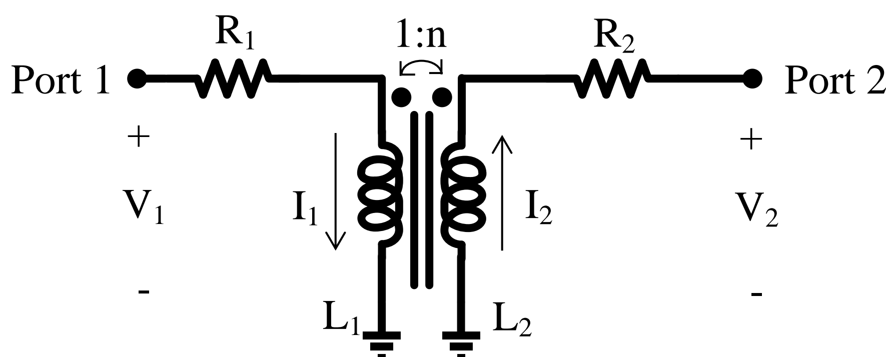

Figure 3.5 Transformer model

The equivalent T-model is introduced and shown as in Figure 3.6 to clearly illustrate the transformation of impedance by an actual transformer. The parameter n in Figure 3.6 is the turn ratio between primary and secondary coil of a transformer design.

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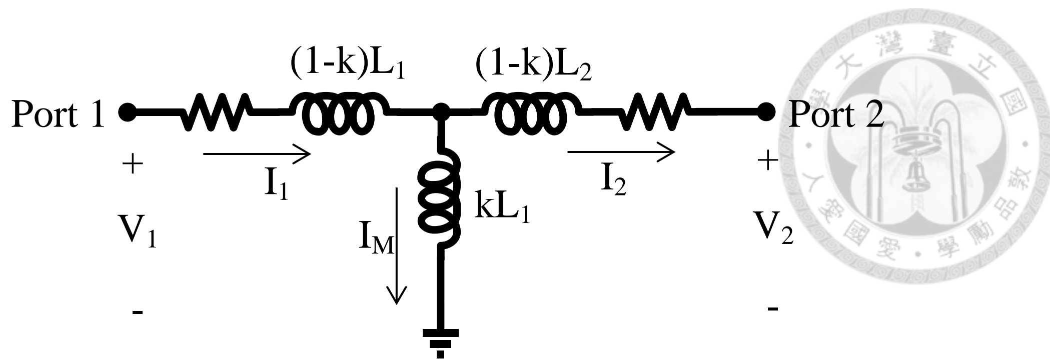

Figure 3.6 The equivalent T-model of transformer with n=1

CMOS process has multi-layer environment, the more advanced CMOS process the more multiple layers it provides. As considering of horizontally-coupled and vertically-coupled, there are two main methods to approach to the transformer designs, edge couple and broadside couple. The two types of coupling structures give different coupling coefficients, which indicate different magnetic coupling efficiency and different amount of losses.

The method of adjusting coupling coefficient for the edge-coupled transformer is to change the spacing between metals of primary and secondary coils. However, as the method of adjusting coupling coefficient for broadside couple is to use different metal width. The simulation results are shown in Figure 3.7 and Figure 3.8, respectively. The simulation result of coupling coefficient k using metal 9 and metal 10 with 300μm length by broadside couple and edge couple. The ground plane degrade coupling factor slightly in broadside coupling design but significantly in edge coupling design.

Although the broadside coupling has larger coupling factor than the edge coupling, the edge coupling is used for the transformer design in this power amplifier because the design in low frequency will require more inductance. The more routings give the more inductance. The top metal of 40-nm process (M10) is 30.2mA/μm, metal 9 (M9) is 8mA/μm, and the rest of the bottom metal layers are less conductivity and more loss. In order to use the top two metals which has more conductivity and less loss,

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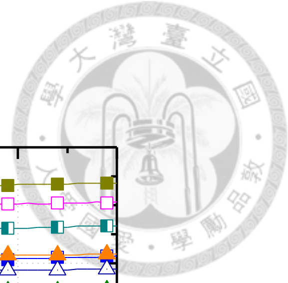
the edge coupling is selected.



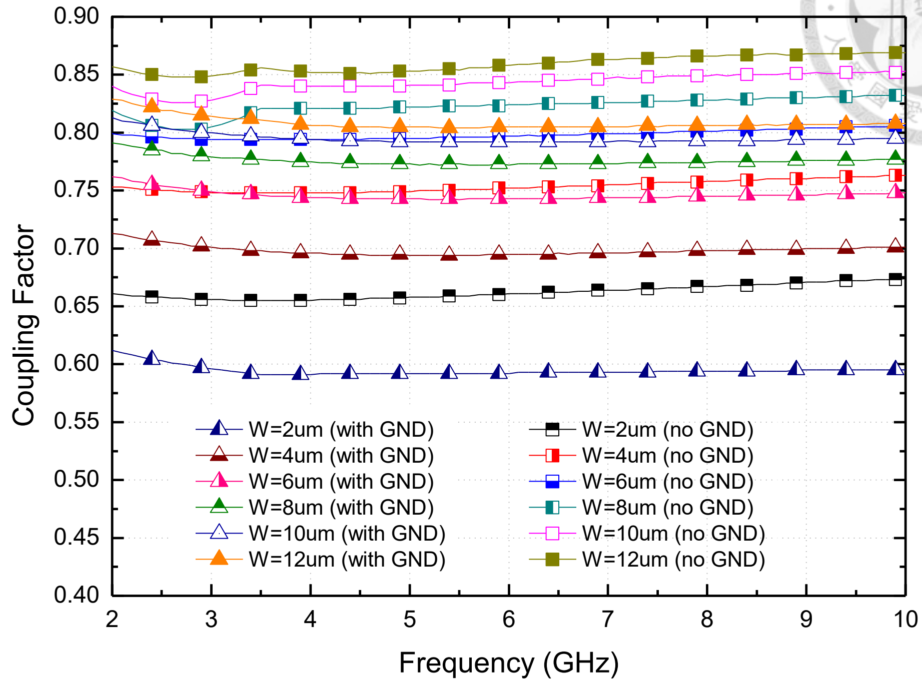


Figure 3.7 The broadside couple simulation with different metal widths

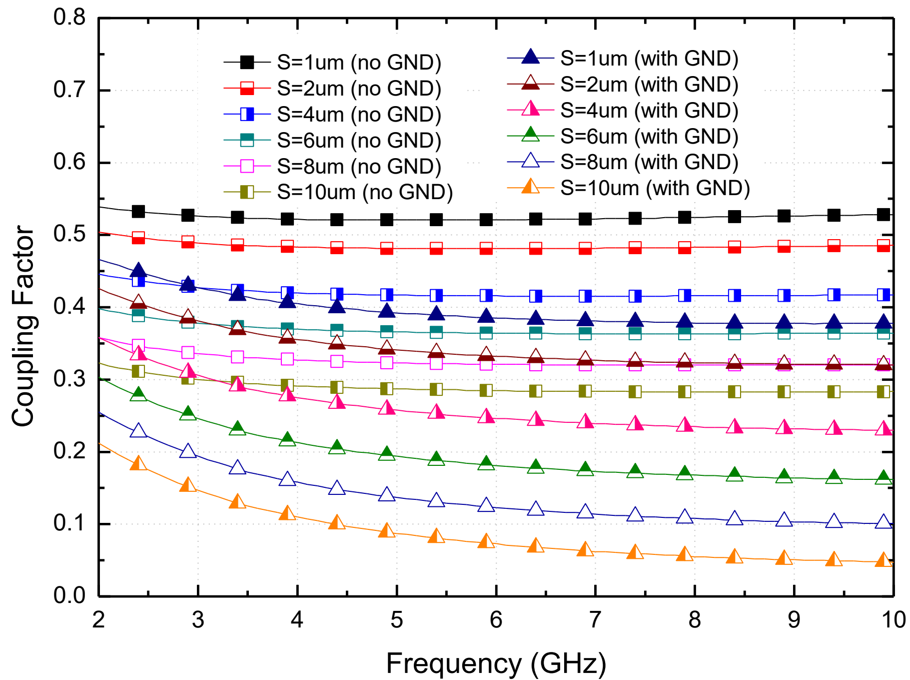


Figure 3.8 The edge couple with different spacings

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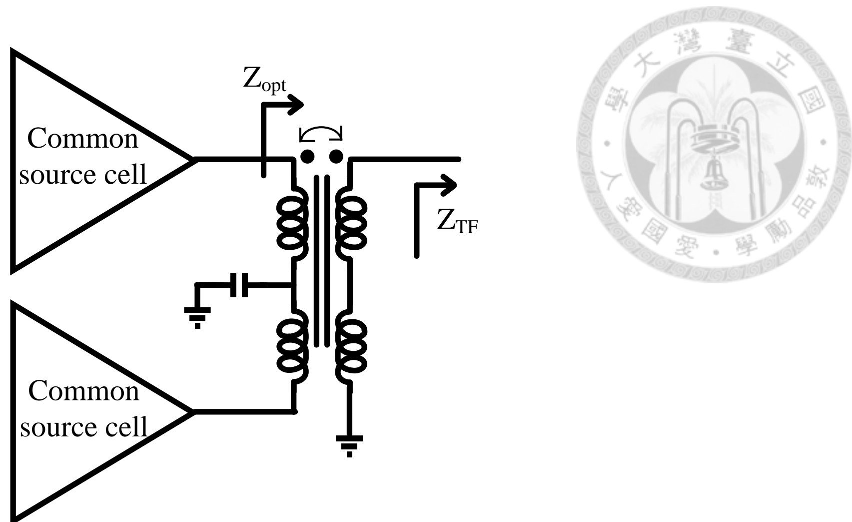

Figure 3.9 Schematic of output transformer at power cell output terminal

The quiescent DC current of common source cell is 77.4 mA. Since the current density of metal 10 in TSMC 40-nm CMOS Technology is 30.2 mA/μm; as the result, the metal width of the DC transmission line must be wider than 2.6 μm. To keep more margins for the DC current when the dynamic DC current increases in the large signal operation, the maximum width of the layout restriction is used as 12 μm. The more margins can also provide a low resistance path from the voltage source of V_{DD} and indirectly avoid the IR drop.

Transformer type can be classified into five categories as shown in Figure 3.10: single to single, single to differential, single to differential with center-tapped ground, differential to differential, and differential to differential with center-tapped ground.

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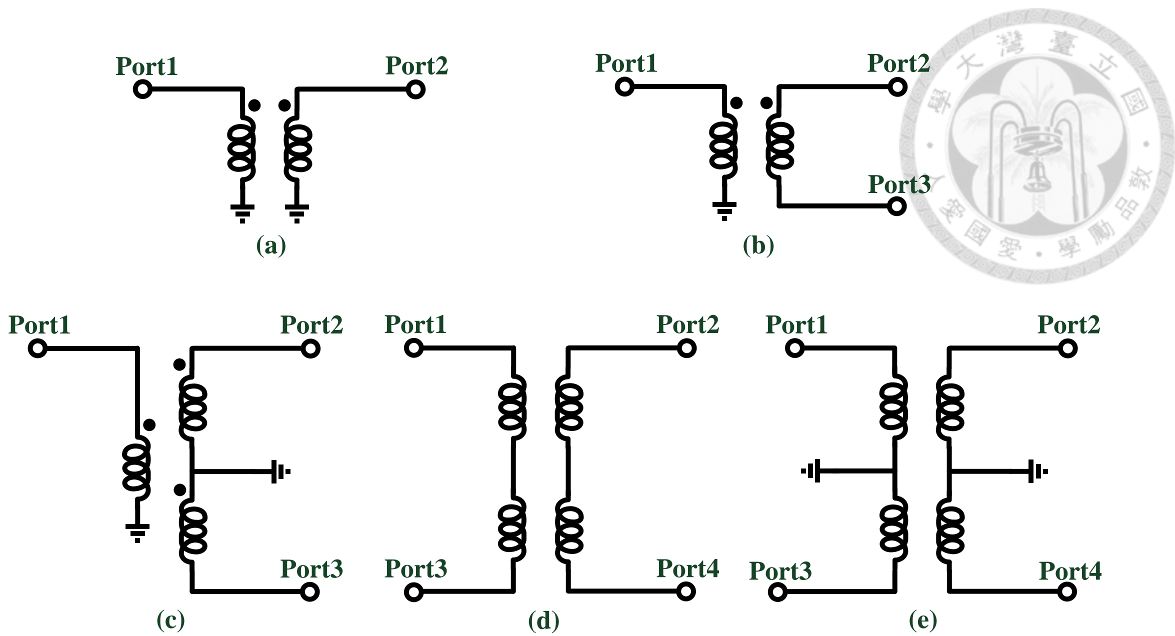

Figure 3.10 (a) Single to single (b) single to differential (c) single to differential with center-tapped ground (d) differential to differential (e) differential to differential with center-tapped ground

For the output transformer of the power amplifier as shown in Figure 3.11 uses differential-to-single ended topology. Transformer design provides isolation between primary windings and secondary windings which indicates the DC block can be removed from the output path. The primary windings provide the path of voltage source (V_{DD}) and combine the two differential power cells; while the secondary windings sum up the voltage to deliver output power from electromagnetic induction of the primary windings. The DC bias voltage is fed from the AC virtual ground with a large resistor for blocking DC and RF signals and 8 pF bypass capacitor for common-mode suppression. The ground plane uses both metal 1 and metal 2 to increase the current density.

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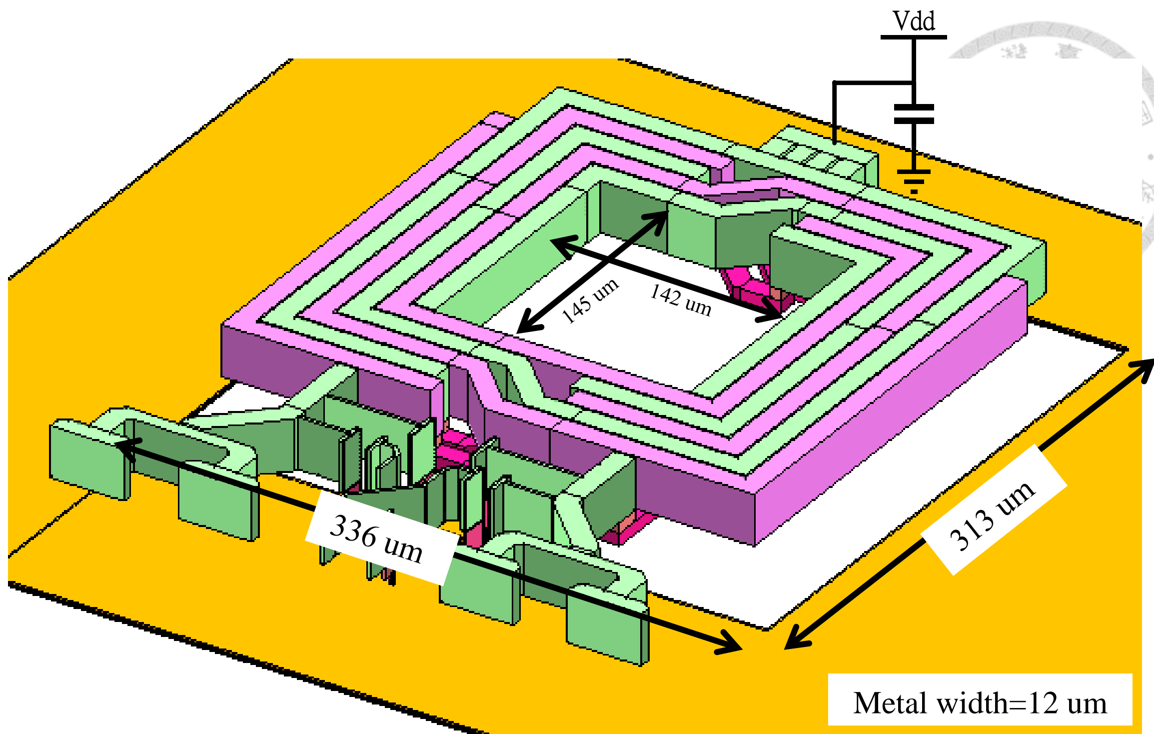

Figure 3.11 View of output transformer

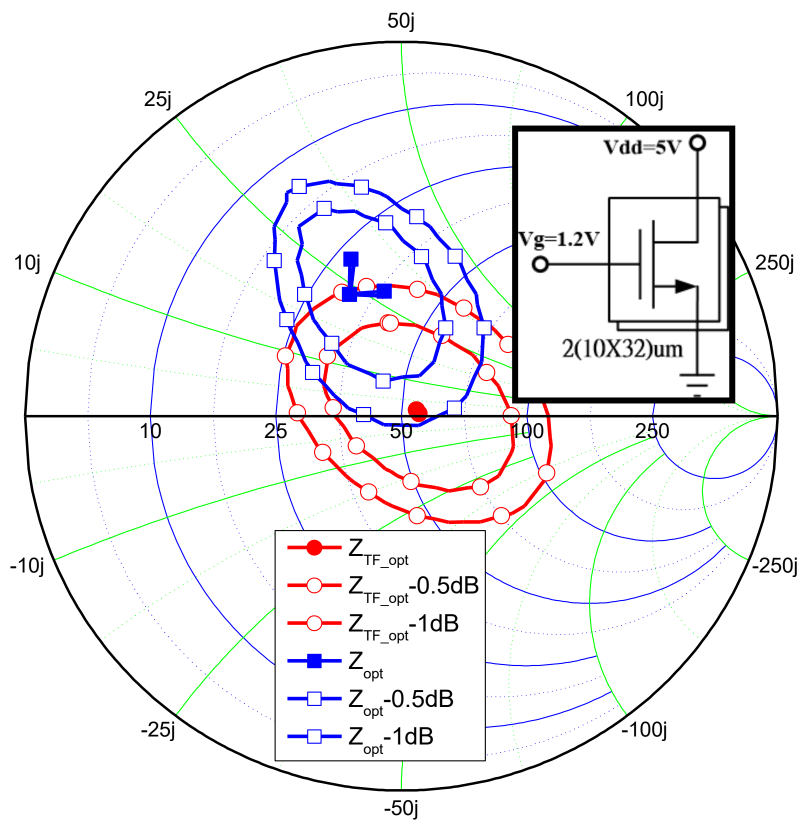

Figure 3.12 Impedance transformation by the output transformer

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The output transformer design is optimized by full electromagnetic simulating in Sonnet software. It occupies $336 \times 316\,\mu m^2$ included the slotted ground. The inductance value of the primary winding is 1.023 nH and the secondary is 2.704 nH. The turning capacitor is 0.72 pF for amplitude and phase balance. The simulated amplitude imbalance of output transformer is below 0.5 dB and phase imbalance is below 0.2 degree from 3 to 4 GHz that is shown in Figure 3.14 and Figure 3.15.

Transformer can combine the output power and transform the impedance Z_{opt} to Z_{TF}. The transformed impedance Z_{TF} is near 50 Ω which means no extra matching component is needed when R_L is 50 ohm as shown in Figure 3.12. Power transfer efficiency is another indicator which presents the combination efficiency of combiner; power transfer efficiency is defined as:

$$\eta \equiv \frac{P_{load}}{P_{in}} \tag{3.9}$$

where P_{in} is the total input power of transformer and P_{load} is the total output power of transformer. Figure 3.13 presents the power transfer efficiency of output transformer, the peak value of the efficiency is 74% which is about 1.3 dB power loss, and from 2.35 GHz to 5.67 GHz the efficiency is more than 70 %.

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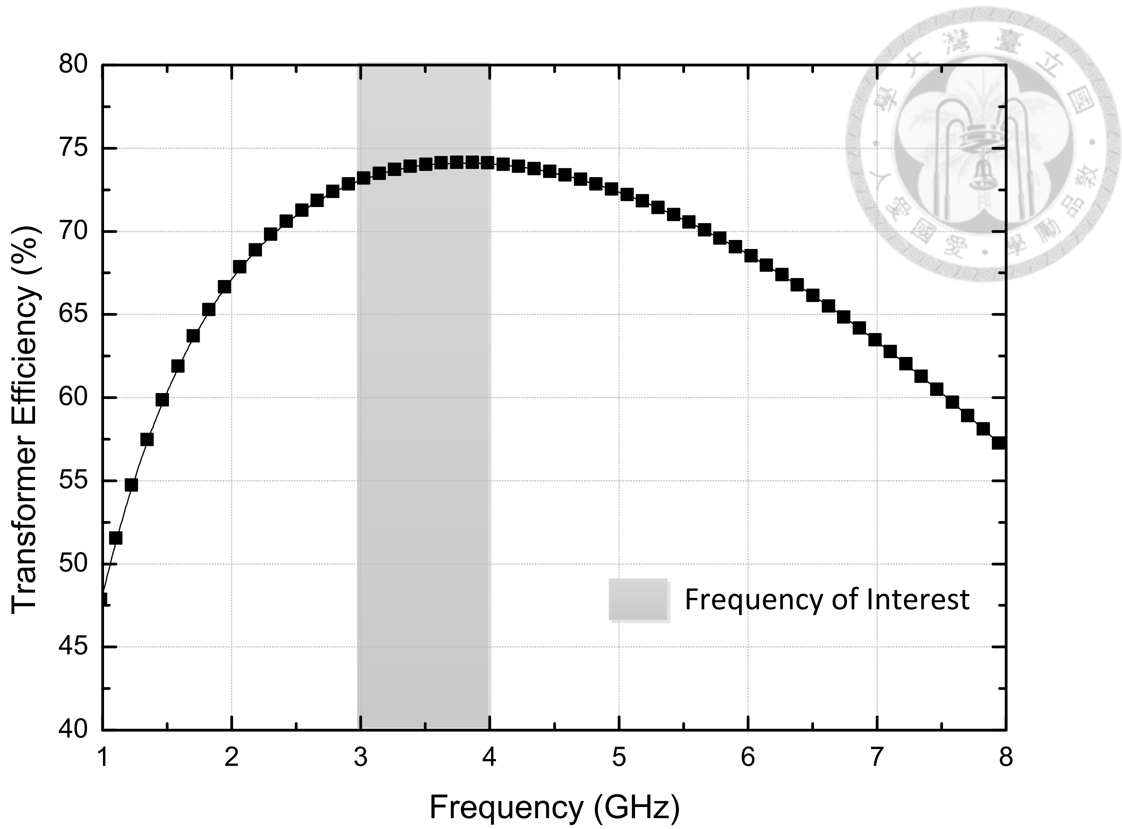

Figure 3.13 Simulated output transformer power transfer efficiency

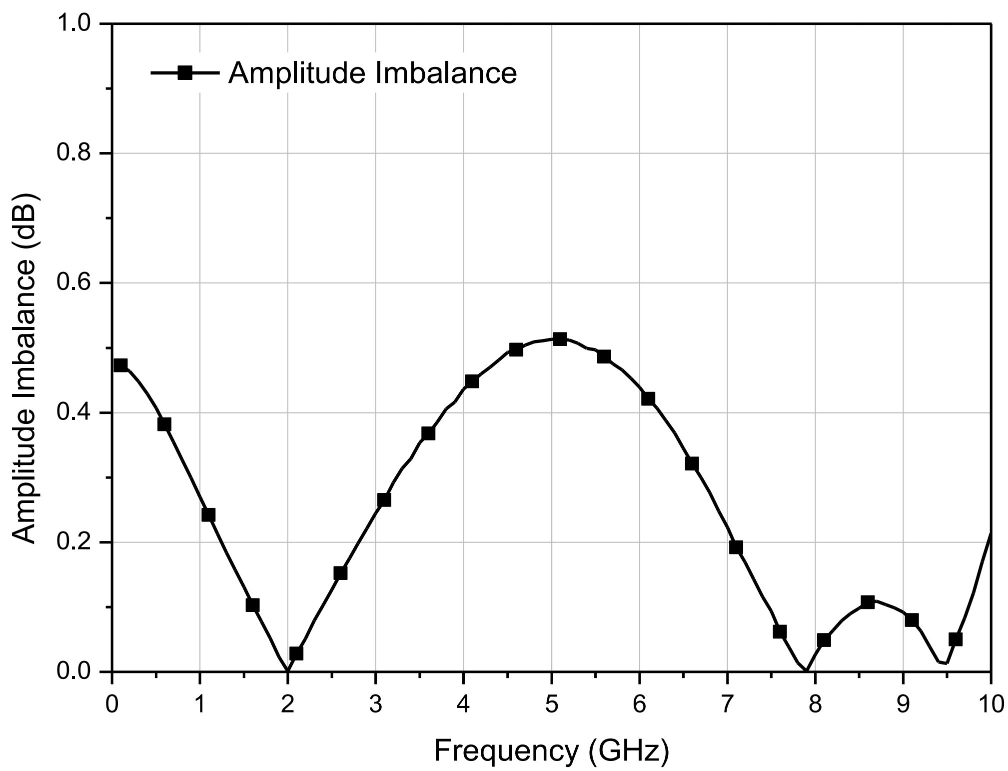

Figure 3.14 Amplitude imbalance of output transformer

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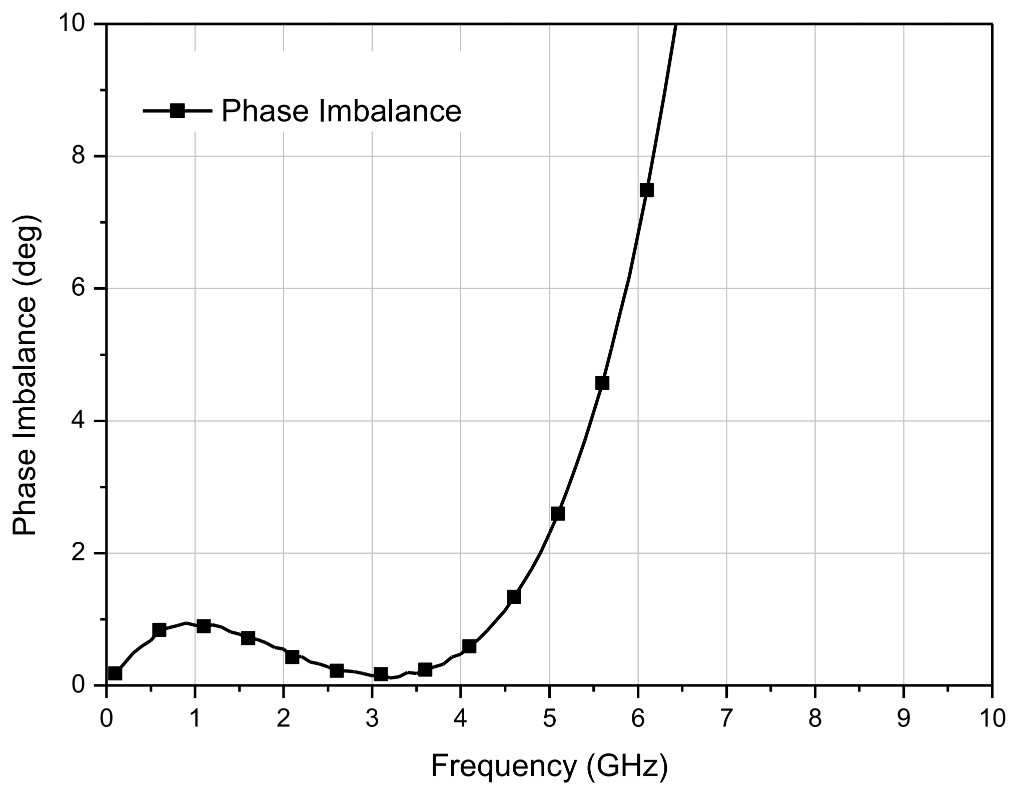

Figure 3.15 Phase imbalance of output transformer

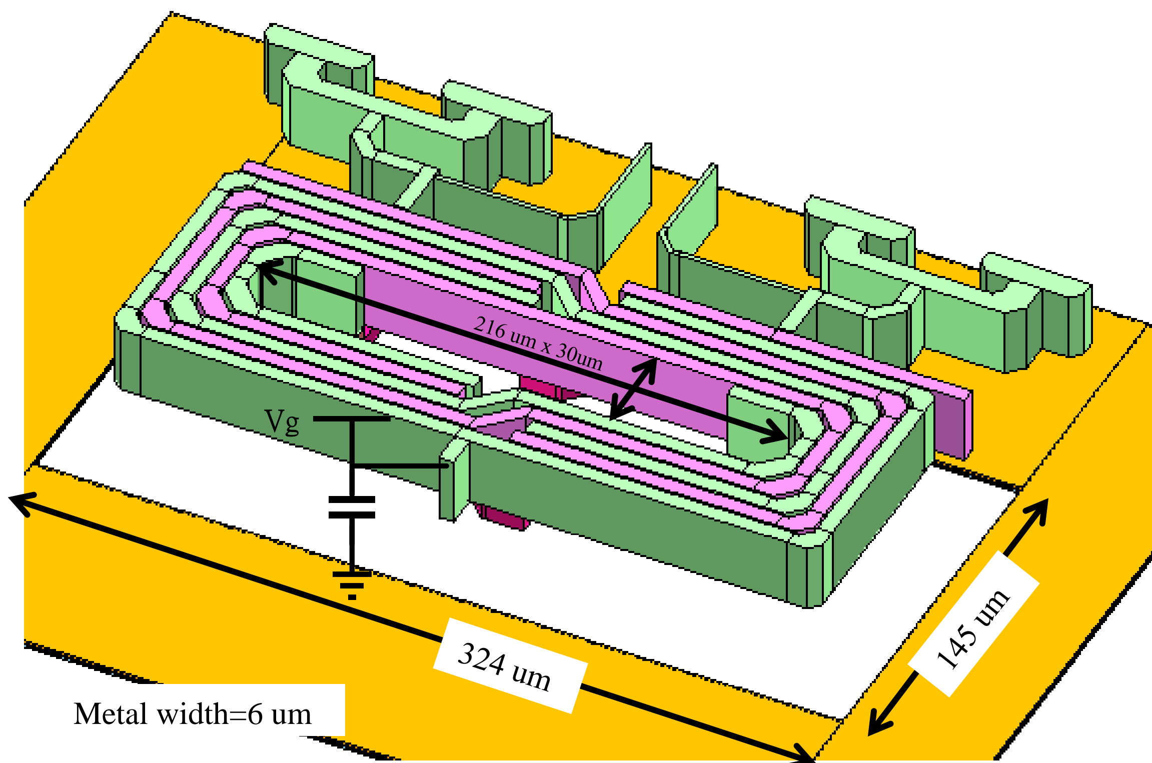

Figure 3.16 View of input transformer

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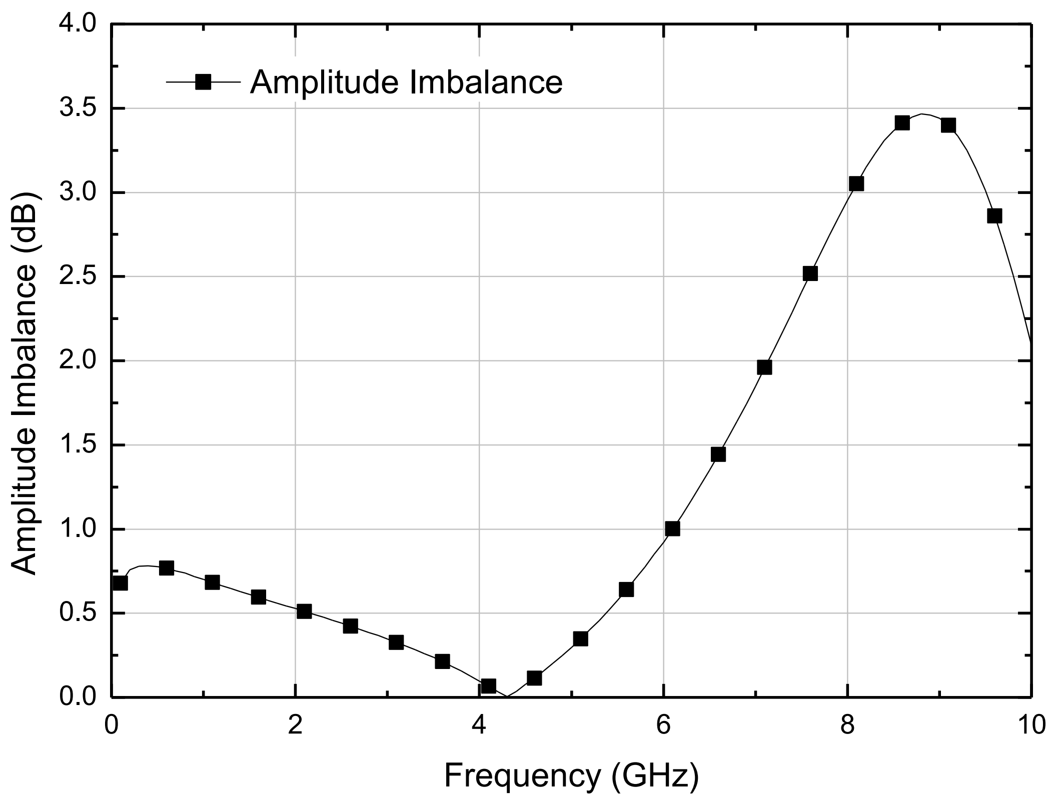

Figure 3.17 Amplitude imbalance of input transformer

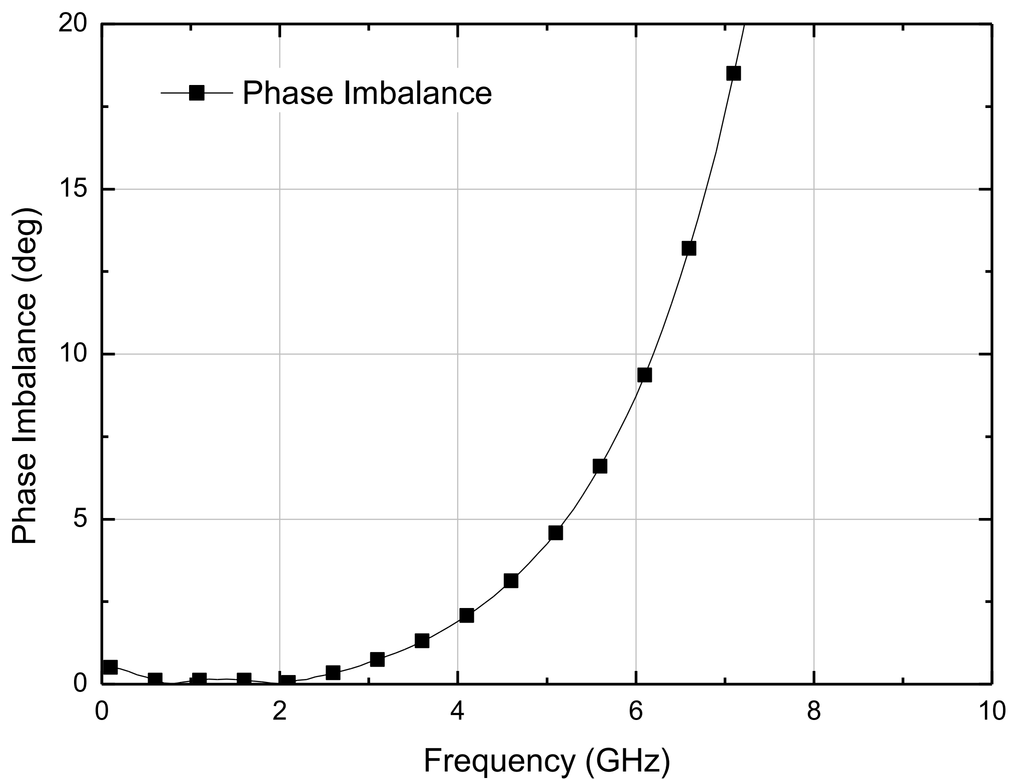

Figure 3.18 Phase imbalance of input transformer

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The geometry size of input transformer occupies $324 \times 145\ \mu m^2$ included the slotted ground as shown in Figure 3.16. The primary inductance is 2.087 nH and the secondary inductance is 2.142 nH. The amplitude imbalance is below 0.3 dB, phase imbalance is below 2 degree, and -7 dB insertion loss at 3.5 GHz as shown in Figure 3.17 and Figure 3.18.

In Figure 3.29, the small resistor R_1 which is inserted in the center tap of input transformer can have lossy matching and reduce the common-mode effect on unsymmetrical issues of differential-to-single transformers. The small value of resistance will degrade the quality factor of input transformer and solve the common-mode problem without effecting differential mode. Furthermore, the large resistor R_2 is placed before the bias voltage that can isolate RF signal from DC supply.

The common-source cell is composed by two common-source NMOSs and an odd-mode suppression resistor. Two common-source cells in differential operation are combined with input and output transformers, and which all construct the power cell as shown in Figure 3.29 below. Design parameters of the power cell are listed in Table 4-1.

Moreover, an odd-mode suppression resistor is shunted at the output of the two combined transistors to prevent odd-mode oscillation and ensure the amplifier stability. The K-factor stability check for power amplifier designs is only suitable for even modes. The combination of power cells in differential operation do not need the odd-mode oscillation test, only the N parallel combined devices require this test. Two-way direct-shunt combined power amplifier for the n=2 case is discussed here as an example to analyze the odd-mode oscillation. With the 2-port symmetrical z-matrix analysis, the even- and odd-mode impedances seen at each port can be expressed as

$$Z_e = Z_{11} + Z_{12} \qquad \text{even mode} \tag{3.10}$$

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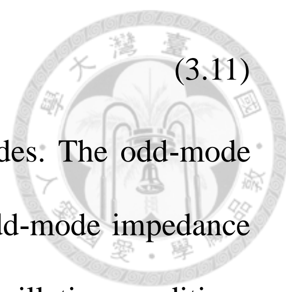

$$Z_o = Z_{11} - Z_{12} \qquad \text{odd mode} \tag{3.11}$$

Each power-combined power amplifier has even and odd modes. The odd-mode impedance seen at the power device is denoted by $Z_{in,o}$, and the odd-mode impedance seen at the output matching network is denoted by $Z_{out,o}$. Then the oscillation conditions can be expressed as

$$\mathrm{Re}\left\{Z_{in,o} + Z_{out,o}\right\} < 0 \tag{3.12}$$

$$\mathrm{Im}\left\{Z_{in,o} + Z_{out,o}\right\} = 0 \tag{3.13}$$

Hence, the odd-mode oscillation will happen if the above oscillation conditions are satisfied at some frequency. An odd-mode suppression resistor, R_{odd}, is required as shown in Figure 3.19 to avoid odd-mode oscillation between two parallel combined power devices in direct-shunt combining power amplifier design. The virtual ground at the center of the resistor is achieved in odd-mode operation. The odd-mode oscillation can be terminated if the half of R_{odd} is equal to the output impedance of a single transistor M_1 or M_2. The value of the odd-mode suppression resistor after fine-tuning has the sum of the real parts of the odd-mode impedance at each port that is greater than 0. As a result, the odd-mode oscillation conditions will not be occurred.

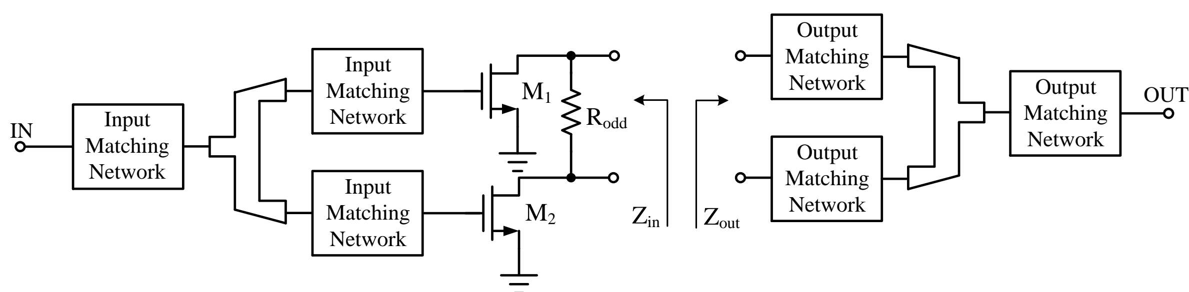

Figure 3.19 Schematic of a 2-way direct-shunt combining power amplifier. [54]

There are two methods to approach to simulate for the odd-mode suppression resistors. The first method is used the above theoretical descriptions and equations, and

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schematics of the simulated setup are shown in Figure 3.20 and Figure 3.23. The simulated results at the transistor gate are shown in Figure 3.21 and Figure 3.22, and the simulated results at the transistor drain are shown in Figure 3.24 and Figure 3.25. The simulated results express they are not in oscillation condition, as a result, the circuit is stable and the odd-mode suppression resistors are not necessary.

The second method is simply observing the input return loss at the combined nodes of the combined transistors that illustrates in Figure 3.26. This simulation is to force an odd-mode signal occur in the power amplifier, if the input return loss is more than zero then the power amplifier will be oscillated. In order to avoid the oscillation, the odd-mode suppression resistor is inserted and can deduct the return loss where the lower return loss the better it is in the simulation.

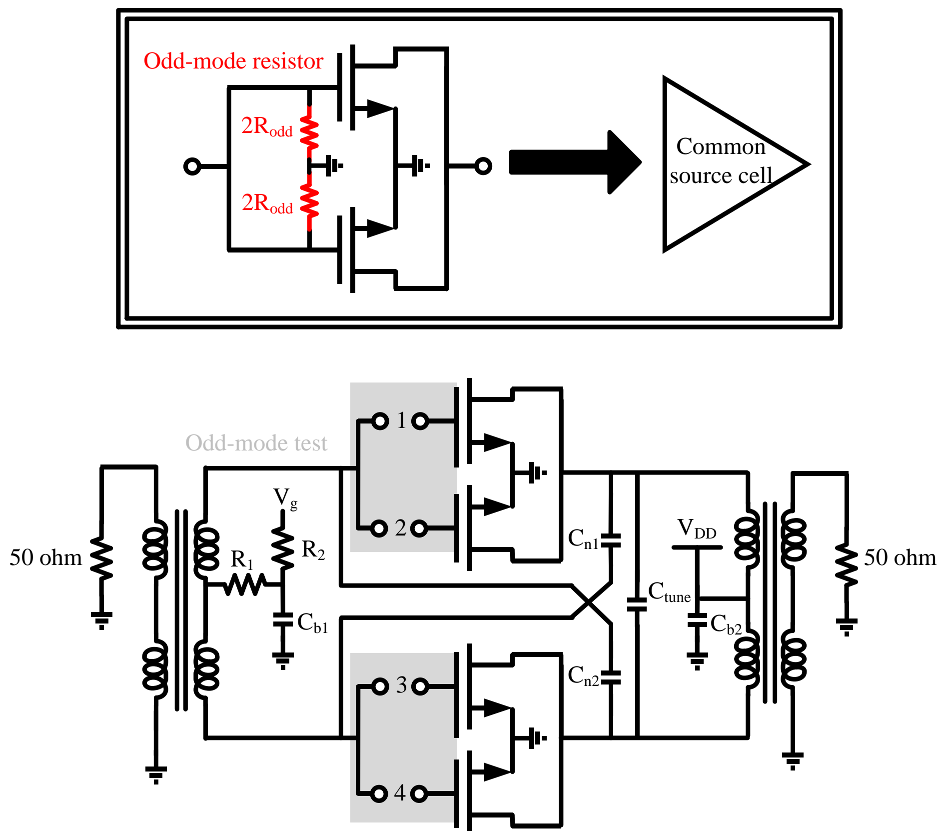

Figure 3.20 The schematics of odd-mode test at transistor gate

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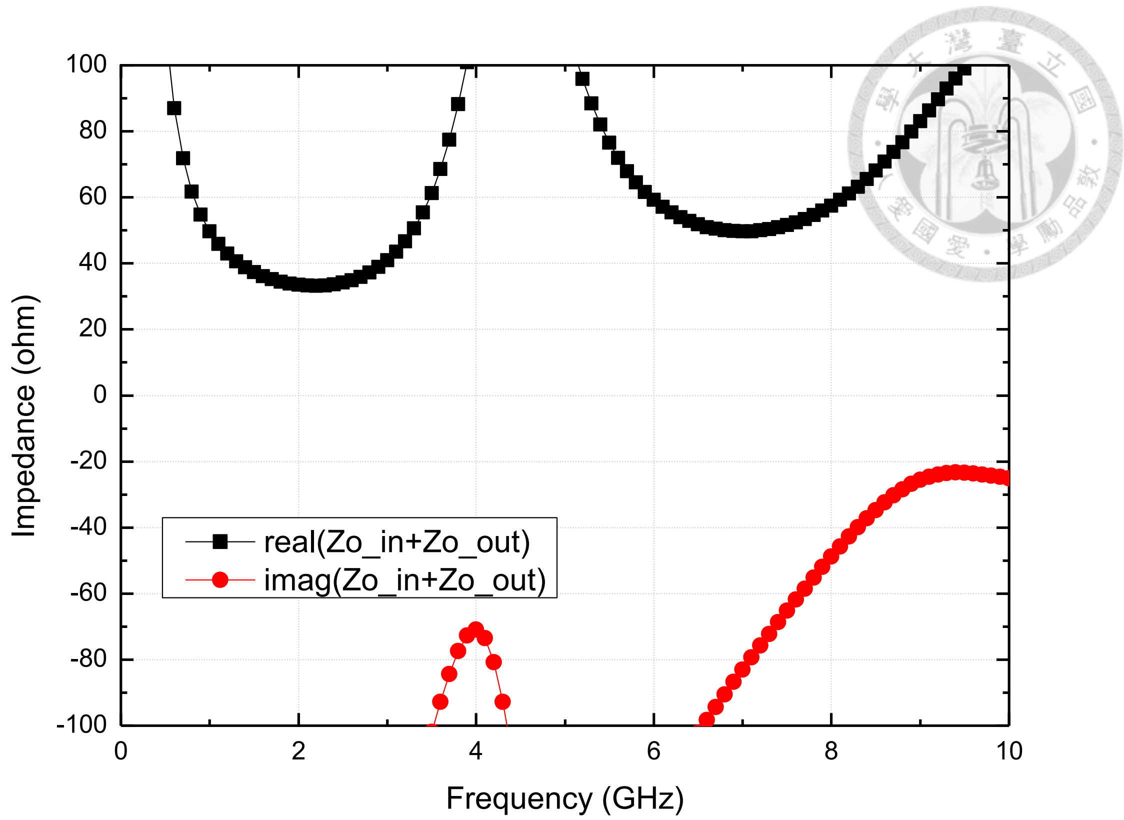

Figure 3.21 The measured result of odd-mode test at top part of transistor gate

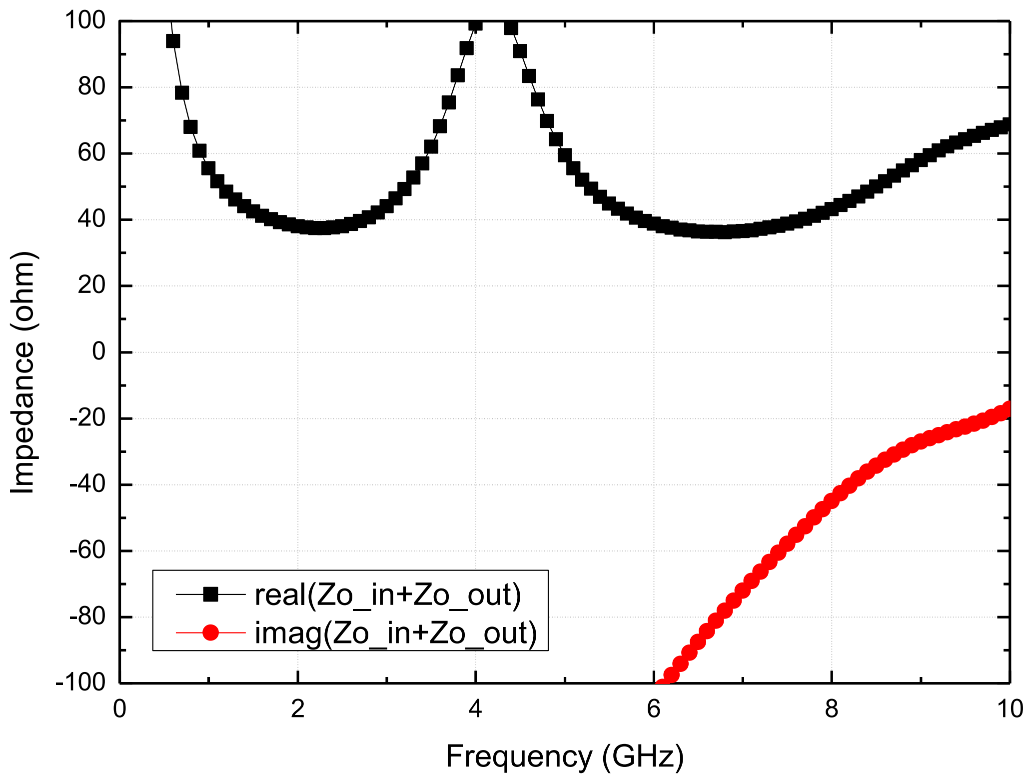

Figure 3.22 The measured result of odd-mode test at bottom part of transistor gate

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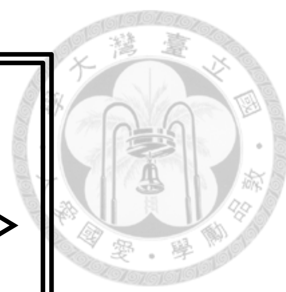

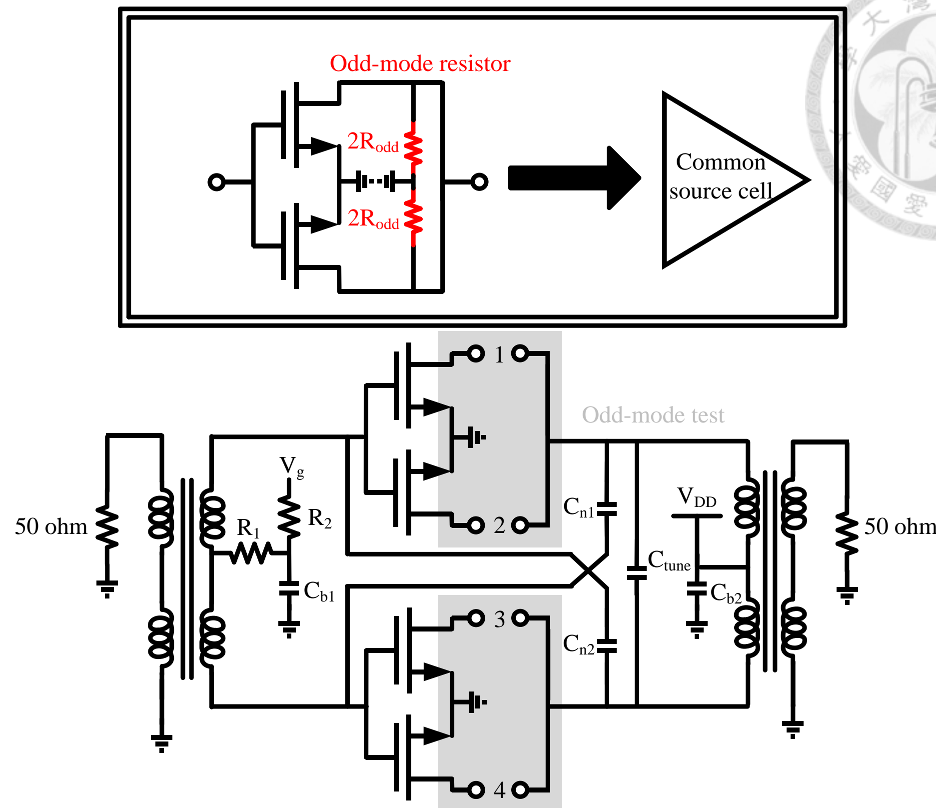

Figure 3.23 The schematics of odd-mode test at transistor drain

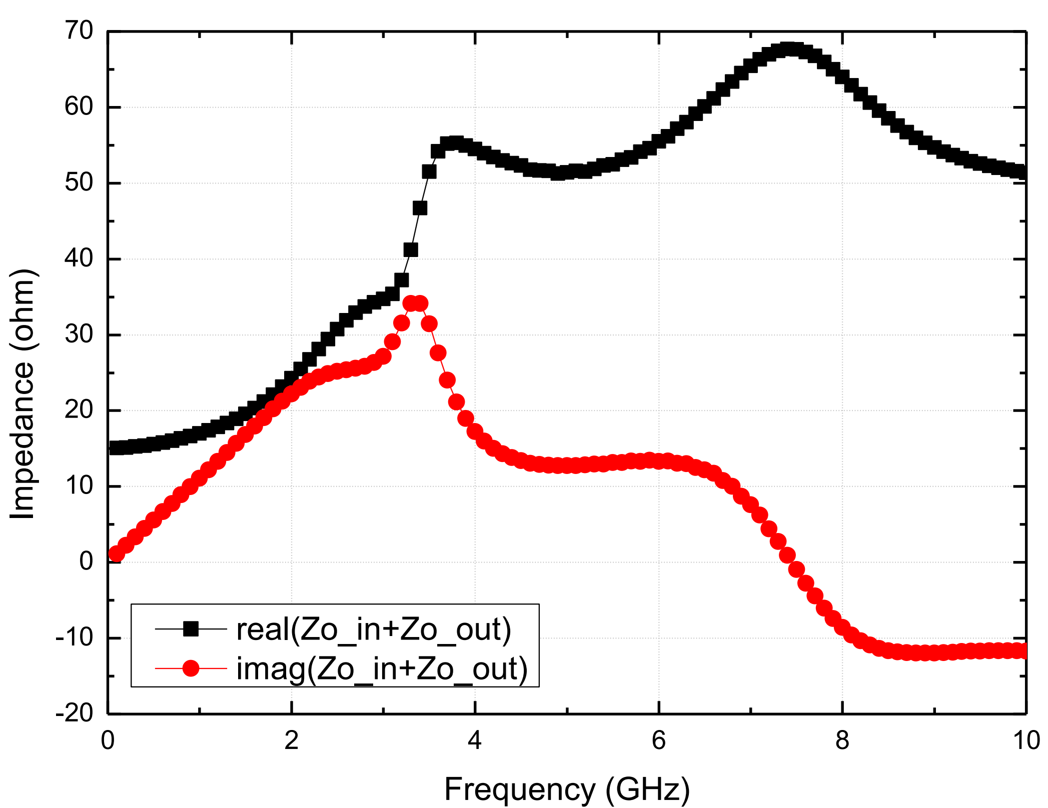

Figure 3.24 The measured result of odd-mode test at top part of transistor drain

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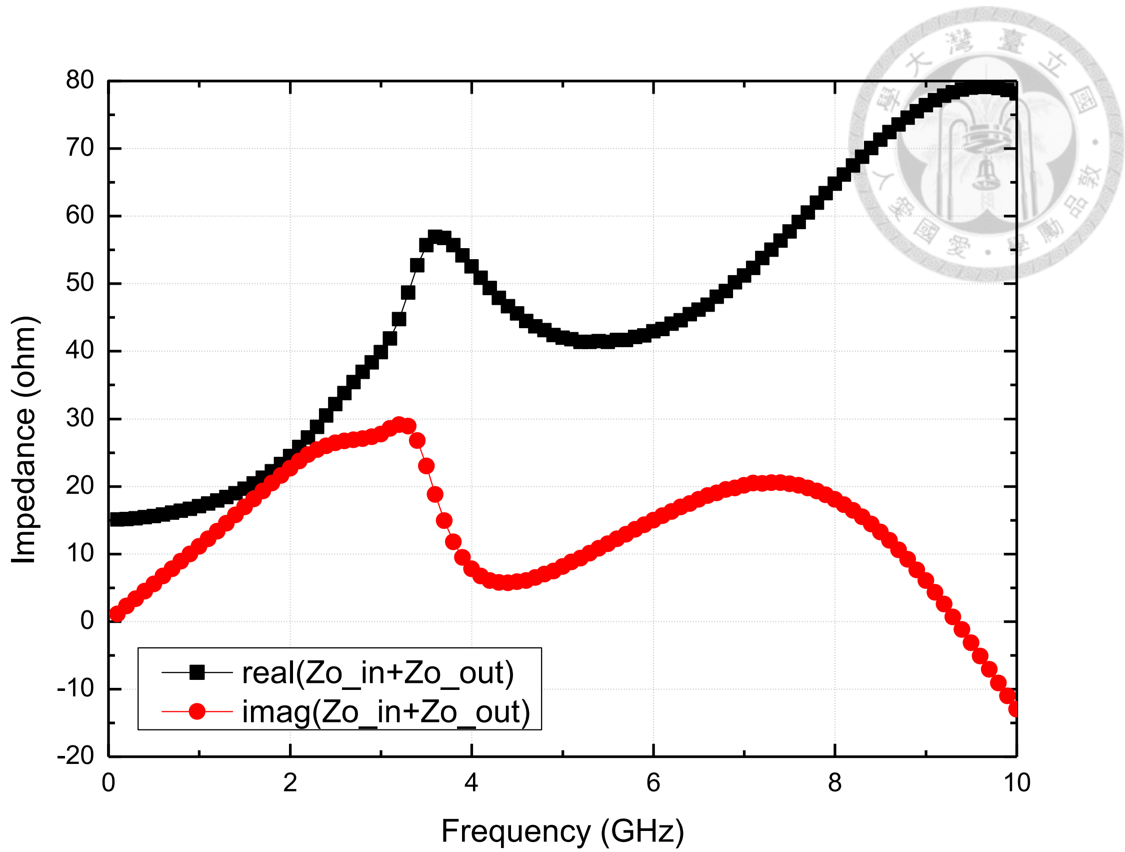
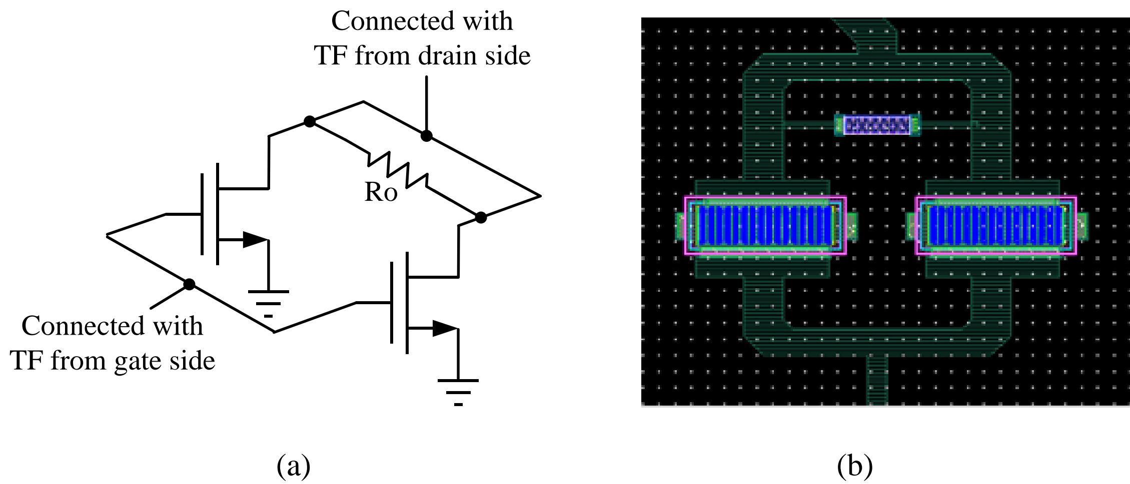


Figure 3.25 The measured result of odd-mode test at bottom part of transistor drain



(a) (b)

Figure 3.26 (a) Odd-mode test concept (b) layout view

Between shorted and very large resistance, there is appropriate values in the range. The simulated results are shown in Figure 3.27 and Figure 3.28. The odd-mode suppression resistor is decided as 56 ohm according to the simulated results and layout spacing consideration.

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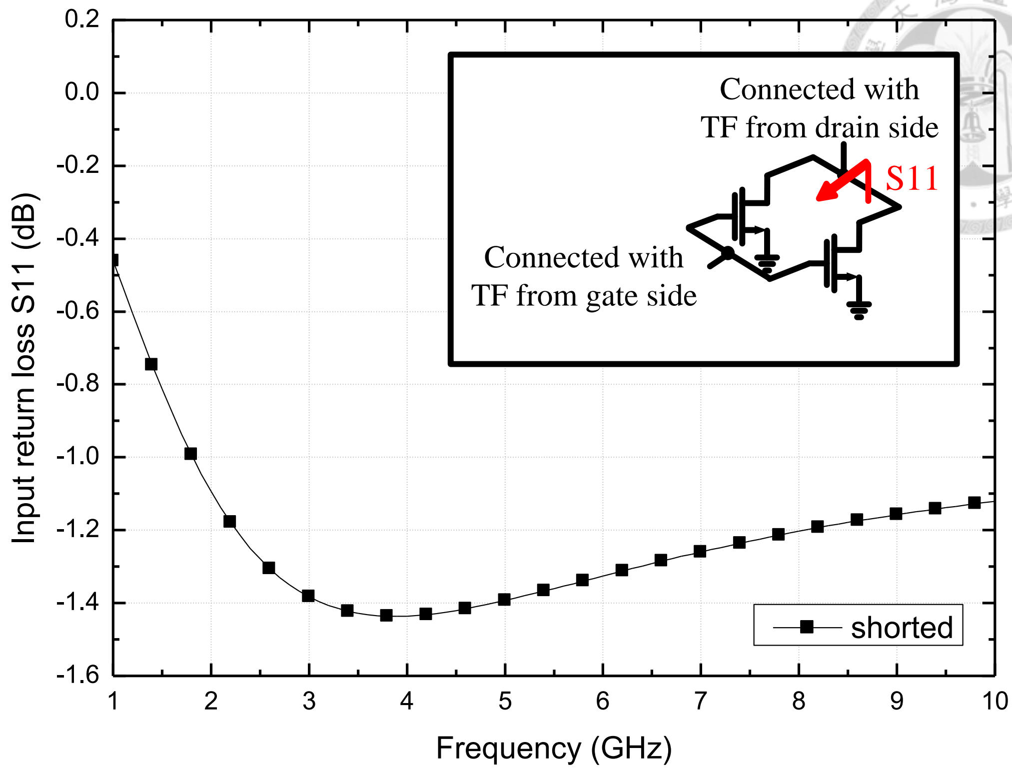

Figure 3.27 Odd-mode simulation from transistor drain

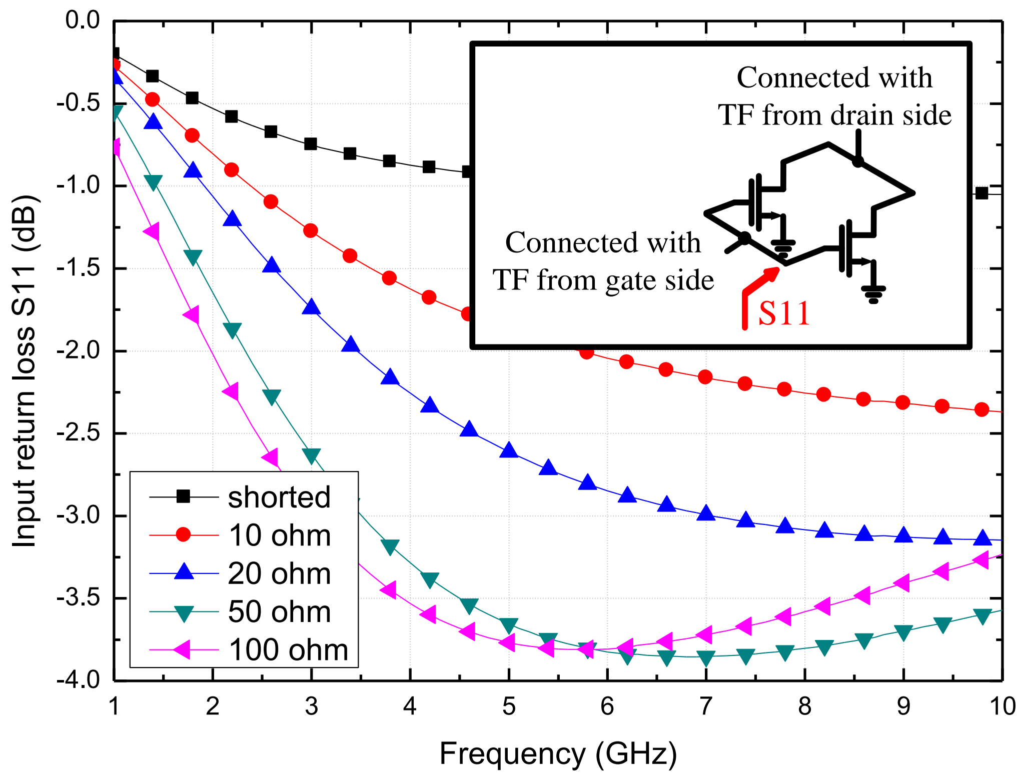

Figure 3.28 Odd-mode simulation from transistor gate

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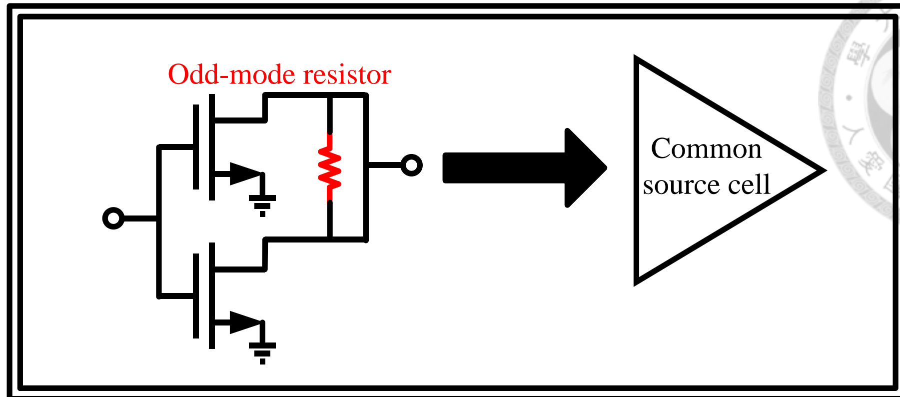

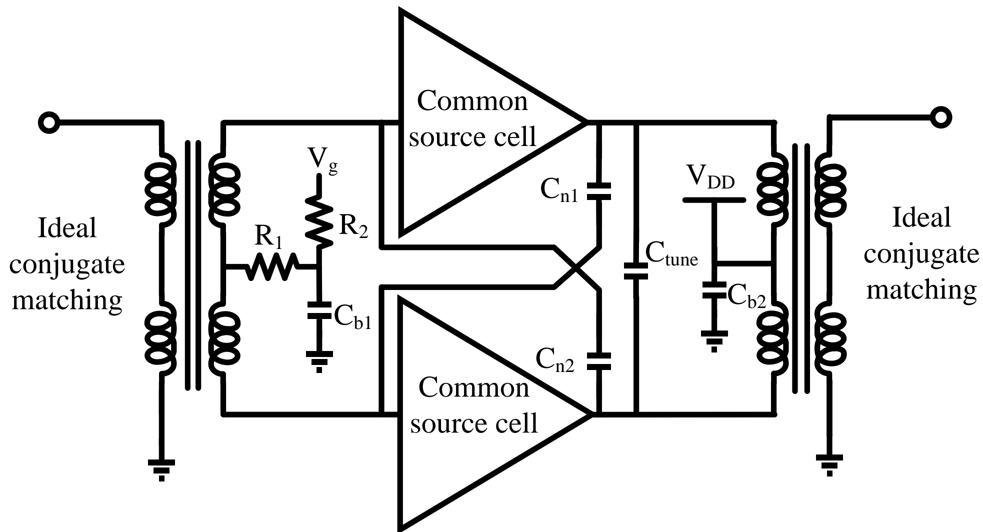

Figure 3.29 Schematic of a power cell

Table 3-3 The Listed Parameters of a Power Cell

Transistor Size		(10μm × 32) × 2	
Parameter	**Value**	**Parameter**	**Value**
L_{p_out}	1.023 nH	C_{b1}	8 pF
L_{s_out}	2.704 nH	C_{b2}	20 pF
L_{p_in}	2.087 nH	C_{tune}	720 fF
L_{s_in}	2.142 nH	C_{n1}, C_{n2}	185 fF
R_1	14 Ω	R_2	3 kΩ
Bias Voltage			
V_{DD}		5V	
V_g		1.2V	

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3.1.3 Neutralization Design

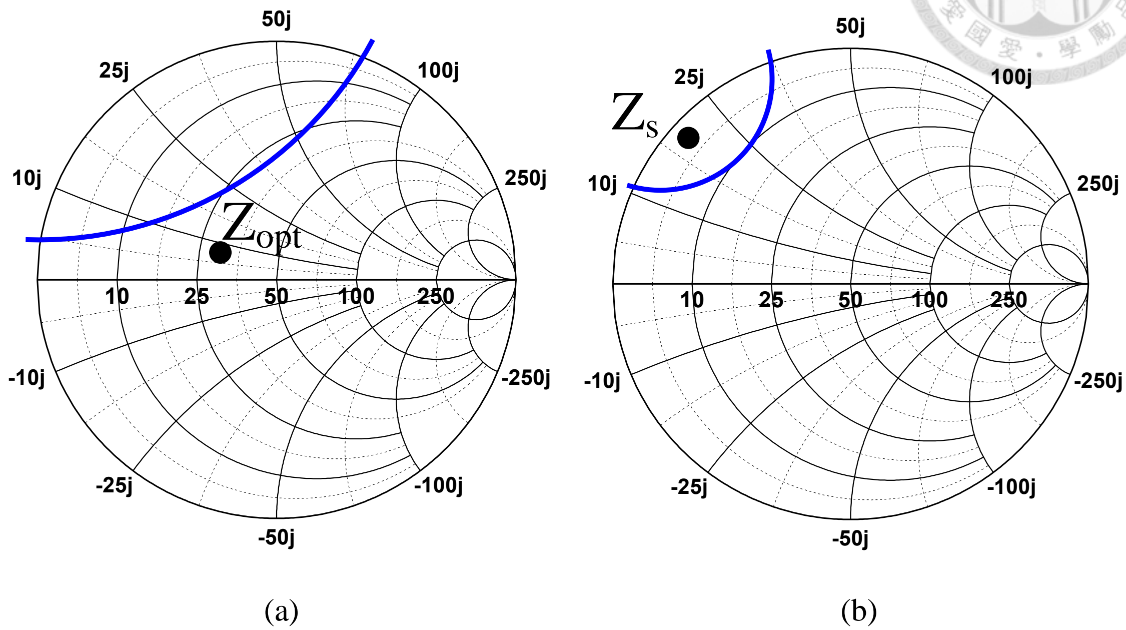

Figure 3.30 (a) Z_{opt} and load stability circle (b) Z_s and source stability circle of LDMOS at 3.5 GHz.

Although the optimal load (Z_{opt}) of LDMOS device is higher than core MOS transistor due to the high supply voltage, the very low conjugate source impedance (Z_s) of the LDMOS device becomes a design challenge contrarily. Take the transistor size of 10 µm width and 32 fingers for example; the Z_{opt} of two LDMOS transistors in parallel is 30.3+8.3j Ω at 3.5 GHz from load-pull simulation, which is higher than core MOS devices in 40-nm process. Therefore, LDMOS provides an easier output matching network that reduces the complexity of transformer design for miniature area. Also, the Z_{opt} is located in stable region shown in Figure 3.30(a). However, the Z_s of the two LDMOS transistors in parallel is 3.87+20.2j Ω at 3.5 GHz, which is the major number limitation of direct-combined transistor in practical implementation. In addition, Z_s of LDMOS falls in unstable region of source stability circle as shown in Figure 3.30(b). To solve the stability problem, the neutralization of cross-coupled capacitors C_n is allocated

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between the gate and drain terminals of differential PA-cells. Capacitive neutralization can cancel undesired feedback through the gate-to-drain capacitor (C_{gd}) to avoid oscillation [9].

Large transistor size is usually used to achieve high output power in power amplifier design. However, the larger the transistor size, the higher the intrinsic capacitance of C_{gd}, and the lower the reverse isolation of transistor. Moreover, the reverse isolation is directly related to S_{12} of the transistor, and increasing S_{12} will degrade the maximum stable/available gain (MSG/MAG) of the transistor where MSG and MAG can be expressed as

$$\begin{aligned} \text{MSG} &= \left|\frac{S_{21}}{S_{12}}\right| \\ \text{MAG} &= \left|\frac{S_{21}}{S_{12}}\right|(K - \sqrt{K^2 - 1}) \end{aligned} \tag{3.14}$$

The effect of intrinsic capacitor C_{gd} on the reverse isolation will become more significant in the millimeter-wave frequency designs, and the poor reverse isolation may lead to instability of the power amplifier. Furthermore, if the gain of power stage is too low, the performance of PAE will become poor. As a result, the gain of the power amplifier becomes more precious in higher frequency band.

Neutralization technique is one of the methods to increase the power gain of the transistor. The neutralization can use the equivalent negative capacitance ($-C_N$) to cancel the gate-to-drain intrinsic capacitance (C_{gd}) of the transistor. By using cross-couple capacitors between the gate and drain of the two transistors in differential operation, it can produce the negative capacitance. Figure 3.31 shows the circuit topology of a pseudo-differential common-source cell with the neutralization capacitors (C_N) and its ac equivalent model. To verify this concept, the Y-parameters of the circuit shown in Fig. are calculated to derive the correlation between the MSG/MAG, C_{gd} and C_N. The

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Y-parameters of the differential common-source cell can be expressed as

$$\begin{aligned} Y_{11} &= 1/R_G + j\omega C_{gs} + j\omega(C_{gd} + C_N) \\ Y_{12} &= -j\omega(C_{gd} - C_N) \\ Y_{21} &= g_m - j\omega(C_{gd} - C_N) \\ Y_{22} &= 1/R_D + j\omega C_{db} + j\omega(C_{gd} + C_N) \end{aligned} \qquad (3.15)$$

where R_G, C_{gs}, and C_{db} are the equivalent parallel gate resistance, gate-to-source capacitance, and drain-to-body capacitance. Since the MAG is related to the stability factor (K), so the relation between K and C_N must be considered first. The stability factor K consisting of Y-parameters can be expressed as

$$K = \frac{2\,\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|} \qquad (3.16)$$

Substituting the Y-parameters derived in Eqn. (3.15), and then K can be equal to

$$K = \frac{2 + \omega^2 (C_{gd} - C_N)^2 \mathrm{R}_G \mathrm{R}_D}{\omega |C_{gd} - C_N| R_G R_D \sqrt{\omega^2 (C_{gd} - C_N)^2 + g_m{}^2}} \qquad (3.17)$$

The stability factor related to C_N shows the value of K when C_N equals C_{gd}, which means the differential cell achieves the highest stability when C_{gd} is neutralized.

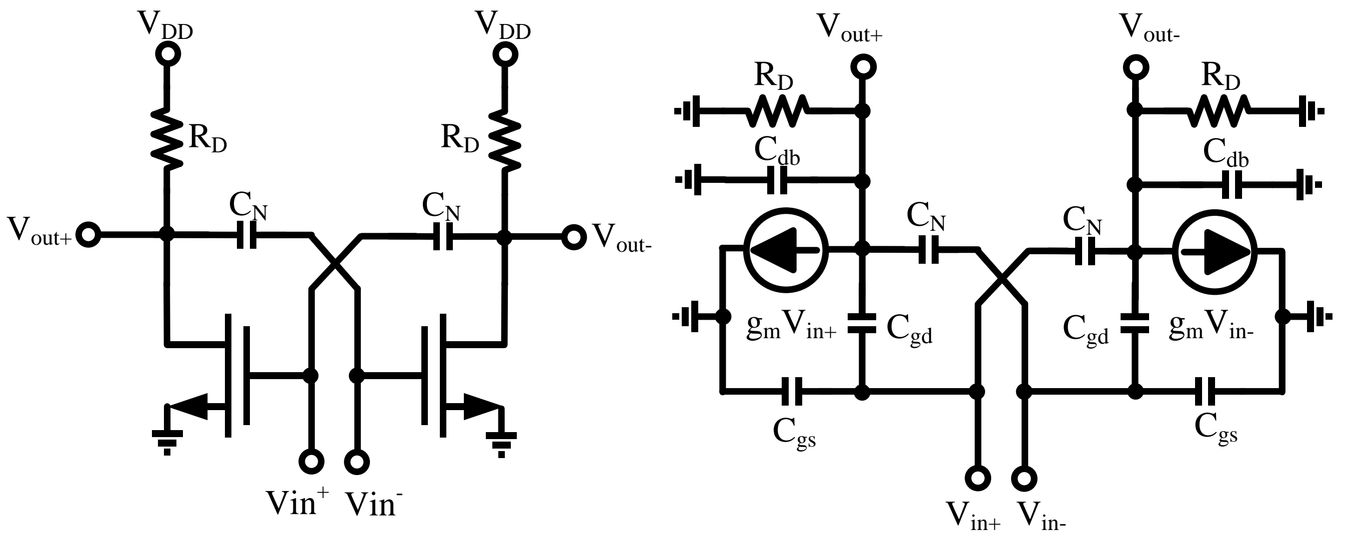

Figure 3.31 (a) Differential common-source cell with the neutralization capacitor (C_N) in cross-couple connection and (b) its ac equivalent circuit.

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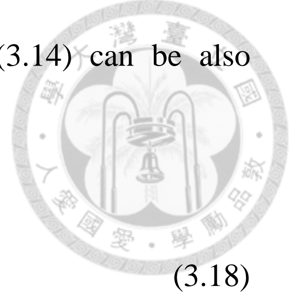
Moreover, S_{21} and S_{12} in the MSG/MAG shown in Eqn. (3.14) can be also substituted by the Y-parameters, and they can be expressed as



$$S_{21} = \frac{-2Y_{21}Y_0}{(Y_{11}+Y_0)(Y_{22}+Y_0)-Y_{12}Y_{21}}$$
$$S_{12} = \frac{-2Y_{12}Y_0}{(Y_{11}+Y_0)(Y_{22}+Y_0)-Y_{12}Y_{21}} \tag{3.18}$$

where Y_0 is equal to $1/Z_0$. Then, MSG/MAG composed of Y-parameters is expressed as

$$\text{MSG}=\left|\frac{Y_{21}}{Y_{12}}\right|$$
$$\text{MAG}=\left|\frac{Y_{21}}{Y_{12}}\right|(K-\sqrt{K^2-1}) \tag{3.19}$$

Finally, substituting the Y-parameters shown in Eqn. (3.15) into Eqn. (3.19), the MSG/MAG can be expressed as

$$\text{MSG}=\frac{\sqrt{\omega^2(C_{gd}-C_N)^2+{g_m}^2}}{\omega\left|C_{gd}-C_N\right|}$$
$$\text{MAG}=\frac{\sqrt{\omega^2(C_{gd}-C_N)^2+{g_m}^2}}{\omega\left|C_{gd}-C_N\right|}(K-\sqrt{K^2-1}) \tag{3.20}$$

where K composed of the Y-parameters can be found in Eqn. (3.16). From Eqn. (3.20), the MSG achieves the maximum value when C_{gd} is neutralized by C_N. Considering the gain and stability, the neutralization capacitance close to or slightly over C_{gd} is usually chosen instead of selecting the value of C_N that is equal to C_{gd}. When C_N is close to C_{gd}, the gain of the differential cell approaches the maximum value with an acceptable stability factor. Figure 3.32 shows the simulated MSG/MAG, K, and S_{12} of the differential cell at 3.5 GHz and from 3 to 4 GHz versus different values of C_N. This differential cell with the transistor size (M) of 2×10μm×32fingers in 40-nm CMOS process is biased at 1.2-V V_{DD} and Class AB. C_{gd} of the transistors which can be calculated from Eqn. (3.20) in this differential cell under Class-AB bias are about 185 fF.

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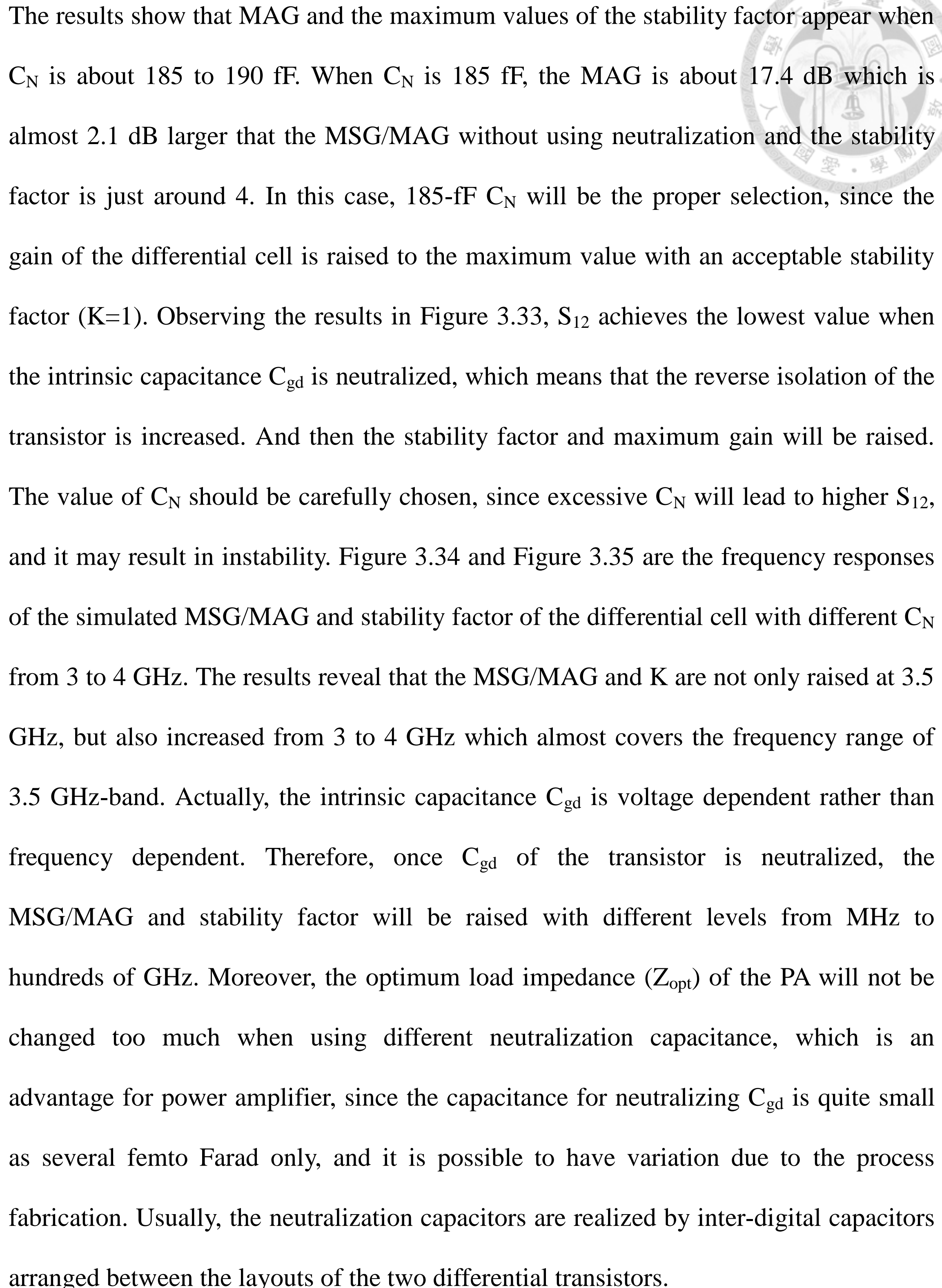

The results show that MAG and the maximum values of the stability factor appear when C_N is about 185 to 190 fF. When C_N is 185 fF, the MAG is about 17.4 dB which is almost 2.1 dB larger that the MSG/MAG without using neutralization and the stability factor is just around 4. In this case, 185-fF C_N will be the proper selection, since the gain of the differential cell is raised to the maximum value with an acceptable stability factor (K=1). Observing the results in Figure 3.33, S_{12} achieves the lowest value when the intrinsic capacitance C_{gd} is neutralized, which means that the reverse isolation of the transistor is increased. And then the stability factor and maximum gain will be raised. The value of C_N should be carefully chosen, since excessive C_N will lead to higher S_{12}, and it may result in instability. Figure 3.34 and Figure 3.35 are the frequency responses of the simulated MSG/MAG and stability factor of the differential cell with different C_N from 3 to 4 GHz. The results reveal that the MSG/MAG and K are not only raised at 3.5 GHz, but also increased from 3 to 4 GHz which almost covers the frequency range of 3.5 GHz-band. Actually, the intrinsic capacitance C_{gd} is voltage dependent rather than frequency dependent. Therefore, once C_{gd} of the transistor is neutralized, the MSG/MAG and stability factor will be raised with different levels from MHz to hundreds of GHz. Moreover, the optimum load impedance (Z_{opt}) of the PA will not be changed too much when using different neutralization capacitance, which is an advantage for power amplifier, since the capacitance for neutralizing C_{gd} is quite small as several femto Farad only, and it is possible to have variation due to the process fabrication. Usually, the neutralization capacitors are realized by inter-digital capacitors arranged between the layouts of the two differential transistors.

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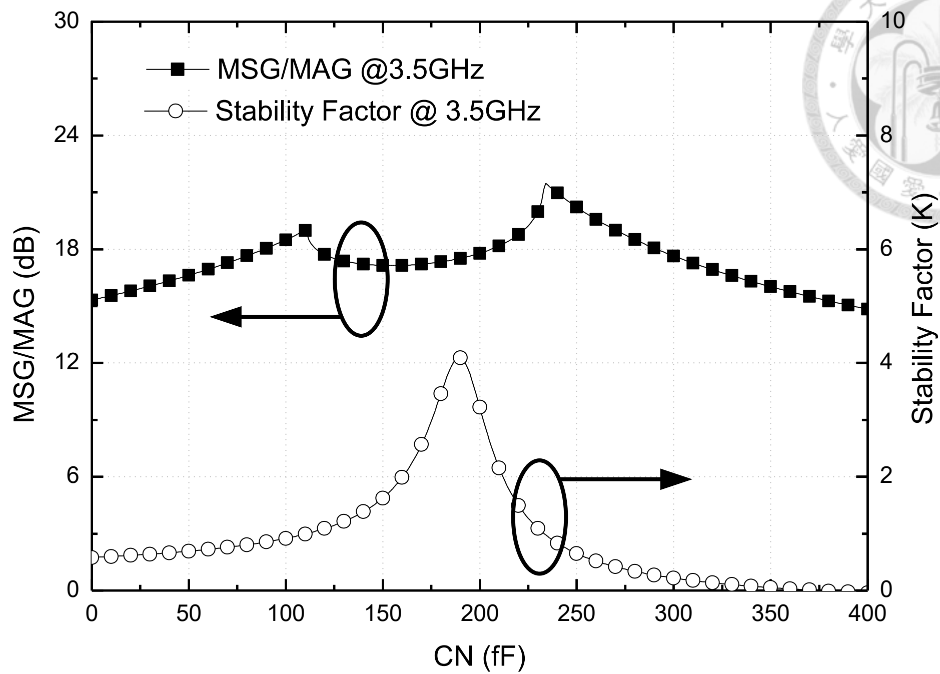

Figure 3.32 The simulated MSG/MAG and stability factor (K) of the differential cell versus neutralization capacitance (C_N). The cell with transistor size of 2×10μm×32 fingers is biased at 1.2-V V_{DD} Class AB.

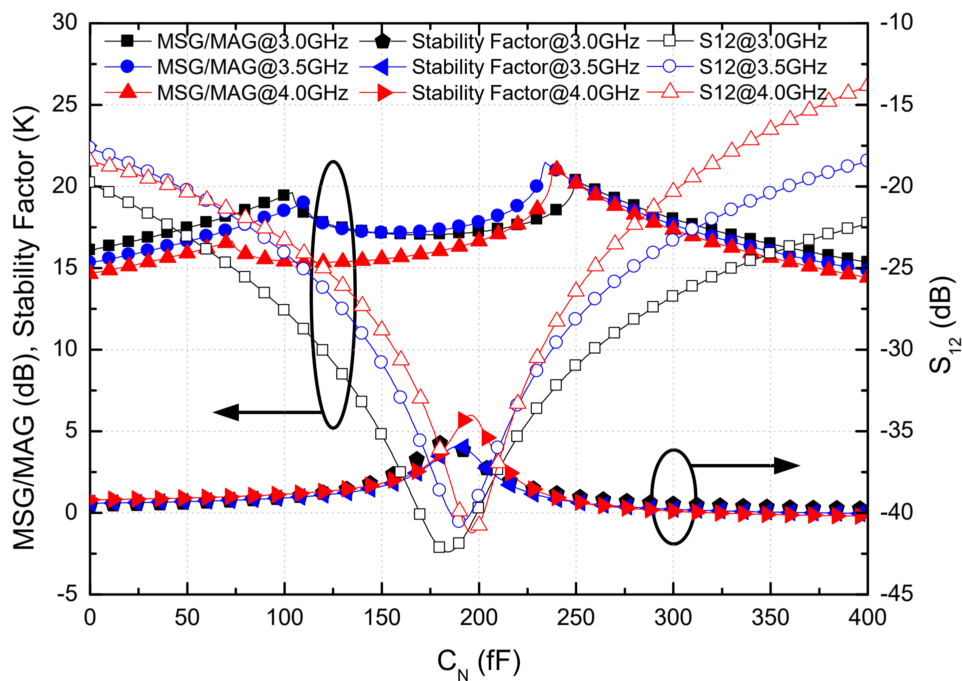

Figure 3.33 The simulated MSG/MAG, stability factor (K), and S_{12} of the differential cell versus neutralization capacitance (C_N) from 3 to 4 GHz.

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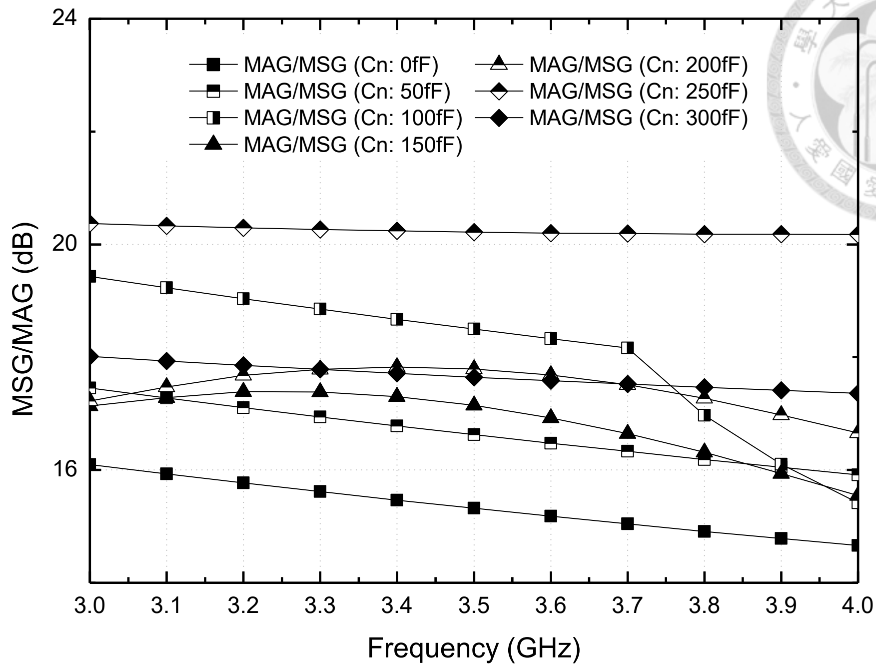

Figure 3.34 The simulated MSG/MAG of the differential cell with different C_N from 3 to 4 GHz. The cell with the transistor size of 2×10μm×32 fingers is biased at 5-V V_{DD} and Class AB.

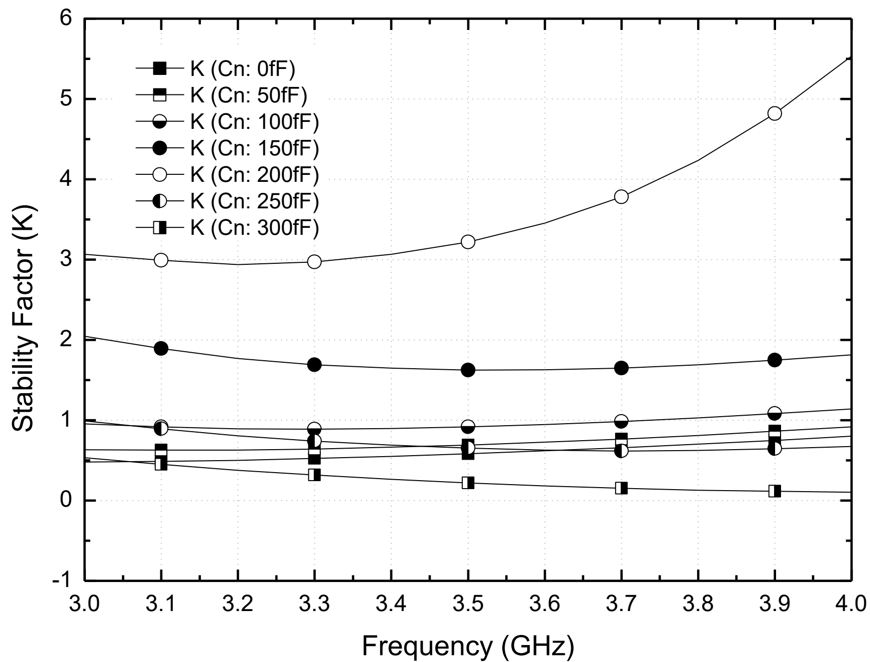

Figure 3.35 The simulated stability factor of the differential cell with different C_N from 3 to 4 GHz. The simulation conditions are the same as in Figure 3.34.

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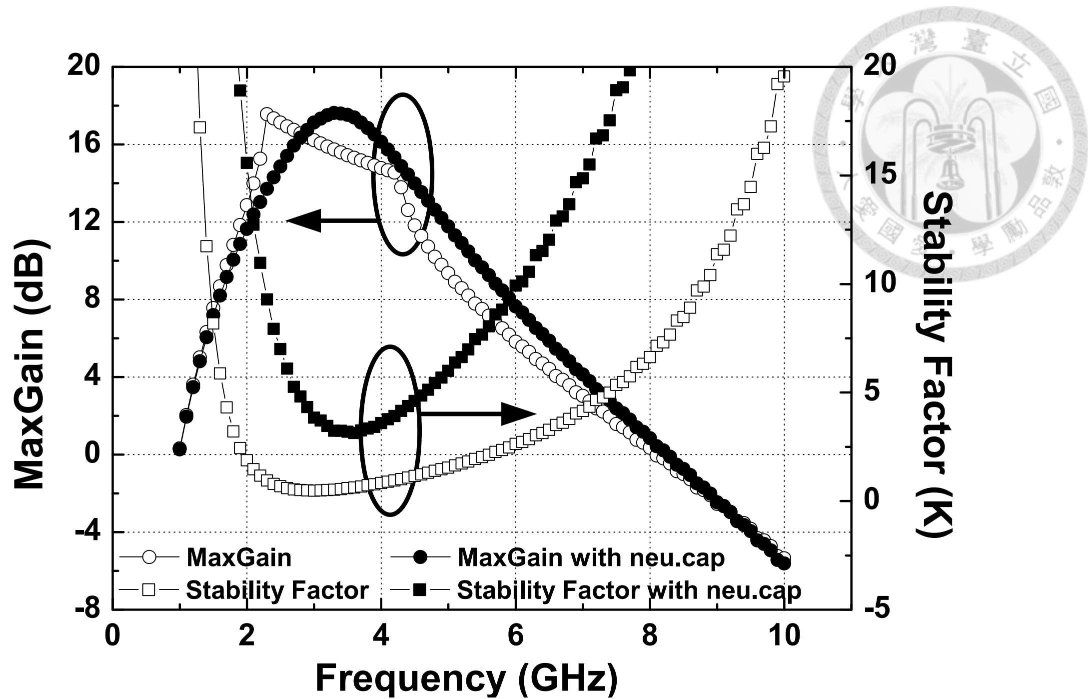

Figure 3.36 Stability factor and maximum gain with/without capacitive neutralization.

Since the device itself has the instability issues, the maximum power gain and stability factor with and without capacitive neutralization are plotted in Figure 3.36. With the neutralization technique, the stability factor is higher than 1 and maximum power gain is improved substantially.

Figure 3.37 is the circuit schematic setup of a differential cell of common-source with neutralization capacitors for load-pull simulation in ADS. The transistors in the differential cell are biased at 1.2-V V_{DD} and Class AB with both sizes of 2×10 μm×32 fingers. Table 3-4 summarizes the differential optimum load impedance ($Z_{opt,diff}$), P_{SAT}, and PAE_{max} of the differential cell under different C_N. From Table 3-4, the differential cell has the average $Z_{opt,diff}$ of 35.1-j9.34 Ω with <13.7% real-part and <11.1% imaginary-part variations, P_{SAT} of 25.84dBm with <0.155% variation, and PAE_{max} of 31.7% with <2.2% variation under 0 to 400-fF C_N. The results show that P_{SAT}, PAE_{max}, and $Z_{opt,diff}$ are only slightly affected by the neutralization capacitors C_N.

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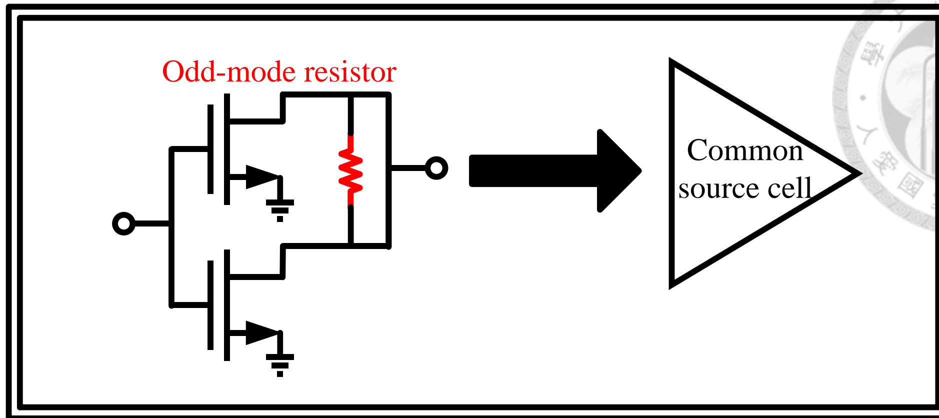

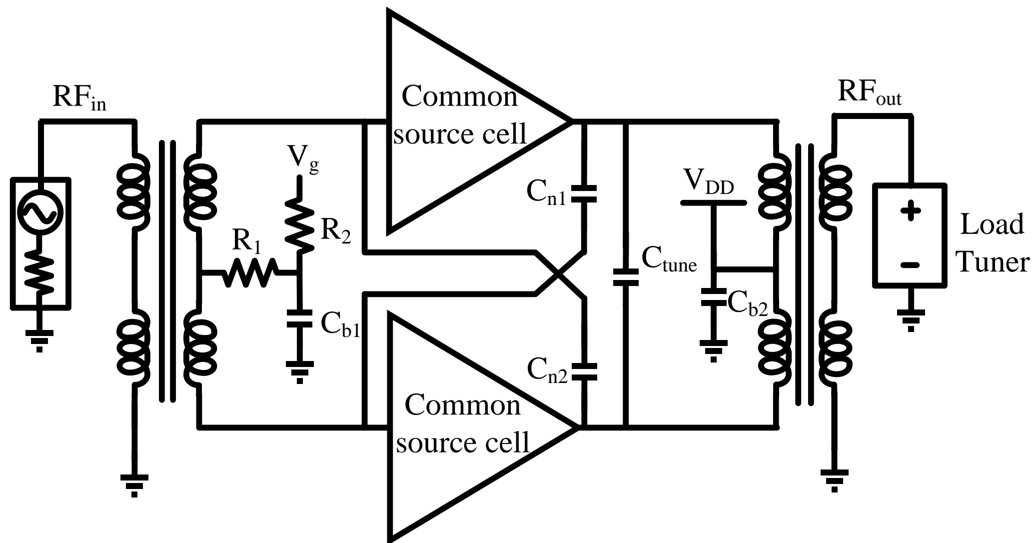

Figure 3.37 The circuit schematic setup of the load-pull simulation with C_N in the ADS. The transistors with the size of 2×10μm×32 fingers are biased at Class AB and 5-V V_{DD} for load-pull demonstration.

Table 3-4 The $Z_{opt,diff}$, P_{SAT}, PAE_{max} versus Different C_N at 3.5 GHz

C_N	**0 fF**	**50 fF**	**100 fF**	**150 fF**	**200 fF**
$Z_{opt,diff}$	36.3-j9.6 Ω	36.3-j9.6 Ω	36.3-j9.6 Ω	36.3-j9.6 Ω	30.3-j8.3 Ω
P_{SAT}	25.80 dBm	25.81 dBm	25.82 dBm	25.83 dBm	25.84 dBm
PAE_{max}	31.93 %	31.90 %	31.86 %	31.80 %	31.01 %

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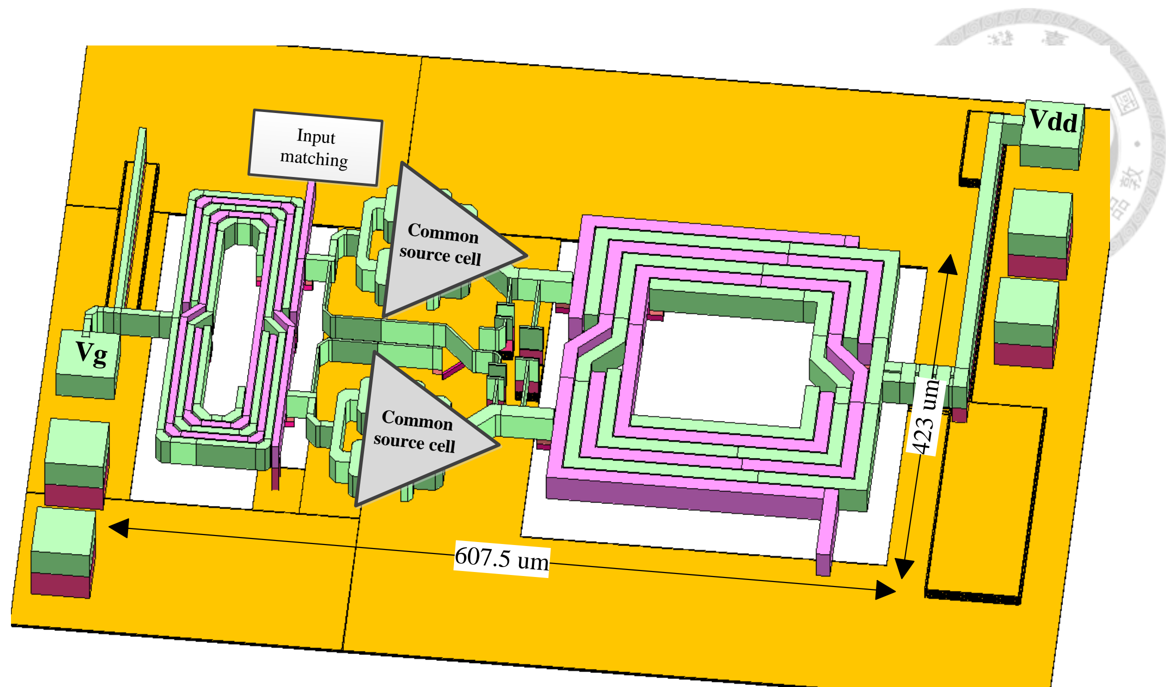

Figure 3.38 View of a whole power cell

3.1.4 I/O Matching Network

Output matching network is neglected since the resultant value of impedance transformation from the transistor device to the output transformer is approximate to the 50-Ω load. However, the input impedance of the transistor device from load-pull simulation is 3.87+20.2j **Ω**. The input matching network uses a 1-pF capacitor in series and a 0.9-pF shunt capacitor to match the input impedance to approximate 50 **Ω**. The impedance transformation is as shown in Figure 3.39. The method of using series and shunt lump components can make the conjugate matching more precisely than using transmission line matching. Also, the large EM simulation is simulated for more practically.

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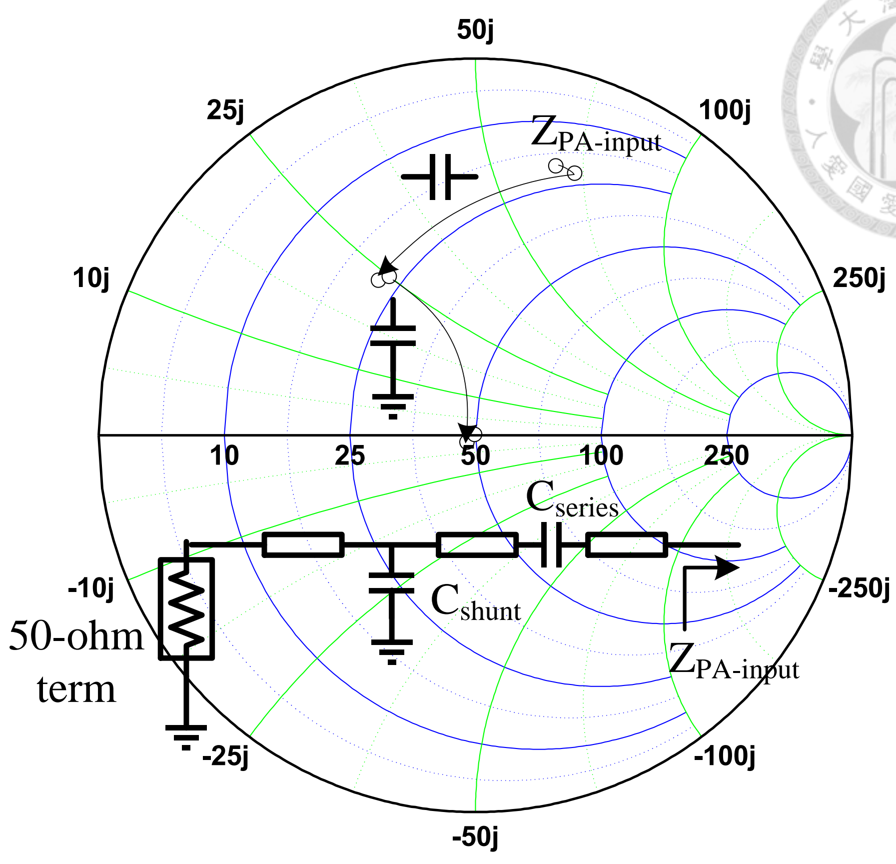

Figure 3.39 The impedance transformation of the input matching network where Z_S=50-Ω term and Z_L=19.8+63.4j Ω

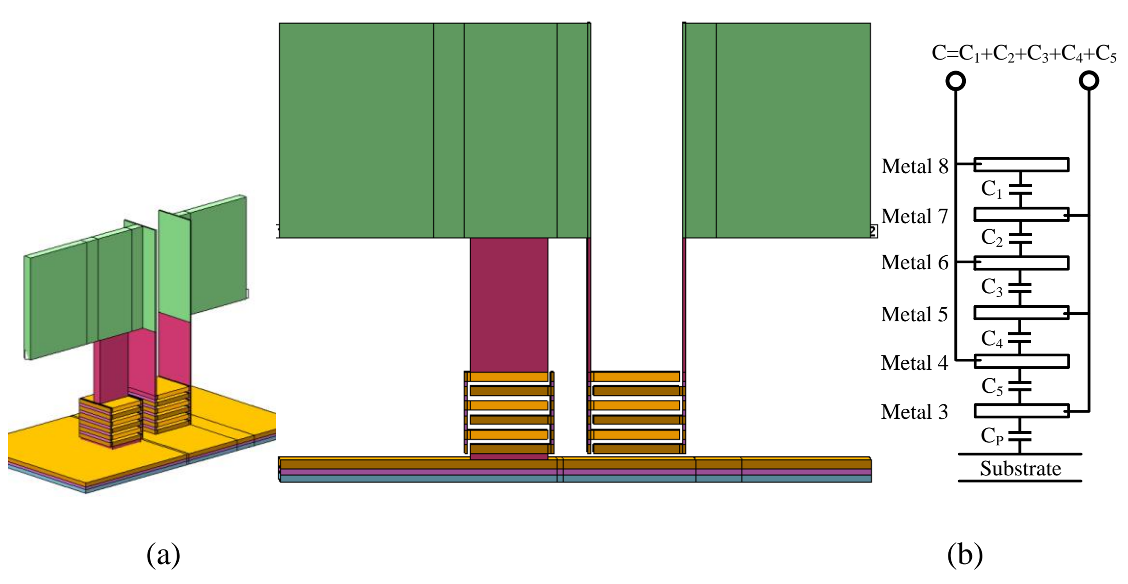

Figure 3.40 (a) Side view (b) front view of the parallel-plate capacitors

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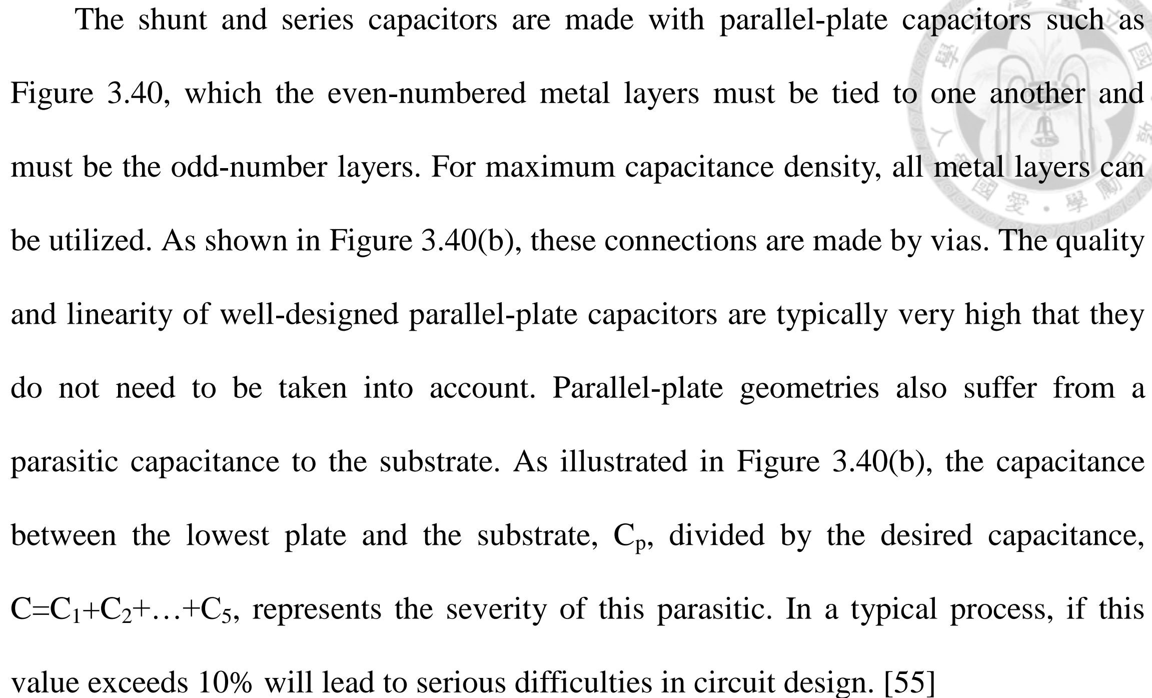

The shunt and series capacitors are made with parallel-plate capacitors such as Figure 3.40, which the even-numbered metal layers must be tied to one another and must be the odd-number layers. For maximum capacitance density, all metal layers can be utilized. As shown in Figure 3.40(b), these connections are made by vias. The quality and linearity of well-designed parallel-plate capacitors are typically very high that they do not need to be taken into account. Parallel-plate geometries also suffer from a parasitic capacitance to the substrate. As illustrated in Figure 3.40(b), the capacitance between the lowest plate and the substrate, C_p, divided by the desired capacitance, $C=C_1+C_2+\ldots+C_5$, represents the severity of this parasitic. In a typical process, if this value exceeds 10% will lead to serious difficulties in circuit design. [55]

3.2 Post-Layout Simulation

All passive components and structures are simulated by full-wave EM simulator (Sonnet) to obtain the post-simulation result. The amplifier with passive element is completely simulated by Agilent Advanced Design System (ADS).

The simulated S-parameter of 3.5-GHz LDMOS power amplifier is shown in Figure 3.41. The peak gain S_{21} is 16.7 dB at 3.36 GHz, the 3-dB bandwidth is from 3.06 to 3.73 GHz and S_{11} is below -10 dB from 3.28 GHz to 3.53 GHz. The small-signal gain is 16.1 dB at 3.5 GHz. The simulated stability factor (K) is 2.26 at 3.5 GHz which is the valley as shown in Figure 3.42. The factor K is high than 1, which means the amplifier is unconditionally stable. Figure 3.43 shows the simulated results of large-signal performance, the power gain is about 16.1 dB and the saturated output power is 26.7 dBm, respectively.

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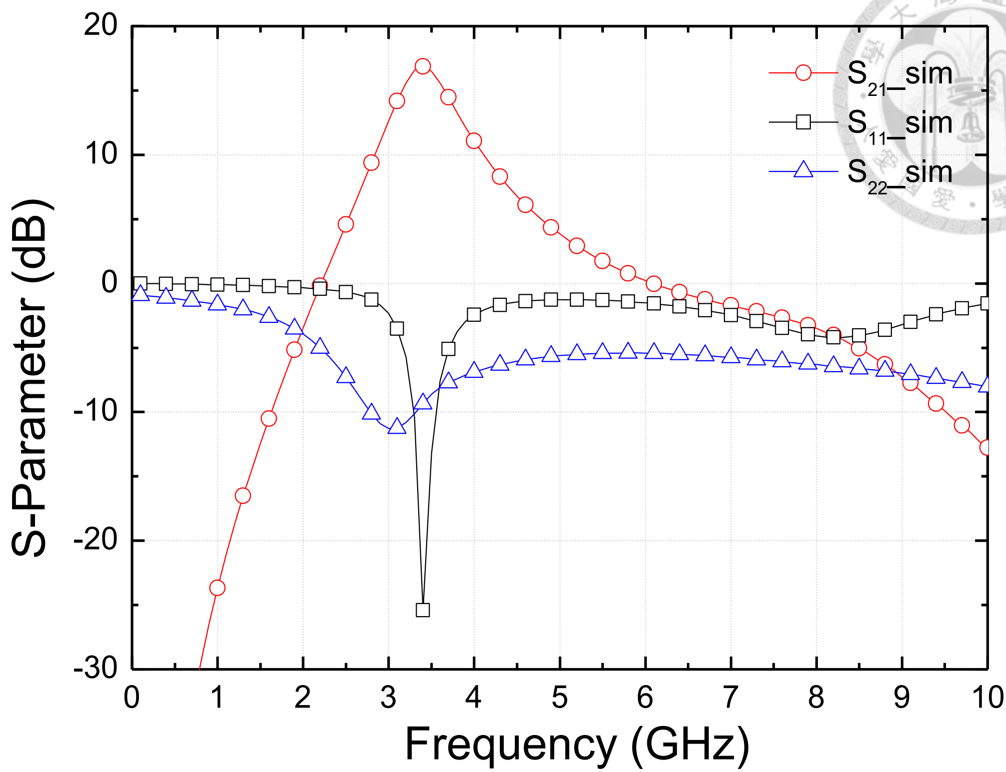

Figure 3.41 The simulated S-parameter of 3.5-GHz PA

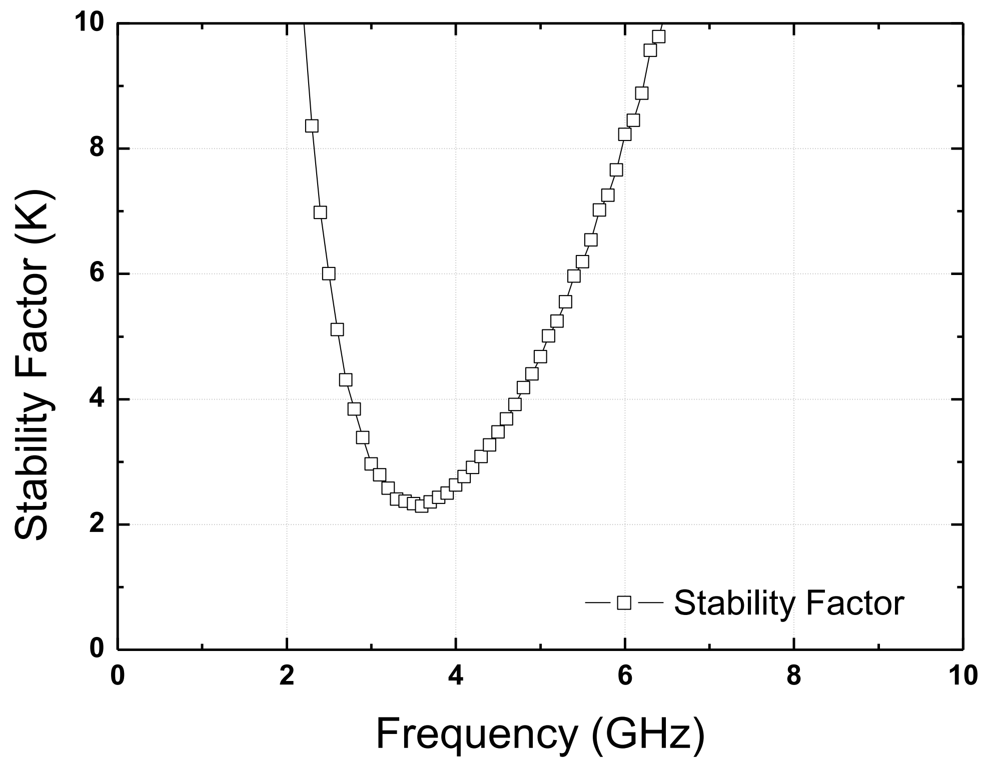

Figure 3.42 The simulated stability factor (K) of 3.5-GHz single stage PA.

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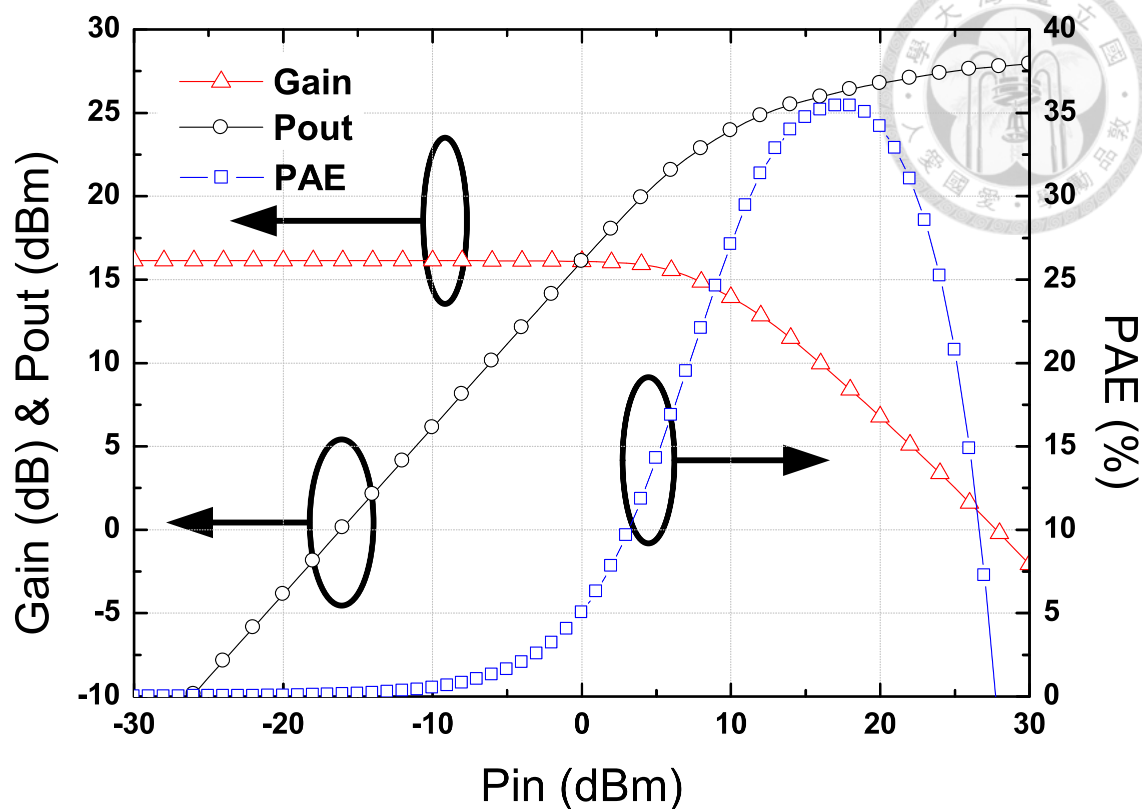

Figure 3.43 The large-signal simulation of 3.5-GHz single stage PA

3.3 Experiment Results and Discussions

3.3.1 Experiment Results

The miniature high power area density 3.5 GHz power amplifier has been designed and fabricated in 40-nm CMOS process. Figure 3.44 shows the chip micrograph of the proposed power amplifier with area 0.259 mm^2 excluding all testing pads. The circuit is measured via on-wafer probing. The simulated and measured results of S-parameter are shown in Figure 3.45, and closely look at the in-band small-signal performances are shown in Figure 3.47 and Figure 3.48. The measured power gain $|S_{21}|$ is 15.4 dB at 3.5 GHz. In Figure 3.46, the measured OP_{1dB} is 24.1 dBm at 3.5 GHz, P_{SAT} is 26.5 dBm and the corresponding peak PAE is 25 % at 3.5 GHz. Table 3-5 summarized the performance of recent fully-integrated power amplifiers. The miniature 3.5 GHz power amplifier

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reaches the highest P_{SAT} power area density of 1724 mW/mm^2, and OP_{1dB} power area density of 992.4 mW/mm^2 compared to other power amplifier designs with competitive performance.

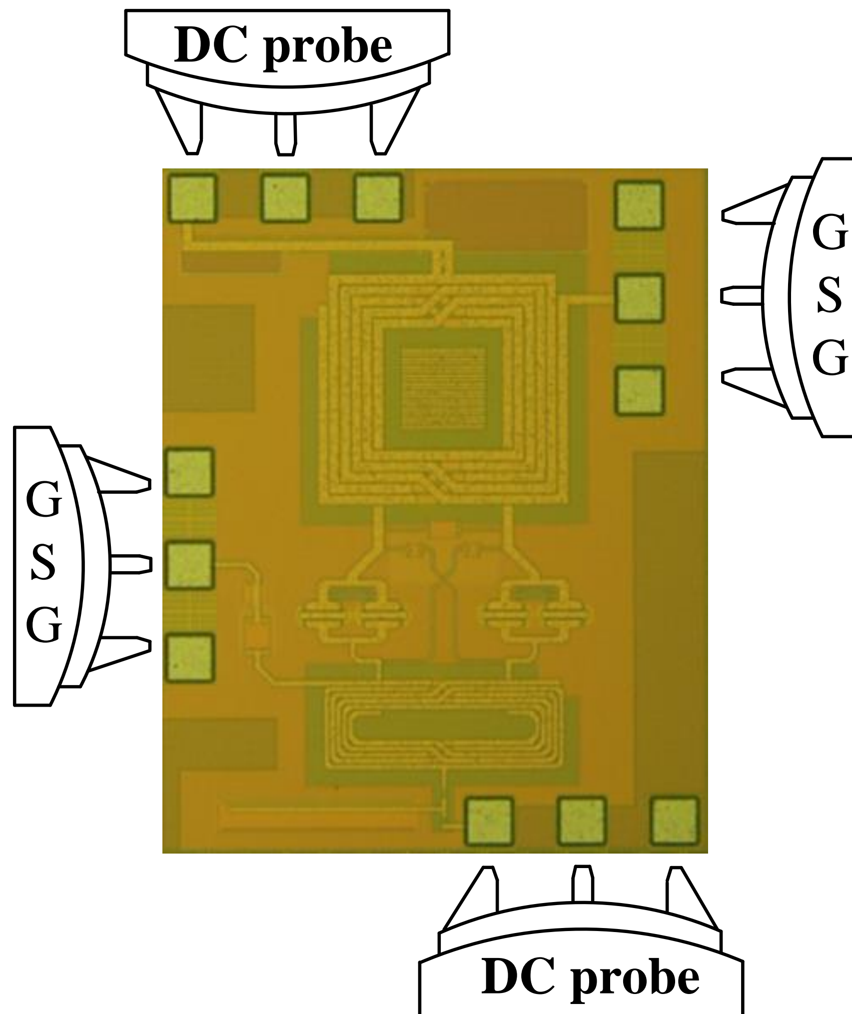

Figure 3.44 Chip micrograph of 3.5 GHz PA with area 0.259 mm^2 (excluding pads)

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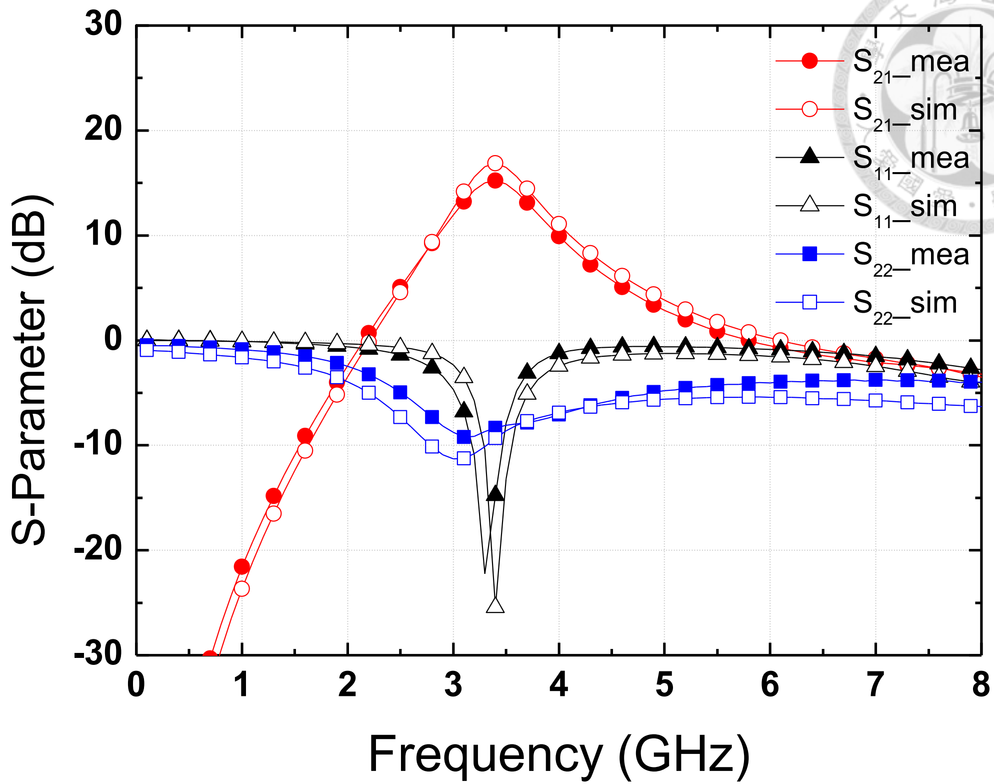

Figure 3.45 The simulated and measured small-signal performances of 3.5-GHz PA

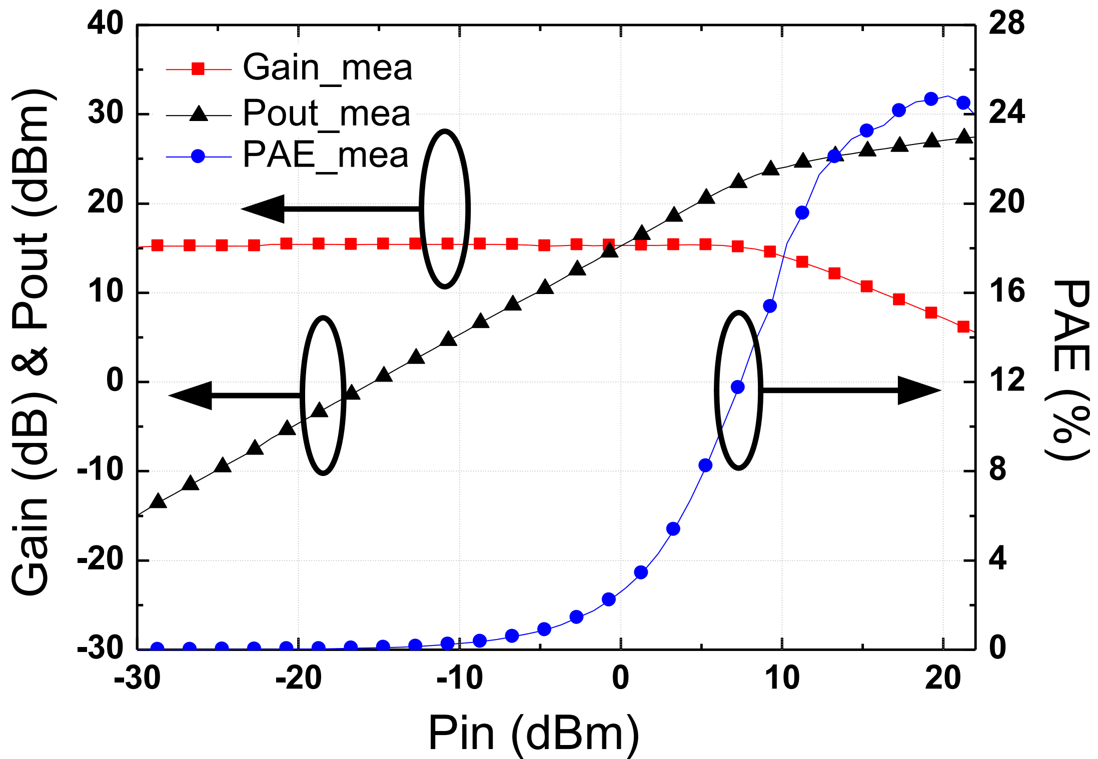

Figure 3.46 Measured large-signal performance at 3.5 GHz

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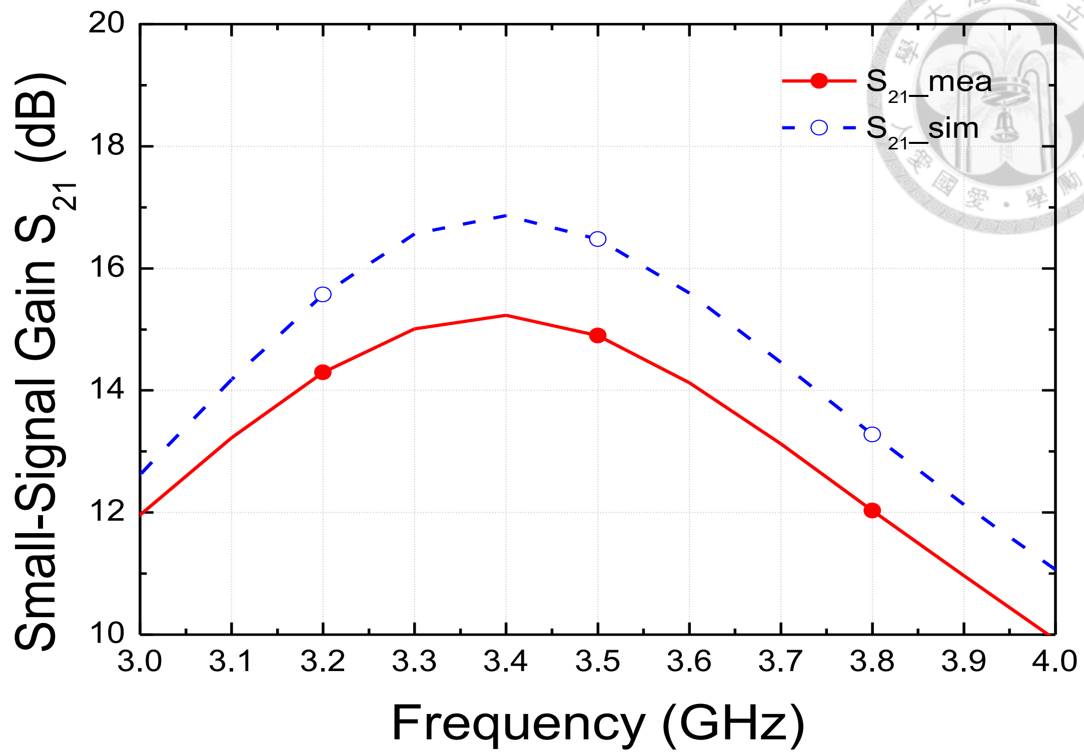

Figure 3.47 The simulated and measured small-signal gain at 3-4 GHz

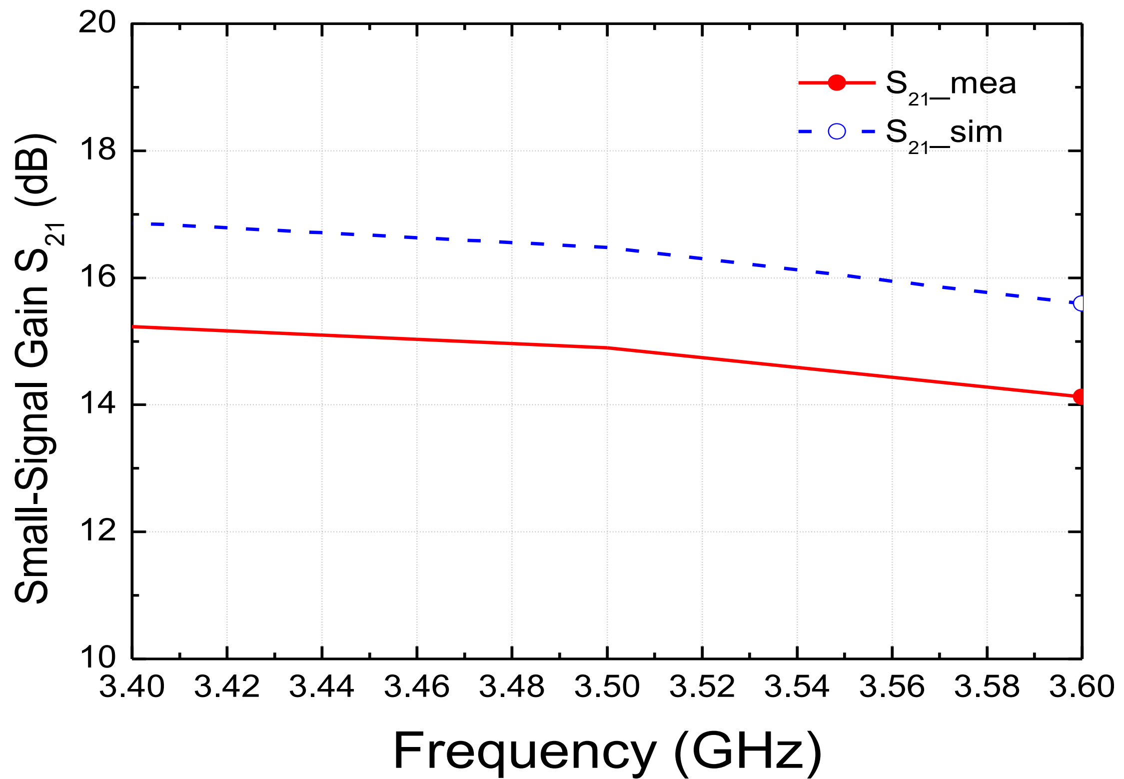

Figure 3.48 The simulated and measured small-signal gain at 3.4-3.6GHz

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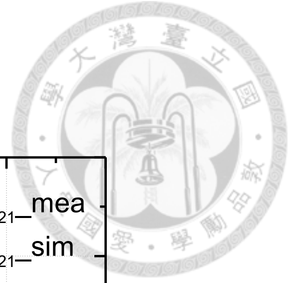
3.3.2 Re-simulations According to the Measured Results



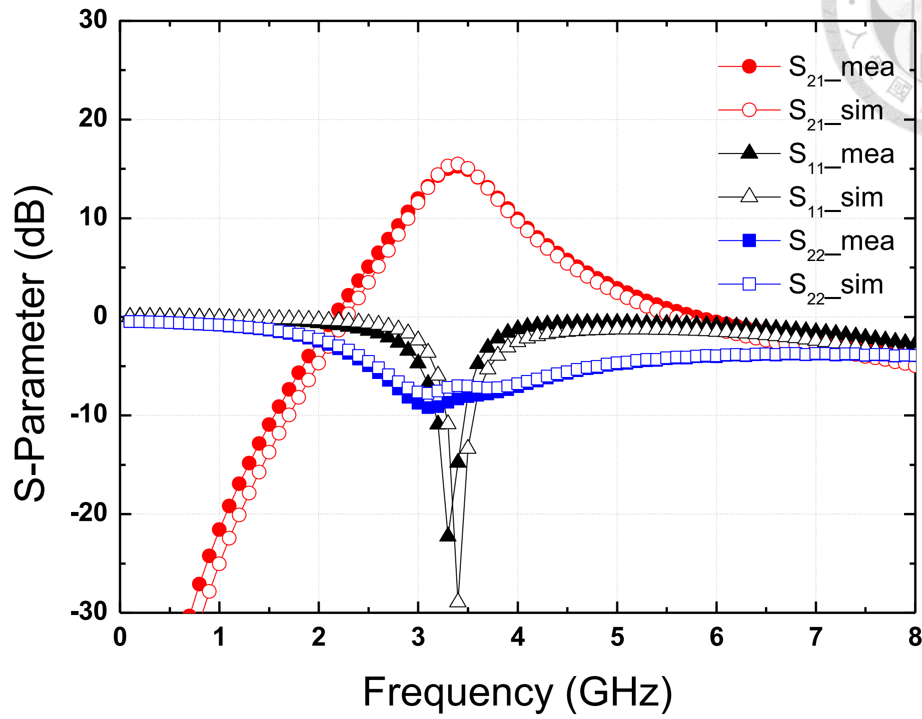


Figure 3.49 The re-simulation of small signal for 3.5-GHz PA

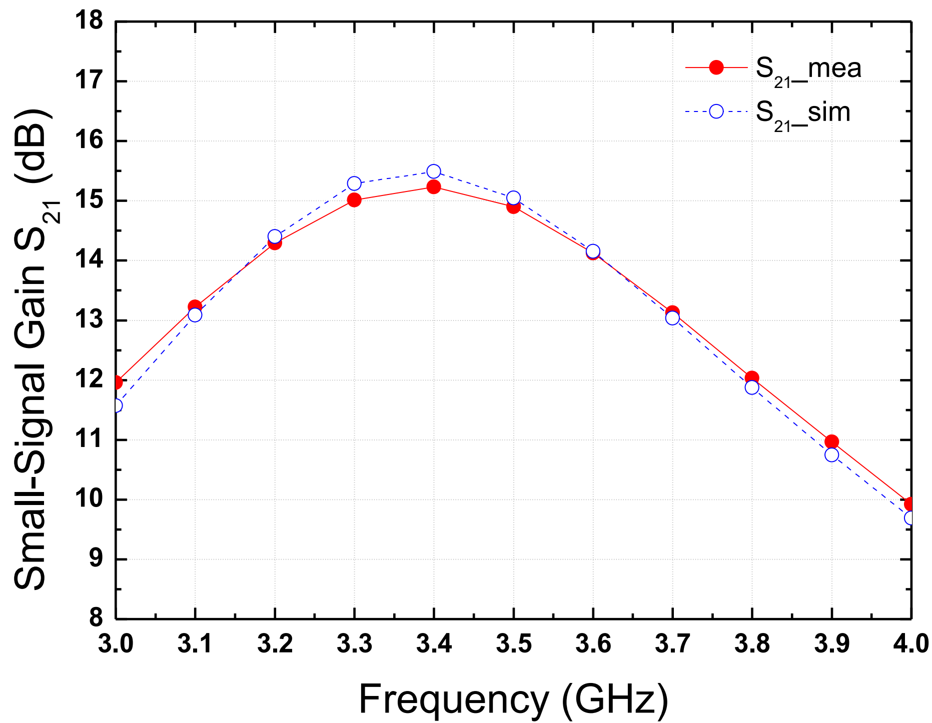


Figure 3.50 The re-simulation of small-signal gain at 3-4 GHz

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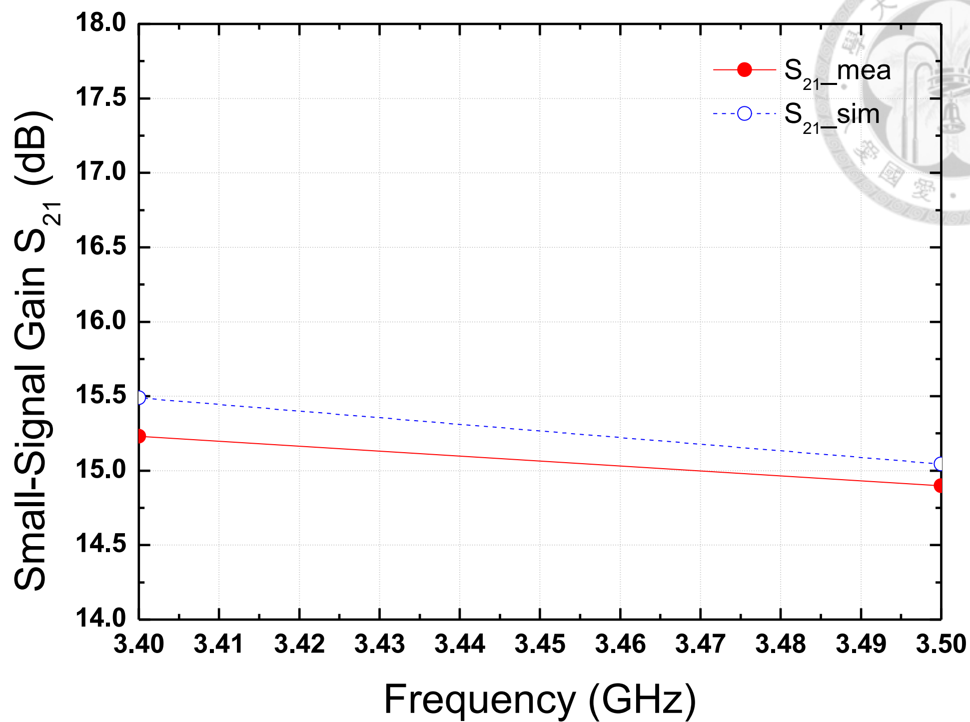

Figure 3.51 The re-simulation of small-signal gain at 3.4-3.6 GHz

The re-simulation of small signal performance which includes the thermal issues performs the perfectly match with the measured results as shown in Figure 3.49. The original simulated gain is 16.1 dB at 3.5 GHz which is under 25℃ as room temperature condition. However, the measured gain is 15.4 dB at 3.5 GHz which drops 0.7 dB from the original simulated result. The re-simulated gain is 15.5 dB at 3.5 GHz which is high temperature at the junction temperature. The gain percentage error turns to be less than 0.6%, and effectively proof the thermal issues should be taken into design simulation for the practical results that are close to the measurement. The in-band results for 4G/LTE applications are shown in Figure 3.50, and Figure 3.51.

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Table 3-5 Comparison Table with Relevant State-of-the-Art PAs

Ref.	[4] 2011 JSSC	[23] 2009 APMC	[24] 2010 TMTT	[25] 2015 ISSCC	[26] 2009 JSSC	[27] 2012 JSSC	**This work**
Process	0.18 um CMOS	0.13 um CMOS	90 nm CMOS	65 nm CMOS	90nm CMOS	0.18 um CMOS	**40 nm LDMOS**
f_o (GHz)	2.5	2.5	2.5	2-6	2.3~2.7	2.4	**3.5**
Class/Stage	AB/2	AB/2	AB/1	AB/2	AB/2	AB/2	**A/1**
Vdd (V)	3.3	3.3	3.3	1.8/3.3	3.3	3.3/3.2	**5**
P_{sat} (dBm)	31	25.5	32	22.4	30.1	34	**26.5**
PAE(%)	34.8	32	48	28.4	33	34.9	**25**
OP_{1dB} (dBm)	28	21.4	29.5	20.7	27.7	31.5	**24.1**
Gain (dB) per stage	15.65	15.5	18	11.8 ±0.4	14	11	**15.4**
$Area_{core}$*/ $Area_{power\ stage}$** (mm^2)	1.57/ 1.09	2.52/ 1.92	1.95/ 1.95	0.75/ 0.7	3.57/ 2.59	3.045/ 1.825	**0.259/ 0.259**
$P_{sat}PAD_{core}$# /$PAD_{power\ stage}$## (mW/ mm^2)	801/ 1154.7	140.8/ 185	812.8/ 812.8	231/ 248.2	286.6/ 395	824.9/ 1376	**1724/ 1724**
OP_{1dB} $PAD_{core}$$/$PAD_{power\ stage}$$$ (mW/ mm^2)	401.9/ 578.9	54.8/ 72	457.1 / 457.1	86.08/ 167.8	164.9/ 227.4	463.9/ 774	**992.4/ 992.4**

*chip area without pad ** power stage area from chip photo #$P_{sat}/Area_{core}$

##$P_{sat}/Area_{power\ stage}$ $ $OP_{1dB}/Area_{core}$ $$ $OP_{1dB}/Area_{power\ stage}$

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Chapter 4 A 3.5-GHz Fully-Integrated High Power Transformer Combined LDMOS Power Amplifier with 3D Architecture

4.1 Circuit Design

4.1.1 Device and Bias Selection

The device and bias selection are similarly selected as in Chapter 3. The one-way fully-integrated transformer-combined power amplifier which illustrates in Chapter 3 is fabricated as the test kit for each of power cells in this watt-level four-way fully-integrated transformer combined power amplifier design. Recall that the device size of LDMOS is chosen in two 10-μm width and 32 fingers in parallel, and the bias voltage is 1.2 V that is operated in Class-AB.

4.1.2 Power Budget and Power Cells

According to the measured results of 1-way power amplifier, the power budget is shown in Figure 4.1 to achieve in the target of 29 dBm output power. In order to achieve on the maximum output power performance, the direction of the power amplifier should be designed from the output side to the input side. Due to the loss from the power stage is 1 dB; the 4-way combination will be 29 dBm minus 6 dB then remain 24 dBm of output power for each power cell. Since each of the power cell gain is 15 dB, the input power of each power cell in power stage is 8 dBm. At the splitting point of the power stage is 9 dBm plus 6 dB and turns to be 15 dBm. The loss from inter-stage matching is approximate 1 dB as well. The output power of the driver stage is 16 dBm and the gain is 15 dB, which can indicate the input power should be 1 dBm.

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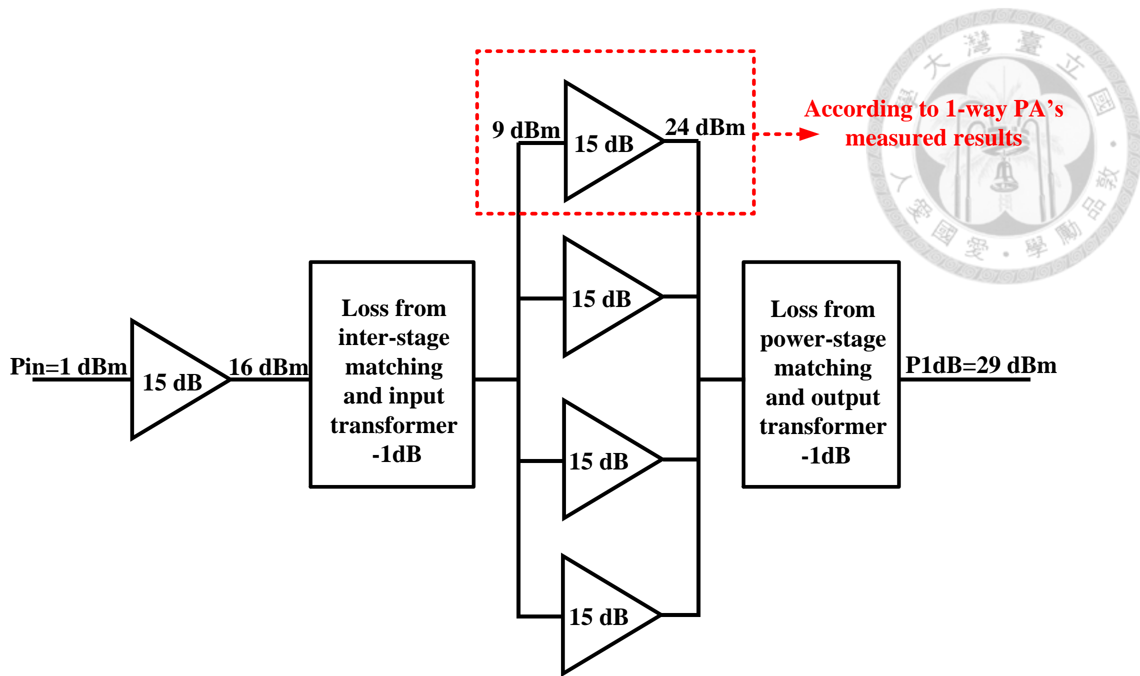

Figure 4.1 The power budget of 4-way combined power amplifier

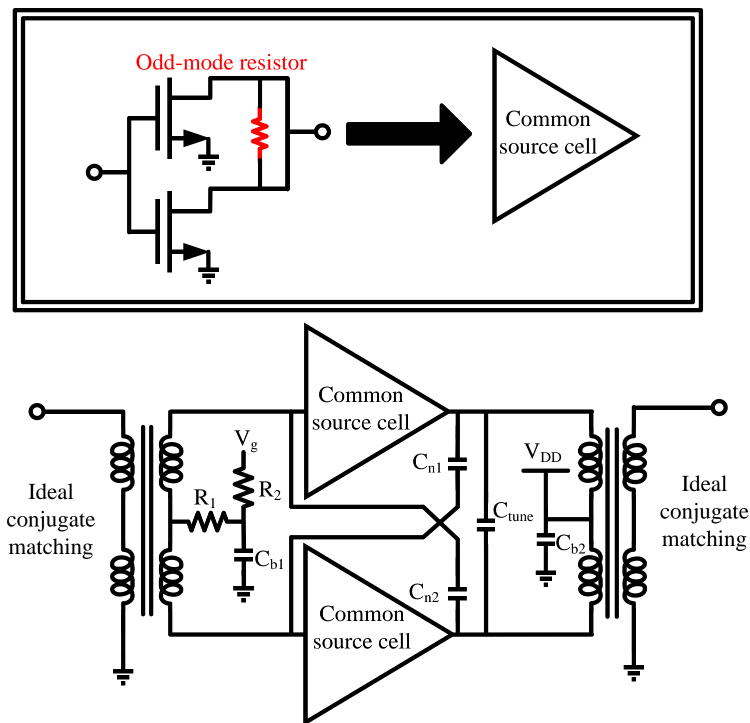

Figure 4.2 Schematic of a power cell

From the load-pull simulation, the optimal load impedance of two common-source transistors is read as 40.2+24.5j. Two power cells are combined by input and output transformers and are regarded as push-pull (differential) topology. The schematic is

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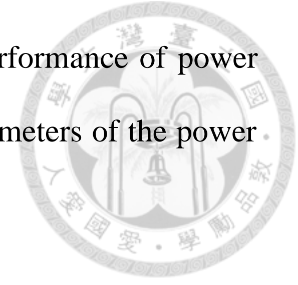

shown in Figure 4.2 and the 3D structure is in Figure 4.3. The performance of power cell can be estimated by input conjugate matching. The design parameters of the power cell are listed in Table 4-1.

Table 4-1 Design Parameters of Power Cell

Transistor Size		10 μm × 32	
Parameter	**Value**	**Parameter**	**Value**
L_{p_out}	1.023 nH	C_{b1}	8 pF
L_{s_out}	2.704 nH	C_{b2}	20 pF
L_{p_in}	2.087 nH	C_{tune}	720 fF
L_{s_in}	2.142 nH	C_{n1}, C_{n2}	185 fF
R_1	14 ohm	R_2	3 kΩ
Bias voltage			
V_{DD}	5V	V_g	1.2V

Table 4-2 The Parameters of Input / Output and Inter-Stage Matching Network

Parameter	**Value**	**Parameter**	**Value**
C_{input1}	0.9 pF	L_{output}	0.85 nH
C_{input2}	1 pF	C_{output}	1.44 pF
L_{inter_stage}	1.1 nH	C_{inter_stage}	2.5 pF

The design of the gain stage amplifier is similar with power stage design, but the difference is the total device size ratio should be taken into the design consideration. The total device size ratio between gain stage and power stage is decided by gain and power performance of power stage. For this power amplifier case, the size ratio is 1:4.

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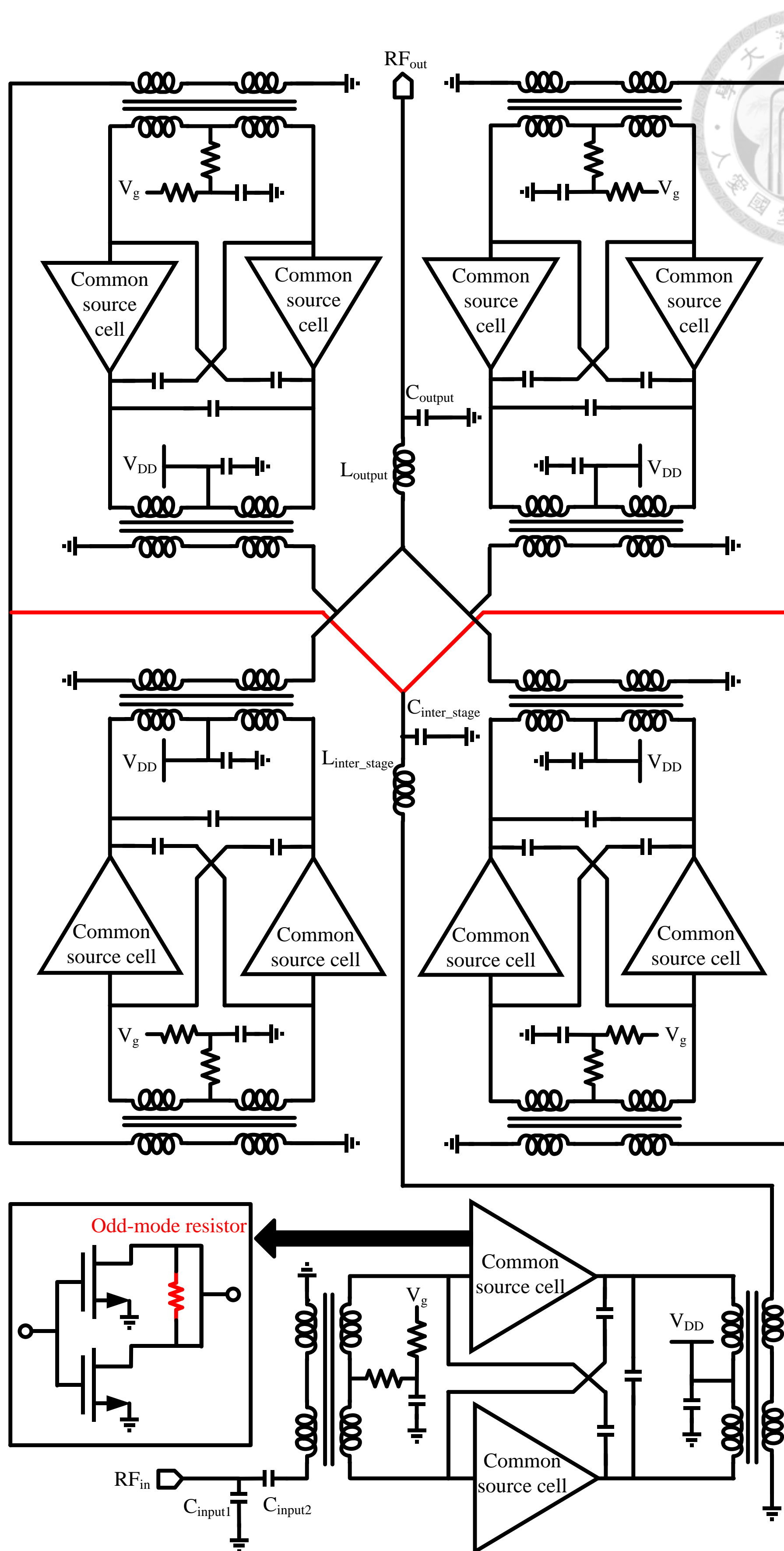

Figure 4.3 Complete schematic of two stage 3.5GHz power amplifier

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4.1.3 Radial Power Splitter and Combiner

In order to reach the watt-level output power, the more power cells are combined. Since a power cell can only deliver about 26 dBm of saturated output power, Figure 4.4 shows the schematic of four-way current combination. The saturated output power can increase from 26 dBm to 32 dB ideally, but the passive loss will degrade the performance. The optimal load impedance of the four-way combination is the one-way divided by four.

For instance, the load impedance of 1-way power amplifier is 40.2+24.5j Ω and the load impedance of 4 way combined power amplifier becomes the impedance of 1-way power amplifier by a factor of 4 which is 10.05+6.125j Ω as shown in Figure 4.5. The output matching network will transform this load impedance of 4-way combined power amplifier into the 50- Ω term, and it will be illustrated in later section of I/O matching network of this Chapter.

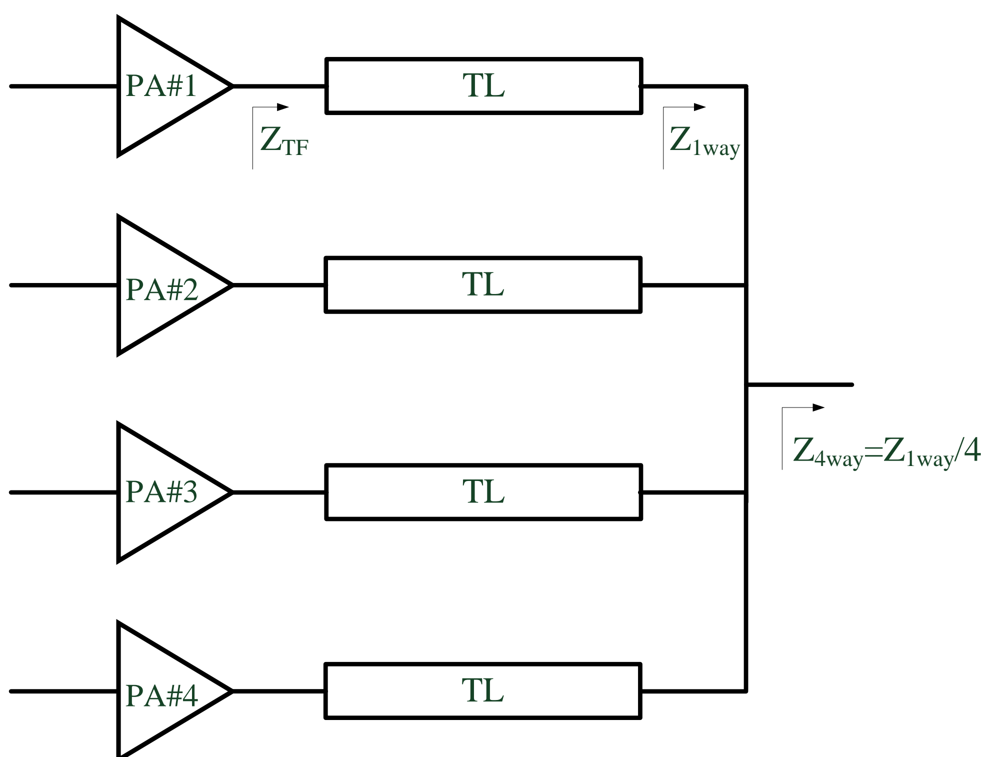

Figure 4.4 Schematic of 4-way current combine.

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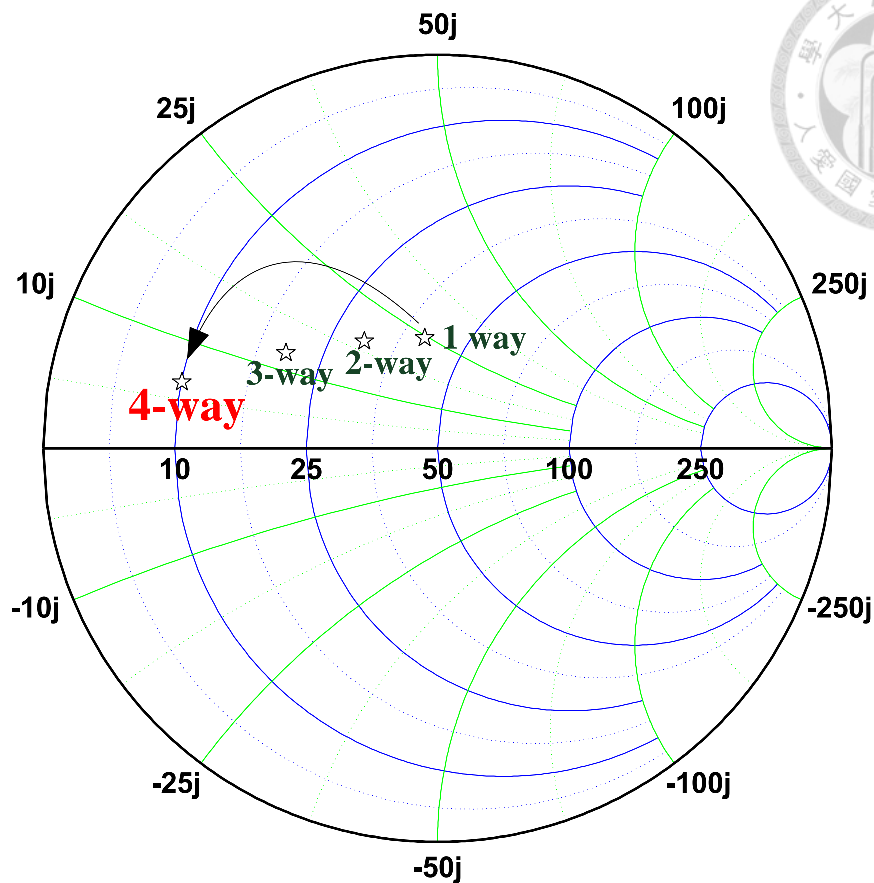

Figure 4.5 The impedance transformation from 1-way PA to 4-way combined PA

From the simulation result, 50-Ω line width is 12 μm, 54-Ω line width is 10 μm, 59-Ω line width is 8 μm, 63-Ω line width is 6 μm, 73-Ω line width is 4 μm and 84-Ω line width is 2 μm. Under the same metal length, parasitic resistance of 50-Ω line is the less than other sampling of 54-Ω line and 68-Ω line. Since 12 μm is the maximum width for 40-nm process, the characteristic impedance with various metal widths in 40-nm CMOS is shown in Figure 4.6. Due to the output power consideration, the metal width of the output combiner should use 12 μm. However, input part of the metal width is not necessary to concern about the power transformation, and the metal width can use 6 μm.

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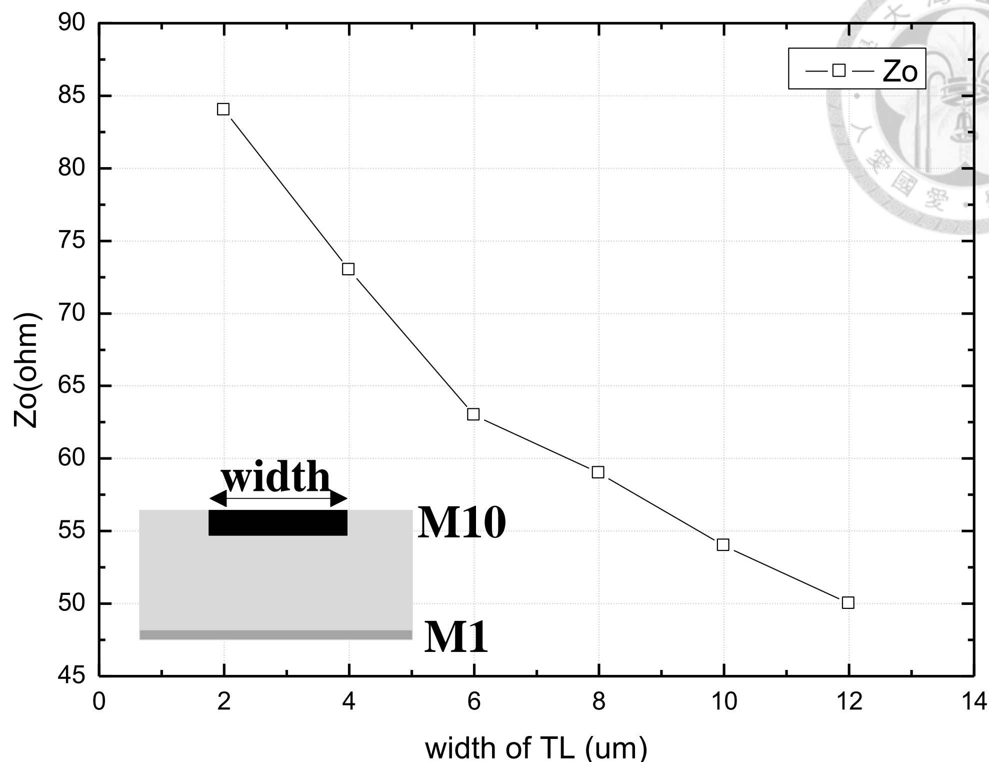

Figure 4.6 The characteristic impedance of TFML (thin-film microstrip line) with various metal widths in 40-nm CMOS.

The output combiner of the 4-way power amplifier combination is shown in Figure 4.7, while the input splitter of the 4 power cells is shown in Figure 4.8. The cross-section of the input splitter and the output combiner is shown in Figure 4.9.

The differences from the previous works, the output combiner and input splitter are alternated since the output loss is highly considered but the input part does not care that much. Figure 4.7 shows the output combiner uses the maximum width and shorter path for its transmission line design, and Figure 4.8 shows the input splitter does not care about the loss that much and uses 6-μm width and longer path for its transmission line design. In Figure 4.9, it will have some intrinsic capacitances at the cross section of input path and output path. As a result, the cross-sectional part of this larger EM should be taken into account. The 3-D structure of four power cells with input splitter and output combiner are shown in Figure 4.10.

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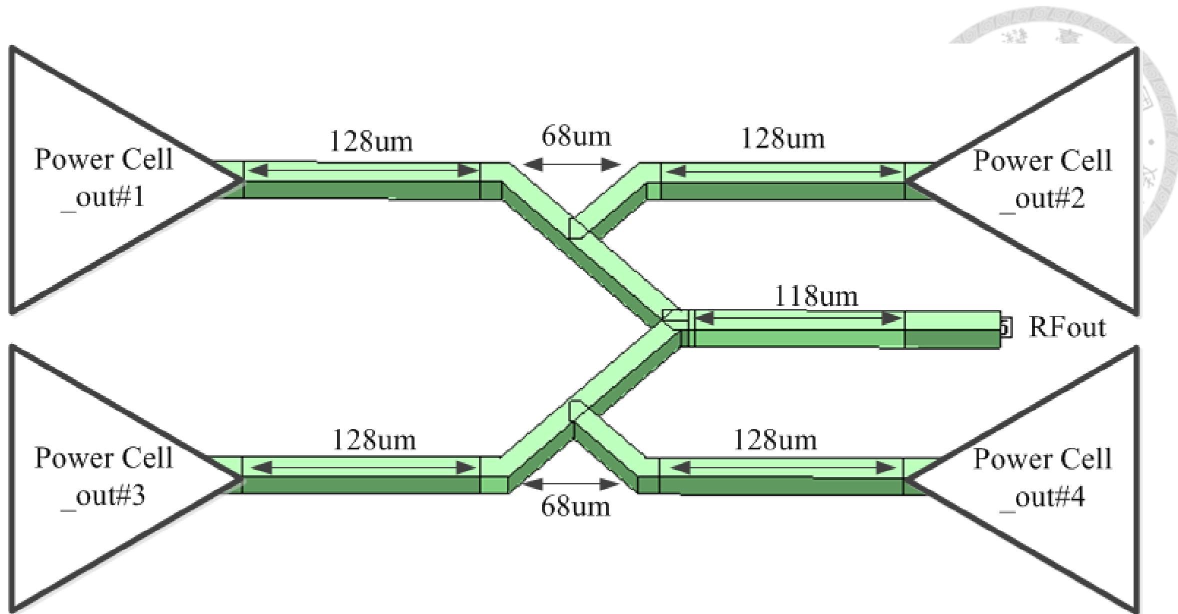

Figure 4.7 The output combiner of the 4-way power amplifier combination

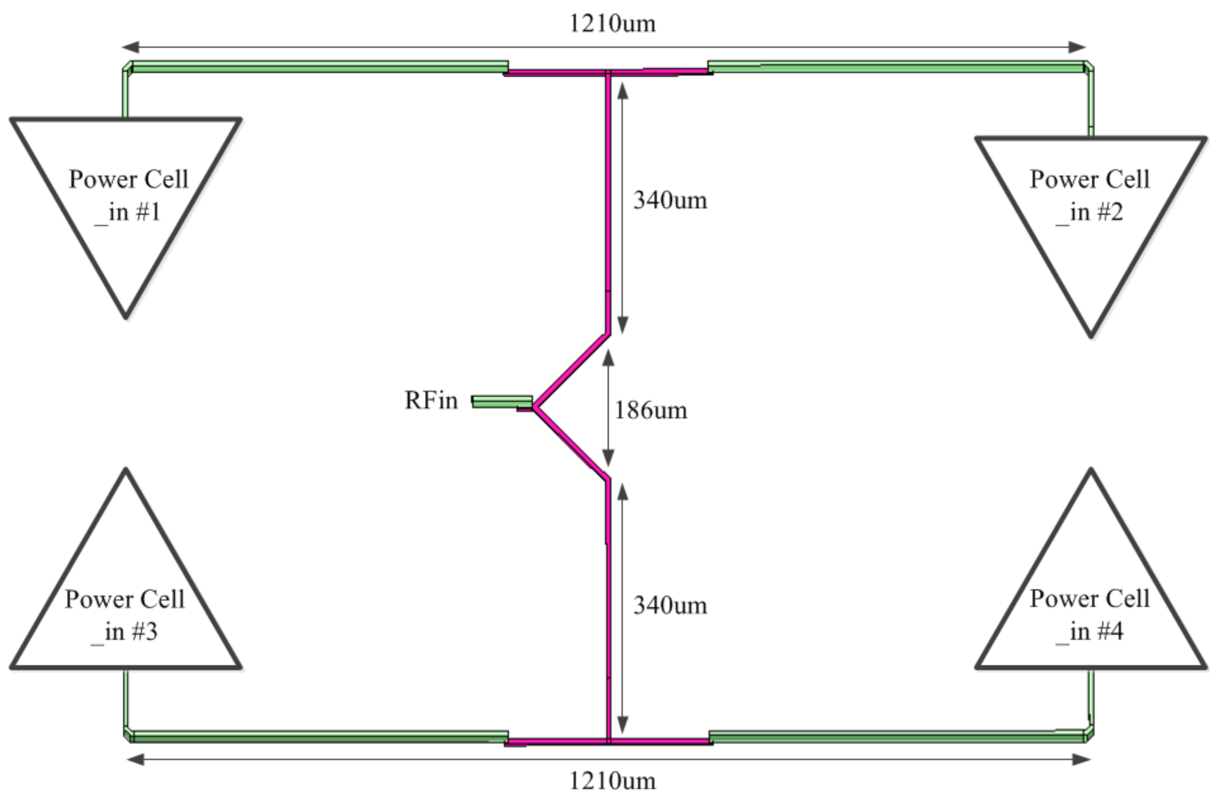

Figure 4.8 The input splitter of the 4 power cells

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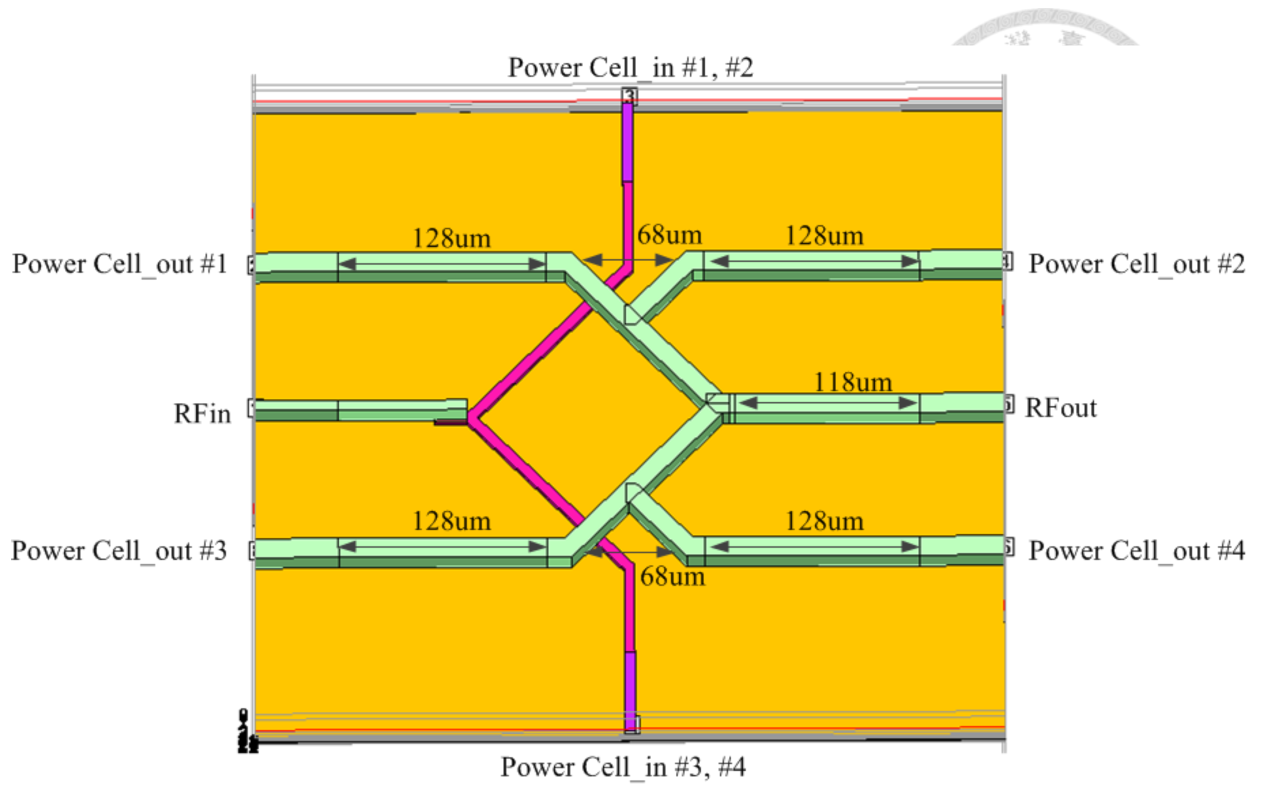

Figure 4.9 The cross section of input splitter and the output combiner

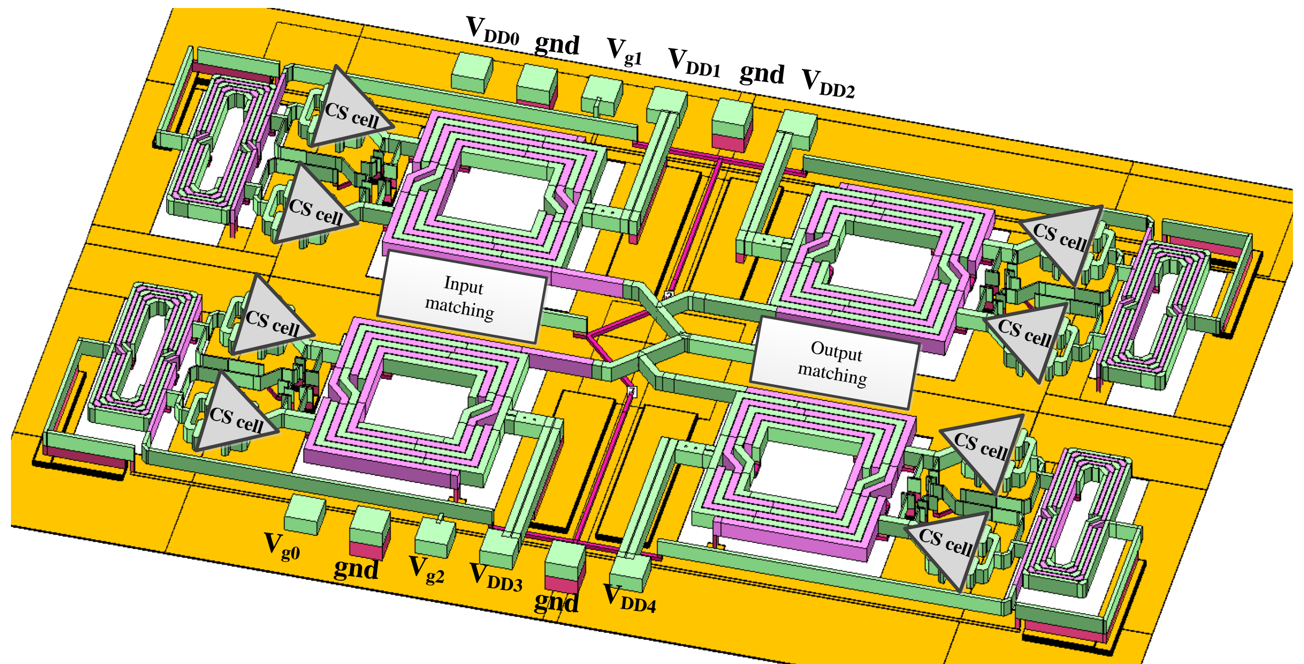

Figure 4.10 3D structure of four power cells with input splitter and output combiner

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4.1.4 I/O Matching Network and Inter-Stage Matching Network

The last thing of the 3.5-GHz two-stage power amplifier design is the input/output matching network and the inter-stage matching network. The output matching network is composed by a series inductor and a shunt capacitor as shown in Figure 4.11. From the source impedance of the 4-way combined power amplifier, the impedance is transformed from 16.46+0.33j Ω to the 50-Ω load. The output matching network uses a 0.85-nF inductor in series and a 1.44-pF shunt capacitor to match the output impedance to the load where is approximate to 50 Ω.

The inter-stage matching network is also composed by a series inductor and a shunt capacitor as shown in Figure 4.12. Between the gain stage and the power stage of the power amplifier design, the impedance is transformed from 30.8+2.9j Ω to 6.85+21j Ω load. The inter-stage matching network uses a 1.72-nF inductor in series and a 2.68-pF shunt capacitor to complete the impedance transformation.

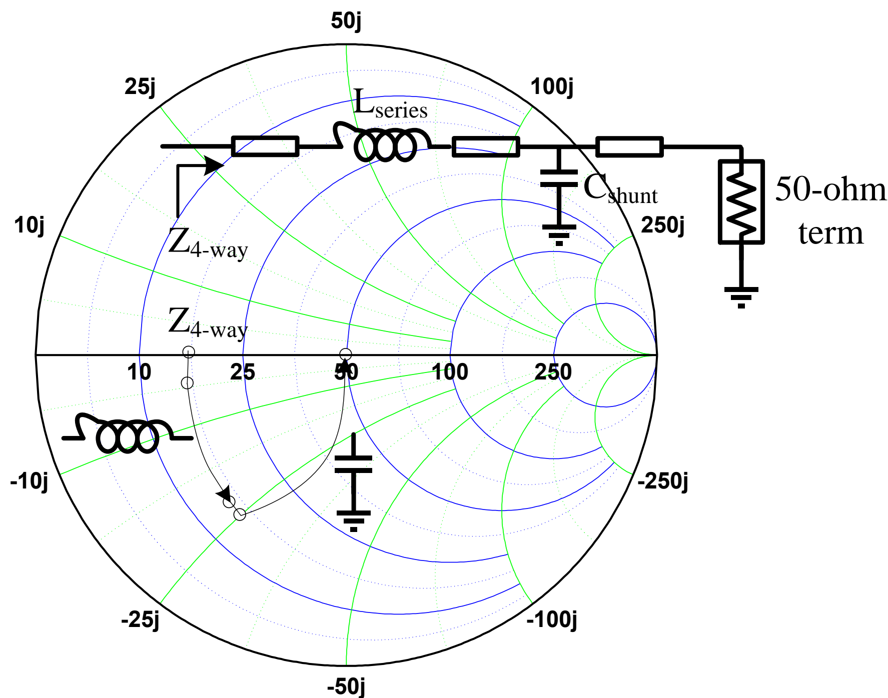

Figure 4.11 The impedance transformation of the output matching network where $Z_{4\text{-way}}$=16.46+0.33j Ω and 50-Ω term

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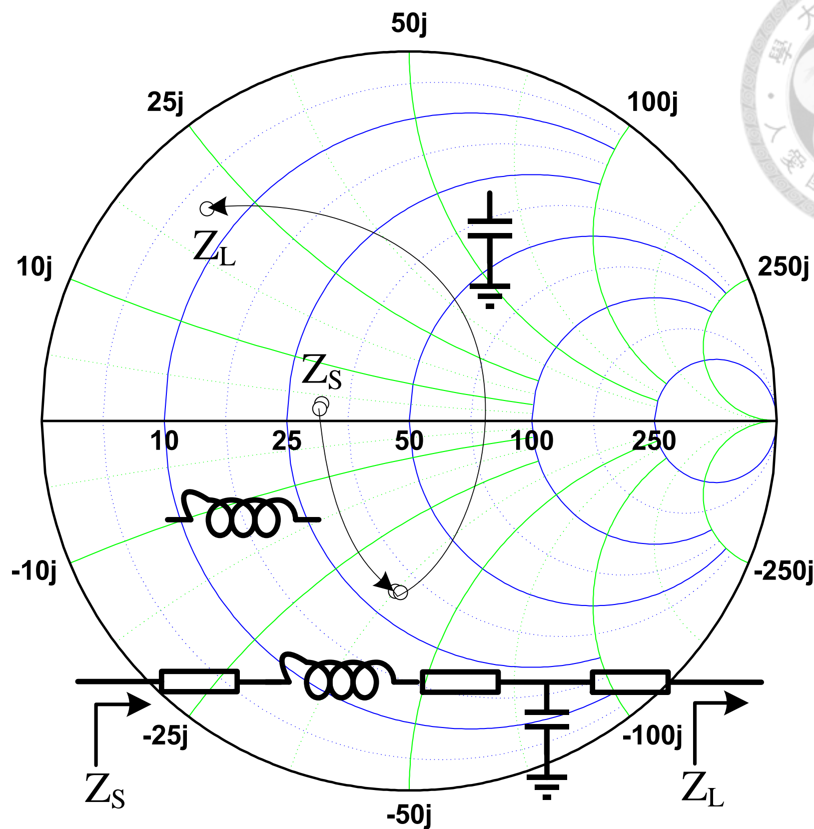

Figure 4.12 The impedance transformation of the inter-stage matching network where Z_S=30.8+2.9j Ω and Z_L=6.85+21 Ω

4.2 Post-Layout Simulation

4.2.1 Small-Signal and Large-Signal Simulation

The simulated results of small-signal simulation from ADS simulation show the small-signal gain and input/output return loss in Figure 4.13. The simulated small-signal gain has peak gain 29.94 dB at 3.3 GHz, 29.355 dB at 3.5 GHz, and the 3-dB bandwidth is from 3.06 GHz to 3.73 GHz. When bias voltage is 1.2 V and the supply voltage is 5 V, the results of large-signal simulation at 3.5 GHz show in Figure 4.14 as the gain is 29.355 dB. The output power at the 1-dB compression point is 28 dBm and the saturated output power is 32.87 dBm at the peak PAE of 30.18 %.

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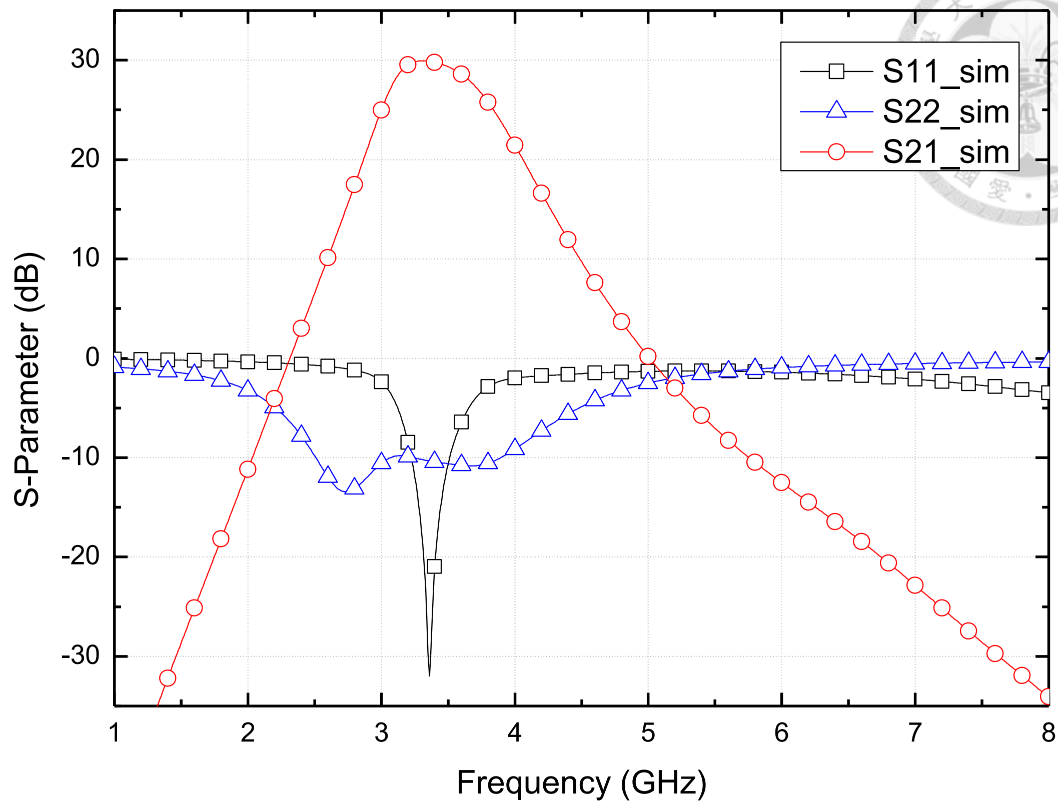

Figure 4.13 The simulation of small-signal performance

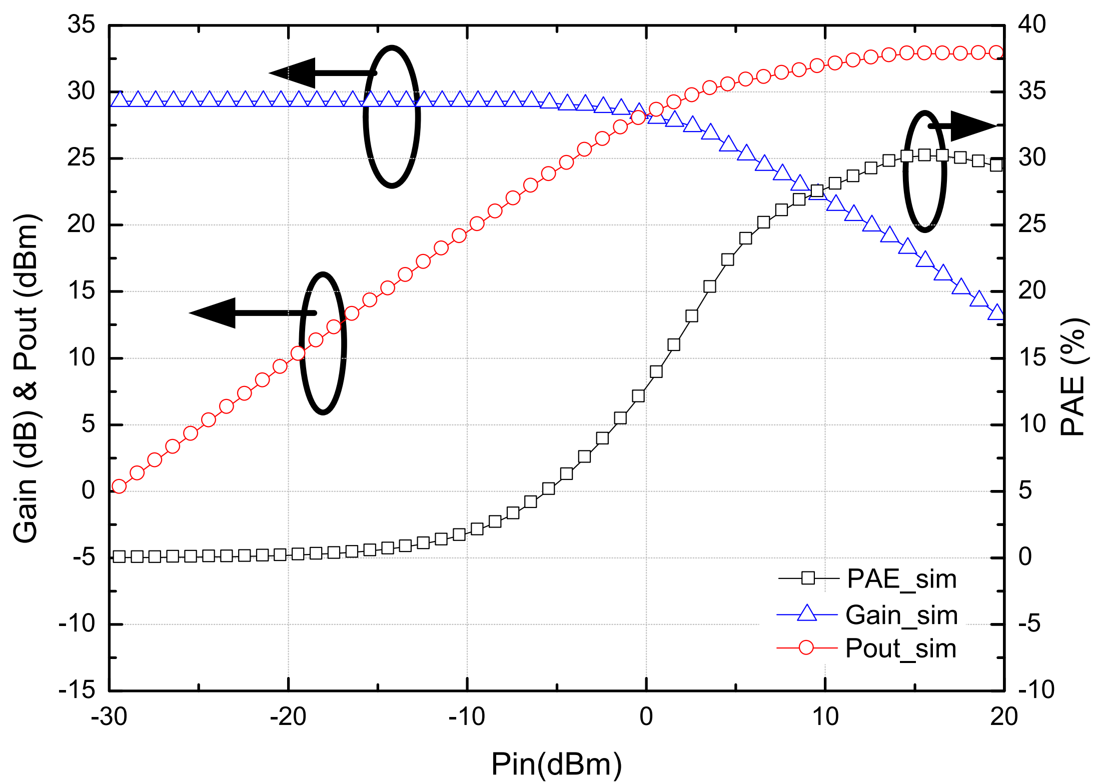

Figure 4.14 The large signal performance of 3.5 GHz 4-way combined PA

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4.2.2 Stability Check

Since the first priority of a successful power amplifier design is stability, the stability has to be checked carefully. There are multiple methods to check the stability of a power amplifier: the first is K-factor according to the S-parameter, the second is inter-stage stability check, and the third is S-probe from the ADS simulation.

Firstly, the K>1 means the power amplifier is in the stable region, for instance, the K-factor of this power amplifier is 31.12 at 3.5 GHz and the valley is 26.9 at 3.7 GHz as shown in Figure 4.15 that mean the circuit is unconditionally stable. Secondly, the inter-stage stability check is in Figure 4.16, which shows the frequency paths of the first stage and the second stage of the power amplifier are not inter-connected. Finally, the S-probe from the ADS simulation is used to check the stability of power amplifier. S-probe is shown in Figure 4.17 that has to be in the region of positive one and negative one to ensure this power amplifier in unconditionally stable.

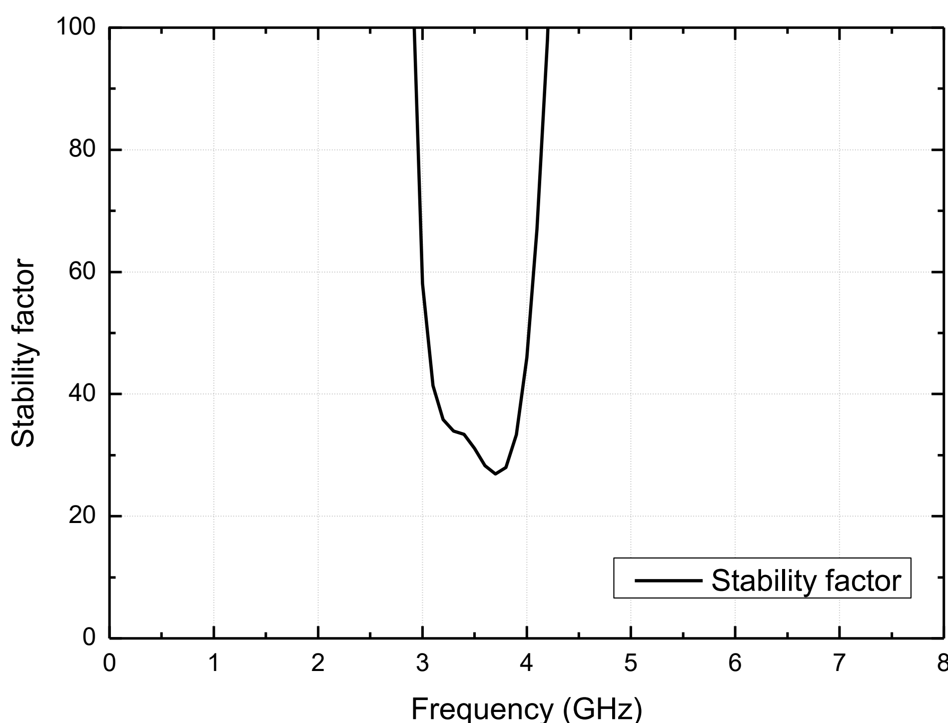

Figure 4.15 The simulated K-factor stability of 4-way PA

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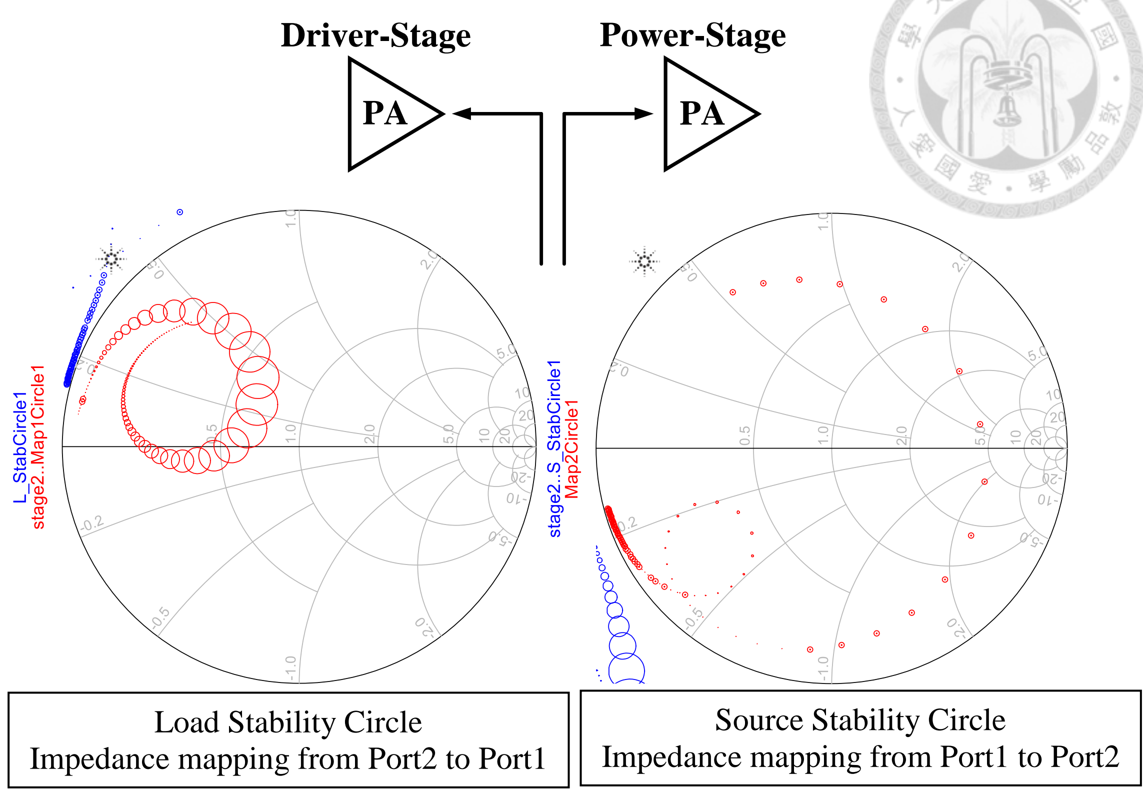

Figure 4.16 The inter-stage stability simulation of 4-way PA

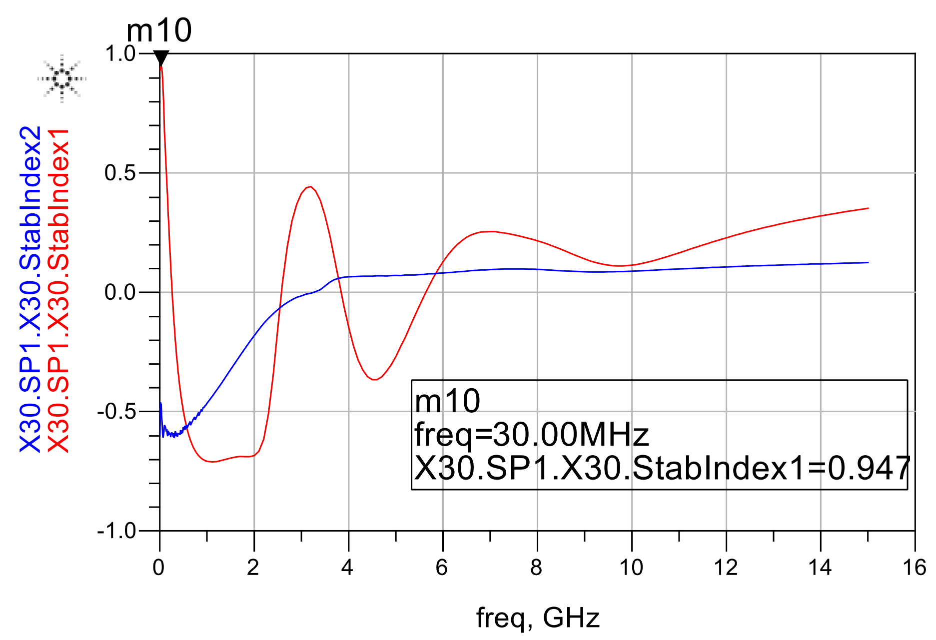

Figure 4.17 The stability simulation with S-probe for 4-way PA

For the high output power like a watt-level power amplifier design, the ground path and better bypass capacitors on the DC parts have to be considered. Recall the

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previous work of the 5.3-GHz Fully-Integrated High Power Transformer Combined CMOS Power Amplifier from Ian Tseng [59], the more complete grounding and ground pads surrounding around the chip would make good ground path for effectively reducing the thermal issues.

The initial design of this 4-way combined power amplifier is used the previous method and the layout is shown in Figure 4.18. However, since the closer bypass capacitors from the supply voltage to the circuit will reduce the uncertainty and have a better performance, the completely on-wafer design for the six DC-probes design is improved from Figure 4.18 to Figure 4.19. In Figure 4.19, the DC-probes are P-G-P, P-G-P, and the correlation of the bias voltages are shown in Table 4-3. In conclusion, on-probing design has better performance to reduce the DC uncertainty from PCB wire bonds, and the previous method of ground surrounding can be used in PCB design if the bias voltages are more than the exist DC-probes.

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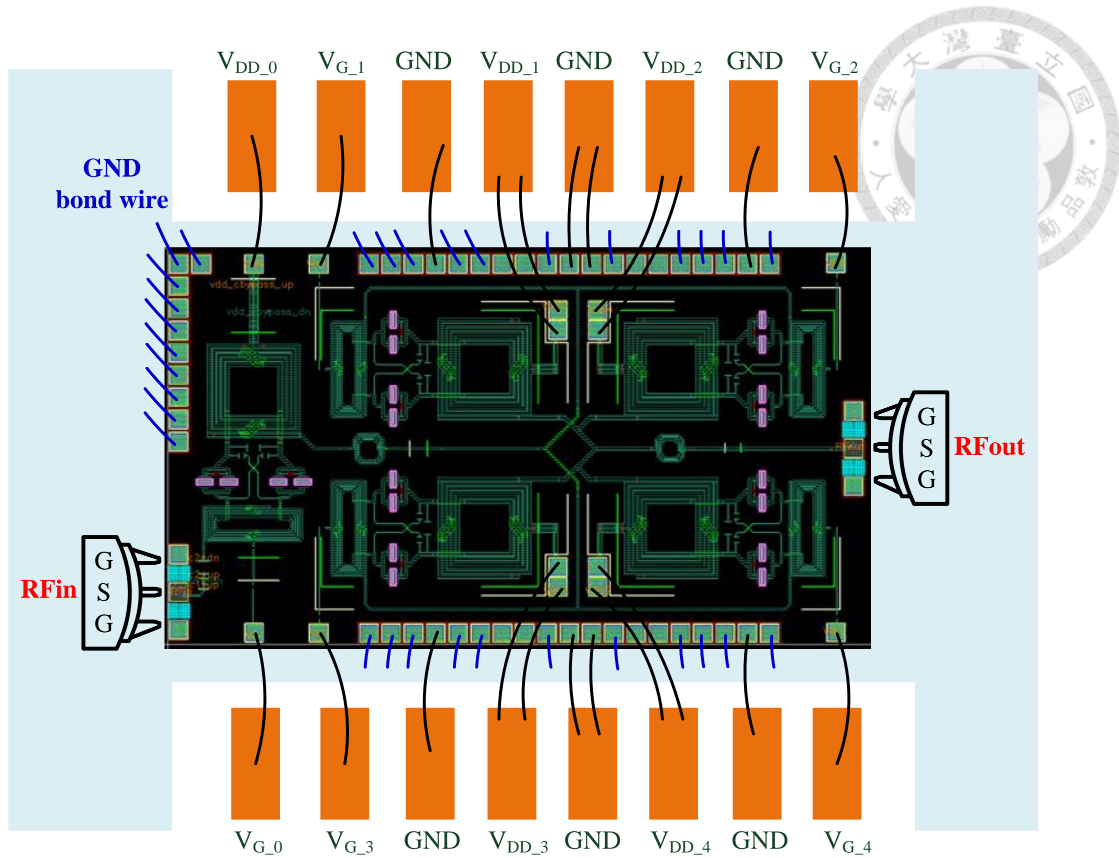

Figure 4.18 Layout of 3.5 GHz 4-way combined PA (surrounding ground pads)

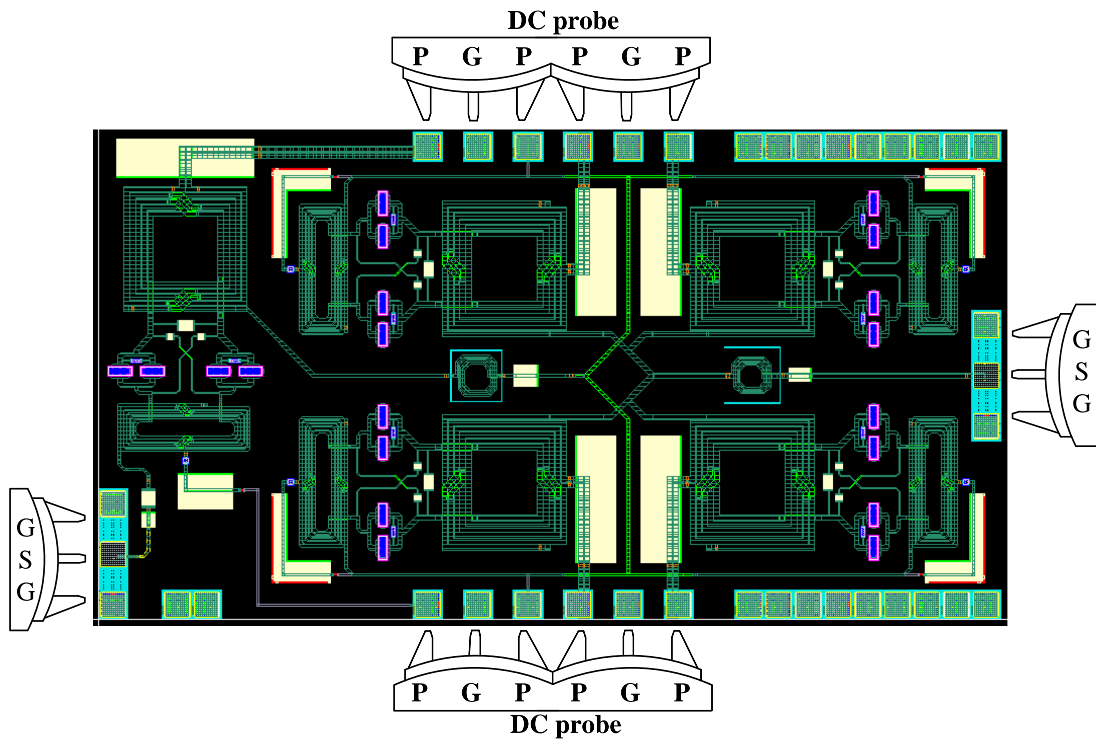

Figure 4.19 Layout of 3.5 GHz 4-way combined power amplifier (on-wafer design)

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4.3 Experimental Results and Discussions

4.3.1 Experimental Results

The watt-level high output power 3.5 GHz power amplifier has been designed and fabricated in 40-nm CMOS process. Figure 4.25 shows the chip micrograph of the proposed power amplifier with area 1.712 mm^2 including all testing pads. The circuit is measured on-wafer probing. The simulated and measured results of S-parameter are shown in Figure 4.20. The measured power gain $|S_{21}|$ is 20.8 dB at 3.5 GHz. In Figure 4.21, the measured OP_{1dB} is 26.5 dBm at 3.5 GHz, P_{SAT} is 30.9 dBm and the corresponding peak PAE is 22.7 % at 3.5 GHz.

The measured results of the large-signal performance in 3-dB bandwidth are shown in Figure 4.22. The saturated output power can reach above 29.6 dBm in 3-dB bandwidth, and the maximum saturated output power is 31.26 dBm at 3.42 GHz and 30.9 dBm at 3.5 GHz. Due to the high gain of this power amplifier which is all above 18.2 dB in the 3-dB bandwidth, the maximum gain is 21.16 dB and the peak PAE can be highly reached as 23.95% at 3.42 GHz and 22.7 % at 3.5 GHz.

From observing the simulated and measured values of the input/output matching networks on smith chart, the measured results of S_{11} and S_{22} have slightly larger resistances than the simulated ones due to the passive loss. The small-signal performance of S_{11} in smith chart is shown in Figure 4.23 and the marked points are 56.5-32j Ω for the simulation and 39.1-26.66j Ω for the measurement. Similarly, the small-signal performance of S_{22} in smith chart is shown in Figure 4.24 and the marked points are 32.2+17.2j Ω for the simulation and 39.7-5.2j Ω for the measurement, respectively. The measured S_{22} is closer to 50 Ω to obtain a better output return loss than the simulated one.

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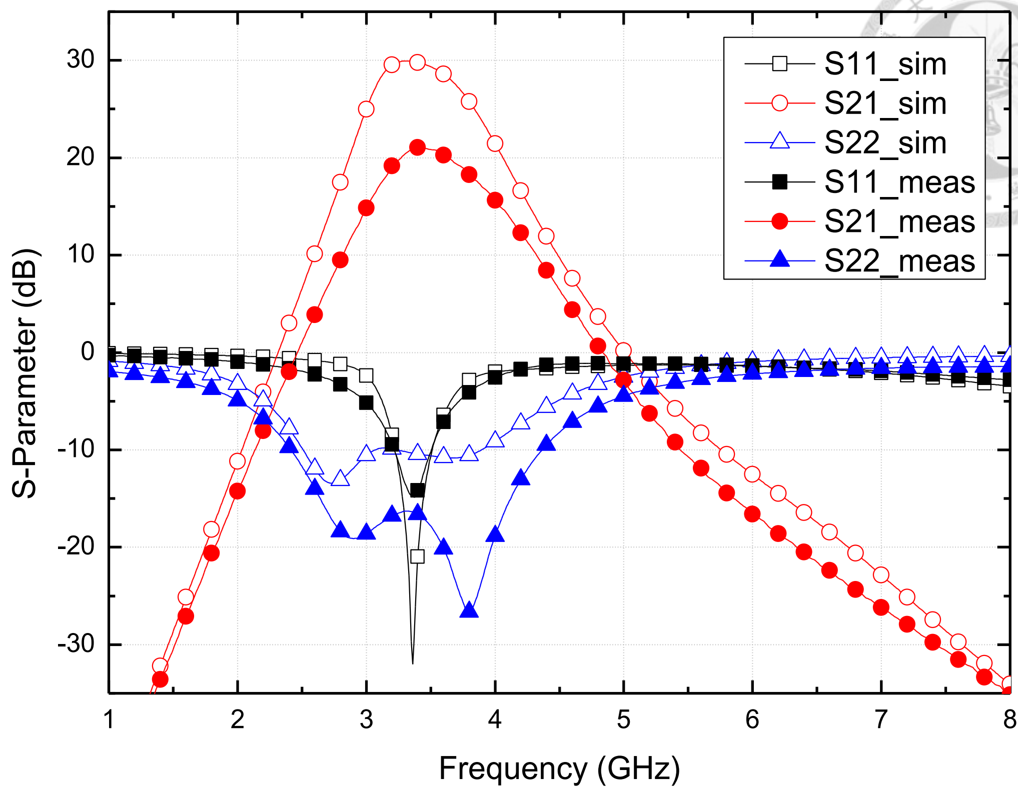

Figure 4.20 The small-signal simulated and measured results on 3.5 GHz 4-way PA

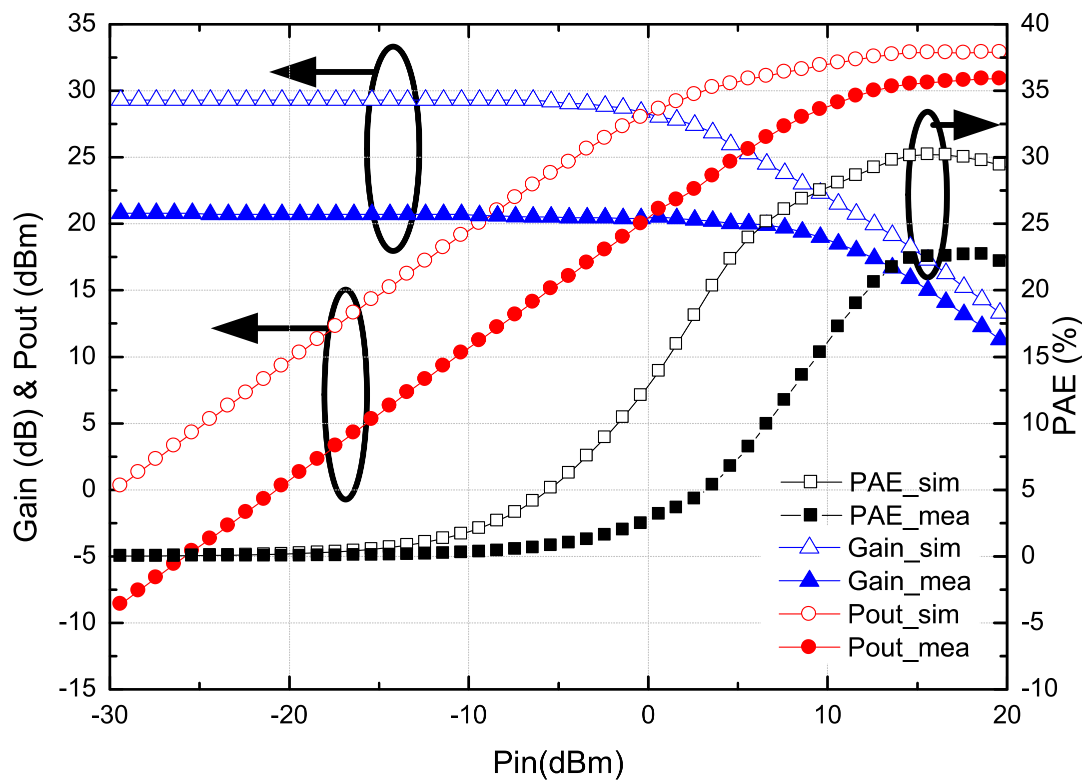

Figure 4.21 The large-signal simulated and measured results on 3.5 GHz 4-way PA

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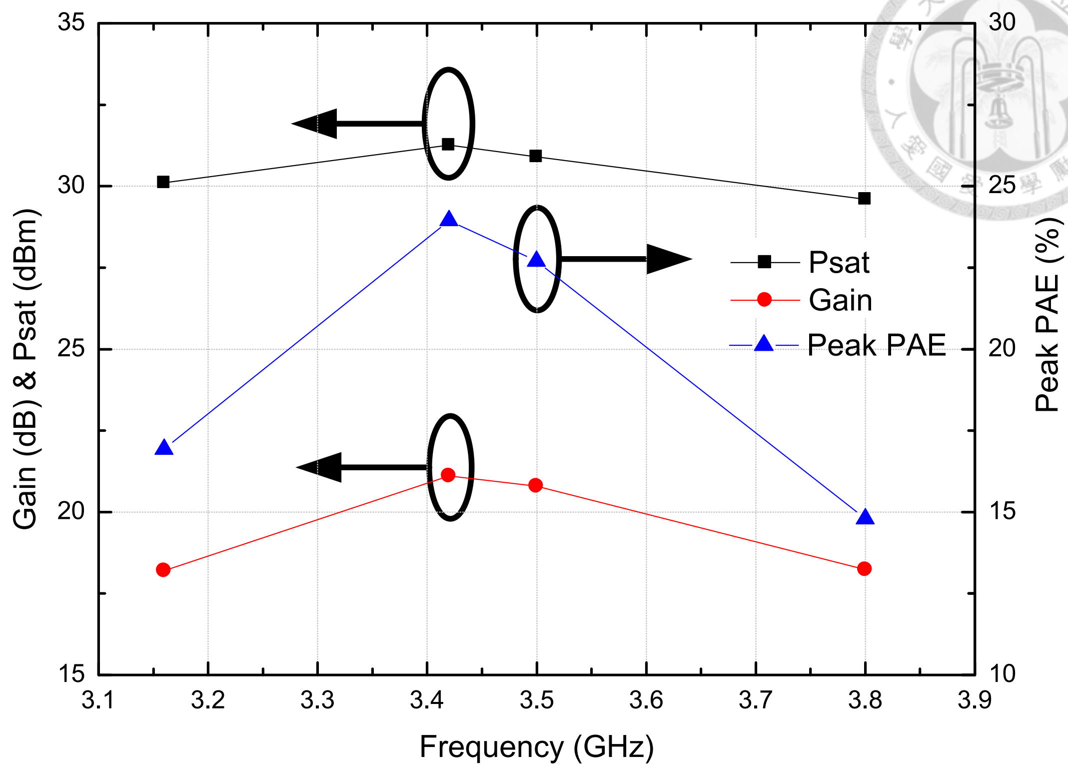

Figure 4.22 The large-signal performance in 3-dB bandwidth

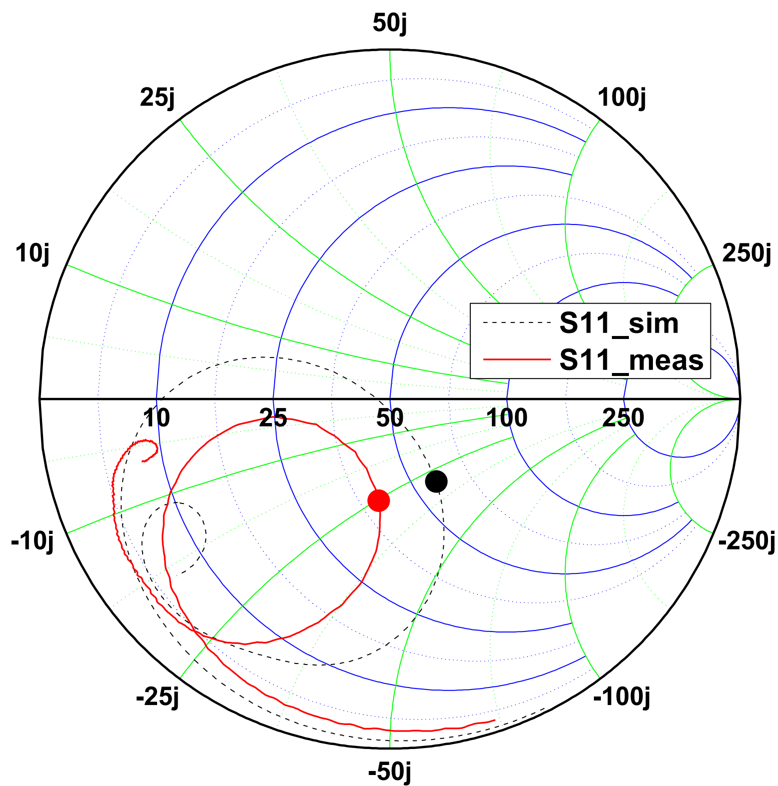

Figure 4.23 The simulated and measured smith chart of S_{11}

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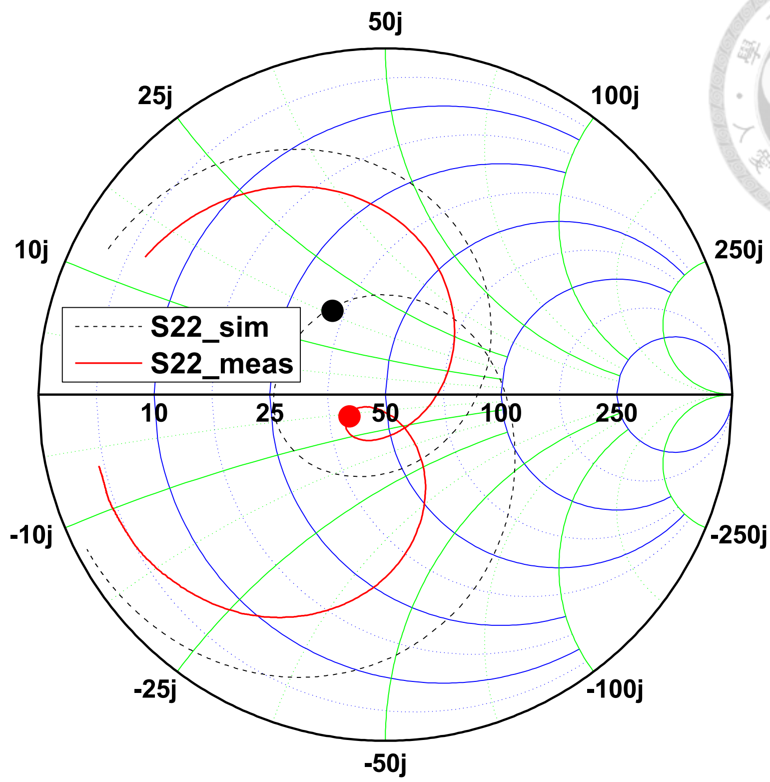

Figure 4.24 The simulated and measured smith chart of S_{22}

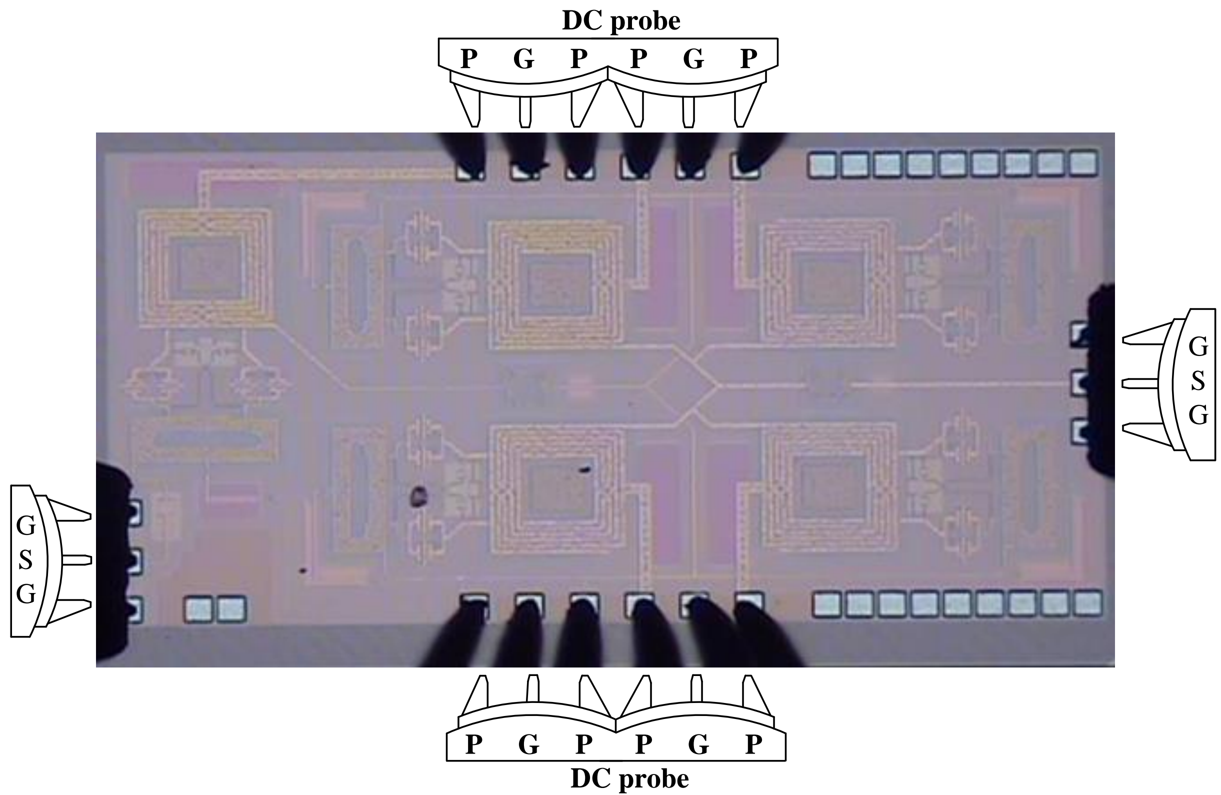

Figure 4.25 Chip micrograph of the 3.5 GHz PA with area 1.712 mm^2

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Table 4-3 DC Pin of the Correlated Bias Voltages of the 4-Way Combined PA

DC pin	P	G	P	P	G	P
Upper	V_{DD_0}=5V	GND	V_{G_1}=1.2V	V_{DD_1}=5V	GND	V_{DD_2}=5V
Lower	V_{G_0}=1.2V	GND	V_{G_2}=1.2V	V_{DD_3}=5V	GND	V_{DD_4}=5V

4.3.2 Re-simulations According to the Measured Results

Due to the thermal issues, passive loss, and parasitic resistance and inductance between transistor source and ground pad, the re-simulation of small-signal and large-signal results are made with taking all these factors into accounts.

The thermal management technology in Figure 4.26 shows the methods to release the self-heating issues from an integrated circuit design. Firstly, since the limitation of on-wafer probing cannot be packaged, the active method can only use gas cooler and thermoelectric/thermionic coolers. The simplest gas cooler is fan, and it can drop temperature about 10℃ to 30℃. Thermoelectric coolers can only be observed under thermal camera but the on-wafer probing for thickness of thermoelectric cooler.

Secondly, the thermal vias method is applied in the design of the printed circuit board (PCB), which is top and bottom layers of PCB with through vias. This method can effectively release the heat and drop the temperature. Thirdly, the silver gel is a very common thermal gel material that is used to have chip and PCB fully attached.

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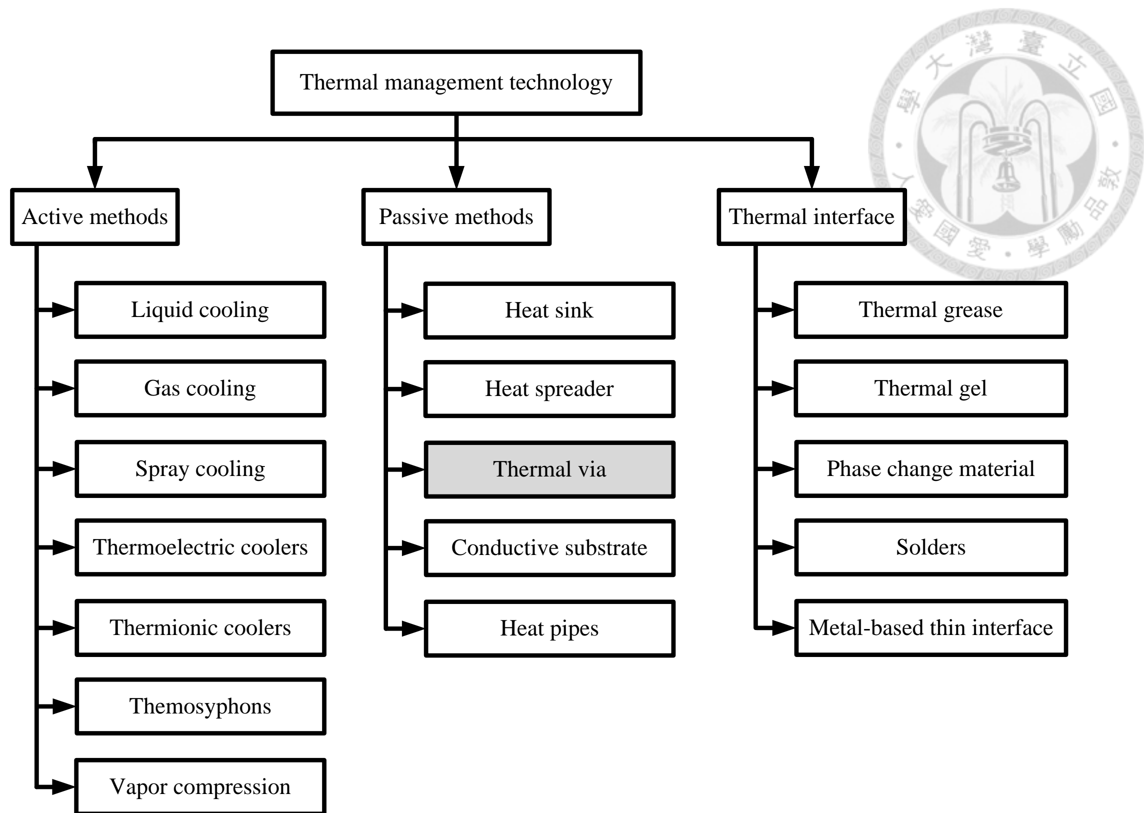

Figure 4.26 Thermal management technology

The re-simulation of small-signal gain is dropped from 29.355 dB to 24.2 dB at 3.5 GHz. With parasitic resistance and inductance consideration, the re-simulation of small-signal result is dropped slightly with an extra 0.68 dB as the resultant value of 23.48 dB at 3.5 GHz. The re-simulation of small-signal result is shown in Figure 4.27 and the re-simulation of the large-signal results is shown in Figure 4.28. The in-band small-signal performances of the re-simulation and measurement are very close as shown in Figure 4.29 and Figure 4.30.

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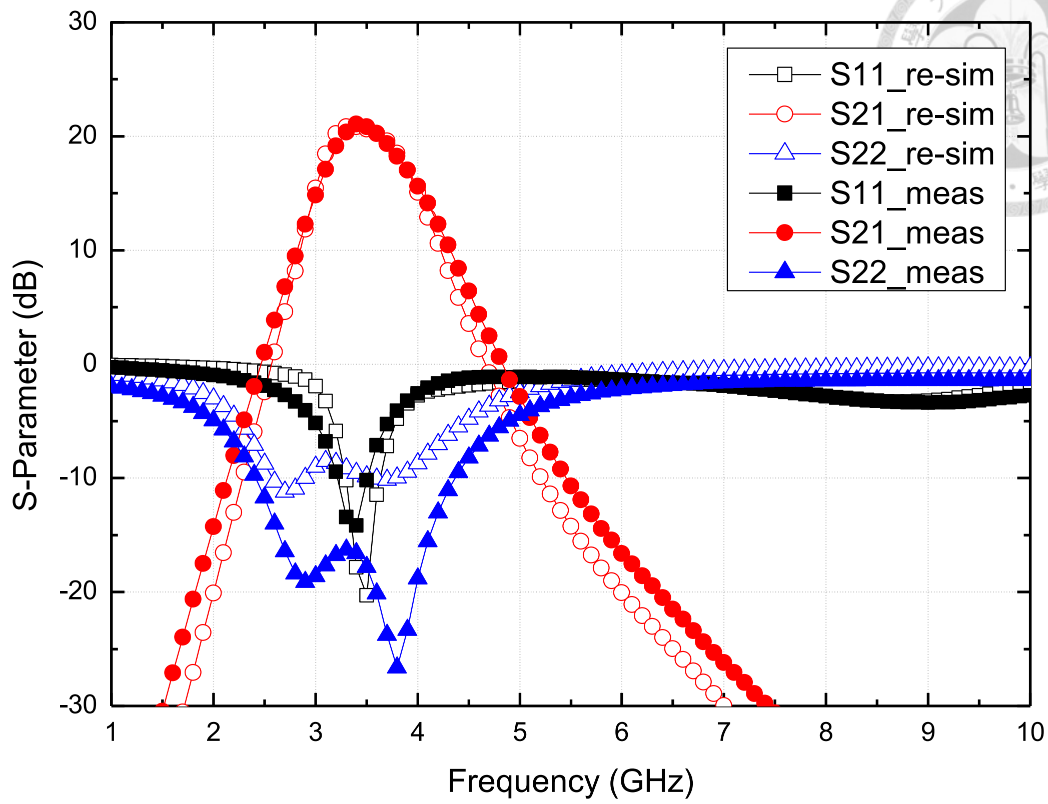

Figure 4.27 The small-signal re-simulation on 3.5 GHz 4-way PA

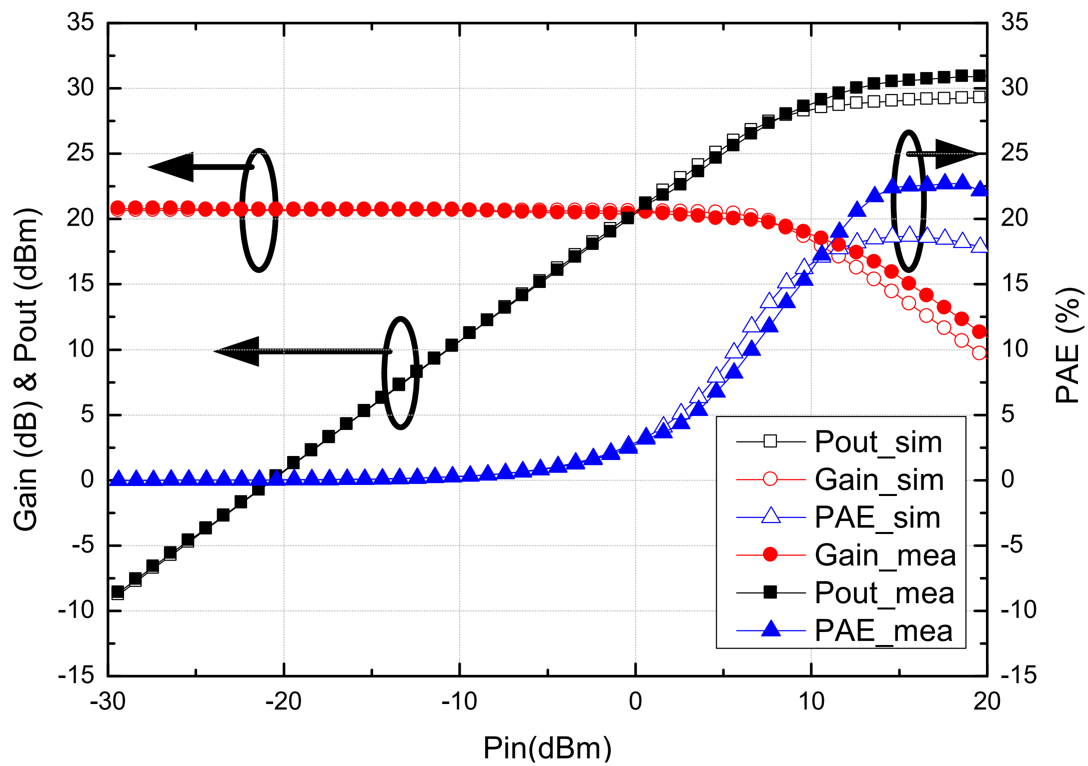

Figure 4.28 The large-signal re-simulation on 3.5 GHz 4-way PA

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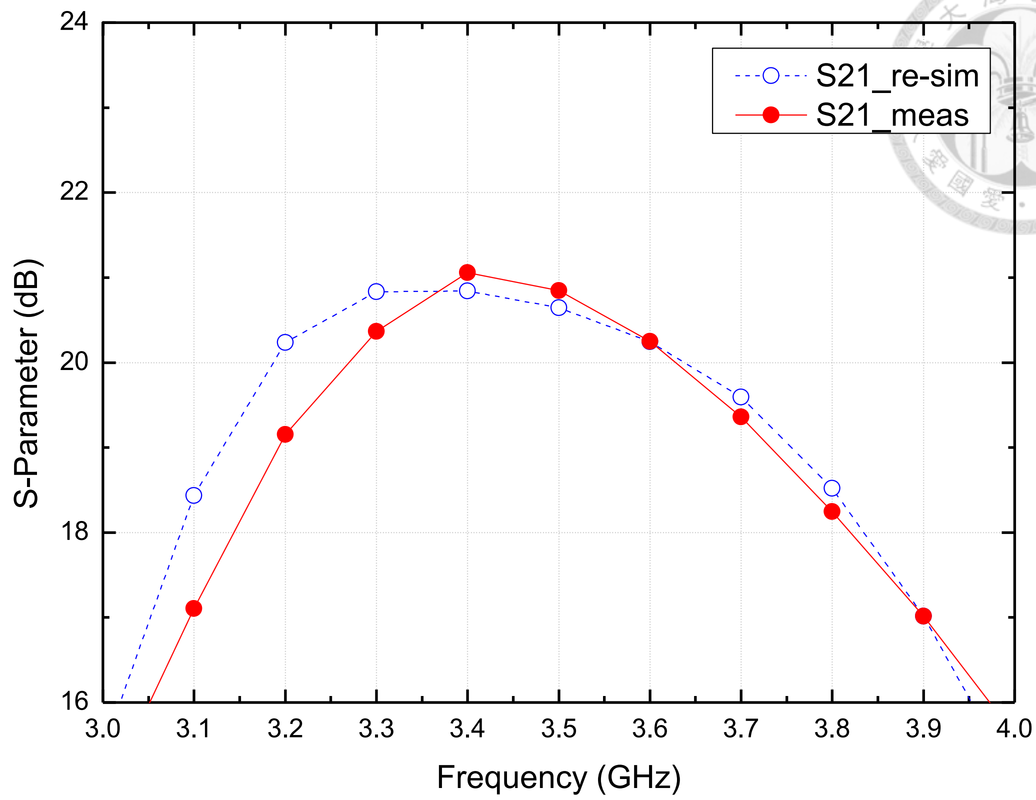

Figure 4.29 The small-signal re-simulation at 3-4 GHz

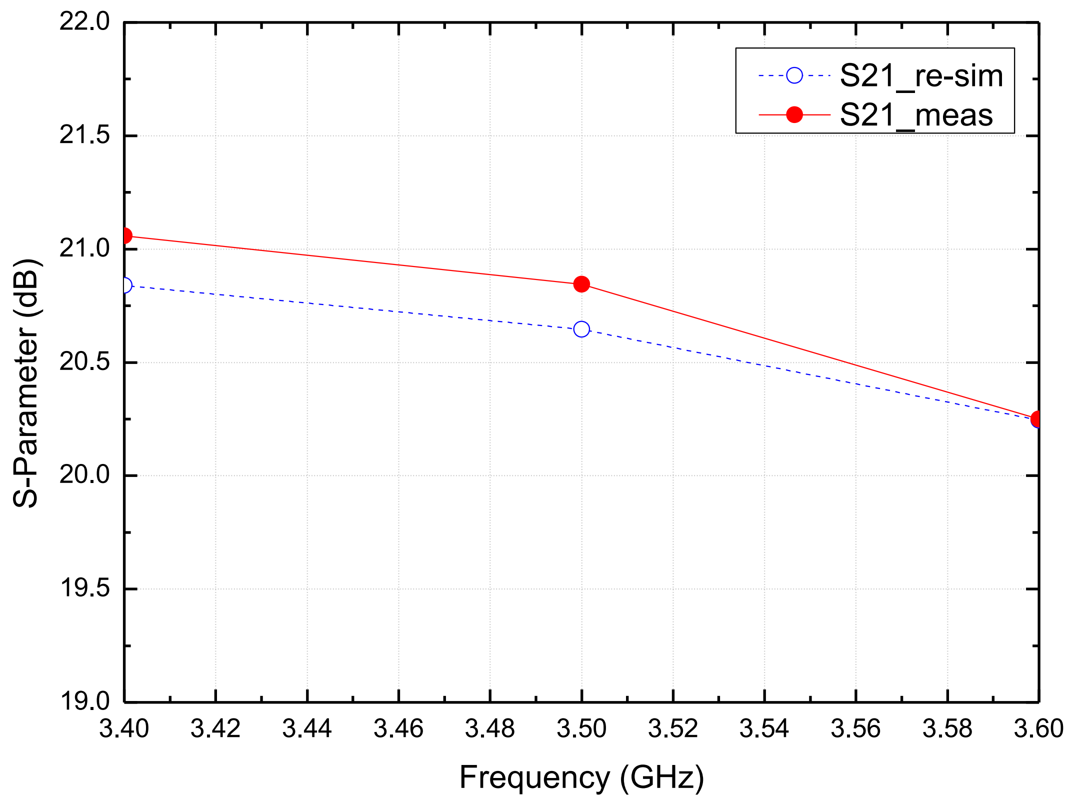

Figure 4.30 The small-signal re-simulation at 3.4-3.6 GHz

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Table 4-4 Comparison Table with Relevant State-of-the-Art PAs

Ref.	Process	f_o (GHz)	P_{sat} (dBm)	Peak PAE (%)	OP_{1dB} (dBm)	Gain (dB)
[31] 2012 MWCL	2 μm GaAs HBT-HEMT	3.5-6.5	27	38	26.4	13.5
[31] 2012 MWCL	0.5 μm GaAs HBT-HEMT	3.5-6.5	29.4	27.2	29.1	11
[32] 2007 IMS	2 μm GaAs HBT	4.5-5.8	29	38	26	13.1
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	28	35	22	14
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	30.5	31	21	26.5
[33] 2011 APMC	SiGe 0.35 μm HBT	3.5	30	31	23.5	18
[34] 2003 RFICS	SiGe HBT	5	30	27	26	21
This Work	**40 nm LDMOS**	**3.5**	**30.9**	**22.7**	**26.5**	**20.8**

In the comparison table of Table 4-4 shows this watt-level 3.5-GHz power amplifier design is the highest output power among the published 3.5-GHz band and 5-GHz band power amplifiers in the recent years. Most other power amplifiers in this frequency band are used GaAs HBT-HEMT and SiGe 0.35-μm HBT process with higher supply voltages. The first three designs use stacked power amplifiers and the three of SiGe 0.35-μm HBT process use Quasi-Doherty power amplifier. Other than high supply voltage, some techniques induce in the power amplifier designs can effectively achieve in a high output power design. This work of power amplifier design is used only 5-V supply voltage with LDMOS device in 40-nm CMOS process to reach the highest output power above all.

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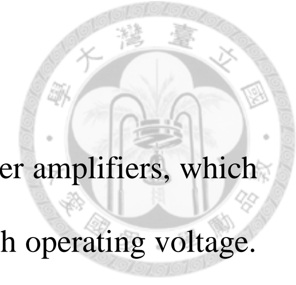
Chapter 5 Conclusion



This thesis presents the design and implementation of two power amplifiers, which are designed based on high output power, compact chip size and high operating voltage. The two power amplifiers are fabricated in TSMC 40 nm process.

In chapter 3, a compact 3.5-GHz fully-integrated transformer combined LDMOS power amplifier is presented. With the neutralization technique, the instability issue has been solved. The proposed miniature 3.5-GHz transformer-based LDMOS power amplifier has gain of 15.4 dB at 3.5 GHz, OP_{1dB} of 24.1 dBm, P_{sat} of 26.5 dBm and peak PAE is 25 % under 5 V supply voltage with chip size 0.259 mm^2; in addition, it reaches the highest P_{sat} power area density of 1724 mW/mm^2 and OP_{1dB} power area density of 992.4 mW/mm^2.

In chapter 4, a watt-level 3.5-GHz fully-integrated transformer combined LDMOS power amplifier is presented. With the radial passive structure, a fully symmetric power splitter and combiner without length routing components is realized, and the distributed power cells reduce the burden of large DC current and thermal issue. The 3-D architecture let power combiner and power splitter share the same area and minimize the chip size. The proposed 3.5-GHz transformer-based high output power amplifier has gain of 20.8 dB at 3.5 GHz, OP_{1dB} of 26.5 dBm, P_{sat} of 30.9 dBm and peak PAE is 22.7 % under 5 V supply voltage with chip size 1.712 mm^2. The maximum P_{sat} is 31.26 dBm at 3.42 GHz with peak PAE of 23.95 % and gain of 21.16 dB.

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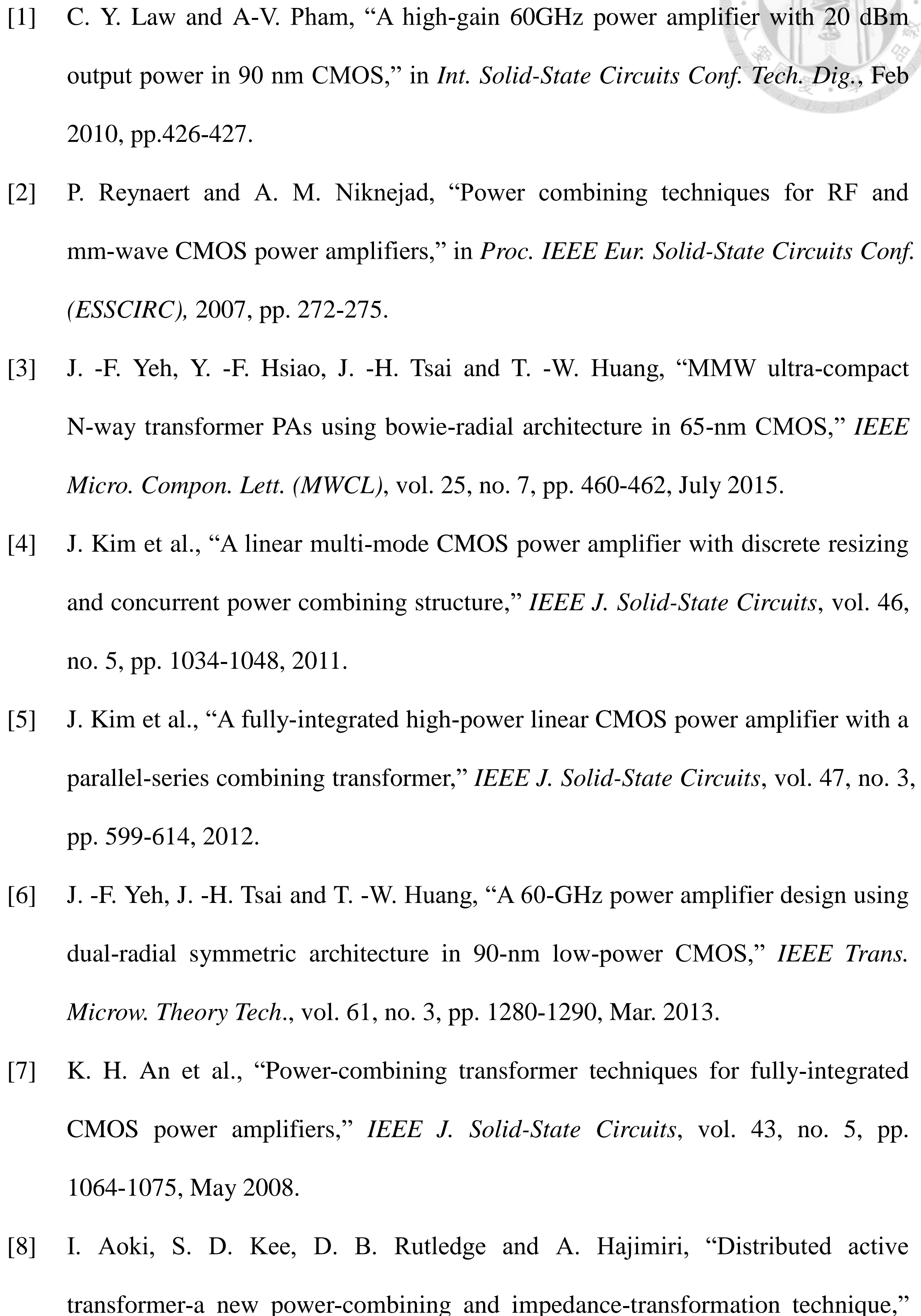
REFERENCE



[1] C. Y. Law and A-V. Pham, "A high-gain 60GHz power amplifier with 20 dBm output power in 90 nm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb 2010, pp.426-427.

[2] P. Reynaert and A. M. Niknejad, "Power combining techniques for RF and mm-wave CMOS power amplifiers," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC),* 2007, pp. 272-275.

[3] J. -F. Yeh, Y. -F. Hsiao, J. -H. Tsai and T. -W. Huang, "MMW ultra-compact N-way transformer PAs using bowie-radial architecture in 65-nm CMOS," *IEEE Micro. Compon. Lett. (MWCL)*, vol. 25, no. 7, pp. 460-462, July 2015.

[4] J. Kim et al., "A linear multi-mode CMOS power amplifier with discrete resizing and concurrent power combining structure," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1034-1048, 2011.

[5] J. Kim et al., "A fully-integrated high-power linear CMOS power amplifier with a parallel-series combining transformer," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 599-614, 2012.

[6] J. -F. Yeh, J. -H. Tsai and T. -W. Huang, "A 60-GHz power amplifier design using dual-radial symmetric architecture in 90-nm low-power CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1280-1290, Mar. 2013.

[7] K. H. An et al., "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064-1075, May 2008.

[8] I. Aoki, S. D. Kee, D. B. Rutledge and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique,"

doi:10.6342/NTU201603297

IEEE Trans. Microw. Theory Tech., vol. 50, no. 1, pp. 316-331, 2002.

[9] I. Aoki, S. Kee, D. Rutledge and A. Hajimiri, “Fully integrated CMOS power amplifier design using the distributed active-transformer architecture,” *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371-383, Mar. 2002.

[10] D. Gruner, R. Sorge, O. Bengtsson, A. Al Tanany and G. Boeck, “Analysis, design, and evaluation of LDMOS FETs for RF power applications up to 6 GHz,” *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 4022-4030, Dec. 2010.

[11] F. van Rijs, “Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications,” in *Radio Wireless Symp.*, Jan. 2008, pp. 69-72.

[12] R. Sorge et al., “Complementary RF LDMOS module for 12 V DC/DC converter and 6 GHz power applications,” in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2011, pp. 57-60.

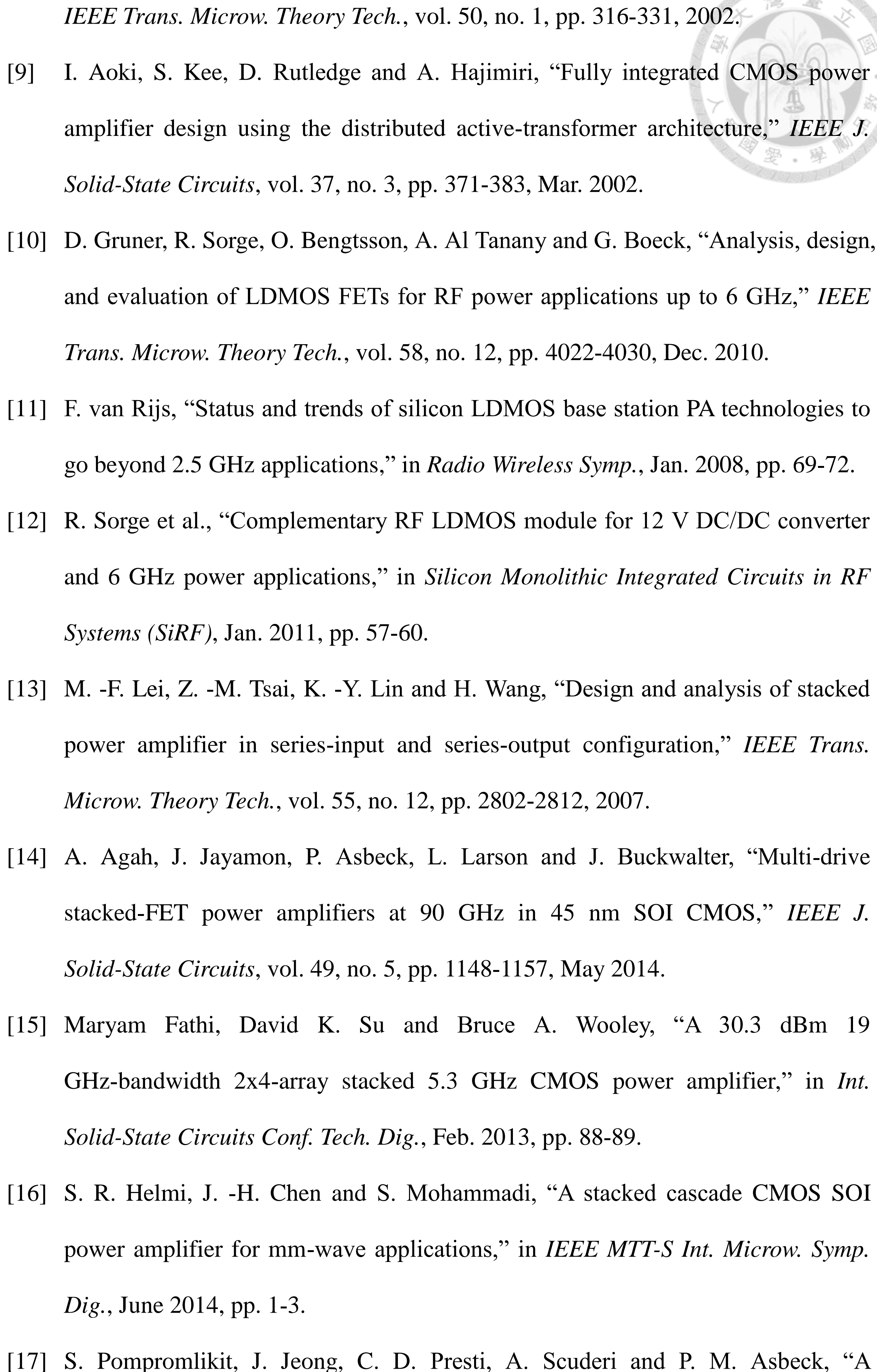
[13] M. -F. Lei, Z. -M. Tsai, K. -Y. Lin and H. Wang, “Design and analysis of stacked power amplifier in series-input and series-output configuration,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2802-2812, 2007.

[14] A. Agah, J. Jayamon, P. Asbeck, L. Larson and J. Buckwalter, “Multi-drive stacked-FET power amplifiers at 90 GHz in 45 nm SOI CMOS,” *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1148-1157, May 2014.

[15] Maryam Fathi, David K. Su and Bruce A. Wooley, “A 30.3 dBm 19 GHz-bandwidth 2x4-array stacked 5.3 GHz CMOS power amplifier,” in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2013, pp. 88-89.

[16] S. R. Helmi, J. -H. Chen and S. Mohammadi, “A stacked cascade CMOS SOI power amplifier for mm-wave applications,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2014, pp. 1-3.

[17] S. Pompromlikit, J. Jeong, C. D. Presti, A. Scuderi and P. M. Asbeck, “A



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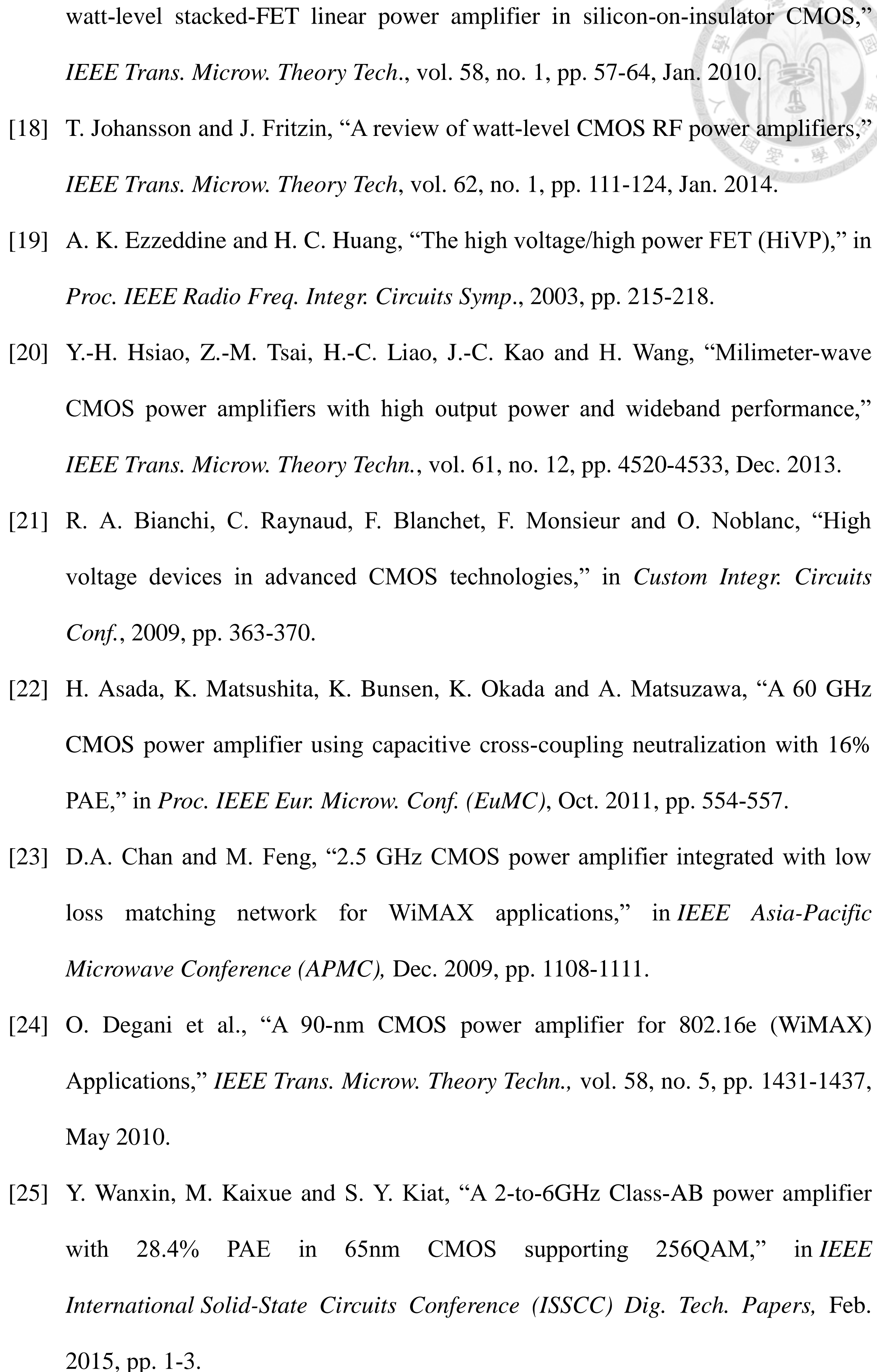


watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 1, pp. 57-64, Jan. 2010.

[18] T. Johansson and J. Fritzin, "A review of watt-level CMOS RF power amplifiers," *IEEE Trans. Microw. Theory Tech*, vol. 62, no. 1, pp. 111-124, Jan. 2014.

[19] A. K. Ezzeddine and H. C. Huang, "The high voltage/high power FET (HiVP)," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2003, pp. 215-218.

[20] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao and H. Wang, "Milimeter-wave CMOS power amplifiers with high output power and wideband performance," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4520-4533, Dec. 2013.

[21] R. A. Bianchi, C. Raynaud, F. Blanchet, F. Monsieur and O. Noblanc, "High voltage devices in advanced CMOS technologies," in *Custom Integr. Circuits Conf.*, 2009, pp. 363-370.

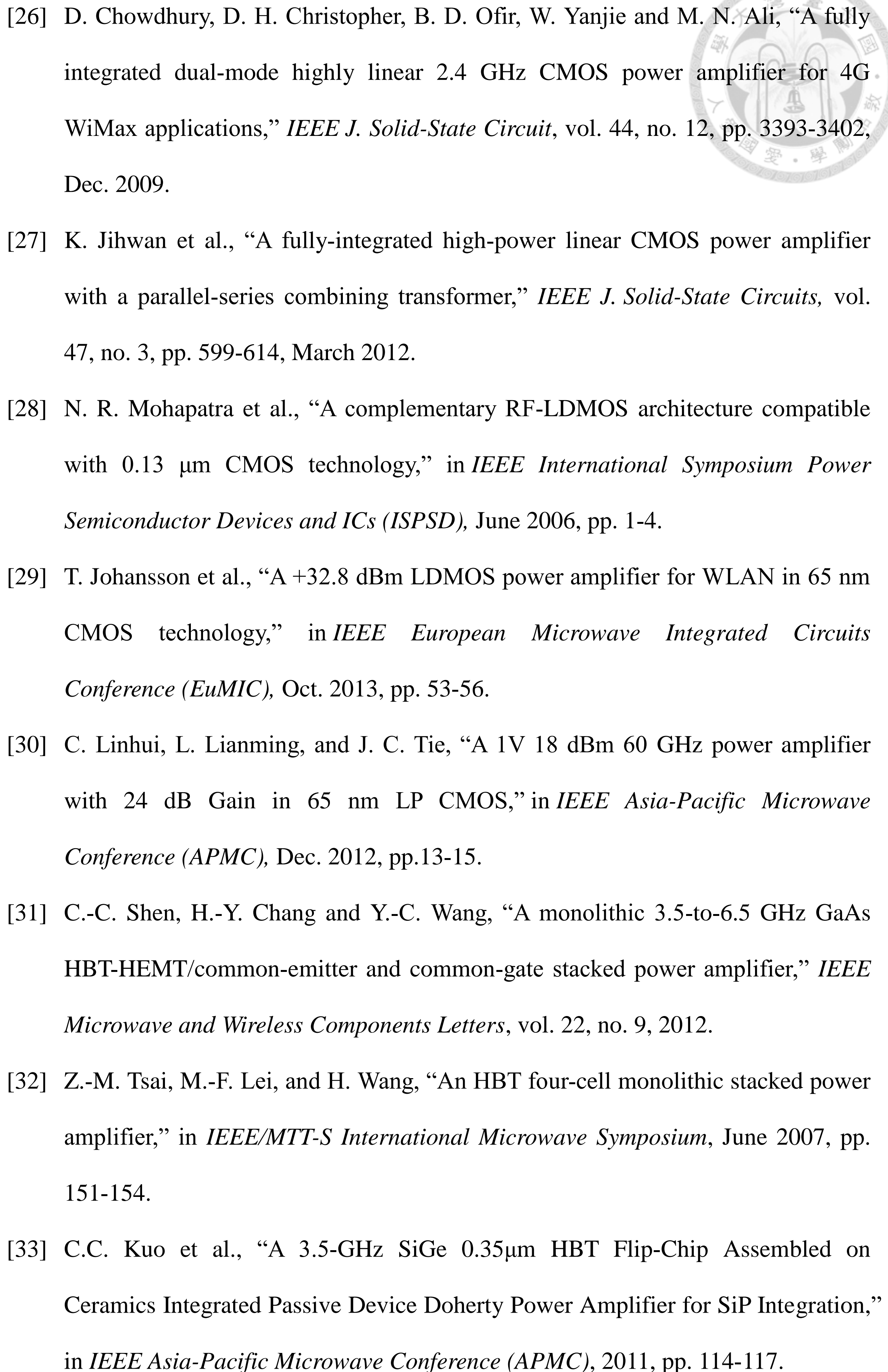
[22] H. Asada, K. Matsushita, K. Bunsen, K. Okada and A. Matsuzawa, "A 60 GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16% PAE," in *Proc. IEEE Eur. Microw. Conf. (EuMC)*, Oct. 2011, pp. 554-557.

[23] D.A. Chan and M. Feng, "2.5 GHz CMOS power amplifier integrated with low loss matching network for WiMAX applications," in *IEEE Asia-Pacific Microwave Conference (APMC),* Dec. 2009, pp. 1108-1111.

[24] O. Degani et al., "A 90-nm CMOS power amplifier for 802.16e (WiMAX) Applications," *IEEE Trans. Microw. Theory Techn.,* vol. 58, no. 5, pp. 1431-1437, May 2010.

[25] Y. Wanxin, M. Kaixue and S. Y. Kiat, "A 2-to-6GHz Class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256QAM," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers,* Feb. 2015, pp. 1-3.

doi:10.6342/NTU201603297



[26] D. Chowdhury, D. H. Christopher, B. D. Ofir, W. Yanjie and M. N. Ali, “A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMax applications,” *IEEE J. Solid-State Circuit*, vol. 44, no. 12, pp. 3393-3402, Dec. 2009.

[27] K. Jihwan et al., “A fully-integrated high-power linear CMOS power amplifier with a parallel-series combining transformer,” *IEEE J. Solid-State Circuits,* vol. 47, no. 3, pp. 599-614, March 2012.

[28] N. R. Mohapatra et al., “A complementary RF-LDMOS architecture compatible with 0.13 μm CMOS technology,” in *IEEE International Symposium Power Semiconductor Devices and ICs (ISPSD),* June 2006, pp. 1-4.

[29] T. Johansson et al., “A +32.8 dBm LDMOS power amplifier for WLAN in 65 nm CMOS technology,” in *IEEE European Microwave Integrated Circuits Conference (EuMIC),* Oct. 2013, pp. 53-56.

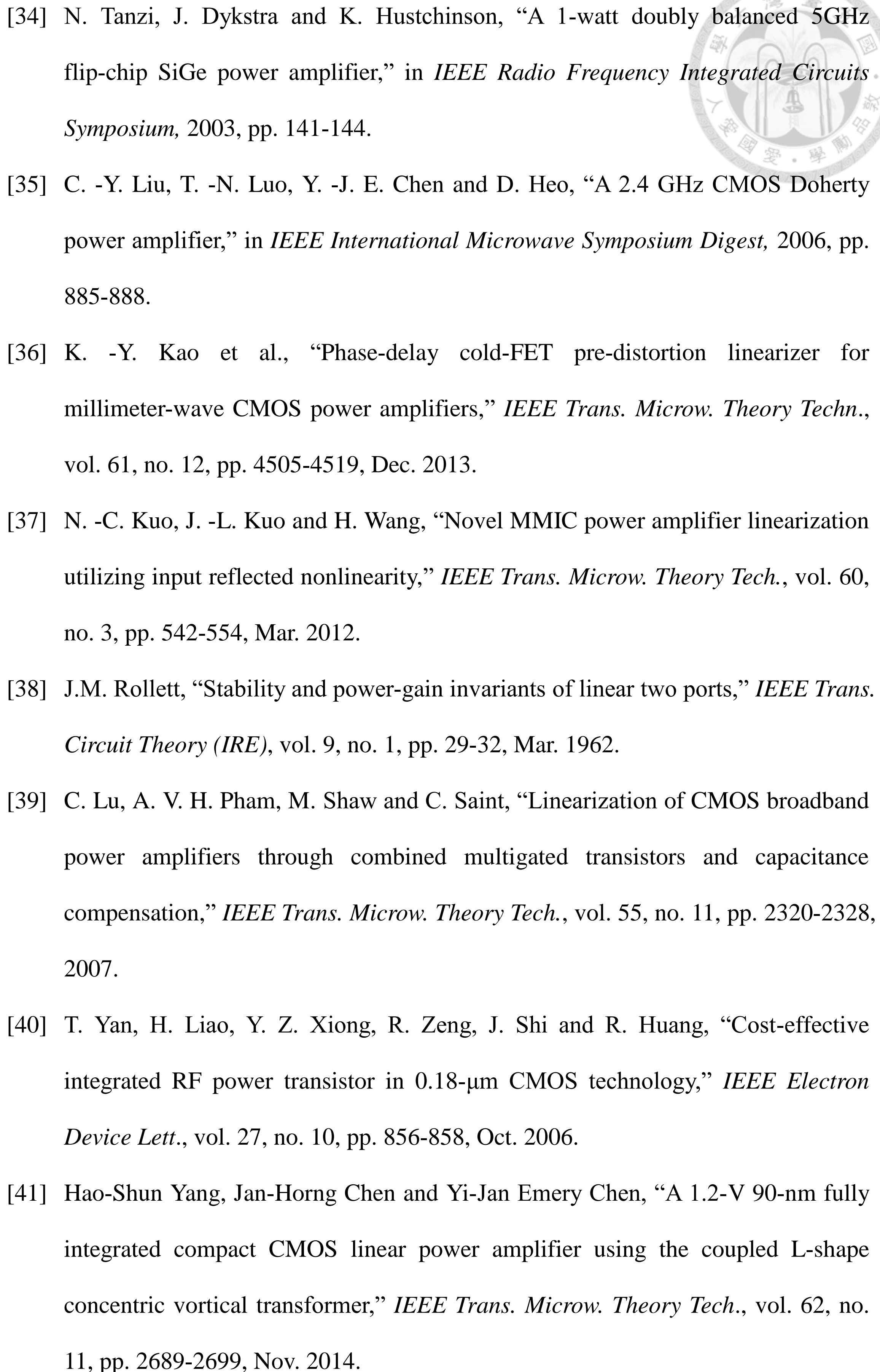
[30] C. Linhui, L. Lianming, and J. C. Tie, “A 1V 18 dBm 60 GHz power amplifier with 24 dB Gain in 65 nm LP CMOS,” in *IEEE Asia-Pacific Microwave Conference (APMC),* Dec. 2012, pp.13-15.

[31] C.-C. Shen, H.-Y. Chang and Y.-C. Wang, “A monolithic 3.5-to-6.5 GHz GaAs HBT-HEMT/common-emitter and common-gate stacked power amplifier,” *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 9, 2012.

[32] Z.-M. Tsai, M.-F. Lei, and H. Wang, “An HBT four-cell monolithic stacked power amplifier,” in *IEEE/MTT-S International Microwave Symposium*, June 2007, pp. 151-154.

[33] C.C. Kuo et al., “A 3.5-GHz SiGe 0.35μm HBT Flip-Chip Assembled on Ceramics Integrated Passive Device Doherty Power Amplifier for SiP Integration,” in *IEEE Asia-Pacific Microwave Conference (APMC)*, 2011, pp. 114-117.

doi:10.6342/NTU201603297



[34] N. Tanzi, J. Dykstra and K. Hustchinson, “A 1-watt doubly balanced 5GHz flip-chip SiGe power amplifier,” in *IEEE Radio Frequency Integrated Circuits Symposium,* 2003, pp. 141-144.

[35] C. -Y. Liu, T. -N. Luo, Y. -J. E. Chen and D. Heo, “A 2.4 GHz CMOS Doherty power amplifier,” in *IEEE International Microwave Symposium Digest,* 2006, pp. 885-888.

[36] K. -Y. Kao et al., “Phase-delay cold-FET pre-distortion linearizer for millimeter-wave CMOS power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4505-4519, Dec. 2013.

[37] N. -C. Kuo, J. -L. Kuo and H. Wang, “Novel MMIC power amplifier linearization utilizing input reflected nonlinearity,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 542-554, Mar. 2012.

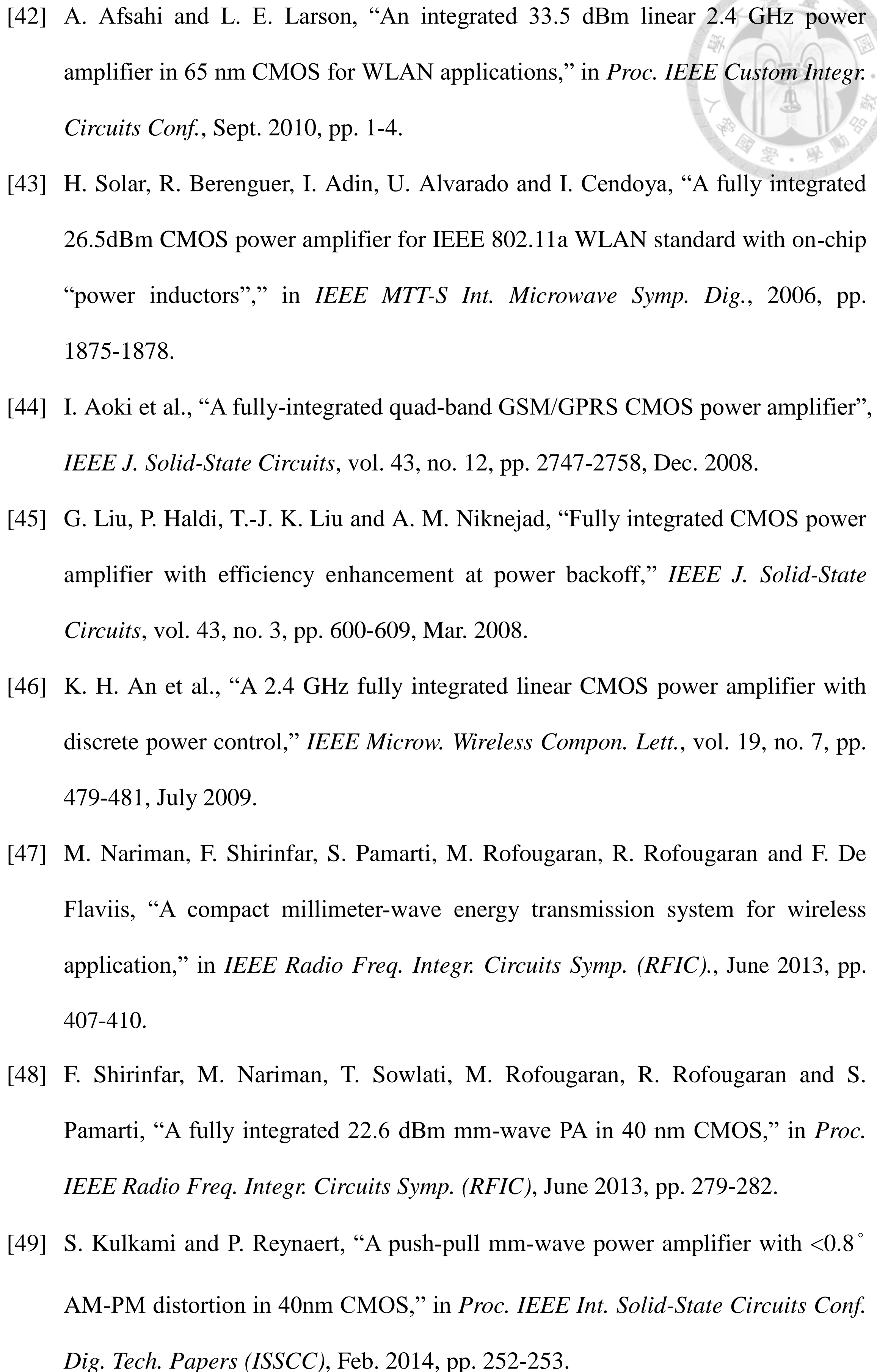
[38] J.M. Rollett, “Stability and power-gain invariants of linear two ports,” *IEEE Trans. Circuit Theory (IRE)*, vol. 9, no. 1, pp. 29-32, Mar. 1962.

[39] C. Lu, A. V. H. Pham, M. Shaw and C. Saint, “Linearization of CMOS broadband power amplifiers through combined multigated transistors and capacitance compensation,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 11, pp. 2320-2328, 2007.

[40] T. Yan, H. Liao, Y. Z. Xiong, R. Zeng, J. Shi and R. Huang, “Cost-effective integrated RF power transistor in 0.18-μm CMOS technology,” *IEEE Electron Device Lett.*, vol. 27, no. 10, pp. 856-858, Oct. 2006.

[41] Hao-Shun Yang, Jan-Horng Chen and Yi-Jan Emery Chen, “A 1.2-V 90-nm fully integrated compact CMOS linear power amplifier using the coupled L-shape concentric vortical transformer,” *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 11, pp. 2689-2699, Nov. 2014.

doi:10.6342/NTU201603297



[42] A. Afsahi and L. E. Larson, “An integrated 33.5 dBm linear 2.4 GHz power amplifier in 65 nm CMOS for WLAN applications,” in *Proc. IEEE Custom Integr. Circuits Conf.*, Sept. 2010, pp. 1-4.

[43] H. Solar, R. Berenguer, I. Adin, U. Alvarado and I. Cendoya, “A fully integrated 26.5dBm CMOS power amplifier for IEEE 802.11a WLAN standard with on-chip “power inductors”,” in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2006, pp. 1875-1878.

[44] I. Aoki et al., “A fully-integrated quad-band GSM/GPRS CMOS power amplifier”, *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2747-2758, Dec. 2008.

[45] G. Liu, P. Haldi, T.-J. K. Liu and A. M. Niknejad, “Fully integrated CMOS power amplifier with efficiency enhancement at power backoff,” *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600-609, Mar. 2008.

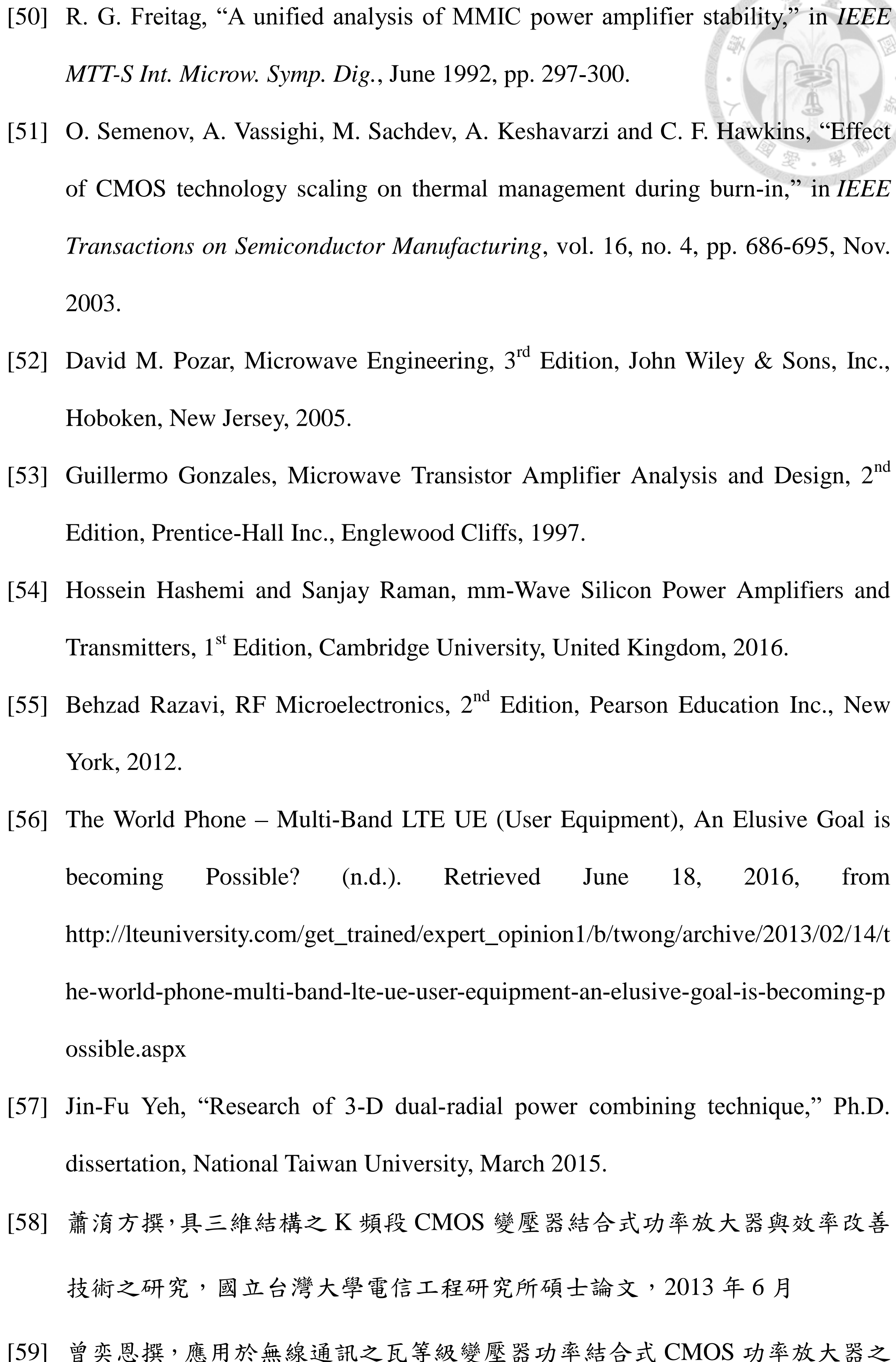
[46] K. H. An et al., “A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control,” *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 7, pp. 479-481, July 2009.

[47] M. Nariman, F. Shirinfar, S. Pamarti, M. Rofougaran, R. Rofougaran and F. De Flaviis, “A compact millimeter-wave energy transmission system for wireless application,” in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC).*, June 2013, pp. 407-410.

[48] F. Shirinfar, M. Nariman, T. Sowlati, M. Rofougaran, R. Rofougaran and S. Pamarti, “A fully integrated 22.6 dBm mm-wave PA in 40 nm CMOS,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, June 2013, pp. 279-282.

[49] S. Kulkami and P. Reynaert, “A push-pull mm-wave power amplifier with <0.8° AM-PM distortion in 40nm CMOS,” in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 252-253.

doi:10.6342/NTU201603297



[50] R. G. Freitag, "A unified analysis of MMIC power amplifier stability," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 1992, pp. 297-300.

[51] O. Semenov, A. Vassighi, M. Sachdev, A. Keshavarzi and C. F. Hawkins, "Effect of CMOS technology scaling on thermal management during burn-in," in *IEEE Transactions on Semiconductor Manufacturing*, vol. 16, no. 4, pp. 686-695, Nov. 2003.

[52] David M. Pozar, Microwave Engineering, 3rd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2005.

[53] Guillermo Gonzales, Microwave Transistor Amplifier Analysis and Design, 2nd Edition, Prentice-Hall Inc., Englewood Cliffs, 1997.

[54] Hossein Hashemi and Sanjay Raman, mm-Wave Silicon Power Amplifiers and Transmitters, 1st Edition, Cambridge University, United Kingdom, 2016.

[55] Behzad Razavi, RF Microelectronics, 2nd Edition, Pearson Education Inc., New York, 2012.

[56] The World Phone – Multi-Band LTE UE (User Equipment), An Elusive Goal is becoming Possible? (n.d.). Retrieved June 18, 2016, from http://lteuniversity.com/get_trained/expert_opinion1/b/twong/archive/2013/02/14/the-world-phone-multi-band-lte-ue-user-equipment-an-elusive-goal-is-becoming-possible.aspx

[57] Jin-Fu Yeh, "Research of 3-D dual-radial power combining technique," Ph.D. dissertation, National Taiwan University, March 2015.

[58] 蕭湞方撰,具三維結構之 K 頻段 CMOS 變壓器結合式功率放大器與效率改善技術之研究，國立台灣大學電信工程研究所碩士論文，2013 年 6 月

[59] 曾奕恩撰,應用於無線通訊之瓦等級變壓器功率結合式 CMOS 功率放大器之

doi:10.6342/NTU201603297

研製，國立台灣大學電信工程所碩士論文，2014 年 7 月

[60] 羅士駿撰，具三維結構之瓦級並聯變壓器結合式 CMOS 功率放大器之研製，國立台灣大學電信工程所碩士論文，2015 年 7 月

[61] 黃梓原撰，微波及毫米波系統關鍵元件之設計與研究，國立台灣大學電信工程所碩士論文，2015 年 1 月

[62] 周正峯撰，微波低雜訊放大器及使用寬頻變壓器對稱放射狀功率結合技術之毫米波功率放大器研究，國立台灣大學電信工程所碩士論文，2016 年 1 月

doi:10.6342/NTU201603297