國立臺灣大學電機資訊學院電子工程學研究所

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Master Thesis

一個操作在 0.9 伏特電壓的高速雙通道時間交錯連續漸進式類比至數位轉換器

A 0.9V High-Speed Two-Channel Time-Interleaved SAR ADC

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A 0.9V High-Speed Two-Channel Time-Interleaved SAR ADC

By

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THESIS

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摘要

近年來，每秒幾億次至十幾億次的中解析度類比至數位轉換器的應用越來越廣泛。本論文提出了一個操作在 0.9 伏特電壓每秒十五億次取樣的八位元兩通道時間交錯式連續漸進式類比至數位轉換器，是以 40 奈米 CMOS 設計。

本論文為了解決時間交錯式類比至數位轉換器的子通道間時脈偏移不匹配問題，提出了一個不需要時脈偏移校正的低時脈偏移的解多工器。為了提高子通道的取樣速度與電能效益，提出了一個使用電荷分配的兩階段連續漸進式類比至數位轉換器與自我觸發閘的技巧。

本時間交錯式連續漸進式類比至數位轉換器在每秒十五億次的取樣速度與奈奎斯特的輸入頻率之下有七點一位元的有效位元，其主動面積只有 0.014mm^2。功率消耗為 3.1mW，達到一個優異的品質因數為 15 fJ/conversion-step，其適合用在高電能效益的無線通訊與乙太網路應用中。

關鍵詞：類比至數位轉換器、時間交錯式、連續漸進式、高速、高電能效益、低時脈偏移解多工器、兩階段

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Abstract

Recently, hundreds MS/s to 1GS/s medium resolution Analog-to-Digital Convertors (ADCs) are used extensively in applications. This thesis proposes a 0.9V 8-bit 1.5GS/s two-channel time-interleaved SAR ADC in 40nm CMOS.

This thesis proposes a low-skew demultiplexer to solve the timing skew problem between the sub-channels without timing skew calibration. In order to improve the sampling frequency and the energy-efficiency of the sub-channel, the two-step SAR ADC with charge sharing technique and the self-triggered latch technique are proposed.

This time-interleaved SAR ADC achieves an ENOB of 7.1 at the conversion rate of 1.5GS/s with Nyquist rate input. The active area is only 0.014 mm^2. It consumes 3.1mW and gets the good FoM of 15fJ/conversion-step. It is suitable for the energy-efficient wireless communication and Ethernet network application.

Keyword: analog-to-digital converter (ADC), time-interleaved, successive-approximation register (SAR), high speed, energy-efficient, low-skew demultiplexer, two-step

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Chapter 1 Introduction

1.1 Motivation

Hundreds MS/s to 1GS/s medium resolution Analog-to-Digital Convertors (ADCs) are used in applications such as Ethernet networks, wireless communication systems and hard disk read channels.

Flash ADC is the fastest architecture to achieve GS/s sampling rate (F_S), but its power consumption and area turns up exponential when its resolution rises. Pipelined ADC is also a high-speed architecture and its cost increases linearly as its resolution grows. However, it needs lots of high-bandwidth but power-hungry residue amplifiers.

Successive-approximation register (SAR) ADC is a popular architecture due to its simple, energy-efficient architecture. But, the speed of SAR ADC is limited by the regeneration time of the comparator and the digital loop delay time. Several methods are reported to speed up F_S of the SAR ADCs such as [1][2]. However, it degrades the charming FoM performance when single-channel 8-bit ADCs work at their speed limitations of around 0.9-1.3GS/s [1]-[3].

Time-interleaved (TI) ADC [12]-[15] is the most intuitive method to increase F_S by paralleling many slow but energy-efficient sub-ADC channels. Besides,

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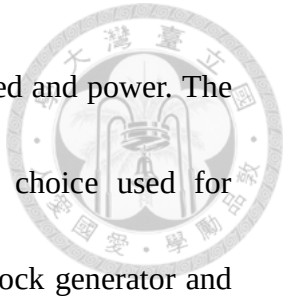

time-interleaved architecture can relax the tradeoff between the speed and power. The small area and energy-efficient SAR ADC is one of the best choice used for interleaved sub-ADCs. Nevertheless, the high-speed multi-phase clock generator and the complex timing skew calibration circuit consume large power dissipation [36]-[38] calibration. The high-speed and energy-efficient two-step SAR ADCs are selected for sub-ADCs. The sub-ADC utilizes the charge-sharing (CS) technique and self-triggered latch (STL) technique to achieve high-speed and low-power dissipation.

1.2 Thesis Organization

There are 6 chapters in this thesis. In chapter 1, the motivation and thesis organization are introduced briefly. In chapter 2, the fundamentals of Analog-to-Digital Converter are discussed. Besides, the commonly used high speed ADC architectures are described. In chapter 3, the error source of the time-interleaved ADC is reviewed. Then the proposed two-channel time-interleaved SAR ADC is presented to solve the timing skew problem of the time-interleaved ADC. Besides, the design consideration of the proposed high-speed and energy-efficient two-step SAR sub-ADC is present. In chapter 4, the circuit implementation of the proposed two-channel time-interleaved SAR ADC is present in detail. In chapter 5, the

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measurement results and measurement methods are presented. Finally, the conclusion and future work are discussed in chapter 6.

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Chapter 2 Fundamentals of Analog-to-Digital Converter

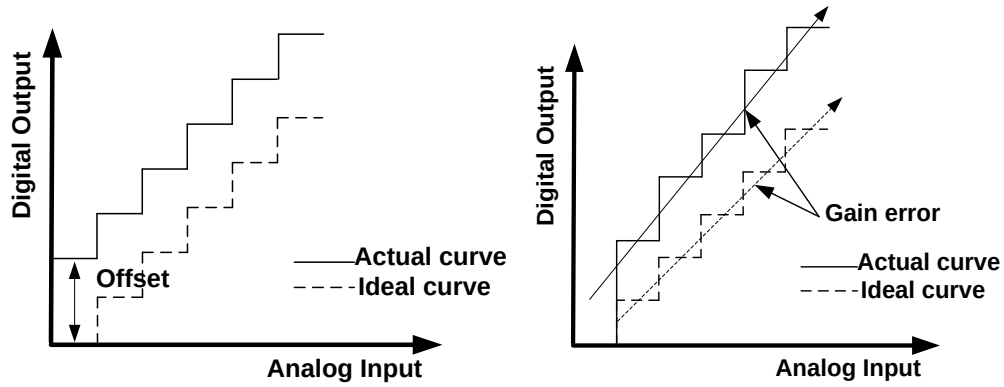
2.1 Introduction

ADC is used extensively in many applications such as portable devices and sensors. The different applications pay attention on different characteristics of ADC. In order to judge the performance of ADC, the performance metrics are defined in Section 2.2. Besides, the various architectures of ADC are introduced in Section 2.3.

2.2 Performance Metrics

2.2.1 Offset and Gain Error

Fig. 2.1 (a) shows the offset error in the transfer curve of ADC. The offset error is defined as the shift of the actual curve from the ideal curve. Fig. 2.1 (b) depicts the gain error in the transfer curve of ADC. The gain error is defined as the difference of the slope of the ideal curve and actual curve, where the offset error is removed.



(a) (b)

Fig. 2.1 ADC transfer characteristic with (a) offset and (b) gain error

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2.2.2 Differential and Integral Nonlinearity (DNL and INL)

Differential nonlinearity (DNL) is given as the difference between each step size of the actual ADC from the ideal width of 1 LSB, where the offset and gain error are removed. Therefore, DNL can be written as:

$$DNL = \frac{V_{n+1} - V_n}{V_{LSB}} - 1,\ 0 \le n \le (2^N - 1) \tag{2.1}$$

where V_n is the transition point of digital output code n, N is number bit resolution of ADC and V_{LSB} is the voltage level of 1LSB which equals to the ADC full scale amplitude divided by 2^N. Therefore, DNL is expressed in LSB. If each step size of the actual ADC is equal to 1 LSB, DNL is equal to zero. And, if digital output code *n* is never appeared, the corresponding DNL is equal to -1.

Integral nonlinearity (INL) is defined as the maximum deviation of the actual curve from the ideal curve and its unit is also expressed in LSB. The INL can be derived by integrating DNL from code 0 to code n. The plot describes DNL and INL is shown in Fig. 2.2.

$$INL(n) = \sum_{i=1}^{n} DNL(i) \tag{2.2}$$

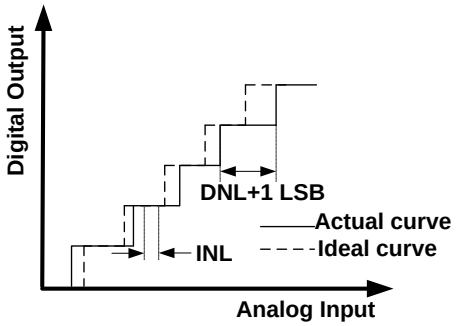

Fig. 2.2 DNL and INL in the ADC transfer characteristic

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2.2.3 Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is the ratio of the signal power (usually measured for a sine input) to the total noise power produced by quantization in the output code domain and the ADC circuitry in the band of interest. Quantization noise ε_q is a major noise source of ADC caused by the limited quantization levels. It means the difference of the analog input and the digital output. The waveform after the A/D conversion experiences both positive and negative quantization error. It can be assumed that the quantization noise ε_q is a random variable uniformly distributed between [–Δ/2, +Δ/2], where Δ is equal to 1 LSB. Thus, the noise power can be used to express the influence by quantization noise. The power of quantization noise can be expressed as

$$P_{\varepsilon q} = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} \varepsilon_q^2 \times d\varepsilon_q = \frac{\Delta^2}{12} \tag{2.3}$$

If input signal is a sinusoid wave with amplitude $\frac{V_{ref}}{2}$, the power of input signal is equal to

$$P_{in} = \frac{1}{T}\int_0^T \left(\frac{V_{ref}}{2}\sin(2\pi ft)\right)^2 \cdot dt = \frac{\left(2^N \cdot \Delta\right)^2}{8} \tag{2.4}$$

where f is the input frequency, N is the resolution of the ADC.

According to (2-3) and (2-4), SNR is generally expressed in dB as follows:

$$SNR\big|_{dB} = 10\log\left(\frac{P_{in}}{P_{\varepsilon q}}\right) = 10\log\left(\frac{3\cdot 2^{2N}}{2}\right) = 6.02N + 1.76 \tag{2.5}$$

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2.2.4 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the power of all the harmonics to the power of signal. The result is generally expressed in dB and it is usually a positive number. THD is an indication of nonlinearity while harmonics are dominated by the repetitive error sources in the convertor. The plot presents THD is shown in Fig. 2.3 and THD is expressed as follows:

$$THD\big|_{dB} = 10\log\left(\frac{P_{hd}}{P_{in}}\right) \tag{2.6}$$

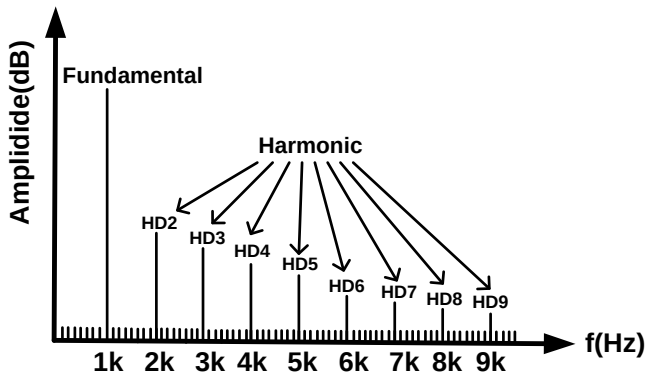

Fig. 2.3 Total harmonic distortion in FFT spectrum

2.2.5 Spurious Free Dynamic Range (SFDR)

The spurious-free dynamic range (SFDR) is the ratio of the signal power to the largest spurious in the frequency domain. SFDR means how well an ADC can detect a very small signal simultaneously in the presence of a very large signal. It is one of the crucial requirements in the wireless communication application. The plot presents SFDR is shown in Fig. 2.4 and SFDR can be defined as:

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$$SFDR|_{dB} = 10\log\left(\frac{P_{in}}{\text{The largest spurious power}}\right) \quad (2.7)$$

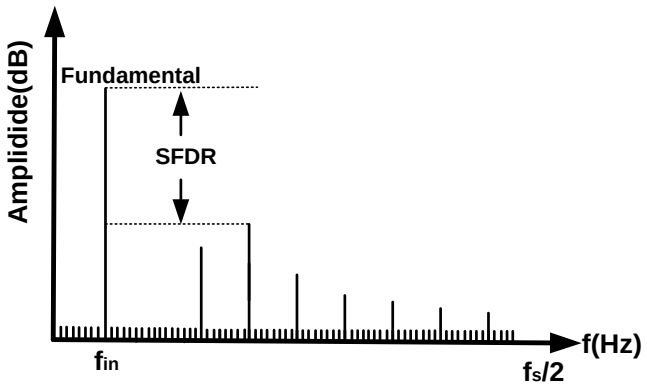

Fig. 2.4 Spurious free dynamic range in FFT spectrum

2.2.6 Signal to Noise and Distortion Ratio (SNDR)

Signal to noise and distortion ratio (SNDR) is the ratio of the signal power to the sum of total noise power and total harmonic distortion power. SNDR is written as:

$$SNDR|_{dB} = 10\log\left(\frac{P_{in}}{P_n + P_{hd}}\right) \quad (2.8)$$

2.2.7 Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is a measure based on the SNDR of an ADC converter. It describes the achieved resolution of ADC including noise and harmonic distortion. In equation (2-5), SNDR is replaced by SNR to calculate ENOB:

$$ENOB|_{\text{bit}} = \frac{SNDR|_{dB} - 1.76}{6.02} \quad (2.9)$$

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2.2.8 Figure of Merit (FoM)

Figure of Merit (FoM) is a mixed performance metric for ADC based on the total power dissipation, sampling frequency and accuracy. It is used to judge the performance of ADC. There are two commonly used FoM definitions: Walden FoM and Schreier FoM.

$$Walden\ FoM = \frac{Total\ Power\ Dissipation}{F_s \times 2^{ENOB}} \tag{2.10}$$

$$Schreier\ FoM = SNDR\big|_{dB} + 10\log\left(\frac{F_s/2}{Total\ Power\ Dissipation}\right) \tag{2.11}$$

Walden FoM is suitable for low-resolution designs. Schreier FoM is suitable for high-resolution designs that also push bandwidth. In this thesis, Walden FoM is used to compare this work with previous works and state-of-the-art.

2.3 ADC Architectures

ADC can be classified into two types, Nyquist rate ADC and oversampling ADC. The sampling rate of Nyquist rate ADC is slightly larger than twice the input bandwidth, which allows the accuracy reproduction the original waveform.

For an oversampling ADC, the signal is sampled many times with a sampling frequency such higher than Nyquist rate to remove the noise outside the band of interest to improve the accuracy. In the following section, several Nyquist rate ADC architectures are discussed for high-speed application.

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2.3.1 Flash Architecture

Fig. 2.5 shows the normal architecture of flash ADC. It is composed of $2^N - 1$ comparators, a resistor ladder and a decoder, where N represents the resolution of ADC. The resistor ladder consists of 2^N equal segments and provides 2^N voltage level for comparison. The operation process is that the comparators compare the input signal with these voltage levels simultaneously and generate the comparator outputs. The comparator outputs are in the form of the thermometer code and converted to binary code by the decoder. Consequently, the flash ADC has the smallest latency time than other architectures for the single-channel ADC.

However, flash ADC suffers from the input-referred offset of comparators and the exponential growing area when its resolution rises up. Pre-amplifier and average network are commonly used to solve the problem of the input-referred offset. Besides, interpolation technique is proposed to reduce the hardware area caused by numerous comparators [16]. Nevertheless, the flash ADC still consumes large power dissipation.

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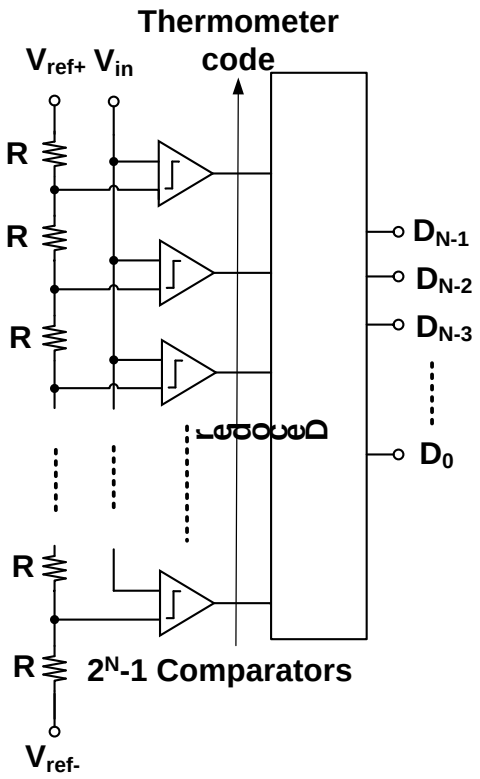

Fig. 2.5 Flash architecture

2.3.2 Pipelined Architecture

Fig. 2.6 depicts the block diagram of pipelined ADC. It consists of a series of identical stages separated by a sample-and-hold amplifier (SHA) where SHA is the part of sub-stage. If the resolution of the sub-stage is M-bit, it generates the M-bit digital output and a residue voltage for the next stage. The residue voltage will be amplified for the next stage by the residue amplifier. Compared with flash architecture, the number of the comparators can be reduced because the residue is amplified to full-scale. By utilizing the pipelined architecture, the latency can be greatly reduced and it can achieve the high conversion rate.

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However, the bottleneck of the pipelined ADC is the high-bandwidth but power-hungry residue amplifiers in the sub-stages. The residue amplifiers consume large power dissipation to achieve the speed and accuracy requirements.

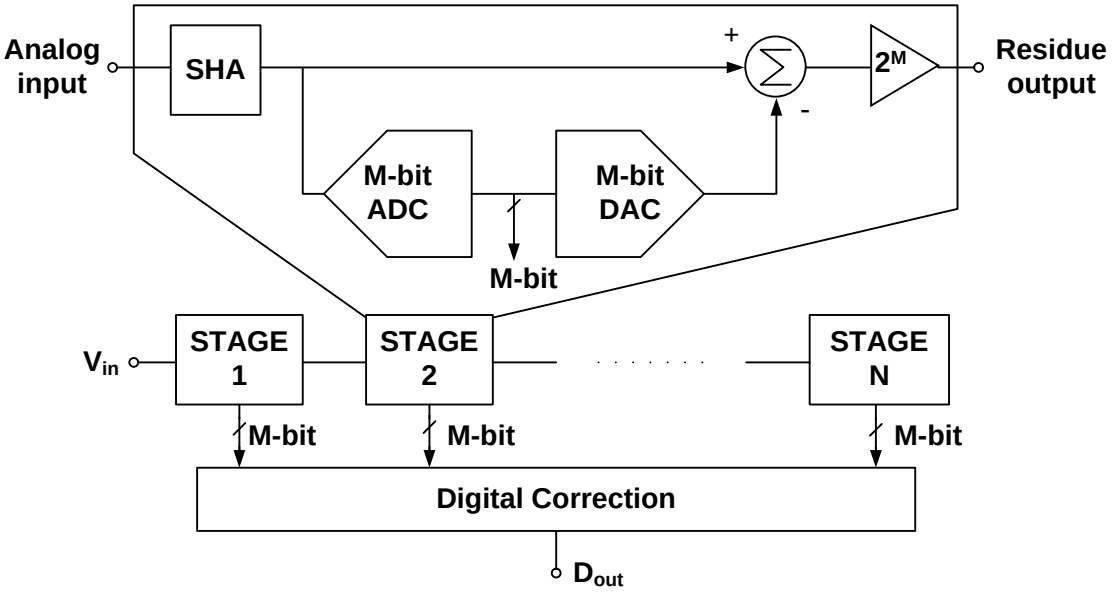

Fig. 2.6 Pipelined ADC architecture

2.3.3 Successive-Approximation-Register (SAR) Architecture

Recently, successive-approximation-register (SAR) ADC becomes popular with the advanced CMOS process because most parts of SAR ADC are digital circuits. Fig. 2.7 shows the block diagram of the successive-approximation-register (SAR) ADC. SAR ADC consists of a sampling DAC, a comparator, loop delay cells and the SAR logic.

The operation process is that input signal is sampled on the sampling DAC, and then the comparator regenerates input signal and generates the comparator results.

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The comparator results are delivered to the SAR logic and the DAC. The SAR logic stores the comparator results and the DAC sets the corresponding switching for the following SAR conversion. Thanks to the SAR algorithm and the simple architecture without residue amplifier, it results in the good power-efficiency and small area. Furthermore, the offset issue caused by the comparator doesn't degrade the linearity of the SAR ADC. The offset can be removed in the digital domain.

However, in the N-bit conventional SAR ADC, the latency is very long because it needs to regenerative input signal for N times in one data conversion. The speed of SAR ADC is limited by the regeneration time of the comparator and the digital loop delay time. It results in the long latency which is N times larger than the flash architecture.

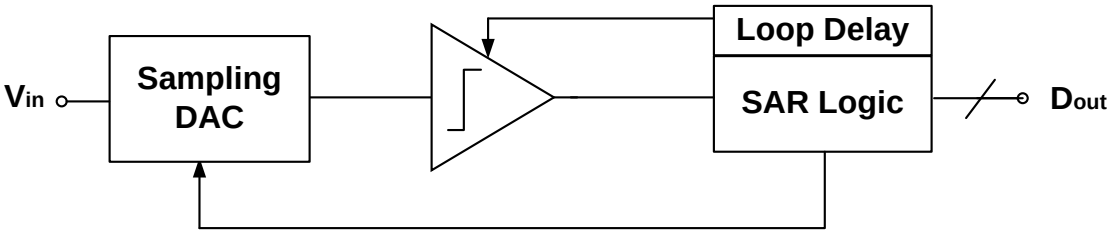

Fig. 2.7 SAR ADC architecture

2.3.4 Pipelined-SAR Architecture

Fig. 2.8 shows the block diagram of a Pipelined-SAR ADC[11]. The block diagram of the pipelined-SAR ADC consists of two stages of SAR ADCs and an inter-stage residue amplifier. Combining the high conversion rate of pipelined ADC

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and the energy efficiency of SAR ADC, the pipelined-SAR ADC gets the advantages from these two architectures.

The operation process is that the 1st stage SAR ADC samples input signal and then resolves the MSB decision. After the MSB decision, the residue is stored on the 1st stage SAR ADC and be delivered to the 2nd stage SAR ADC by the residue amplifier. Thus, the 2nd stage SAR ADC resolves the LSB decision of the previous input signal and the 1st stage SAR ADC samples the next input signal.

But, a low-noise high-bandwidth residue amplifier is not only power-hungry, but also hard to design in advanced CMOS process.

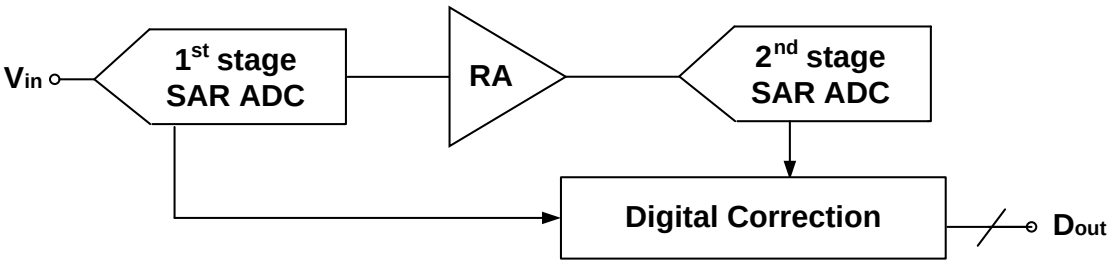

Fig. 2.8 Pipelined-SAR ADC architecture

2.3.5 Time-Interleaved Architecture

Time-interleaved (TI) ADC is the most intuitive method to increase FS by paralleling many sub-ADC channels. Fig. 2.9 shows the block diagram of time-interleaved ADC. Time-interleaved ADC consists of the clock generator and M channels sub-ADCs, which perform as the single channel ADC and can be implemented by any ADC architecture such as flash, pipelined or SAR.

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The operation process is that the clock generator generates Clk1 to ClkM, which trigger M channels sub-ADCS to sample input signal and perform the conversion. When the conversion of the sub-ADCs is finished, the conversion results are realigned and delivered to the output. Fig. 2.10 shows the timing diagram of time-interleaved ADC.

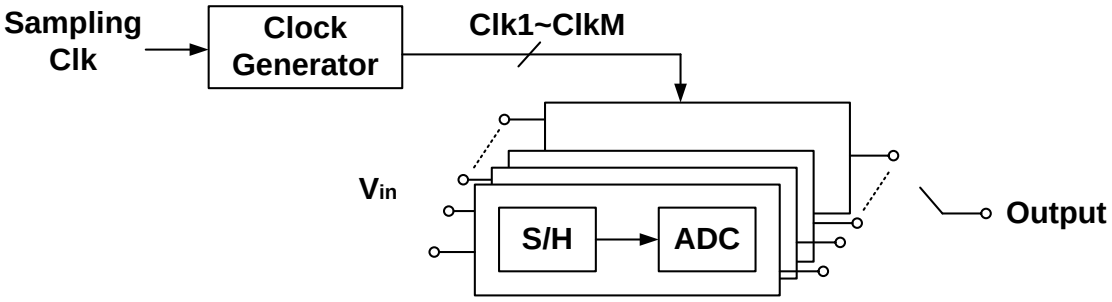

Fig. 2.9 Time-interleaved ADC architecture

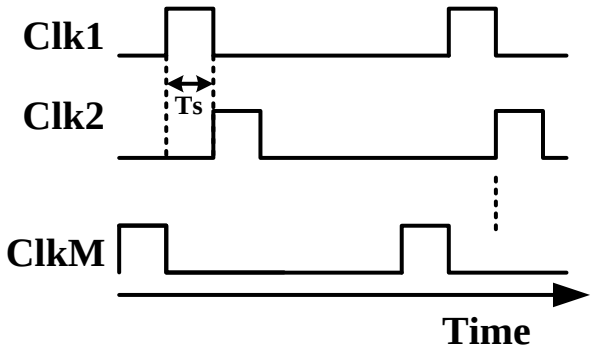

Fig. 2.10 Timing diagram of time-interleaved ADC

The small area and energy-efficient SAR ADC is one of the best choice used for interleaved sub-ADCs. Accordingly, by paralleling many sub-ADC channels, time-interleaved ADC can relax the tradeoff between the speed and power. Nevertheless, the high-speed multi-phase clock generator consumes large power dissipation when the number of sub-ADC channels grows.

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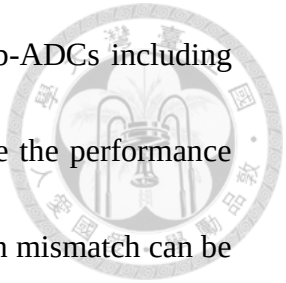

Besides, the channel mismatches between the M channel sub-ADCs including the offset mismatch, gain mismatch and skew mismatch deteriorate the performance of time-interleaved ADC. Although the offset mismatch and the gain mismatch can be calibrated without complex calibration [8], the timing skew mismatch degrades of time-interleaved ADC and needs complicated calibration circuit to eliminate the timing skew mismatch.

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Chapter 3 Time-Interleaved SAR ADC

3.1 Introduction

This chapter will describe the proposed time-interleaved SAR ADC. First, the error sources in time-interleaved ADC will be discussed in Section 3.2. After understanding the error sources in time-interleaved ADC, the proposed low-skew demultiplexer will be described in Section 3.3. In Section 3.4, the two-step SAR sub-ADC architecture is elaborated. The design consideration of the time-interleaved SAR ADC will be discussed and analyzed. Finally, the summary will be discussed in Section 3.6.

3.2 Error Sources in Time-Interleaved ADC Architecture

3.2.1 Offset Mismatch

Fig. 3.1 shows a two-channel ADC with offset mismatch. The two sub-ADCs are identical except for the offset voltages V_{osi}, where i represents 1 or 2. The different offset voltages V_{osi} cause the offset of the transfer characteristic of time-interleaved architecture, as shown in Fig. 3.2.

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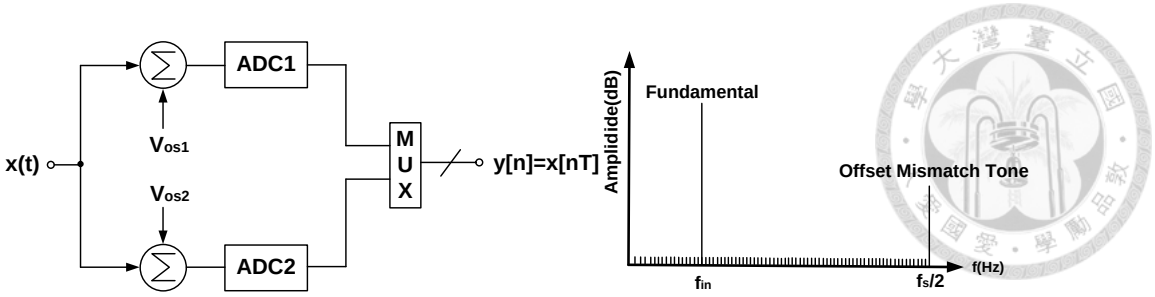

Fig. 3.1 Time-interleaved architecture with offset mismatch

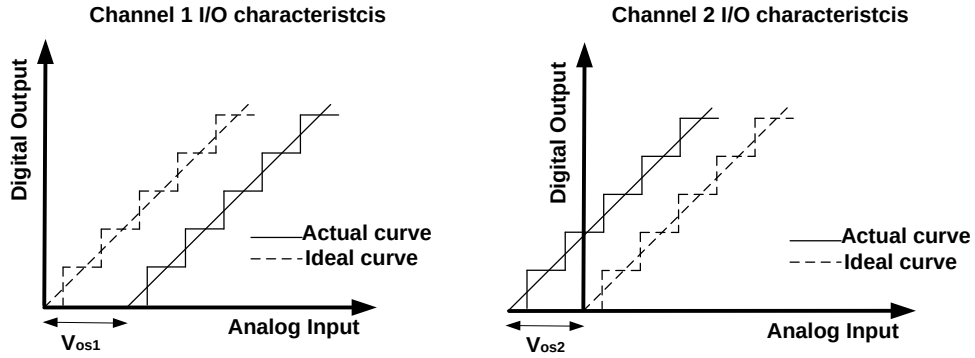

Fig. 3.2 Transfer characteristic of time-interleaved architecture with offset mismatch

A mathematical analysis of the output of the time-interleaved ADC with only offset mismatch is derived in the following equation. A two-channel time-interleaved ADC is taken for the example. The output of the time-interleaved ADC [9] in Fig. 3.1 with a sinusoidal input $x(t) = \cos(2\pi f_{in} nT_s)$ is

$$y[n] = \cos(2\pi f_{in} nT_s) + V_{os1}, n = even \tag{3.1}$$

$$y[n] = \cos(2\pi f_{in} nT_s) + V_{os2}, n = odd \tag{3.2}$$

Let $V_{os} = \frac{(V_{os1} + V_{os2})}{2}$ and $\Delta V_{os} = V_{os1} - V_{os2}$. Then the output of the time-interleaved ADC can be given as

$$y[n] = \cos(2\pi f_{in} nT_s) + V_{os} + (-1)^n \frac{\Delta V_{os}}{2} \tag{3.3}$$

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Using $(-1)^n = \cos(\frac{2\pi f_s n T_s}{2})$, (3.3) can be written as

$$y[n] = \cos(2\pi f_{in} n T_s) + V_{os} + \frac{\Delta V_{os}}{2} \cos\left[2\pi (\frac{f_s}{2}) n T_s \right] \quad (3.4)$$

The second and third terms in (3.4) validates that the different offset voltage of the time-interleaved ADC give a dc value and a periodic additive pattern in the output of the time-interleaved ADC. In frequency domain, the different offset voltages V_{osi} cause a distortion tone at $f_s / 2$.

Generally, for an M-channel time-interleaved ADC, the distortion caused by offset mismatch is signal independent and appears at

$$f_{noise} = k \cdot f_s / M, k = 0,1,...,M-1 \quad (3.5)$$

The noise power caused by offset mismatch can be expressed as

$$P_{noise} = \sigma_{offset}^2 \quad (3.6)$$

where the channel offset mismatches are Gaussian random variables with zero mean, and σ_{offset} is the standard deviation of offset mismatch.

3.2.2 Gain Mismatch

Fig. 3.3 shows a two-channel ADC with gain mismatch. The two sub-ADCs are identical except for the gain of each channel A_i, where i represents 1 or 2. The different gains of each channel A_i cause the difference of the slope of the transfer characteristic of time-interleaved architecture, as shown in Fig. 3.4.

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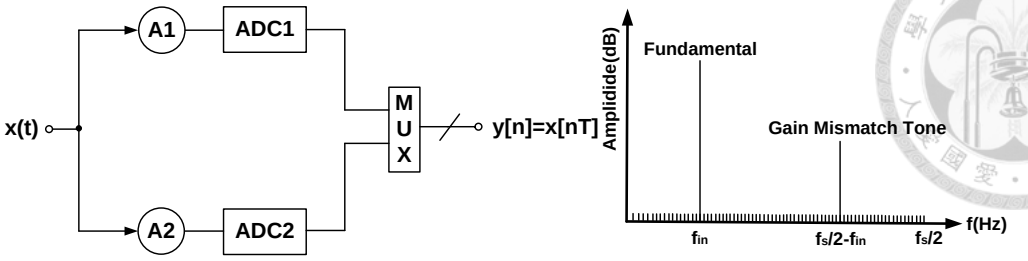

Fig. 3.3 Time-interleaved architecture with gain mismatch

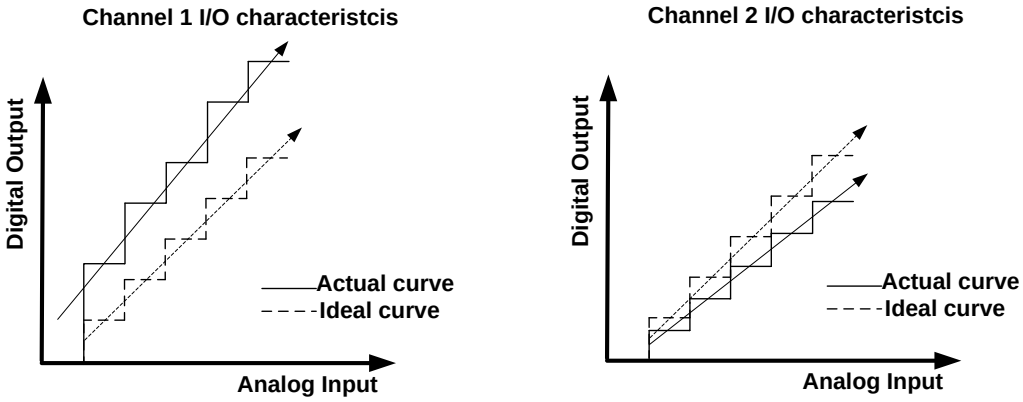

Fig. 3.4 Transfer characteristic of time-interleaved architecture with gain mismatch

A mathematical analysis of the output of the time-interleaved ADC with only gain mismatch is derived in the following equation. A two-channel time-interleaved ADC is taken for the example. The output of the time-interleaved ADC [9] in Fig. 3.3 with a sinusoidal input $x(t) = \cos(2\pi f_{in} nT_s)$ is

$$y[n] = A_1 \cos(2\pi f_{in} nT_s), n = even \tag{3.7}$$

$$y[n] = A_2 \cos(2\pi f_{in} nT_s), n = odd \tag{3.8}$$

Let $A = \frac{(A_1 + A_2)}{2}$ and $\Delta A = A_1 - A_2$. Then the output of the time-interleaved ADC can be given as

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$$y[n] = \left[A + (-1)^n \frac{\Delta A}{2} \right] \cos(2\pi f_{in} n T_s) \tag{3.9}$$

Using $(-1)^n = \cos(\frac{2\pi f_s n T_s}{2})$, the (3.9) can be written as

$$y[n] = A\cos(2\pi f_{in} n T_s) + \frac{\Delta A}{2} \cos\left[2\pi (f_{in} - \frac{f_s}{2}) n T_s \right] \tag{3.10}$$

In (3.10), the first term is the scaled input and the second term is the image due to channel gain mismatch. The second term in (3.10) shows that the image amplitude is proportional to the gain error ΔA. In frequency domain, the different gain of each channel A_i cause a distortion tone at $f_s / 2 - f_{in}$.

In general, M-channel time-interleaved ADC, the distortion caused by gain mismatch occurs at

$$f_{noise} = \pm f_{in} + k \cdot f_s / M, k = 0,1,...,M-1 \tag{3.11}$$

The noise power caused by gain mismatch can be expressed as

$$P_{noise} = \left(A \cdot \sigma_{gain} \right)^2 \tag{3.12}$$

where A is the amplitude of a sine input and the channel gain mismatches are Gaussian random variables, and σ_{gain} is the standard deviation of gain mismatch.

3.2.3 Timing Skew Mismatch

Fig. 3.5 shows a two-channel ADC with timing skew mismatch. The two sub-ADCs are identical except for the skewed CLK_i, where i represents 1 or 2. The skewed CLK_i causes the different sampling time shift of the time-interleaved

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architecture, as shown in Fig. 3.6. The error caused by the timing skew is terrible when the input signal has large slew rate. That is, the error is signal-dependent and serious with high frequency input signal.

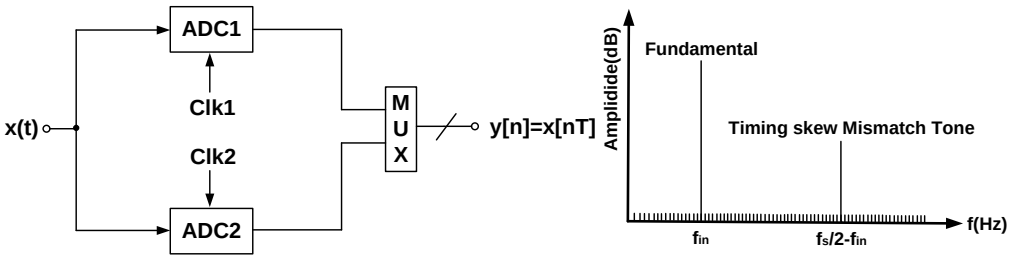

Fig. 3.5 Time-interleaved architecture with timing skew mismatch

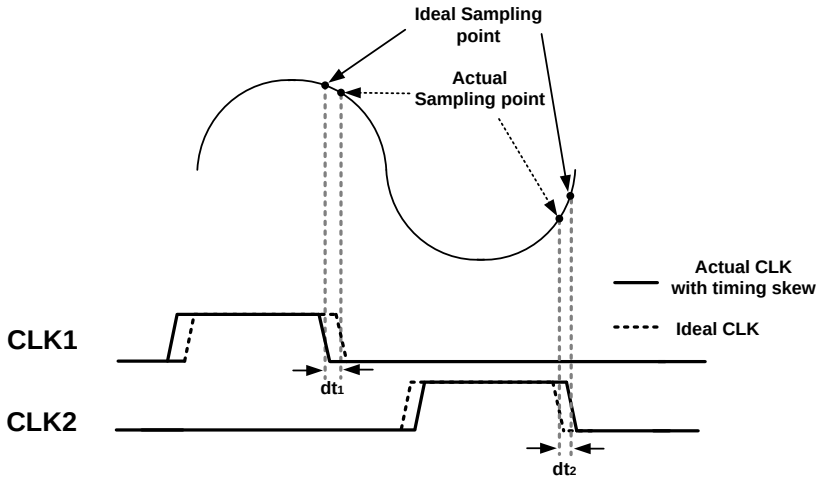

Fig. 3.6 Time-interleaved architecture with timing skew mismatch

A mathematical analysis of the output of the time-interleaved ADC with only timing skew mismatch is derived in the following equation. A two-channel time-interleaved ADC is taken for the example. Assuming that ADC1 samples input signal at a time $T_s + \Delta t$ after ADC2, where Δt is the timing skew deviated from ideal timing, so the combination of the two channels samples the input signal at times

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$nT_s + \frac{\Delta t}{2} - (-1)^n \frac{\Delta t}{2}$. The output of the time-interleaved ADC [9] in Fig. 3.5 with a sinusoidal input $x(t) = \cos(2\pi f_{in} nT_s)$ is

$$y[n] = \cos\left\{2\pi f_{in}\left[nT_s + \frac{\Delta t}{2} - (-1)^n \frac{\Delta t}{2}\right]\right\} \tag{3.13}$$

$$= \cos\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2})\right]\cos\left[(-1)^n 2\pi f_{in}\frac{\Delta t}{2}\right] + \sin\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2})\right]\sin\left[(-1)^n 2\pi f_{in}\frac{\Delta t}{2}\right] \tag{3.14}$$

Using the facts that cos(x) is an even function and sin(x) is an odd function, and $(-1)^n = \cos(n\pi)$,(3.14) can be given as

$$y[n] = \cos\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2})\right]\cos\left(2\pi f_{in}\frac{\Delta t}{2}\right) + \sin\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2})\right]\cos(n\pi)\sin\left(2\pi f_{in}\frac{\Delta t}{2}\right) \tag{3.15}$$

Using the facts that $\sin(a)\cos(n\pi) = \sin(a - n\pi)$, and $n\pi = \frac{2\pi f_s nT_s}{2}$, the output of the time-interleaved ADC can be given as

$$y[n] = \cos\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2})\right]\cos\left(2\pi f_{in}\frac{\Delta t}{2}\right) + \sin\left[2\pi f_{in}(nT_s + \frac{\Delta t}{2}) + \frac{2\pi f_s nT_s}{2}\right]\sin\left(2\pi f_{in}\frac{\Delta t}{2}\right) \tag{3.16}$$

$$= \cos\left(2\pi f_{in}\frac{\Delta t}{2}\right)\cos\left[2\pi f_{in}nT_s + 2\pi f_{in}\frac{\Delta t}{2}\right] + \sin\left(2\pi f_{in}\frac{\Delta t}{2}\right)\sin\left[2\pi\left(f_{in} - \frac{f_s}{2}\right)nT_s + 2\pi f_{in}\frac{\Delta t}{2}\right] \tag{3.17}$$

In (3.17), the first term is input signal which phase shift is $2\pi f_{in}\frac{\Delta t}{2}$, and the second term shows that the image is 90° out of phase with the image due to gain mismatch in (3.10). The added phase shift $2\pi f_{in}\frac{\Delta t}{2}$ results from the average delay of

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$\frac{\Delta t}{2}$ caused by the timing skew mismatch of Δt. In frequency domain, the distortion which is caused by the skewed CLK_i results in a distortion tone at $f_s/2-f_{in}$. It represents that the error signal with a period of M/f_s is modulated by input frequency f_{in}.

For an M-channel time-interleaved ADC, the distortion caused by timing skew mismatch occurs at

$$f_{noise} = \pm f_{in} + k \cdot f_s / M, k = 0,1,...,M-1 \tag{3.18}$$

The noise power caused by timing skew mismatch can be expressed as

$$P_{noise} = \left(A \cdot 2\pi f_{in} \cdot \sigma_{skew}\right)^2 \tag{3.19}$$

where A is the amplitude of a sine input and the channel timing skew mismatches are Gaussian random variables with zero mean, and σ_{skew} is the standard deviation of timing skew. As a result, SNDR can be approximated as [35],

$$SNDR \cong 20 \cdot \log\left(\frac{1}{\sigma_{skew} 2\pi f_{in}}\right) - 10\log\left(1-\frac{1}{M}\right) \tag{3.20}$$

For an 8 bit 1.5GS/s time-interleaved ADC with the Nyquist rate input frequency, σ_{skew} should be less than 1ps to fit in with the 8-bits requirement. Such a good timing matching is difficult to realize in modern CMOS process.

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3.3 Proposed Low-Skew Demultiplexer Architecture

3.3.1 Principle

There are some methods to solve the problem of timing skew mismatch without complicated timing skew calibration.

A global S/H and a source follower are used in [4] to solve the skew issue. The static power consumption of the source follower cannot be overlooked with its heavy-loading and high-linearity characteristics. Besides, in order to provide full-swing inputs for the sub-ADCs, it also needs another higher-than-nominal supply voltage, which worsens the FoM performance.

The channel-selection-embedded bootstrap circuit [5] is reported to replace the power-hungry source follower [4]. However, it takes different discharging paths for two bootstrap channels, which suppresses its low-skew feature. The stored sampled signal is also hard to pass another set of bootstrap switch without re-buffering.

The low-skew demultiplexer (De-MUX) is proposed to suppress the skew issue without the complicated timing skew calibration or the power-hungry source follower. The proposed low-skew De-MUX combines the global clock signal with the bootstrap circuit. Even though the clock signal of each channel is skewed, the actual sampling timing of each channel is aligned with global clock signal. Besides, the proposed low-skew De-MUX takes the common discharge path of each channel. It results in the

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low-skew characteristic because the sampling timing is dependent on global clock signal. Besides, the common discharge path of each channel ensures the skew issue can be suppressed furthermore. Therefore, the timing skew of each channel will not cause the different sampling time shift of time-interleaved architecture.

3.3.2 Low-Skew Demultiplexer

Fig. 3.7 illustrates the block diagram of the overall ADC. It consists of two sub-ADCs, a 1-to-2 low-skew De-MUX, a shared clock generator, an offset calibration circuit and a 2-to-1 digital output multiplexer. Fig. 3.8 illustrates its timing diagram and the states of the sub-ADCs. The global clock, Φ_{CLK}, is divided by 2 to generate the control signals of sub-ADCs, Φ_1 and Φ_2.

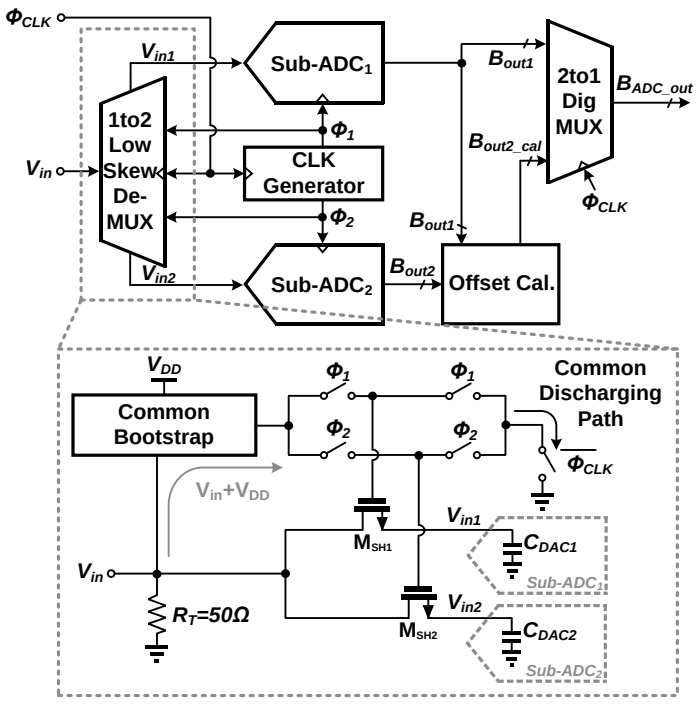

Fig. 3.7 Architecture of the proposed ADC with low-skew De-MUX

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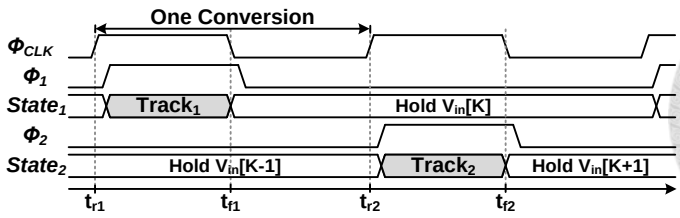

Fig. 3.8 Timing diagram of the proposed ADC

At the Track_1 phase, the gate of M_{SH1} is bootstrapped to $V_{in}+V_{DD}$ to make the turn-on resistance of M_{SH1} a small constant value. It increases tracking linearity of the low-skew De-MUX. On the other hand, the sub-ADC_2 is resolving the previous sampled signal, $V_{in}[K-1]$, at the Hold_2 phase. By using the common discharging path, the low-skew De-MUX suppresses the skew mismatch between the two sub-ADCs. It ensures that C_{DAC1} of the sub-ADC_1 holds $V_{in}[K]$, which is aligned with the falling edge of the global clock, Φ_{CLK}, at t_{f1}. Subsequently, the sub-ADC_2 tracks and holds the next input signal, $V_{in}[K+1]$, and so on. In contrast to Φ_1 and Φ_2, Φ_{CLK} is directly from the clock buffers, so it also has low-noise characteristic. It improves the accuracy of low-skew De-MUX.

A single-end schematic of the proposed low-skew De-MUX is shown in Fig. 3.9. Four major parts with sub-ADC sampling switches, M_{SH1} and M_{SH2}, in this De-MUX includes a common bootstrap circuit, a common discharging switch, constant-R_{on} cells and tie-low cells.

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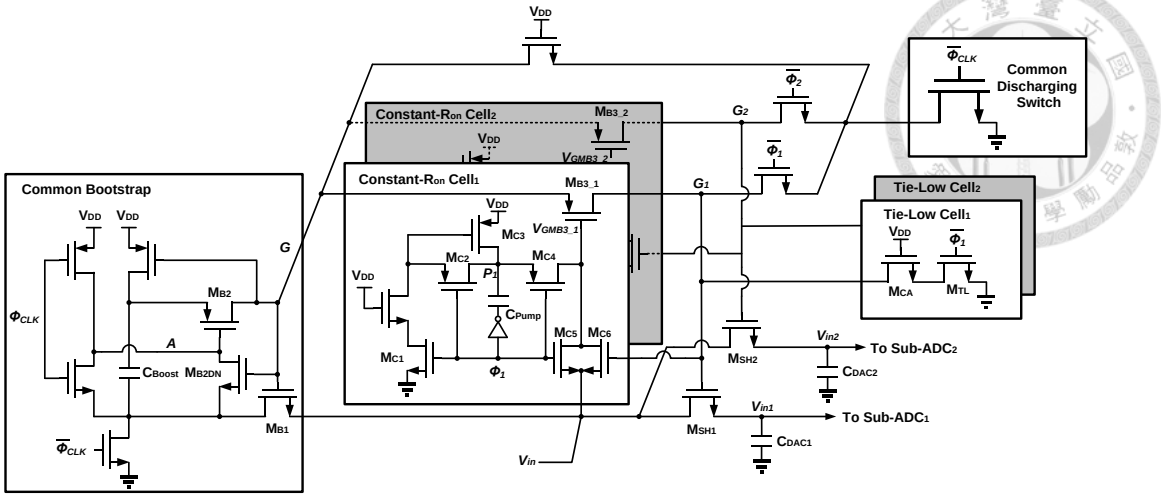

Fig. 3.9 Single-ended schematic of the proposed low-skew demultiplexer

The common bootstrap circuit uses C_{Boost} to boost node G to $V_{in}+V_{DD}$ at the $Track_i$ phases, which are depicted as the gray intervals in Fig. 3.8, where i either 1 or 2 for the ith channel. C_{Boost} resets its stored charge when Φ_{CLK} is low. The bootstrapped voltage on the node G is transferred to nodes G_i and it keeps the turn-on resistance (R_{on}) of M_{SHi} constant and independent of V_{in}. Since the two $Track_i$ phases between the two sub-ADCs are not overlapped, the bootstrap circuit can be shared by both channels. Thus, it reduces the number of C_{Boost} by half. In this work, the capacitance value of C_{Boost} is about 500fF and it dominates the area of the bootstrap circuit.

Φ_1 and Φ_2 are generated by a clock phase generator. It has large skew mismatch and bad noise performance. To suppress the skew sensitivity of Φ_1 and Φ_2, the low-skew De-MUX lets the nodes G_1 and G_2 use the same discharging path at the falling edge of Φ_{CLK}, which is t_{f1} and t_{f2} in Fig. 3.8, respectively. The sampled

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instance of M_{SHi} is synchronized by the falling edge of Φ_{CLK} at t_{f1} and t_{f2}. Thus, the sensitivity of skew mismatch between Φ_1 and Φ_2 can be reduced as long as the falling edge of Φ_{CLK} is precise.

To enhance the linearity of M_{SHi}, it is necessary to sustain the nodes G and G_i higher than V_{in} by V_{DD} at the $Track_i$ phase, as shown in Fig. 3.10.

The turn-on resistance of M_{SHi} can be derive as [24]

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{3.21}$$

Due to the common bootstrap and constant-R_{on} cell, V_{GS} of M_{SHi} is constant and it results in the turn-on resistance of M_{SHi} is signal-independent. Besides, R_{on} of the path from V_{in} to nodes G and G_i also requires to be signal-independent. The common bootstrap uses M_{B2DN} to let nodes A and G equal to V_{in} and $V_{in}+V_{DD}$, respectively, so that R_{on} of M_{B2}/M_{B1} is kept constant.

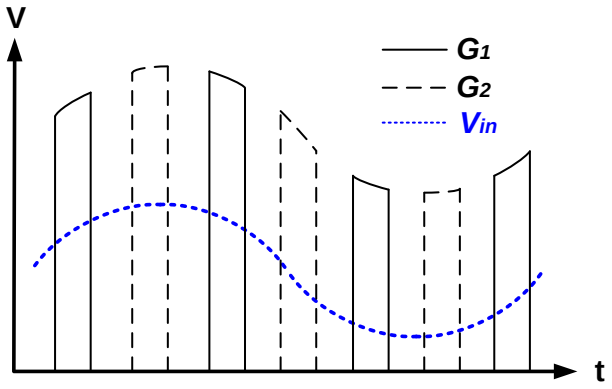

Fig. 3.10 Waveform of G_1, G_2, and Vin of low-skew De-MUX

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The gate of M_{B3_i} cannot be connected to ground at the $Track_i$ phase, because the V_{GS} of M_{B3_i} would become $-(V_{in}+V_{DD})$, which causes signal-dependent R_{on} of M_{B3_i}. The linearity of G_i is affected. Hence, the constant-R_{on} $cell_i$ is used to keep R_{on} of M_{B3_i} constant. It uses $M_{C5\text{-}6}$ to tie V_{GMB3_i} to V_{in} at the $Track_i$ phase and keeps V_{GS} of M_{B3_i} at $-V_{DD}$. To avoid corrupting the sampled signal on C_{DACi}, M_{B3_i} should block the bootstrapped voltage, $V_{in}+V_{DD}$, of the node G at the $Hold_i$ phase, so the constant-R_{on} $cell_i$ pumps V_{GSB3_i} to $2V_{DD}$, by using the $M_{C1\text{-}4}$ and C_{Pump}. All devices in the constant-R_{on} cells are allowed to use small sizes to save area and power, because it only needs to drive the parasitic capacitance of V_{GSB3_i}. In this work, C_{Pump} is designed to be 100fF. However, the V_{GS} or V_{DS} of $M_{C2\text{-}6}$ and M_{B3_i} in the constant-R_{on} cell are near $2V_{DD}$ during the hold phase. If the proposed ADC is used in product, there is a reliability issue in the low-skew De-MUX.

The common discharging switch requires a set of small-sized switches, tie-low cell, which is used to avoid a floating node at the $Hold_i$ phase. It would tie the node G_i to ground when common discharging switch is open. Because the tie-low cells are only used to define the floating nodes, the smallest channel width and length of M_{CA} and M_{TL} are selected in this work.

Two channels of sub-ADCs share the same clock phase generator [3] without any waste of power and area. It is well-known to accelerate the conversion rate in

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high-speed single-channel SAR ADCs by prolonging the conversion phase up to 75% of the clock period. However, it requires twice the clock frequency to generate the quarter phase. It doubles the power consumption of the clock phase generator for only single-channel usage. Fortunately, it is advantageous to utilize this quarter clock generator, which can be shared to generate Φ_1 and Φ_2, for the two-channel SAR ADC.

3.4 Proposed Two-Step SAR Sub-ADC Architecture

3.4.1 Charge sharing technique

The choice of the sub-ADC is important for time-interleaved ADC. The small area and energy-efficient SAR ADC is one of the best choice used for interleaved sub-ADCs. There are various methods to expedite SAR ADCs, such as Multi-bit per cycle [5], [8] or multi-comparator [2], [10] technique which reduces digital loop time to enhance the speed of SAR ADCs. However, the offset mismatch of comparators needs foreground calibration and the kickback noise among comparators deteriorates its accuracy. The opamp-based Pipelined-SAR ADC [18]-[20] or pseudo differential source follower [21] was proposed to enhance the conversion rate of SAR ADC. But, the static current consumption degrades the FoM performance.

One of the two-step SAR architecture [1] was proposed to enhance the conversion rate of SAR ADC. It consists of a coarse stage and two fine stages. During

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the sampling phase and the MSB conversion phase, the coarse stage and one of the fine stages are connected by the switches. After finishing the MSB conversion, the coarse stage and one of the fine stages are isolated by the switches between the coarse and fine stages. Then one of the fine stages starts to resolve the residue. Simultaneously, the coarse stage connected to the other fine stage for sampling next input signal. By utilizing this two-step architecture [1], it can enhance the conversion rate. But, the switch mismatch between the coarse stage and the two fine stages results in the serious bandwidth mismatch. During the sampling phase, the coarse and fine stages sample different input signal due to the different input bandwidth of sampling network, which also causes the terrible bandwidth mismatch.

The proposed energy-efficient two-step SAR sub-ADC is shown in Fig. 3.11. Since its timing arrangement is similar to that of pipelined-SAR ADCs, it can achieve high conversion rate. Rather than using a power-hungry residue amplifier, the charge sharing technique is used to reduce the power consumption of analog-part circuitry.

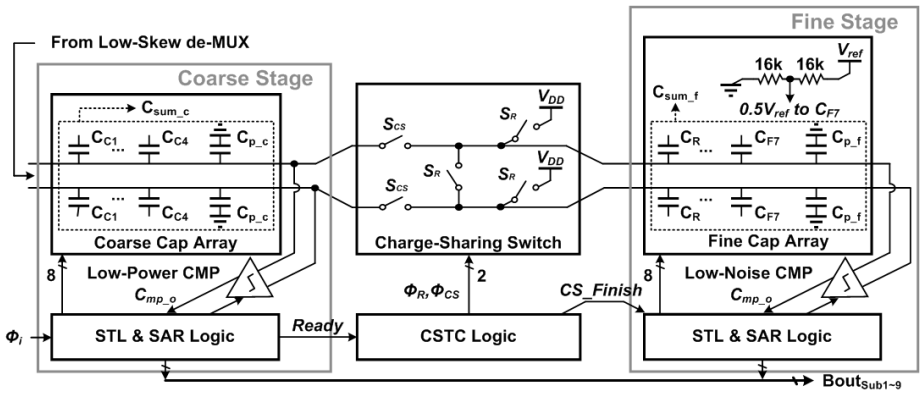

Fig. 3.11 Block diagram of sub-ADC with STL technique

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In order to transfer the residue from the coarse stage to the fine stage, the proposed charge sharing technique is used to transfer the residue passively. Besides, it is also immune from the output voltage headroom and linearity issues.

The proposed SAR sub-ADC comprises a coarse stage, a fine stage, a set of charge sharing switches and charge sharing timing control (CSTC) logic. The coarse and fine stages are connected by the charging sharing switches which include PMOS sharing switches S_{CS} and reset switches S_R. The set of charge sharing switches are controlled by the charge sharing timing control signals Φ_{CS} an Φ_R which are generated by the CSTC logic. Both the coarse and fine stages consist of the proposed STL SAR logic, a capacitor array, a dynamic comparator and loop delay logic. C_{p_c} and C_{p_f} are the whole parasitic capacitance at the top plates of coarse and fine capacitor arrays, respectively. The coarse capacitor array with capacitors [C_{C1} C_{C2} C_{C3} C_{C4}], which equal to [64C 32C 16C 8C], resolves the MSBs, where C is the unit capacitance. The fine capacitor array with capacitors [C_R C_{F5} C_{F6} C_{F7}], which equal to [4C 2C C C], provides the small voltage swing for the residue voltage to resolve the LSBs. The C_R in the fine capacitor array is used for one-bit redundancy [22].

The timing diagram of the proposed sub-ADC is illustrated in Fig. 3.12. During the sampling phase from t_1 to t_2, input signal $V_{in}[K]$ is sampled on the coarse stage by the low-skew De-MUX, where the K represents the K th sampling. After

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sampling the input signal, the low-skew De-MUX is turned off and the coarse stage starts to resolve first 4 MSB of $V_{in}[K]$.

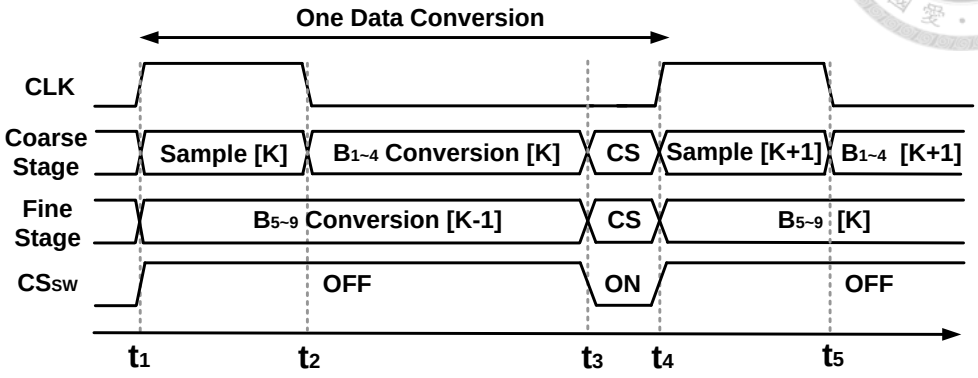

Fig. 3.12 Timing diagram of sub-ADC

During the conversion phase from t_2 to t_3, the coarse and fine stages utilize set-and-up switching method [23] to enhance the conversion rate. When both the coarse and fine stages finish their successive bit conversions, the residue is stored on the top plate of the two capacitor array. In order to prepare for the next charge sharing, the top plate of the fine stage capacitor array is reset to the power supply V_{DD} by S_R. Simultaneously, the bottom plate of the fine stage capacitor array is reset to the ground.

At t_3, the charge sharing timing control signals turn off the S_R and then turn on the S_{CS} to transfer the residue. As mentioned before, by utilizing the set-and-up switching method to a high level, the residue voltage on the coarse cap array is near to

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V_{DD}. Consequently, the charge sharing switches S_{CS} can be only PMOS instead of a transmission gate switch. It not only simplifies the switch design but also increases the conversion rate of the coarse and fine stages. Besides, the charge sharing technique can transfer the residue fast and be low power.

Next, when the CLK is high, charge sharing switches are turned off and the coarse stage starts to sample the next input signal $V_{in}[K+1]$. At the same time, the fine stage starts to resolve the rest of LSB of $V_{in}[K]$. Therefore, the two-step SAR ADC with charge sharing technique can achieve high conversion rate and low power dissipation. Unlike [1], the fine stage only samples the DC residue voltage from the coarse stage, the bandwidth mismatch of the S_{CS} will not cause the bandwidth mismatch tone.

The one-bit redundancy provides +/- 16LSB tolerance, which corrects errors including the offset mismatch between the coarse and fine stages, the large noise of the coarse comparator, the settling error of the coarse capacitor array. Therefore, this redundancy range makes the coarse stage faster and more energy-efficient. The coarse and fine stage could have different design for the speed and power optimization. The coarse stage uses a low-power comparator to resolve the first four MSBs. The one-bit redundancy relieves DAC settling requirement, so the loop delay time of the coarse stage is shorter than that of the conventional architecture. By utilizing the two-step

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architecture, the fine stage has sufficient time to resolve the rest of LSBs with a low-noise comparator. As a result of small voltage swing of the rest of conversion, the loop delay time of the fine stage can much shorter than that of the conventional architecture. It not only saves the power consumption but also increases the conversion rate of the ADC.

Based on the simulation results, the power of the coarse low-power comparator is more energy-efficient than that of the fine low-noise comparator by around 2.7 times in this work. The fine comparator only needs to resolves the rest of 5 comparisons, instead of the conventional 8 comparisons in a complete conversion. The analog power of ADC is saved by about 15% comparing with that of the conventional architecture [23].

Although the multiple reference architecture [1] could reduce the total size of the capacitor arrays and tune the switched voltage headroom of the fine stage, it requires multiple reference voltage generators (RVGs). The reference voltage is one of the most sensitive voltages in the ADC because any noise on the reference voltage would affect its resolution directly. The multiple reference architecture needs an extra strong but power-hungry RVG to suppress the noise on the reference voltage.

The resistor ladder technique [2] can use only one reference voltage to generate another reference voltage. A 32kΩ resistor ladder is used to generate $0.5V_{ref}$ for C_{F7}

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so that C_{sum_c} and C_{sum_f} are smaller than those of [3] by 2 times. Despite the fact that the $0.5V_{ref}$ increases the turn-on resistance of the bottom-plate switches, the $0.5V_{ref}$ generated by the resistor ladder is used for LSB in the fine stage.

Thanks to the resistor ladder, the ADC can use only one reference voltage. It can not only reduce the total capacitance of the coarse and fine stage, but also make the charge sharing technique faster. The speed consideration will be discussed in Sec. 3.5.5.

It is a remarkable fact that the total capacitance size of the coarse stage is designed to be equal to that of the fine stage to use only one reference voltage and to ensure proper switched voltage headroom of the fine capacitor array. The details will be explained in Sec. 3.5.4.1.

3.4.2 Self-Triggered Latch technique

Fig. 3.13(a) shows the loop control block diagram of the conventional asynchronous SAR ADC. It consists of loop delay cells, shift registers and latches [17]. The operation process is that the loop delay cells trigger the shift register to generate latch control signals, SRs. Then, SRs set the latches to store all the results of the comparator output C_{mp_o} [23]. N-bit asynchronous SAR ADC needs N stage shift

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registers and N latches. As a result, the capacitor loading of the comparator control signal LA is derived as

$$C_L = C_{p\_Loop} + N \times C_{DFF} \tag{3.22}$$

where C_{p_loop} is the parasitic capacitance on LA and C_{DFF} is the input capacitance of the shift register clock port. To regenerate N times, the loop would trigger the comparator N times. The dynamic power consumption of the loop delay cells is calculated as

$$PD_{CONV} = N \times C_L \times V_{DD}{}^2 \times f \tag{3.23}$$

where V_{DD} is the digital power supply voltage and f is the conversion frequency of the ADC. C_L is usually large. It increases the dynamic power dissipation and slows down the speed of the loop. The self-triggered latch (STL) technique is proposed as shown in Fig. 3.13(b). By removing the conventional shift-registers, this technique let the latch stage be self-triggered by the previous stage. The CLK signal triggers the loop delay cells and the first stage of STL. The first stage of STL starts to latch the comparator results C_{mp_o}. When the first latch stage is regenerative, it would trigger the next latch stage and so on. The loading capacitor C_{L_STL} on LA in the proposed technique is equal to C_{p_loop}, which is smaller than that of the conventional method. Although this technique adds two NAND gates per stage, their power dissipation is

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still smaller than one D-flip-flop. The dynamic power dissipation of the STL technique is calculated as

$$PD_{STL} = N \times C_{p\_Loop} \times V_{DD}{}^2 \times f \tag{3.24}$$

Based on the post-layout simulation results, the STL technique saves 20% digital power and 50% digital area. It makes the ADC faster and more energy-efficient. Fig. 3.14 shows the timing diagram of the STL technique.

When LA rises at t_A, the comparator starts to regenerate the input signal. The comparison is finished and Done rises at t_B. The time from t_A to t_B is defined to be T_{CMP}. Done takes the duration of T_{Loop} to go through the loop delay cells and then pulls LA to a low level from t_B to t_C. At the same time, the latch starts to latch the comparator results C_{mp_o} and uses T_{Latch} from t_B to t_D. When the latch is finished at t_D, it uses T_{STL} which is two NAND gate delay to pull up STL and opens the next latch. The comparator reset time takes the duration of T_{Rst} from t_C to t_E. To make the STL technique operate normally, the following criterion should be held.

$$T_{Loop} + T_{Rst} < T_{Latch} + T_{STL} \tag{3.25}$$

where T_{Loop} is the delay of one high-speed NAND gate and one inverter. T_{STL} is the delay of two small-sized NAND gates. T_{Rst} is also shorter than T_{Latch}, because T_{Rst} does not require regenerative operation. Accordingly, they can be designed to guarantee no timing issue in the STL technique.

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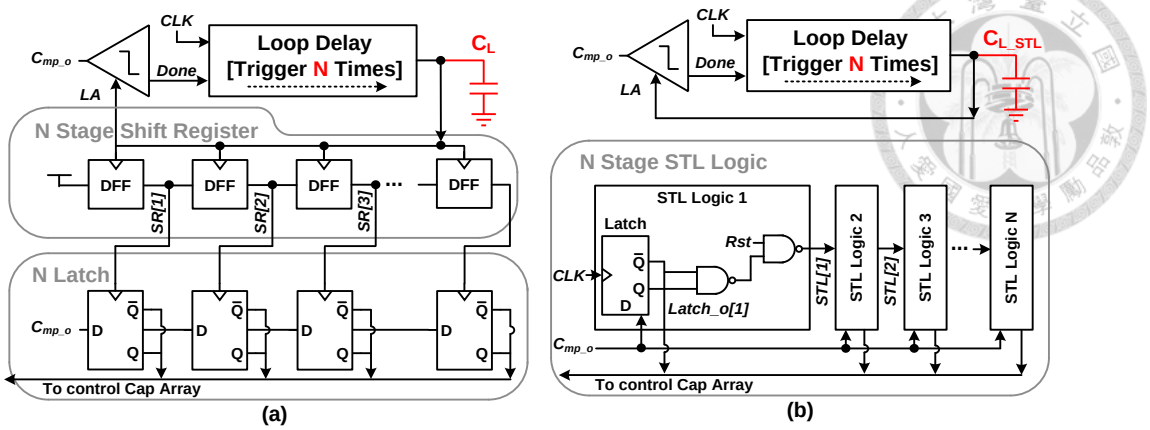

Fig. 3.13 (a) The conventional method (b) the proposed STL technique

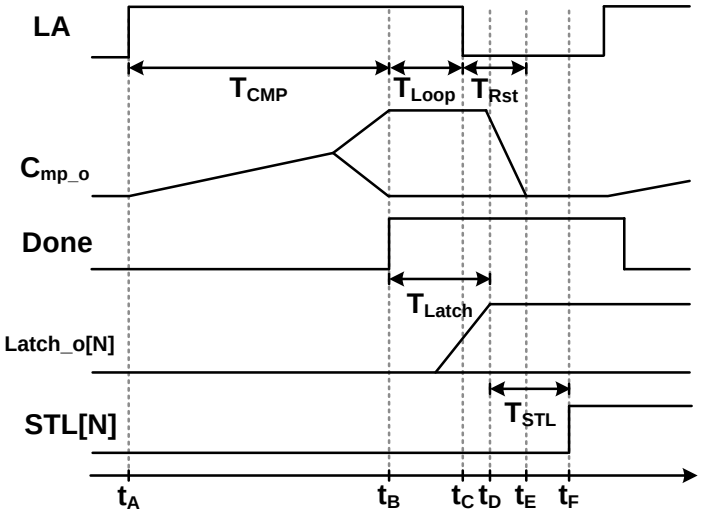

Fig. 3.14 Timing diagram fo STL technique

3.5 Design Consideration

3.5.1 Offset Mismatch Error

The offset mismatch error of the proposed time-interleaved two-step SAR ADC includes the offset mismatch between the sub-ADCs and the offset mismatch error between the coarse and fine stages. The offset mismatch between the sub-ADCs can be calibrated in digital domain. Assuming that the offset voltage of the sub-ADC is

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zero and the input signal is periodical, the averaged digital output is equal to its mid value. The same rule applies to other sub-ADCs suffered from the offset mismatch, and the corresponding averaged digital output is not equal to its mid value. The offset voltage of each channel can be derived by collecting the averaged digital output of each channel and subtracting the mid value. Then the residues can be compensated to the digital output of the corresponding channels.

However, the offset mismatch between the coarse and fine stages cannot be calibrated in digital domain, which results in the serious distortion. The comparator offset between the coarse and fine stages is the main factor. As mentioned in Section 3.4, the one-bit redundancy provides +/- 16LSB tolerance. It provides the code overlapping between the coarse and fine stages, which correct the offset mismatch between the coarse and fine stages. As long as the offset mismatch between the coarse and fine stages is smaller than the redundancy cover range, it will not degrade the linearity of sub-ADCs.

3.5.2 Gain Mismatch Error

The gain mismatch error of the proposed time-interleaved two-step SAR ADC includes the gain mismatch error between the sub-ADCs and the gain mismatch error between the coarse and fine stages. The gain mismatch error between the sub-ADCs

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can be calibrated background in digital domain [8][11]. However, the gain mismatch error between the coarse and fine stages cannot be calibrated in the digital domain, which will cause the serious distortion.

The capacitor mismatch between C_{sum_c} and C_{sum_f} is the main factor. In this work, the mismatch sigma σ of unit switched capacitor is around 1% with a unit capacitance of 1fF. It is an extrapolated result of the fabrication process datasheet. To equalize the gain of the coarse and fine stages, most of C_{p_c} and C_{p_f} are made up of the same architecture with unit capacitance. The other parasitic capacitance of routing metal is relatively smaller so that it can be neglected in this work. Thus, the unit capacitor mismatch of C_{p_c} and C_{p_f} is also assumed to be 1%. Based on the result of 10,000 Monte Carlo simulations, ENOB can reach around 7.9 bits for 3σ variation in this time-interleaved ADC. It indicates that the gain mismatch error caused by the parasitic capacitance mismatch is negligible in this work. Similar to [27]-[29], it also claims that the gain mismatch error can be neglected for medium resolution ADC.

3.5.3 Switching Method

The switching method of ADC is related to the conversion speed, comparator noise, and the switch type of the charge sharing technique. The variation of input common-mode voltage during the conversion is related to the switching method. The V_{CM}-based switching method [30] or the split-and-monotonic switching method [22]

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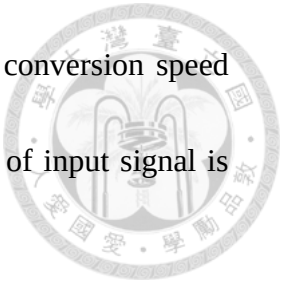

can keep the input common-mode voltage constant. However, the conversion speed during the LSB conversion becomes slower because the difference of input signal is shrunk gradually by SAR algorithm.

The monotonic switching method [23] is used to enhance the conversion speed. Based on [31], assuming that the comparator with N-type input pair is select, the higher input common-mode voltage makes the comparator delay time shorter. It is useful for high-speed application because the longest delay time of the comparator occurs during the LSB conversion.

Although the delay time of the comparator can be improved by the monotonic switching method, the higher comparator noise and the dynamic offset caused by the variation of input common-mode voltage degrade the performance of ADC. Fortunately, the comparator noise is relatively small in this work, and the dynamic offset can be tolerated by the one-bit redundancy.

Consequently, the N-type comparator and set-and-up switching method are selected for coarse and fine stages in this work. By utilizing the set-and-up switching method to a high level, the residue voltage stored on the top plate of the coarse capacitor array is near to V_{DD}. The charge sharing switch S_{CS} can be implemented with only a PMOS switch instead of a transmission-gate switch. It not only simplifies the switch design but also increases the speed of the coarse and fine stages.

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3.5.4 Accuracy Consideration

3.5.4.1 Proper Switching Voltage

Fig. 3.15 illustrates the single-ended equivalent models of the charge sharing switch S_{CS}, and the coarse and fine capacitor arrays to implement the proposed charge sharing technique. C_{sw_c} and C_{sw_f} are the total switched capacitors of the coarse and fine capacitor arrays, respectively. C_{p_c} and C_{p_f} are the sums of dummy capacitors, and all parasitic capacitance at the top plates of the coarse and fine capacitor arrays, respectively. C_{gs}, C_{gd} and C_{ds} are the parasitic capacitance of the charge sharing switch, and Ron is the turn-on resistance of the charge sharing switch.

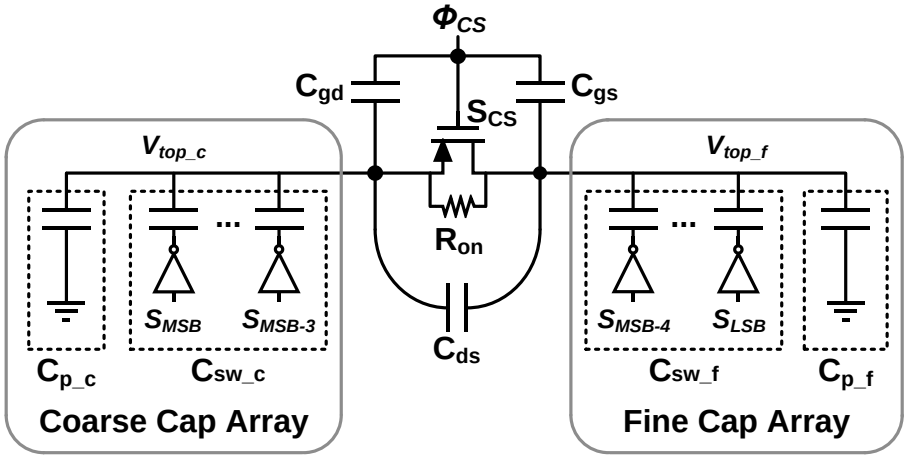

Fig. 3.15 Equivalent model of the proposed charge sharing technique

At the beginning of the CS phase, S_{CS} is turned off. Since the coarse stage has already resolved the first 4 bits, the residue voltage of the input signal $V_{Res}[K]$ is remained on the top plate voltage of the coarse capacitor array, where K denotes the Kth sampling. The top plate of the fine capacitor array is reset to V_{DD} in the

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meanwhile. When S_{CS} is turned on during the CS phase, the top plate voltage of the fine stage $V_{top\_f}[K]$ can be calculated as

$$V_{top\_f}[K] = \alpha \times V_{\mathrm{Res}}[K] + \beta \times V_{DD} \tag{3.26}$$

where α and β are the charge sharing coefficients of the residue voltage and the reference voltage, respectively. In this work, V_{DD} is used as the reference voltage.

$$\alpha = \frac{C_{\mathrm{Sum\_c}}}{C_{\mathrm{Sum\_f}} + C_{\mathrm{Sum\_c}}} \tag{3.27}$$

$$\beta = \frac{C_{\mathrm{Sum\_f}}}{C_{\mathrm{Sum\_f}} + C_{\mathrm{Sum\_c}}} \tag{3.28}$$

where $C_{\mathrm{Sum\_c}}$ and $C_{\mathrm{Sum\_f}}$ are equal to $C_{p\_c} + C_{tot\_c}$,and $C_{p\_f} + C_{tot\_f}$, respectively. Because the second term of (3.26) is independent of K, i.e., signal-independent, it can be canceled in a differential configuration. The value of α is critical to the gain mismatch between the coarse and fine stages, which affects the resolution considerably.

In order to prove that the multiple reference voltage is necessary without the additional dummy capacitor or different size of unit capacitance, we take an N-bit conventional two-step SAR ADC for example: the coarse stage resolves the first M-bit of input signal, and the residue is transferred to the fine stage for the (N-M)-bit conversion. Assuming that

$$C_{\mathrm{Sum\_c}} = k \times C_{\mathrm{Sum\_f}} \tag{3.29}$$

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where k is the capacitor coefficient ratio of the coarse and fine stages and there is no extra parasitic capacitance in the C_{Sum_c} and C_{Sum_f}. That is, the charge sharing coefficient α is equal to $\frac{k}{k+1}$, and

$$C_{Sum\_c} = k \cdot 2^{N-2M-1} \cdot \left[2^{M-1}, 2^{M-2}, ..., 2^1, 2^0, 2^0\right] \tag{3.30}$$

$$C_{Sum\_f} = \left[2^{N-M-2}, 2^{N-M-3}, ..., 2^1, 2^0, 2^0\right] \tag{3.31}$$

In order to performing the binary search of the SAR algorithm, the switching voltage of the first M-bit is equal to

$$\left[\frac{1}{2^1}, \frac{1}{2^2}, ..., \frac{1}{2^M}\right] \times V_{ref\_c} \tag{3.32}$$

where V_{ref_c} is the reference voltage of the coarse stage.

Besides, the switching voltage of the rest of (N-M)-bit is equal to

$$\left[\frac{1}{2^1}, \frac{1}{2^2}, ..., \frac{1}{2^{N-M+1}}\right] \times V_{ref\_f} \tag{3.33}$$

where V_{ref_f} is the reference voltage of the fine stage. According to the binary search and the charge sharing technique, the first term of switching voltage of the fine stage $\frac{1}{2^1} V_{ref\_f}$ is equal to the last term of switching voltage of the coarse stage $\frac{1}{2^M} V_{ref\_c}$ multiply by $\frac{\alpha}{2}$.

Thus,

$$\frac{1}{2} \times V_{ref\_f} = \frac{1}{2^M} \times \frac{\alpha}{2} \times V_{ref\_c} \tag{3.34}$$

$$V_{ref\_f} = \frac{1}{2^M} \times \frac{k}{k+1} \times V_{ref\_c} \tag{3.35}$$

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(3.35) proves that it is impossible to use only one reference without adding the additional dummy capacitor or selecting the different size unit capacitance in the coarse and fine stages.

Because the different size unit capacitance suffers from the serious capacitor mismatch issue, it is an unavailable method in this work. Accordingly, adding the additional dummy capacitor is the only one solution for only one reference voltage. The following equation shows that by adding the additional dummy capacitor is valid for only one reference voltage.

If the dummy capacitor C_{p_f} is added to the fine capacitor array, the corresponding switching voltage of the rest of (N-M)-bit is equal to

$$\left[\frac{2^{N-M-2}}{2^{N-M-1}+C_{p\_f}},\frac{2^{N-M-3}}{2^{N-M-1}+C_{p\_f}},...,\frac{1}{2^{N-M-1}+C_{p\_f}}\right]\times V_{ref\_f} \tag{3.36}$$

Similarly, based on the binary search and the charge sharing technique, the first term of switching voltage of the fine stage $\frac{2^{N-M}}{2^{N-M+1}+C_{p\_f}}V_{ref\_f}$ is equal to the last term of switching voltage of the coarse stage $\frac{1}{2^M}V_{ref\_c}$ multiply by $\frac{\alpha}{2}$.

That is,

$$\frac{2^{N-M-2}}{2^{N-M-1}+C_{p\_f}}V_{ref\_f}=\frac{1}{2^M}\times\frac{\alpha}{2}\times V_{ref\_c} \tag{3.37}$$

$$\frac{2^{N-1}}{\alpha}\times\frac{V_{ref\_f}}{V_{ref\_c}}=2^{N-M-1}+C_{p\_f} \tag{3.38}$$

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$$C_{p\_f} = 2^{N-1} \times \frac{k+1}{k} \times \frac{V_{ref\_f}}{V_{ref\_c}} - 2^{N-M-1} \tag{3.39}$$

If we make V_{ref_c} equals to V_{ref_f}, then

$$C_{p\_f} = 2^{N-1} \times \frac{k+1}{k} - 2^{N-M-1} \tag{3.40}$$

In terms of the consideration of SNR, the capacitor coefficient ratio of the coarse and fine stages k should greater or equal to one to make the fine stage get more residues from the coarse stage.

Thus, k is selected for one to compensate the least comparator in the fine stage and C_{p_f} is added to the fine capacitor array which equals to

$$C_{p\_f} = 2^{N} - 2^{N-M-1} \tag{3.41}$$

Consequently, by adding some capacitor in the fine capacitor array can maintain proper switching for the SAR algorithm and, as mentioned in Sec. 3.4, only one reference voltage is utilized in this work.

Although by selecting the different size unit capacitance in the coarse and fine stages may reduce the total capacitance of the two stages, the different size unit capacitance suffers from the serious capacitance mismatch. It will cause the serious gain mismatch error between the coarse and fine stages which degrade the linearity of ADC.

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Based on the aforementioned reason, k is designed to be 1 and α is equal to be 0.5. That is, C_{Sum_c} equals to C_{Sum_f}, and the gain of the coarse stage is the same as that of the fine stage. The switched voltage headroom of the fine capacitor array is 0.5 time of that of the coarse capacitor array. As mentioned before, to avoid using another reference voltage, the equivalent reference voltage, $0.5V_{DD}$, is designed by accurately controlling the ratio between C_{p_f} and C_{tot_f}. Thus, the fine stage can resolve the shared signal, $0.5V_{res}[K]$, subsequently.

Besides, as mentioned in Sec. 3.4, a 32kΩ resistor ladder is used for the LSB switching in the fine state, which can not only reduce the total capacitance of the coarse and fine stages, but also expedite the speed of the charge sharing.

Because there is no extra redundancy for the LSB decisions in the fine stage, the settling error of the fine stage should be smaller than 0.5 LSB. Although the proposed charge sharing technique results in α times reduction of the residue voltage, which indicates that the V_{LSB} is attenuated by α, the switching voltage for the fine stage is reduced by the same factor. The time t needed for the switching follows [2]

$$\Delta V \cdot e^{\frac{-t}{\tau}} < 0.5 \cdot V_{LSB} \tag{3.42}$$

where ΔV represents the switching voltage , τ represent the RC time constant and t represents the settling time.

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Based on (3.42), despite the attenuation of V_{LSB}, the time needed for settling in the fine stage is the same as the conventional architecture. However, thanks to the two-step architecture and the small voltage swing in the fine stage, the loop delay time of the fine stage can be much shorter than that of the conventional architecture. Values are given in multiples of time constants τ for a settling error 0.5 LSB in the fine stage, as shown in Fig. 3.16. It also indicates that the time needed for LSB switching is relaxed, and the least time for settling within $0.5\,V_{LSB}$ is the LSB switching of the fine stage. The increment of the turn-on resistance caused by the 0.5 V_{ref} from the resistor ladder can be tolerated. Thus, the 0.5Vref from the resistor ladder is used only for LSB in the fine stage.

Besides, the gain mismatch error between the coarse and fine stages can be tolerated in this work, as mentioned in Sec. 3.5.2.

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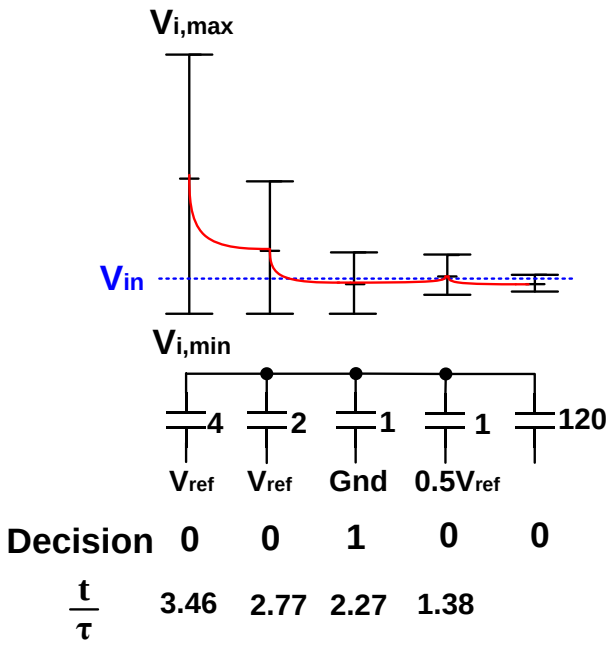

Fig. 3.16 Detail of the switching scheme and the time needed for settling is given in multiples of time constant for a settling error < $0.5V_{LSB}$ in the fine stage

3.5.4.2 Nonlinearity of Charge Sharing Switch

Although the proposed charge sharing technique has a lot of advantages, there are some nonlinearity in the charge sharing switches S_{CS}, which includes clock feedthrough, charge injection, signal feedthrough and switching voltage feedthrough. By utilizing the proposed charge sharing technique, the residue transferred to the fine stage is used for the LSB conversion and its accuracy is important. Besides, after finishing the charge sharing, the coarse stage is used to sample next input signal. The

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nonlinearity of the coarse stage which results from charge sharing switch can be ignored. Consequently, the nonlinearity analysis is only for the fine stage.

The first nonlinearity is clock feedthrough, which can be modelled as shown in Fig. 3.17. In the beginning of the charge sharing, Φ_{CS} is from V_{DD} to ground to turn on the charge sharing switch, and the voltage variation of Φ_{CS} results in the voltage variation by C_{gs} and C_{gd} .

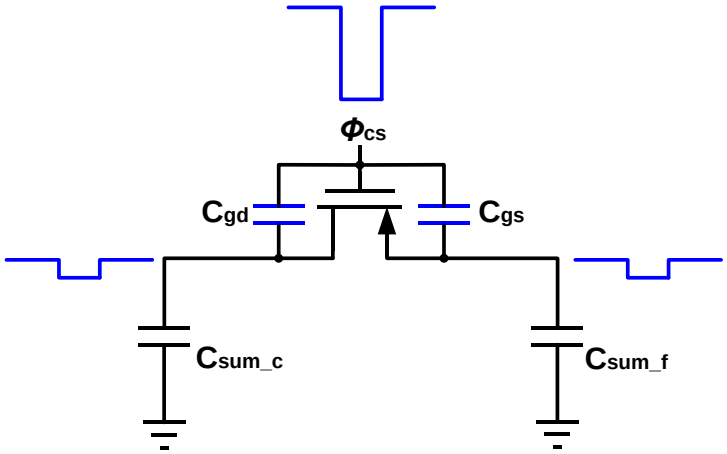

Fig. 3.17 Clock feedthrough model of the charge sharing switch

When Φ_{CS} is from V_{DD} to ground, the voltage variation of the clock feedthrough is equal to [24]

$$\frac{C_{gs,1}}{C_{gs,1}+C_{sum\_f}}V_{DD} \tag{3.43}$$

where $C_{gs,1}$ is the parasitic capacitance between gate and source at the beginning of the charge sharing. At the end of the charge sharing, Φ_{CS} is from ground to V_{DD} to

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turn off the charge sharing switch, and the voltage variation of Φ_{CS} results in the voltage variation by C_{gs} and C_{gd}.

On the other hand, when Φ_{CS} is from ground to V_{DD}, the voltage variation of the clock feedthrough is equal to

$$\frac{C_{gs,2}}{C_{gs,2}+C_{sum\_f}}V_{DD} \tag{3.44}$$

where $C_{gs,2}$ is the parasitic capacitance between gate and source at the end of the charge sharing.

Thus, the voltage variation of the fine stage V_{cf} caused by the clock feedthrough

$$V_{cf}=\left(\frac{C_{gs,2}}{C_{gs,1}+C_{sum\_f}}-\frac{C_{gs,1}}{C_{gs,2}+C_{sum\_f}}\right)V_{DD} \tag{3.45}$$

which is dependent on the variation of C_{gs}.

In this work, the variation of C_{gs} can be neglected because the residue variation during the charge sharing is small. It indicates that the nonlinearity caused by the clock feedthrough of the charge sharing switch can be ignored.

The second nonlinearity is charge injection, which can be modelled as shown in Fig. 3.18, where R_s is the turn-off resistance of M_{SHi} from low-skew De-MUX, R_{on} is the turn-on resistance of the charge sharing switch S_{CS}, C_{ox} is oxide capacitance between the gate and the channel.

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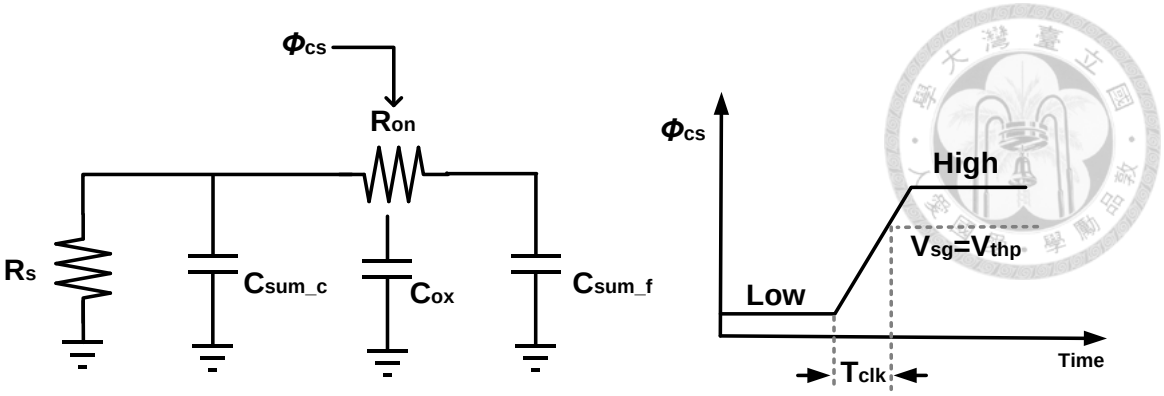

Fig. 3.18 Charge injection model of the charge sharing switch

After the charge sharing, Φ_{CS} will turn off S_{CS}, the charge stored in the channel of S_{CS} will be injected from the channel [32][33]. The amount of charge injection is dependent on the rise/fall time of the charge sharing switch T_{clk}. T_{clk} is defined as the time it takes for the gate voltage of charge sharing switch from 0 to V_{thp}, where the PMOS is implemented for charge sharing switch in this work. If $\tau_{ox} \ll T_{clk} \ll \tau_s$, we define it as fast turnoff, where

$$\tau_{ox} = R_{on} \cdot C_{ox} \tag{3.46}$$

$$\tau_s = R_s \cdot C_{sum\_c} \tag{3.47}$$

When the charge sharing switch is fast turnoff, the channel charge

$$Q_{ch} = WLC_{ox}(V_{res} - V_{thp}) \tag{3.48}$$

splits to the drain and the source by the charge split ratio, where V_{res} is the final residue voltage on the top plate of the fine stage.

The charge split ratio between the coarse and fine capacitor array is

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$$\frac{Q_{fine}}{Q_{Coarse}} = \frac{C_{sum\_f}}{C_{sum\_c}(1-e^{-\frac{T_{clk}}{\tau_s}})} \tag{3.49}$$

The amount of charge injection [33] to the fine stage is equal to

$$Q_{fine} = \frac{1}{2}Q_{ch}\left[1-\frac{C_{sum\_c}(1+\frac{T_{clk}}{\tau_s})-C_{sum\_f}}{C_{sum\_c}(1+\frac{T_{clk}}{\tau_s})+C_{sum\_f}}(1-e^{-\frac{T_{clk}}{\tau_L}})\right] \tag{3.50}$$

where

$$\tau_L = R_{on}\cdot\frac{C_{sum\_c}\cdot C_{sum\_f}}{C_{sum\_c}+C_{sum\_f}} \tag{3.51}$$

On the other hand, if $T_{clk} \gg \tau_s$ and $T_{clk} \gg \tau_{ox}$, we define it as slow turnoff.

The amount of charge injection to the fine stage is equal to

$$Q_{fine} = \frac{1}{2}\left\{\begin{aligned}&e^{-\frac{T_{clk}}{\tau_s}}\left[Q_{ch}-(1-e^{-\frac{T_{clk}}{\tau_{ox}}})\frac{C_{ox}^2}{4T_{clk}K_n\frac{W}{L}}\right]\times\left[1-\frac{C_{sum\_c}(1+\frac{T_{clk}}{\tau_s})-C_{sum\_f}}{C_{sum\_c}(1+\frac{T_{clk}}{\tau_s})+C_{sum\_f}}(1-e^{-\frac{T_{clk}}{\tau_L}})\right]\\&+[(1-\delta)(1-e^{-\frac{T_{clk}}{\tau_{ox}}})\frac{C_{ox}^2}{4T_{clk}K_n\frac{W}{L}}]\end{aligned}\right\} \tag{3.52}$$

where

$$\delta = \frac{R_{pn}}{R_{pn}+2R_{ch-sub}} \tag{3.53}$$

$$R_{pn} = \frac{U_T}{I_s e^{\frac{V_a}{U_T}}} \tag{3.54}$$

$$U_T = \frac{kT}{q} \tag{3.55}$$

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When the charge sharing switch is slow turnoff, $T_{clk} \gg \tau_s$ and $T_{clk} \gg \tau_{ox}$. As a result, from (3.52), the amount of charge injection Q_{fine} to the fine stage is much smaller than that of the fast turnoff.

In this work, C_{sum_c} is equal to C_{sum_f}, $T_{clk} \ll \tau_s$ and $T_{clk} \ll \tau_L$. The charge injected to the fine stage can be approximated by

$$Q_{fine} \cong \frac{1}{2} Q_{ch} \tag{3.56}$$

$$\cong \frac{1}{2} WLC_{ox}(V_{res} - V_{thp}) \tag{3.57}$$

From (3.57), the charge injection is signal dependent to V_{res} and proportional to the size of charge sharing switch and related to V_{thp}. The body effect can be ignored due to the connection of the source and body of the PMOS switch. As a result of the fact that V_{thp} is signal independent. However, the different V_{res} result in the different amount of charge, which result in the gain error in the fine stage.

Although the slow turnoff results in less amount of charge injection, but it is not suitable for high-speed application. Accordingly, the fast turnoff is selected. Based on the simulation, the maximum gain error caused by charge injection is 0.9957, so the influence of the charge injection can be ignored.

The third nonlinearity is signal feedthrough, which can be modelled as shown in Fig. 3.19. After the charge sharing, the charge sharing switch S_{CS} is turned off. However, when the fine stage starts to resolve the residue, the coarse stage is in the

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tracking phase. The variation of the top plate of the coarse stage during the tracking phase interferes with the residue on the top plate of the fine stage through the parasitic capacitance C_{ds}.

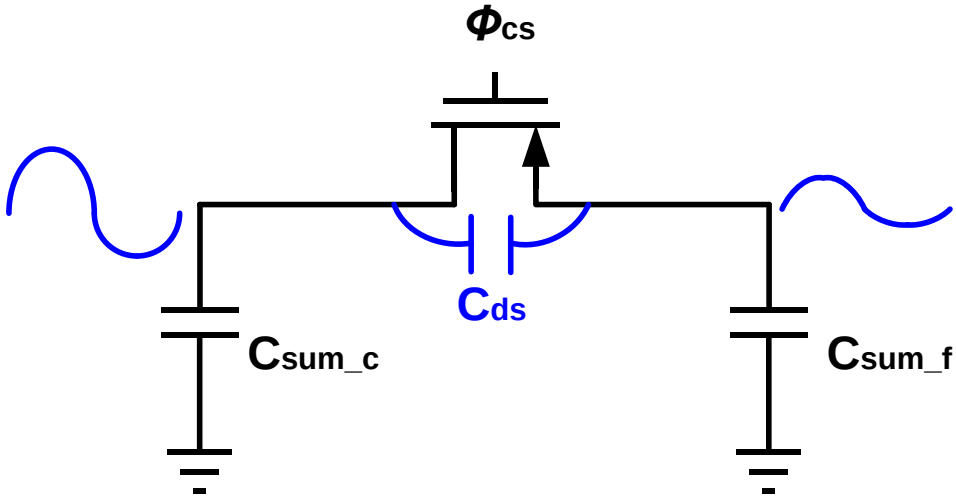

Fig. 3.19 Signal feedthrough model of the charge sharing switch

The signal feedthrough voltage ΔV_{sf} [24] from the coarse stage to the fine can be derived as

$$\Delta V_{sf} = \frac{C_{ds}}{C_{ds} + C_{Sum\_f}} \times \Delta V_{Sample} \tag{3.58}$$

where C_{ds} is the drain-source capacitance of S_{CS} and ΔV_{Sample} is the voltage variation during the next tracking phase.

For the M-channel time-interleaved ADC, the next tracking phase is the time during $(M-D)T_s$ and $(M)T_s$, where D is the duty cycle of the tracking phase of the sub-ADC, as shown in Fig. 3.20.

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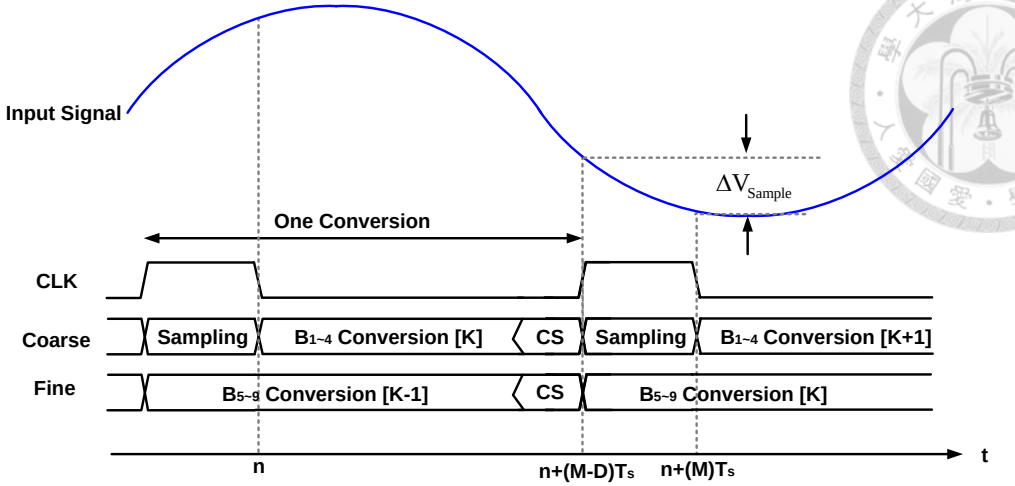

Fig. 3.20 Timing diagram of the signal feedthrough

The following equation is used to estimate ΔV_{sf} which interfere with the fine stage.

The input signal is

$$V_{signal} = A\sin\left[2\pi f_{in}\left(nT_s\right)\right] \tag{3.59}$$

where n represents nth sampling, T_s is the sampling period of the time-interleaved ADC, f_{in} is the input frequency, and A is the amplitude of input signal.

The voltage variation ΔV_{Sample} during the next tracking phase $\left[n+(M-D)Ts, n+(M)Ts\right]$ is

$$\Delta V_{Sample} = A\sin\left[2\pi f_{in}\left(n+M\right)T_s\right] - A\sin\left[2\pi f_{in}\left(n+M-D\right)T_s\right] \tag{3.60}$$

$$= A\sin\left[2\pi f_{in}\left(n\right)T_s\right]\cos\left[2\pi f_{in}\left(M\right)T_s\right] - A\cos\left[2\pi f_{in}\left(n\right)T\right]\sin\left[2\pi f_{in}\left(M\right)T_s\right]$$

$$- A\sin\left[2\pi f_{in}\left(n\right)T_s\right]\cos\left[2\pi f_{in}\left(M-D\right)T\right] + A\cos\left[2\pi f_{in}\left(n\right)T_s\right]\sin\left[2\pi f_{in}\left(M-D\right)T_s\right] \tag{3.61}$$

$$= A\sin\left[2\pi f_{in}\left(n\right)T_s\right]\left\{\cos\left[2\pi f_{in}\left(M\right)T_s\right] - \cos\left[2\pi f_{in}\left(M-D\right)T\right]\right\}$$

$$- A\cos\left[2\pi f_{in}\left(n\right)T_s\right]\left\{\sin\left[2\pi f_{in}\left(M\right)T_s\right] - \sin\left[2\pi f_{in}\left(M-D\right)T\right]\right\} \tag{3.62}$$

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$$= AK_1\sin\theta + AK_2\cos\theta \tag{3.63}$$

$$= A\sqrt{K_1^2 + K_2^2}\left(\frac{K_1}{\sqrt{K_1^2 + K_2^2}}\sin\theta - \frac{K_2}{\sqrt{K_1^2 + K_2^2}}\cos\theta\right) \tag{3.64}$$

$$= A\sqrt{K_1^2 + K_2^2}\ \sin(\theta - \phi) \tag{3.65}$$

where

$$\theta = 2\pi f_{in}(nT_s) \tag{3.66}$$

$$K_1 = \cos\left[2\pi f_{in}(M)T_s\right] - \cos\left[2\pi f_{in}(M-D)T\right] \tag{3.67}$$

$$K_2 = \sin\left[2\pi f_{in}(M)T_s\right] - \sin\left[2\pi f_{in}(M-D)T\right] \tag{3.68}$$

$$\phi = cos^{-1}\frac{K_1}{\sqrt{K_1^2 + K_2^2}} = sin^{-1}\frac{K_2}{\sqrt{K_1^2 + K_2^2}} \tag{3.69}$$

As can be seen in the following equations, the amplitude of the signal feedthrough is

$$\sqrt{K_1^2 + K_2^2} = \sqrt{\begin{matrix}2 - 2\cos\left[2\pi f_{in}(M)T_s\right]\cos\left[2\pi f_{in}(M-D)T\right] \\ -2\sin\left[2\pi f_{in}(M)T_s\right]\sin\left[2\pi f_{in}(M-D)T\right]\end{matrix}} \tag{3.70}$$

$$= \sqrt{2 - 2\cos\left[2\pi f_{in}(D)T_s\right]} \tag{3.71}$$

$$= \sqrt{2\left[2\sin^2\left[\pi f_{in}(D)T_s\right]\right]} \tag{3.72}$$

$$= 2\sin\left[\pi f_{in}(D)T_s\right] \tag{3.73}$$

The phase shift of the signal feedthrough ϕ is

$$\phi = cos^{-1}\frac{K_1}{\sqrt{K_1^2 + K_2^2}} \tag{3.74}$$

$$= cos^{-1}\frac{\cos\left[2\pi f_{in}(M)T_s\right] - \cos\left[2\pi f_{in}(M-D)T\right]}{2\sin\left[\pi f_{in}(D)T_s\right]} \tag{3.75}$$

$$= cos^{-1}\frac{-2\sin\left[\pi f_{in}(2M-D)T_s\right]\sin\left[\pi f_{in}(D)T_s\right]}{2\sin\left[\pi f_{in}(D)T_s\right]} \tag{3.76}$$

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$$= cos^{-1}\left\{-\sin\left[\pi f_{in}(2M-D)T_s\right]\right\} \tag{3.77}$$

For an Nyquist rate ADC, the input frequency f_{in} is below $f_s/2$, and $\sin(\theta) \cong \theta$ when θ is small. Besides, in this work, M=2and the duty cycle of the tracking phase of the sub-ADC D is $1/4$.

Therefore, from (3.73) and (3.77), the amplitude of signal feedthrough and the phase shift of the signal feedthrough ϕ can be approximated by

$$\sqrt{K_1^{\,2}+K_2^{\,2}} \cong 2\pi f_{in}(D)T_s \tag{3.78}$$

$$\phi = \frac{5}{8}\pi \tag{3.79}$$

As can be seen in (3.78), the amplitude of signal feedthrough is direct proportional to input frequency and the amplitude of input signal. Thus, the voltage variation ΔV_{Sample} can be approximated by

$$\Delta V_{Sample} = A\sqrt{K_1^{\,2}+K_2^{\,2}}\ \sin(\theta-\phi) \tag{3.80}$$

$$\cong \frac{A\pi f_{in}T_s\sin(\theta-\frac{5}{8}\pi)}{2} \tag{3.81}$$

The signal feedthrough voltage ΔV_{sf} can be approximated by

$$\Delta V_{sf} = \frac{C_{ds}}{C_{ds}+C_{Sum\_f}} \times \Delta V_{Sample} \tag{3.82}$$

$$= \frac{C_{ds}}{C_{ds}+C_{Sum\_f}} \times \frac{A\pi f_{in}T_s\sin(\theta-\frac{5}{8}\pi)}{2} \tag{3.83}$$

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From (3.83), if the sampling frequency is fixed, the amplitude of the signal feedthrough ΔV_{sf} is proportion to C_{ds}, A, f_{in}, ΔV_{Sample}, and inversely proportional to $C_{ds}+C_{Sum\_f}$.

In this work, C_{ds} and C_{Sum_f} are 0.15fF and 136fF, respectively. According to the simulation, the nonlinearity caused by signal feedthrough with Nyquist rate input degrades ENOB about 0.05 bit, which is tolerable in this design.

The fourth nonlinearity is switching voltage feedthrough, which can be modelled in Fig. 3.21. Assuming that the coarse stage resolves the first M-bit in the N-bit ADC, the switching voltage feedthrough ΔV_{svf} is related to the first M-bit decision.

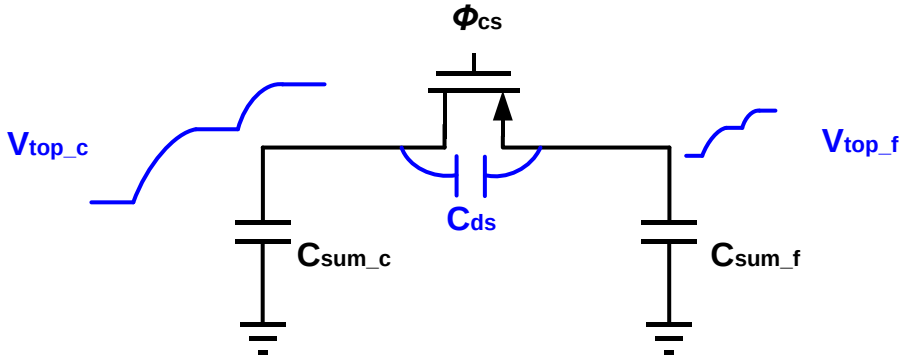

Fig. 3.21 Switching voltage feedthrough model of the charge sharing switch

From (3.59), the input signal is equal to

$$A\sin\left[2\pi f_{in}\left(nT_s\right)\right]=\sum_{i=1}^{M}2^{-i}\mathrm{D}_i V_{ref}+\varepsilon_{q,M} \tag{3.84}$$

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where D_i is the digital output of the first M-bit, and $\varepsilon_{q,M}$ is the M-bit quantization error .

When the fine stage resolves the residue, the coarse stage resolves the next input signal at the same time. The switching voltage of the coarse stage ΔV_{sv}, which is equal to $\sum_{i=1}^{M} 2^{-i} D_i V_{ref}$, will transfer to the top plate of the fine stage through the C_{ds}. Thus, the switching voltage feedthrough ΔV_{svf} from the coarse stage to the fine can be derived as

$$\Delta V_{svf} = \frac{C_{ds}}{C_{ds} + C_{Sum\_f}} \times \sum_{i=1}^{M} 2^{-i} D_i V_{ref} \tag{3.85}$$

where C_{ds} is the drain-source capacitance of S_{CS} and ΔV_{sv} is the voltage variation during the coarse stage resolving. From (3.85), it validates that the switching voltage feedthrough is related to the M-bit decision of the coarse stage, and proportional to C_{ds} and V_{ref}, and inversely proportional to $C_{ds} + C_{Sum\_f}$.

According to the simulation, the nonlinearity caused by switching voltage feedthrough degrades ENOB about 0.1 bit, which is tolerable in this design.

Therefore, the nonlinearity of the charge sharing switch degrades ENOB about 0.2 bit, which can be tolerated in this work.

Although the drain-source capacitance C_{ds} causes the nonlinearity to the ADC, the signal feedthrough and switching voltage feedthrough can be cancelled out by adding the cross-couple capacitor which value is equal to C_{ds}, as shown in Fig. 3.22.

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By doing so, the error voltage results from signal feedthrough and switching voltage feedthrough can be counteracted.

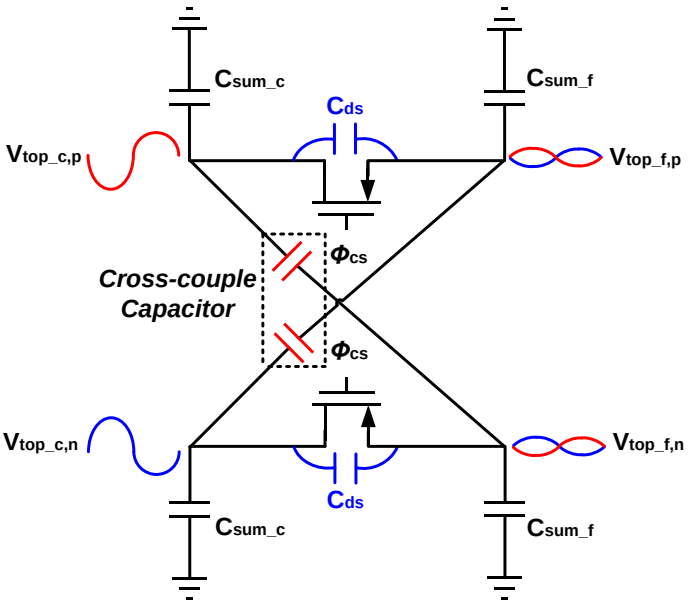

Fig. 3.22 Cross-coupled capacitors with charge sharing switches

3.5.5 Speed Consideration

The speed of SAR ADC is correlated with the time constant of capacitive DAC. Fig. 3.23 (a) shows the simplified block diagram of the prior work [21] with a pseudo differential source follower as its inter-stage residue amplifier. The time constant of the source follower two-step SAR ADC τ_{SF} can be expressed as

$$\tau_{SF} = \left(\frac{1}{g_m} + R_{on}\right) \times C_{SF} = \left(\frac{1}{g_m} + R_{on}\right) \times \frac{C_{Sum\_f}}{2} \tag{3.86}$$

where $1/g_m$ is the output resistance of M_{SF} and R_{on} is the turn-on resistance of the switch. Unlike this work, its residue voltage does not shrink by α, so the value of C_{SF} is equivalently half of C_{Sum_f}. Fig. 3.23(b) depicts the simplified block diagram

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of the conventional pipelined-SAR architecture with an opamp as its residue amplifier. Its time constant τ_{OP} can be written as

$$\tau_{OP} = (R_{out} + R_{on}) \times C_{pipe\_SAR} = (R_{out} + R_{on}) \times \frac{C_{Sum\_f}}{M+1} \tag{3.87}$$

where R_{out} is the output resistance of the opamp. M is the closed-loop gain of the inter-stage residue amplifier. M can make the size of fine capacitor array equivalently shrink by M+1. Therefore, τ_{OP} can be smaller if M is larger.

Fig. 3.23(c) depicts the simplified block diagram of the proposed charge sharing technique. In this work, the time constant of the charge sharing mode τ_{CS} is derived as

$$\tau_{CS} = R_{on} \times (C_{Sum\_c} \,||\, C_{Sum\_f}) \cong R_{on} \times \frac{C_{Sum\_f}}{2} \tag{3.88}$$

where C_{Sum_c} is assumed to be equal to C_{Sum_f}. τ_{CS} is slightly smaller than τ_{SF}.

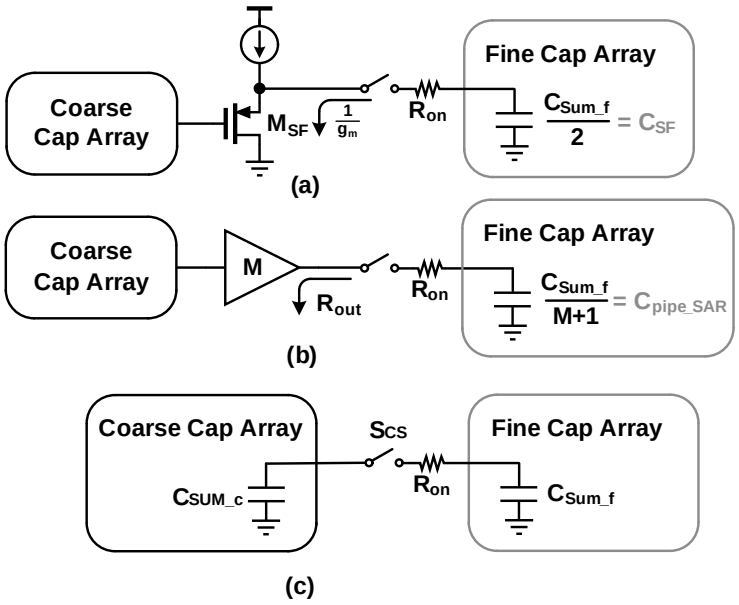

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Fig. 3.23 Block diagram of (a) the source follower topology (b) the traditional pipelined-SAR with opamp (c) the proposed charge sharing technique

However, this work with the proposed dynamic charge sharing switches would be more energy-efficient than the prior work with the static source follower. The conventional pipelined-SAR architecture with the opamp would be the fastest among these three topologies. Nevertheless, the high-gain opamp causes the issues of the output headroom and the power consumption. The charge sharing method has better trade-off between power consumption, speed and design effort than other topologies.

Besides, as mentioned in Sec. 3.4, the resistor ladder used for the LSB conversion can not only reduce the total capacitance of the coarse and fine stage by half, but also make the charge sharing technique faster. τ_{CS} can be half than that in [3] and the residue can be transferred fast. Based on the simulation and (3.88), τ_{CS} is equal to 20ps and it takes 60ps to transfer the residue until the residue voltage is well-settled.

3.6 Summary

The proposed time-interleaved SAR ADC is introduced. The design consideration which includes the channel mismatch and nonlinearity of the proposed ADC is discussed and analyzed.

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Chapter 4 Circuit Implementation

4.1 Introduction

This chapter describes the circuit implementation of the proposed time-interleaved SAR ADC.

4.2 Clock Phase Generator

The schematic of clock phase generator is illustrated in Fig. 4.1. It consists of the invertor chain, D-flip flop, and NOR-gates. The global clock, Φ_{CLK}, is divided by 2 by D-flip flop to generate the control signals of sub-ADCs, Φ_1 and Φ_2, with two NOR-gates. Φ_1 and Φ_2 are 1/4 duty cycle and there frequency is 1/2 of the total sampling rate. The clock phase generator generates Φ_1 and Φ_2 and its waveform is shown in Fig. 4.2. When Φ_1 or Φ_2 is high, the corresponding sub-ADC sampling input signal by the low-skew De-MUX. When the global clock Φ_{CLK} becomes low, the low-skew De-MUX is turned off by the global clock Φ_{CLK}. Then the corresponding sub-ADC starts to regenerative input signal.

The global clock Φ_{CLK} leads Φ_1 or Φ_2 due to the delay of the invertor chain, D-flip flop, and NOR-gates. Despite the fact that the NOR-gates, the different parasitic capacitance and parasitic resistance of clock signal path of Φ_1 and Φ_2 contribute to the timing skew, the global clock Φ_{CLK} which is used for the low-skew

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De-MUX can suppress the skew issue. Besides, in order to generator Φ_1 and Φ_2, Φ_1 and Φ_2 pass through the invertor chain, D-flip flop, and two NOR-gates, it results in bad noise performance if Φ_1 and Φ_2 is used for turning off the sampling switch.

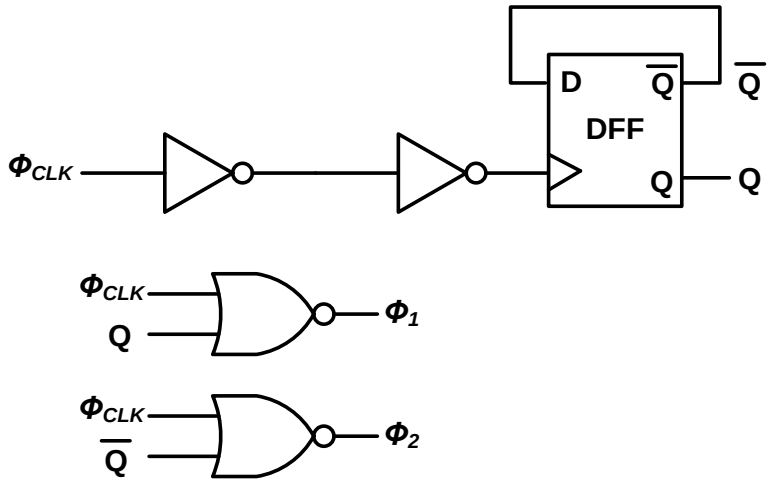

Fig. 4.1 Clock phase generator

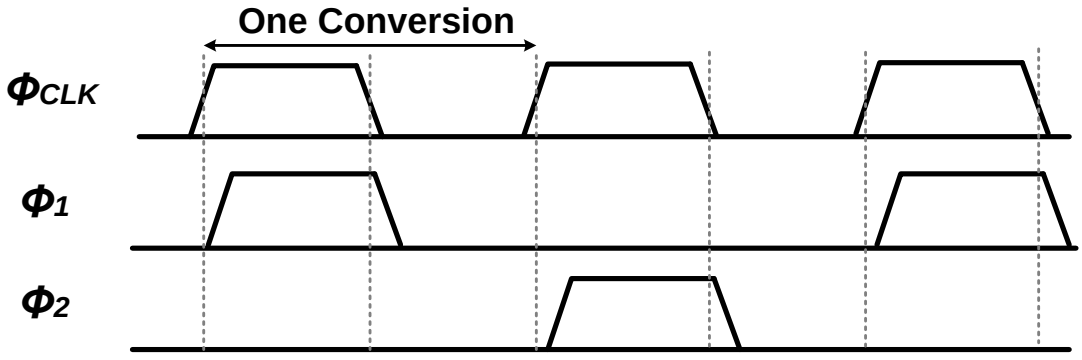

Fig. 4.2 Timing diagram of clock phase generator

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4.3 Two-Step SAR Sub-ADC

4.3.1 Comparator

The comparator used in each sub-ADC is the strong-arm latch dynamic comparator with NMOS input pair, as shown in Fig. 4.3. When the comparator control signal LA is low, the comparator is in reset phase and both the outputs are low. When LA is high, the comparator starts to compare. In the high speed two-step SAR ADC, the design consideration concentrates on speed, noise, and offset [26].

According to [31], the total delay of the strong-arm latch dynamic comparator can be derived as

$$t_{delay} = \frac{2C_L V_{thp}}{I_o} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{thp}} \sqrt{\frac{I_o}{2\beta}} \frac{\Delta V_{out}}{\Delta V_{in}} \right) \tag{4.1}$$

where C_L is the loading capacitance at the latch stage, V_{thp} is the threshold voltage of the PMOS latch, and I_o is the current of tail transistor, β is the aspect ratio of input pair, and $g_{m,eff}$ is the effective transconductance of latch stage.

The noise of the comparator [34] which degrades SNR can be derived as

$$\sigma_{noise} \cong \sqrt{4kT \frac{1}{V_{thp} C_L} \frac{I_o}{g_{m1,2}}} \tag{4.2}$$

where $g_{m1,2}$ is the transconductance of input pair. Based on the simulation, the noise of the coarse and fine stage comparator is 4LSB and 0.2LSB, respectively. As mentioned in Section 3.4, the error caused by the large noise of the coarse stage

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comparator can be tolerated by the one-bit redundancy. Thanks to the two-step architecture, the fine stage has sufficient time to resolve residue, so the comparator of the fine stage has larger C_L and $\frac{g_{m1,2}}{I_o}$. The 0.2LSB noise of the fine stage comparator degrades 0.25 ENOB, which can be tolerated in this work.

The offset mismatch of the comparator [23] can be given as

$$V_{os} = \Delta V_{TH1,2} + \frac{\left(V_{GS} - V_{TH}\right)_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \tag{4.3}$$

where $\Delta V_{TH1,2}$ is the threshold voltage offset of the differential pair of input pair, $\left(V_{GS} - V_{TH}\right)_{1,2}$ is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension, mismatch between the input pair, ΔR is the loading resistance mismatch induced by the latch stage. The first term in (4.4) is a static offset and the second term is a dynamic offset. The dynamic offset is signal dependent and it varies with the input common-mode voltage. Based on the simulation, the dynamic offset is about 4LSB. Fortunately, the static offset can be cancelled in digital domain and the dynamic offset can be tolerated by one-bit redundancy, as mention in Section 3.5.1.

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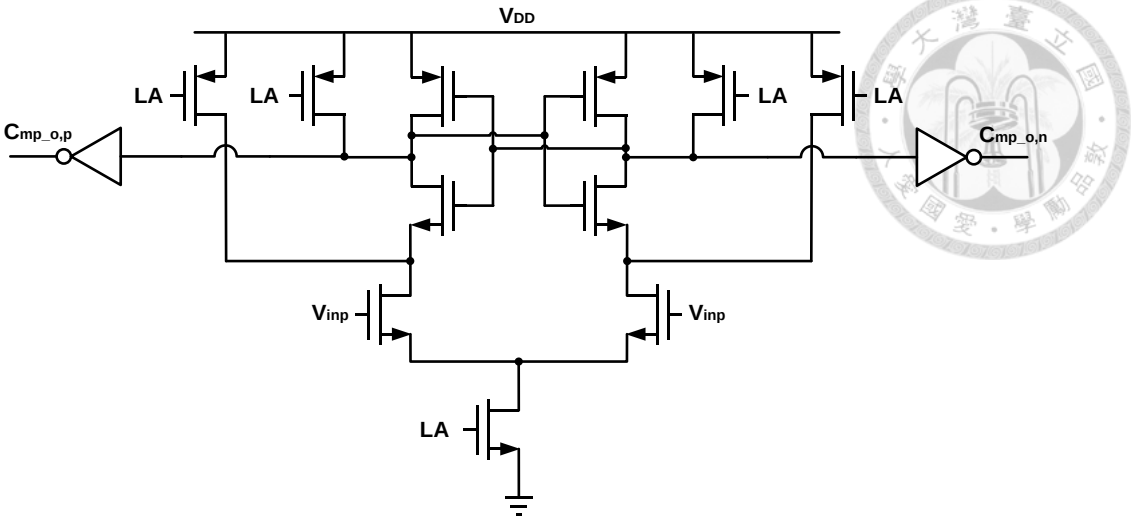

Fig. 4.3 Strong-arm latch dynamic comparator

4.3.2 SAR Logic

To improve the conversion rate of SAR ADC, the asynchronous concept is utilized in the SAR logic. The schematic of the SAR logic is illustrated in Fig. 4.4. It consists of NOR-gates, NAND gate, and the invertor (loop delay cell). Φ_{start} is Φ_1 or Φ_2 and it triggers the SAR logic entering conversion phase after sampling input signal. As mention in Section 4.4.1, LA triggers the comparator to compare input signal. After finishing the comparison, the Done signal is triggered and then LA is low and resetting the comparator for the next comparison. The loop delay time of the asynchronous loop T_{loop} is the propagation delay of the SAR logic. T_{loop} should be slightly longer than the longest DAC setting time to prevent the error caused by the incomplete settling.

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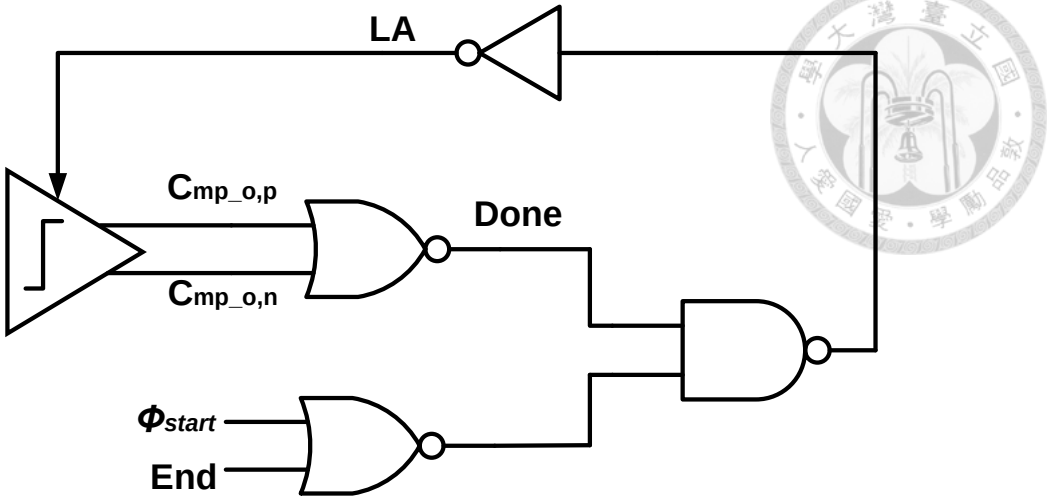

Fig. 4.4 SAR control logic

4.3.4 Capacitive DAC

Fig. 4.5 shows the capacitor array of the coarse and fine stage. The one-bit redundancy in the fine stage is used to cover the error sources. The bottom plate of the capacitor array of the coarse and fine stage is ground initially. After the comparison, the corresponding bottom plate is switched to V_{REF}, the LSB is switched to $V_{REF}/2$ due to the resistor ladder. There are more than 128 unit capacitors and the unit capacitor is 1fF.

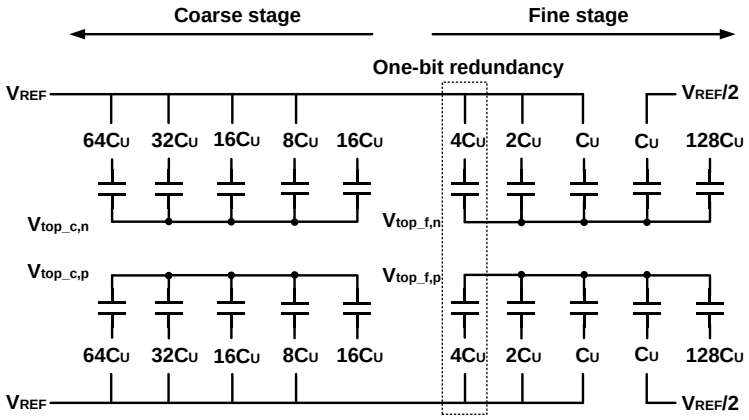

Fig. 4.5 Capacitor array of the coarse and fine stage

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4.3.5 Charge Sharing Timing Control Logic

The charge sharing timing control (CSTC) logic is used for generating the charge sharing timing control signals Φ_{CS} and Φ_R to control the set of charge sharing switches, the sharing switch S_{CS} and the reset switch S_R . It consists of invertor, NAND-gate, and two D-flip flops, as shown in Fig. 4.6. The charge sharing switches are implemented by PMOS switches, so the charge sharing switches is turned on if Φ_{CS} or Φ_R is low.

The Timing diagram of charge sharing timing control logic is depicts in Fig. 4.7. The operation process is that when the fine stage resolves last LSB decision, STL[9] is high and the last latch stage start to latch the comparator output. When the last comparison is finished, F_Done is high and Φ_R becomes high by the D-flip flop. Φ_R is used to reset the top plate of the fine capacitor array. When the coarse stage finishes the last MSB conversion, the C_End becomes high and then Φ_{Start_F} becomes high by the D-flip flop. Simultaneously, Φ_{Start_F} resets Φ_R to turn off the reset switch S_R by the D-flip flop. Then Φ_{CS} becomes low to transfer the residue by the sharing switch S_{CS}. After the charge sharing, the Φ_{CLK} resets Φ_{Start_F} and then Φ_{CS} becomes high to isolate the coarse and fine stage. Finally, the coarse stage starts to sample the next input signal, and the fine stage starts to resolve the residue.

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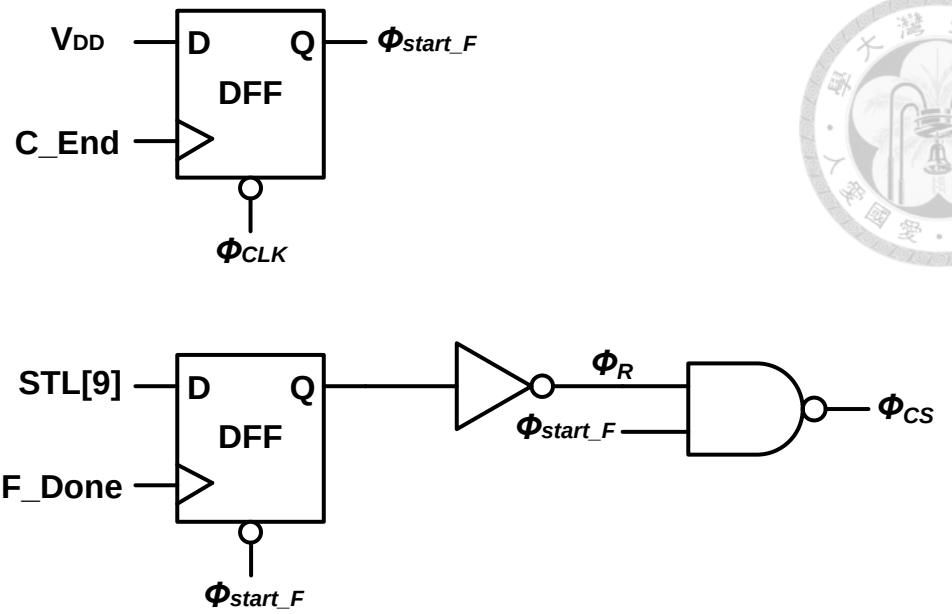

Fig. 4.6 Charge sharing timing control logic

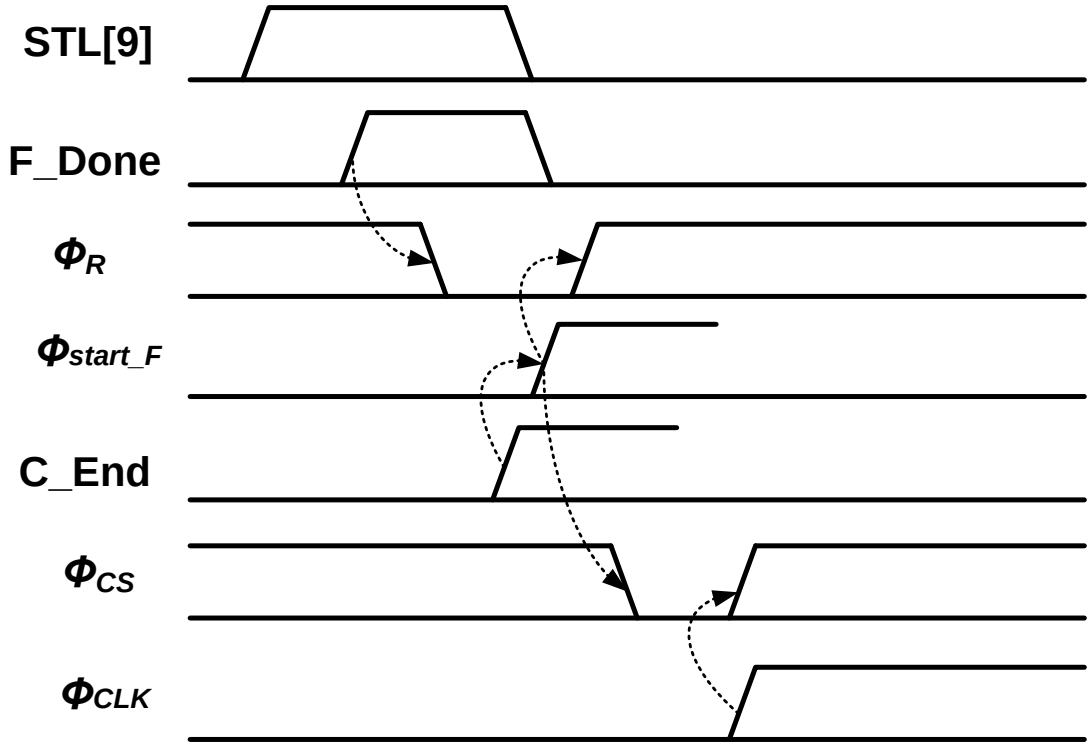

Fig. 4.7 Timing diagram of charge sharing timing control logic

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4.4 Summary

This chapter presents the detailed circuit implementation of the used topology.

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Chapter 5 Measurement Results

5.1 Introduction

This chapter will introduce the measurement preparation and the measurement results. The test setup of the measurement environment is shown in Section. 5.2. Section 5.3 describes the PCB design consideration. Next, the floor plan and chip layout and the measurement results for the 8-bit 1.5GS/s time-interleaved SAR ADC is shown in Section 5.4. Finally, the summary will be discussed in Section 5.5.

5.2 Test Setup

The test setup is shown is Fig. 5.1. The SMB 100A provides a sine wave for the RF transformer though the band-pass filter for suppress the harmonic distortion. The RF transformer converts the single-ended input signal to differential signal. The RF transformer (JTX-4-10T+) is chosen for high frequency input signal (50MHz~1GHz), and the other RF transformer (ADT-1-1WT) is used for low frequency input signal (DC~50MHz). The E8572D generates high frequency sine wave CLK signal for the ADC and the sine wave is translated to square wave CLK signal by the on-chip clock buffer. The input signal and clock generator is connected by SMA cables. The Opamp and LT3020 provide analog reference voltage and power supply for the DUT,

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respectively. The MSO 4034 is used for capturing the digital output of the ADC. The FFT analysis is operated by MATLAB.

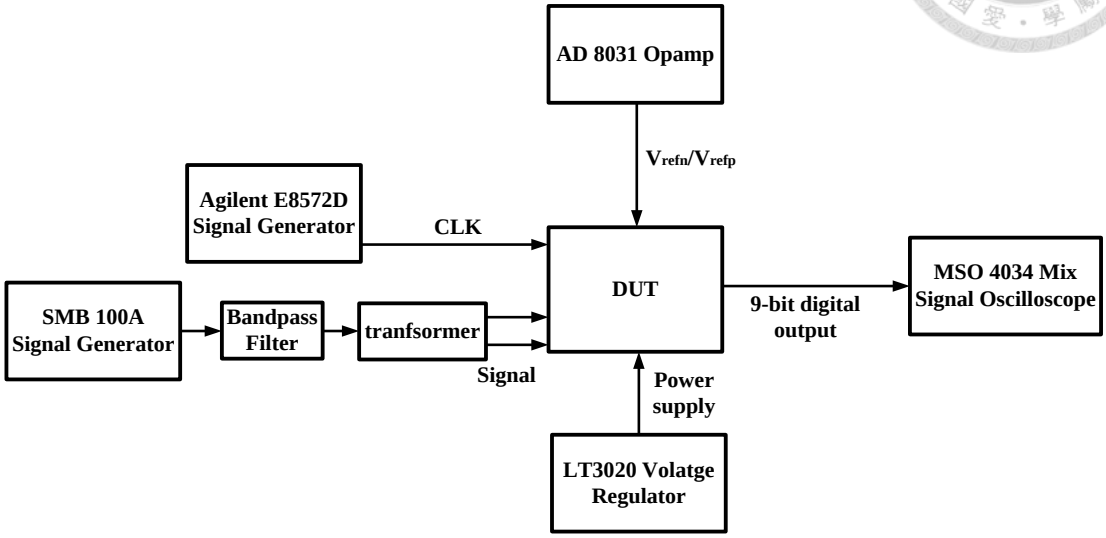

Fig. 5.1 Test setup

5.3 PCB Design

The PCB photo graph is shown in Fig. 5.2. The common-mode voltage of the input signal is provides by analog reference. In order to avoid the coupling noise caused by the digital output buffer and the clock buffer, the grounds of the digital, digital pad, clock, and analog are separated. The separated grounds are connected by the ferrite beads to make the dc level of the grounds equal and suppress high frequency noise. The different values of decoupled capacitors are placed between the chip and power supply to suppress the power supply noise.

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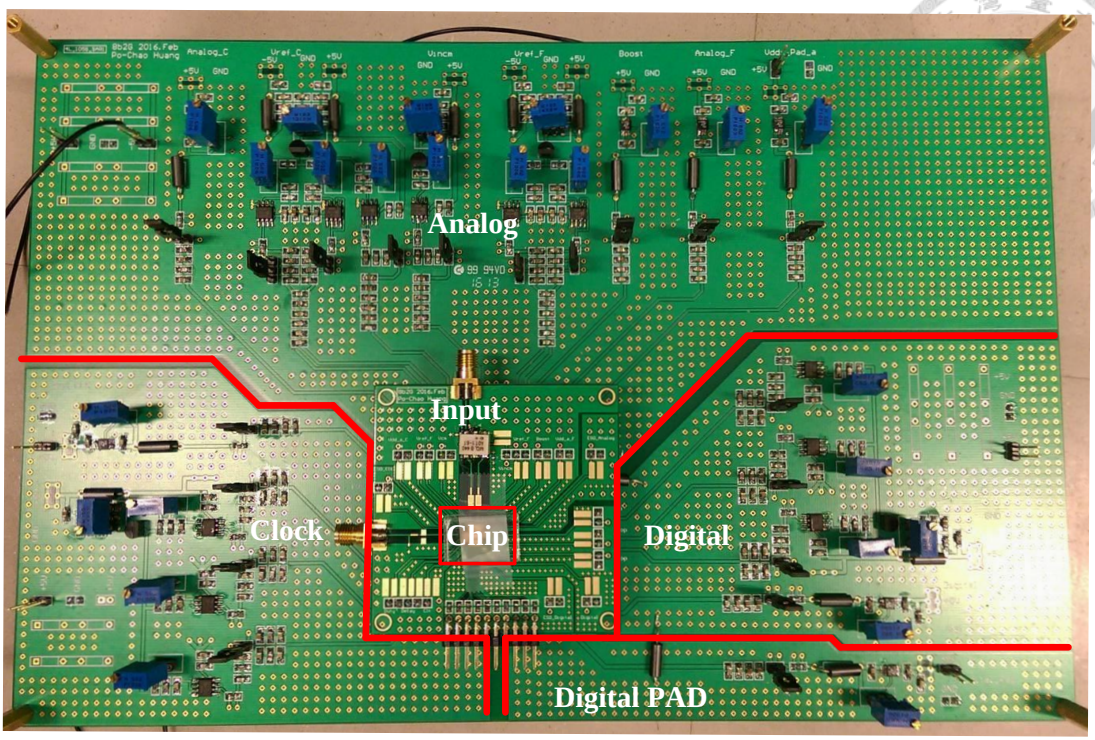

Fig. 5.2 PCB Photo

Fig. 5.3 shows the schematic of single-ended and differential analog reference generation on PCB. LM385 is used to regulate maximum voltage of opamp input at 2.5V. The analog reference generation on PCB is through LM385 to provide the master reference voltage. The master reference voltage is connected to variable resistor to divide V_{POWER_SUPPLY} to desired value, and can be adjusted by tuning the value of variable resistor. All reference voltages are generated by AD8031 blocks, which are used as the unity gain buffer.

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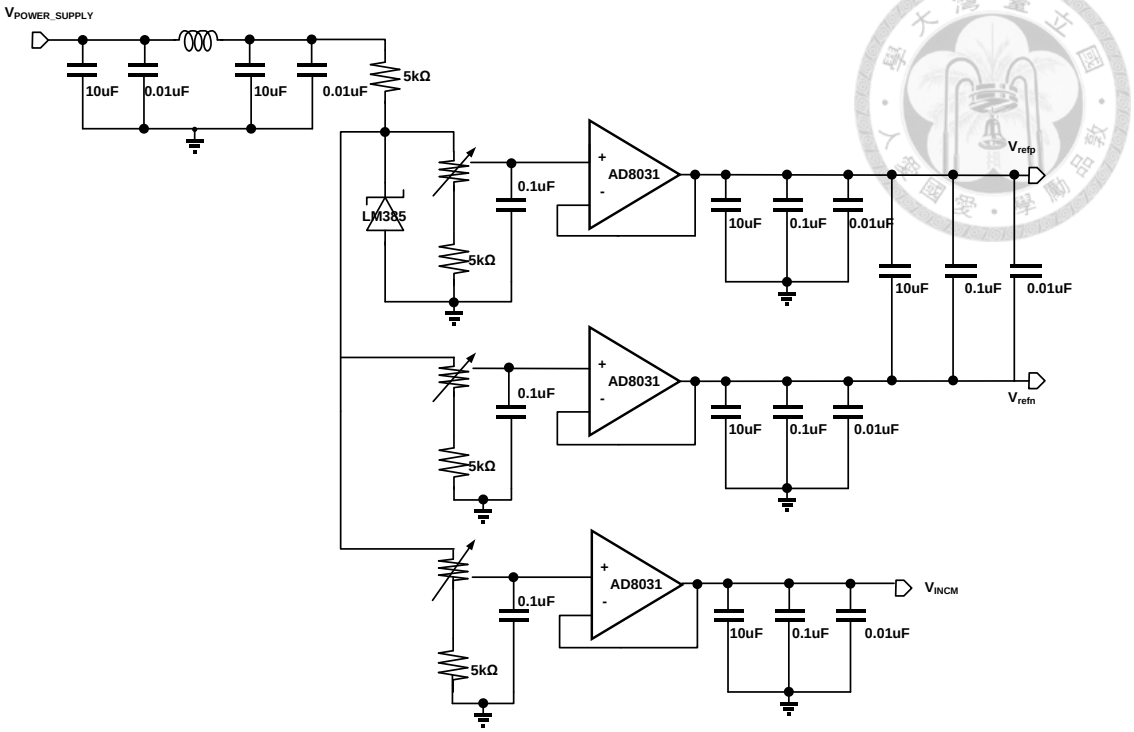

Fig. 5.3 Schemtaic of reference voltage generation

The schematic of power supply generation on PCB, as shown in Fig. 5.4. The power supplies for the DUT are created by LT3020. The decoupling capacitor is also used to suppress the noise.

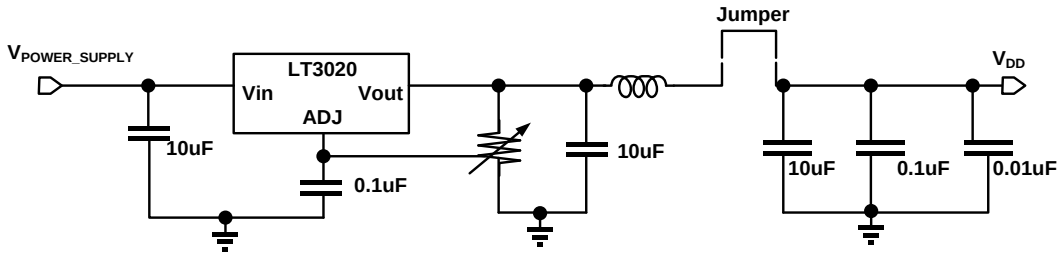

Fig. 5.4 Schematic of power supply generation

5.4 Measurement Results

Fig. 5.5 illustrates the chip micrograph of the prototype ADC fabricated in 40nm CMOS. The ADC output is decimated by 125. This ADC uses the proposed

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small-area low-skew de-MUX circuit to avoid complex skew calibration. Thus, the core circuit occupies an area of 0.014mm^2 (118μm × 117μm). The total power dissipation is 3.1mW with a 0.9V supply. The power dissipation of the proposed ADC is shown in Fig. 5.6. The ADC attains an FoM of 15fJ/conversion-step at Nyquist rate. Table I shows the comparison of recent 8-bit 1-2GS/s range SAR ADCs.

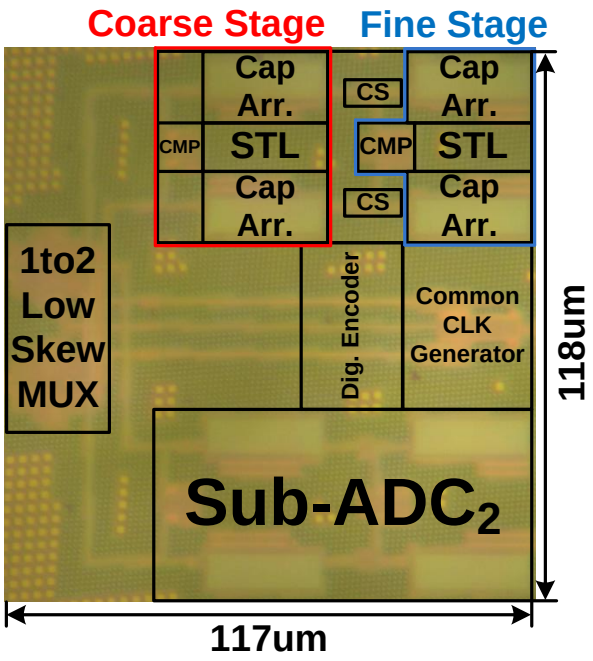

Fig. 5.5 Die photo

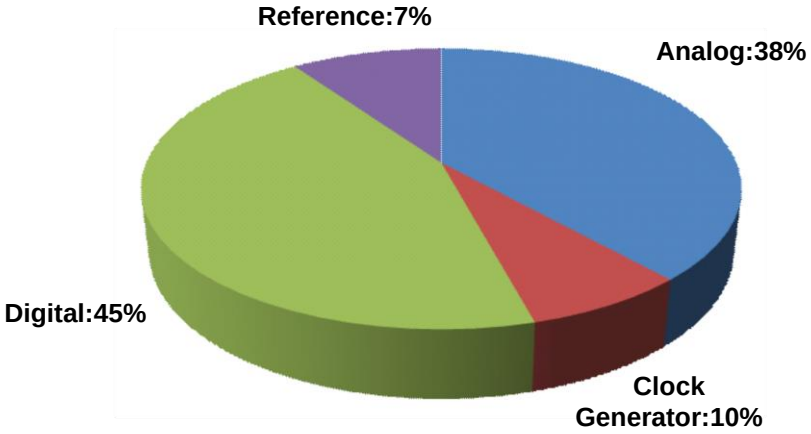

Fig. 5.6 Power dissipation

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5.4.1 Static Performance

The capacitor array is formed by metal-oxide-metal (MOM) type capacitor with a unit capacitance of 1fF. As illustrated in Fig. 5.7, the DNL and INL of the sub-ADC are +0.66/-0.84 and +0.62/-0.82LSB, respectively.

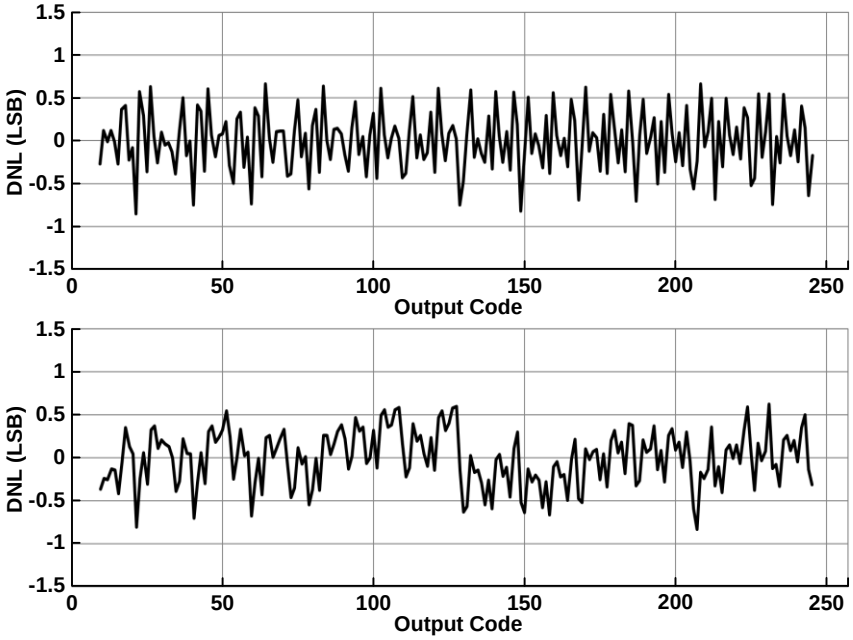

Fig. 5.7 Measured DNL/INL plot

5.4.2 Dynamic Performance

One of the dynamic performances of this ADC is shown in Fig. 5.8. The dynamic performance shows that the SNDR and SFDR versus sampling rate with an input frequency of 1MHz.

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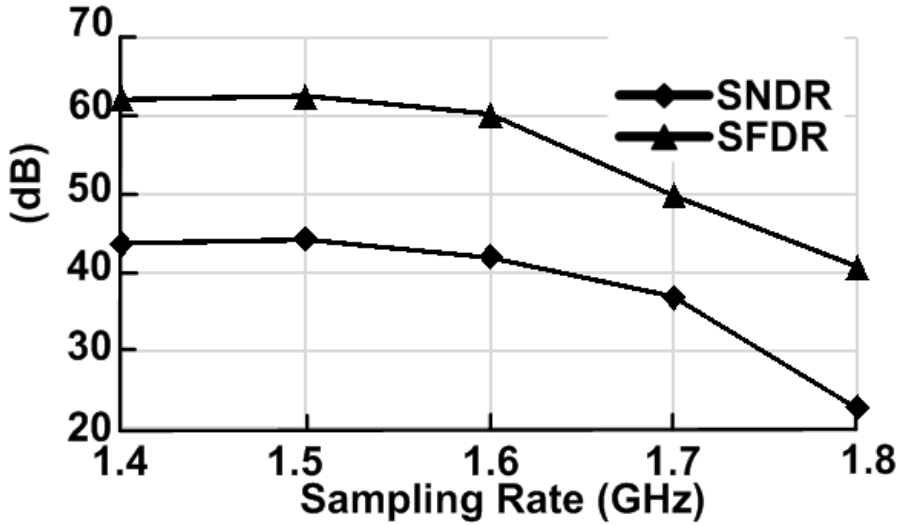

Fig. 5.8 Measured SNDR/SFDR versus sampling rate with 1MHz input

The other the dynamic performance of this ADC is shown in Fig. 5.9, at a sampling rate of 1.5GS/s. The SFDR and SNDR are relatively independent of input frequency (F_{in}) at Nyquist rate.

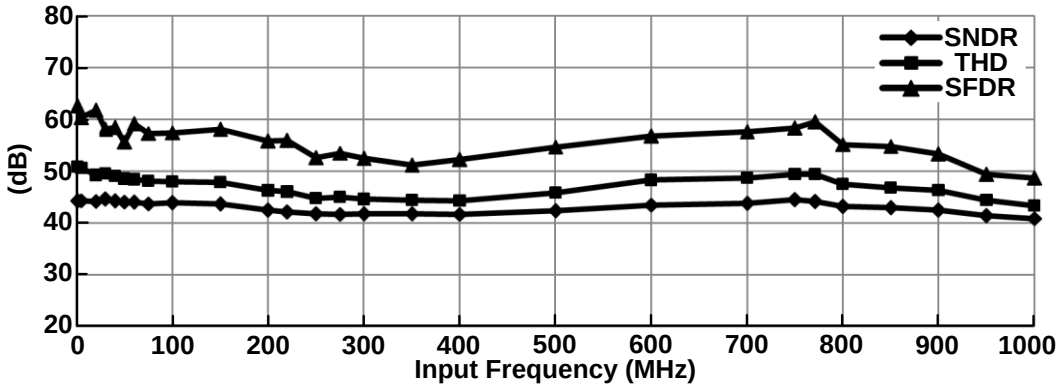

Fig. 5.9 Measured SNDR/SFDR/THD versus input frequency at 1.5GS/s

The measured FFT spectrum at the sampling rate of 1.5GS/s with F_{in} of 0.73MHz is shown in Fig. 5.10. The SFDR and SNDR are 62.58 and 44.63dB, respectively.

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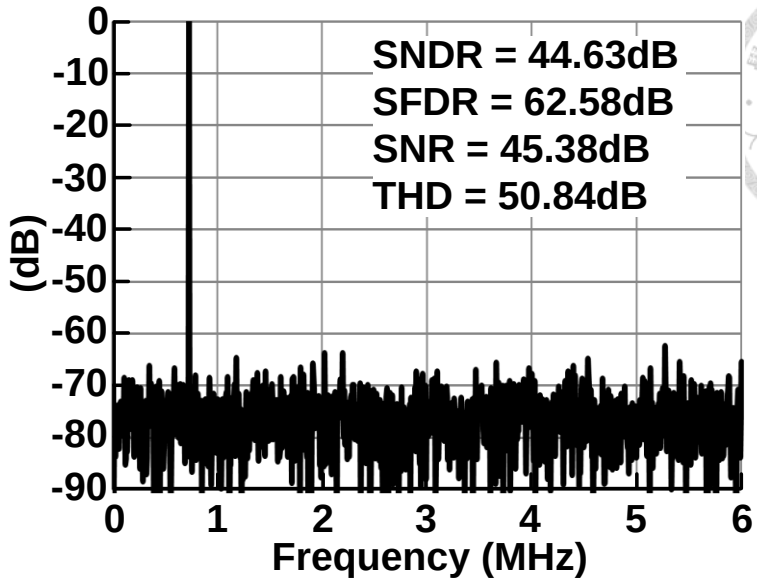

Fig. 5.10 Measured FFT spectrum at 1.5GS/s with 0.73MHz input

The measured FFT spectrum at the sampling rate of 1.5GS/s with F_{in} of 748.5MHz is shown in Fig. 5.10. The SFDR and SNDR are 58.31 and 44.50dB, respectively.

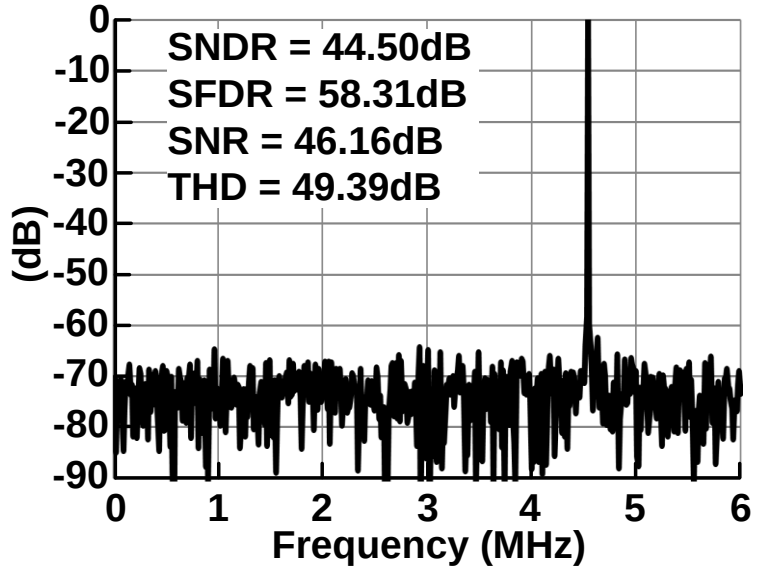

Fig. 5.11 Measured FFT spectrum at 1.5GS/s with 748.5MHz input

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5.5 Summary

The measurement results of the 8-bit time-interleaved SAR ADC are elaborated in this chapter. The PCB design and the test setup are presented. Finally, the measured performance summary and comparison is shown in Table. 5.1.

	VLSI 2012[6]	JSSC 2013[2]	JSSC 2015[7]	ASSCC 2015[1]	This Work
Technology (nm)	**65**	**32SOI**	**45**	**65**	**40**
Num of Channels	**2**	**1**	**1**	**1**	**2**
Resolution (bits)	**8**	**8**	**7**	**8**	**8**
Active Area (mm^2)	**0.013**	**0.0015**	**0.016**	**0.013**	**0.014**
Supply Voltage (V)	**1**	**0.9**	**1.25**	**1.2**	**0.9**
Sampling Rate (GS/s)	**1**	**1**	**1**	**1.2**	**1.5**
Power (mW)	**3.8**	**2**	**3.8**	**5**	**3.1**
$ENOB_{NYQUIST}$ (bit)	**6.8**	**6.15**	**6.24**	**6.8**	**7.1**
$FoM_{NYQUIST}$ (fJ/c.-s.)	**34**	**28**	**80**	**39**	**15**

Table. 5.1Performance summary performance summary and comparison

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Chapter 6 Conclusions and Future Work

6.1 Conclusions

This paper proposes an 8-bit two-channel SAR ADC using the low-skew demultiplexer to avoid complex skew calibration. Its sub-ADCs utilize the energy-efficient two-step SAR ADC with the charge sharing technique and the self-triggered latch technique. This work can achieve a high conversion rate of 1.5GS/s and a low power dissipation of 3.1mW with a 0.9V supply. It results in an FoM of 15fJ/c.-s. The FoM performance of this two-channel ADC is close to that of the previous reported single-channel ADC [3], but its speed is almost double. It is suitable for wireless communication and Ethernet networks applications.

6.2 Future Work

In order to further improve the conversion rate of the proposed time-interleaved SAR ADC, the most intuitive method is to increase the channel number of the sub-ADC. With the proposed low-skew De-MUX, the low-skew characteristic can suppress the skew issue of the time-interleaved ADC even though the channel number rises up. Besides, the layout style and floor plan influence on the conversion rate of the high-speed ADC, the on-chip parasitic capacitance and parasitic resistance caused by the routine metal should be reduced as much as possible [4]. For the

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time-interleave architecture, one of the most important part is the parasitic resistance from the front-end tracking-and-hold circuit (low-skew De-MUX) to the sampling DAC array. It degrades the linearity of the front-end tracking-and-hold circuit seriously. Besides, the different layer metals have different parasitic resistance and parasitic capacitance results from the bandwidth mismatch issue. On the other hand, for the SAR sub-ADC, the nucleus of the SAR ADC is the comparator. In order to optimize the conversion rate of the SAR sub-ADC, the layout of the comparator is the top priority. After finishing the layout of the comparator, the delay time of the SAR logic can match up the comparator. By performing the iteration between layout and simulation, the conversion rate of the high-speed ADC can be optimized.

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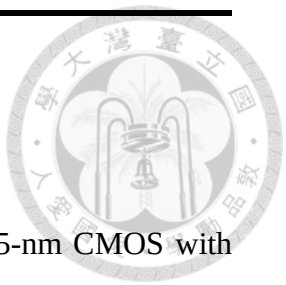

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