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互補式金氧半導體功率放大器之線性化技術研究

Research on Linearization Technique for CMOS Power Amplifier

許譽鐘

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中文摘要

這篇論文將提出一個可以使用在毫米波頻段的改良式線性器，具有改善互補式金氧半導體功率放大器的功能。在此之前所提出的線性器是使用在 40 GHz，並使用了砷化鎵高電子移動率電晶體製程，展現了良好的特性。然而，同樣的架構卻難以在 60 GHz 頻段有效的移植到互補式金氧半導體製程。因此，我們探討了現性器的詳細運作情形，並提出以相位延遲線來改善普通線性器的改進。另外，我們提出了一個偏壓優化的方法，可以保證針對特定功率放大器可以找到最適合的線性器大小及其控制偏壓。

我們使用 90 奈米 LP 互補式金氧半導體來製作一個在 60 GHz 的功率放大器，並且完全的以提升 1 dB 衰減點為目標，來做出優化。量測的結果，功率放大器在增益 1 dB 衰減點呈現了高達 14 %的功率附加效率。並且，其還具有 15 dB 的小訊號增益、13.7 dBm 的增益 1 dB 衰減輸出功率以及 15.4 dBm 的飽和輸出功率。這是我們所知，在所有發表過的電路中，使用互補式金氧半導體製程在增益 1 dB 衰減點有最高功率附加效率的 60 GHz 功率放大器。

關鍵字：功率放大器、60 GHz、高功率附加效率、線性器、V 頻段、前置性衰減、線性化技術

ABSTRACT

In this dissertation, a modified cold-FET pre-distortion linearizer is proposed to improve the linearity of the millimeter-wave CMOS power amplifiers. The previous reported cold-FET linearizer as applied to a 40 GHz power amplifier with a low-loss built-in linearizer in GaAs HEMT technology [6]. However, the effect of the linearizer is not good enough when we try to transplant the technique to 60 GHz using CMOS technology. Therefore, we investigate the operation detail of the linearizer and propose a modified linearizer by adding a delay line. Besides, a bias optimization method that can effectively guarantee the linearity of specific cascode device for power amplifier application is also presented.

A 60GHz cascode power amplifier with modified linearizer is then fabricated under 90-nm LP CMOS technology and fully characterized to enhance its linearity which demonstrated by its extremely well OP_{1dB}. The measurement results of the power amplifier show a power-added-efficiency at OP_{1dB} up to 14% while maintaining 15 dB small signal gain, 13.7 dBm OP_{1dB} and 15.4 dBm P_{sat}. It is the highest power-added-efficiency at OP_{1dB} for millimeter-wave CMOS power amplifiers which ever been published.

Index Terms — Power Amplifier, PA, High PAE, Linearizer, 60 GHz, V-band, Pre-distortion, Linearization Technique

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Chapter 1 Introduction

1.1 Background and Motivation

As the demands for wireless communication technology are growing rapidly recently, higher and higher data rate is required for high speed transmission. Although high frequency and complex digital modulation schemes are solutions for higher data rate communication system, the bottleneck is the linearity of a communication system. Power amplifier, which consumes the most power in a communication system and is the most likely to saturate is the key component that manages the power efficiency and linearity of a communication system. However, traditional linearization techniques are not suitable for high-frequency application and are always complicated. Moreover, the purpose is even more challenged while using CMOS technology because of its higher substrate loss and severe parasitic effect in high frequency band. Our goal is to research possible solution of linearization technique for millimeter-wave frequencies using CMOS technology and design a power amplifier that can achieve excellent performance by the aid of linearization technique.

In the past few years, 7 GHz of contiguous bandwidth have been assigned for unlicensed use at millimeter-wave (MMW) frequencies around 60 GHz in different country, for example U.S. (57–64 GHz) and Japan (59–66 GHz), as shown in Fig. 1.1 [1]. The frequency band planed to be used is called V-band, which is an area that many techniques are still under research. The linearization technique that can help to enhance the precious power performance of power amplifier in the V-band is one of them. Therefore, we would like to develop a linearization technique that can be used in V-band.

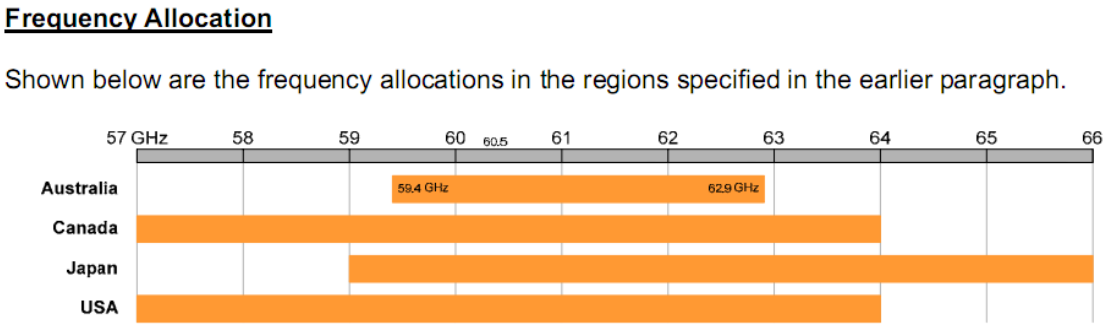


Fig. 1.1 Frequency allocation of different country in V-band [1].

1.2 Literature Survey

As V-band has become a more and more popular frequency band, a lot of power amplifiers for application in V-band are proposed. The power amplifiers have been demonstrated with various monolithic microwave integrated circuit (MMIC) technologies. List of proposed power amplifier on different technologies are shown from Table 1.1 to Table 1.3.

Since HEMT technology has advantages of high electron mobility, power amplifier with more than 27 dBm output power was proposed in 1997 with a 21 % peak power-added-efficiency (PAE) [16] using 0.1 μm pHEMT process. Another circuit demonstrates a even higher peak PAE of 26 % using process 0.15 μm pHEMT process [33]. Since 0.1 μm pHEMT process is a better process than 0.15 μm pHEMT process, the latter PA demonstrate a better design skill and is also practical for commercial use.

SiGe BiCMOS is another technology that provides possible solution for a highly integrated power amplifier in V-band. Some SiGe power amplifier has high peak PAE of 20.9 % with an acceptable output power [35], while some provides higher output power 20 dBm but lower peak PAE [34]. Unfortunately, the latter one has a poor 1-dB-compression output power (OP_{1dB}) of only 13.1 dBm. The largest output power is demonstrated in 2007 with 23.1-dBm saturation power (P_{sat}) [10]. It also demonstrates

good linearity with a 20-dBm OP_{1dB}. However, the PAE only has a value of 6.4% that would consume more DC power.

Table 1.1 V-band power amplifiers on GaAS pHEMT and SiGe BiCMOS process.

Ref.	Topology	Process	Freq. (GHz)	Gain	OP_{1dB}	P_{sat} (dBm)	Peak PAE (%)	Vdd (V)	Area (mm^2)
[16] 1997 JSSCC	2-stage CS	0.1 μm pHEMT	62.5	13	N/A	27.5	21	5	10.35
[33] 2009 IMS	3-stage Cascode	0.15 μm pHEMT	60	17	N/A	27.5	26	6	10.62
[34] 2006 ESSCIRC	2-stage (diff.) Cascode	0.13 μm SiGe	60	18	13.1	20	12.7	4	0.975
[35] 2006 ASSCC	1-stage CS	0.13 μm SiGe	58	4.2	N/A	11.5	20.9	1.2	0.98
[10] 2007 TMTT	2-stage DAT Cascode	0.13 μm SiGe	60	13	20	23.1	6.4	4	3.42

※DC/RF pads are not included

Another most well known Si-based technology is the CMOS technology. The limitation of conductive substrate has been overcome by the smaller gate length which results in higher f_{max}/f_T. The first class of CMOS technology that can be used for designing V-band power amplifier is the 90-nm CMOS technology. A lot of V-band power amplifiers using 90-nm CMOS technology have been proposed from 2007, as listed in Table 1.2. Some have small gain, which is difficult for practical use [17],[19],[21],[24]. Power amplifier constructed with cascode device can provide higher gain and high output power [18], [7], [8]. The milestone is a three stage power cascode power amplifier which can provide gain of 31.3 dB, P_{sat} of 16.2 dBm and peak PAE of 14% [7]. But the power amplifier has poor OP_{1dB} resulted from poor linearity of cascode device. Therefore, some amplifier would use the cascode device for gain stage to

provide higher gain and use common source device for power stage to provide acceptable linearity [14], [28].

Table 1.2 V-band power amplifiers on 90-nm CMOS process.

Ref.	Topology	Process	Freq. (GHz)	Gain	OP_{1dB}	P_{sat} (dBm)	Peak PAE (%)	Vdd (V)	Area (mm^2)
[17] 2007 JSSCC	3-stage CS	90 nm CMOS	60	5.2	6.4	9.3	7.4	1.5	0.15
[14] 2008 ISSCC	1-stage ca. 2-stage CS	90 nm CMOS	60	17	5.1	8.4	5.8	1.5	0.99
[19] 2008 ISSCC	4-stage CS	90 nm CMOS	60	8.3	8.2	10.6	N/A	1.2	N/A
[20] 2008 ISSCC	3-stage CS	90 nm CMOS	62	14.3	10.5	11.5	8.2	1	0.18※
[21] 2008 ISSCC	2-stage CS (diff.)	90 nm CMOS	60	5.6	9	12.3	8.8	1	0.25
[28] 2009 IMS	1-stage ca. 3-stage CS	90nm CMOS	60	20	8.2	12	9	1	0.65
[23] 2009 RFIC	3-stage CS	90 nm CMOS	60	10	8.8	12.6	6.9	1	0.64
[24] 2009 RFIC	3-stage CS	90 nm CMOS	60	4.4	12.1	14.2	5.8	1	1.2
[22] 2010 ISSCC	4-stage CS	90 nm GP CMOS	60	20.6	18.2	19.9	14.2	1	3.25
[18] 2008 JSSCC	3-stage Cascode	90 nm CMOS	51.2	19.5	3.1	8.2	4.2	2	1.13
[7] 2009 MWCL	3-stage Cascode	90nm GP CMOS	50-70	31.3	11.7 (60G)	16.2	14	2.4	0.33
[8] 2008 CSICS	3-stage DAT Cascode	90nm GP CMOS	57-69 (Gain)	26.1	10.5	14.5	10.5 (60 G)	1.8	0.64
			57-69 (Gain)	26.6	14.5	18	12.2 (60 G)	3**	
[9] 2008 RFIC	3-stage CS (diff.)	90nm LP CMOS	58-63	15	10.2	12.5	19.3* (15%)	1.2	0.15※

※DC/RF pads are neglected *for only one chip **2.4 V is nominal value

As to the issue of PAE, some had peak PAE lower than 10 % that would waste too much DC power and not practical for use, which are listed in the top eight columns of Table 1.2. The highest peak PAE of 19.3 % is achieved by a three-stage transformer couple power amplifier with 15 dB gain and 12.5 P_{sat} [9]. However, as shown in the literature, it only has input return loss of 2 dB around 60 GHz, and the highest peak PAE is only achieved by one chip. Power amplifier with distributed active transformer (DAT) can provide 18-dBm P_{sat} and gain of 26.6 dB under 3 V supply voltage with 12.2% peak PAE [8]. A state-of-the-art four stage wikinson combine common source power amplifier is proposed in 2010 [22]. The PAE provides gain of 20.6 dB, OP_{1dB} of 18.2 dBm, P_{sat} of 19.9 dBm, and peak PAE of 14.2 %. The only disadvantage is its large size resulted from wikinson power combiner which is expensive.

45-nm and 65-nm CMOS are more advanced CMOS technology comparing to 90-nm CMOS technology. Since the technologies have higher f_{max}/f_T, almost all the power amplifiers fabricated by the two technologies have peak PAE more than 10 % from 2009, as listed in Table 1.3. Since the two technologies are similar to 90-nm CMOS, some design structures are just the same to those in Table 1.2 [12], [29].

A four-stage common source power amplifier with modified distributed active transformer provides the highest P_{sat} of 17.7 dBm and highest OP_{1dB} of 15.1 dBm among all the circuits designed by the two technologies [27]. Moreover, the power amplifier still has a peak PAE of 14.2 %, gain of 19.2 dB and small size, which shows a possibility for practical use. Another excellent power amplifier is also proposed in 2010, which provides P_{sat} of 14.5 dBm and OP_{1dB} of 11.2 dBm and gain of 20 dB [30]. Since the peak PAE is nearly 15%, it is more efficient than the former one. The best power amplifier is fabricated on the 65-nm SOI CMOS process [32]. The technology is one of the best and most expensive Si-based technologies. By the excellent performance of the

technology, the power amplifier provides gain of 16 dB, P_{sat} of 14.5 dBm and OP_{1dB} of 12.7 dBm and amazing peak PAE of 25%.

Table 1.3 V-band power amplifiers on 65-nm and 45-nm CMOS process.

Ref.	Topology	Process	Freq. (GHz)	Gain	OP_{1dB}	P_{sat} (dBm)	Peak PAE (%)	Vdd (V)	Area (mm^2)
[25] 2008 RFIC	3-stage CS	65nm CMOS	62	4.5	6	9	8.5	1	N/A
[12] 2009 ISSCC	3-stage CS (diff.)	65nm CMOS	57-64	15.8	2.5	11.5	11 (58 G)	1	0.05※
[26] 2010 SIRF	4-stage CS	65nm CMOS	58	13.4	12.2	13.8	7.6	1.2	1.28
[27] 2010 ISSCC	4-stage CS	65nm CMOS	60	19.2	15.1	17.7	11.1	1	0.83
[29] 2010 JSSCC	3-stage CS (diff.)	65nm CMOS	62	15.5	4	11.5	15.2	1	0.05※
[32] 2010 JSSCC	2-stage Cascode	65nm SOI CMOS	60	16	12.7	14.5	25.7	1.8	0.04※
[31] 2009 CSICS	2-stage Cascode	45nm CMOS	60	16	7.6	12	12.3	1.8	0.018※
			60	17	8.7	13.5	13.4	2.1	0.018※
[11] 2009 ISSCC	2-stage CS	45nm LP CMOS	50-67	6	11	13.8	7	1.1	0.06※
[30] 2010 RFIC	3-stage Cascode	45nm CMOS	60	20	11.2	14.5	14.4	2	0.04※

※DC/RF pads are not included

1.3 Contributions

This dissertation presents the research on the pre-distortion linearization technique for power amplifier in V-band using silicon-based 90-nm LP CMOS process. A modification to conventional cold-FET linearizer is proposed. The modification is to connect gate and drain of conventional linearizer together with a delay line with certain phase delay. The modification highly improved the pre-distortion function, and helps

the linearizer to be transplanted to CMOS process from pHEMT process. An attempt of large signal analysis is performed in the investigation of possible effects resulted from the modification. Large signal analysis provides another path to understand the larger signal operation of non-linear device. Based on large signal analysis, we found the cause of three extra effects. The analysis also helps us to choose the proper phase delay, making a compromise between performance and chip size.

The stronger pre-distortion function of modified linearizer can hence be performed in high frequency on 90-nm LP CMOS process. We then try to verify its effectiveness by equipping it on two-stage power amplifier in V-band. Even under the disadvantages of CMOS process and the frequency we want to apply is a higher frequency that is more challenged, the great performance of modified linearizer can still help the power amplifier to have a better power performance. The design flow of inserting a pre-distortion linearizer to a multi-stage power amplifier is introduced. The design flow can ensure an effective design process and good performance. We also develop a device selection process for linearizer that can help us with choosing a most suitable linearizer for certain power amplifier.

The measurement result demonstrates a great power performance. It can provide P_{sat} of 15.4 dBm and OP_{1dB} of 13.7 dBm with an acceptable gain of more than 15 dB. It also has peak PAE value of 16% and 14% at OP_{1dB}. To our best knowledge, it is the CMOS power amplifier that has highest PAE at OP_{1dB} in V-band. Besides its good linearity, the power amplifier can also provide comparable peak PAE and saturation power to other power amplifiers using better technologies. In addition, this is the first amplifier that applies the pre-distortion linearizer under CMOS process in V-band.

1.4 Dissertation Organization

The organization of this dissertation is outlined as follows:

Chapter 2 provides an overview of the important parameters and linearity issue of power amplifier. The introduction of important parameters helps us to understand the trade-off between several figure-of-merits.

Chapter 3 discusses a per-distortion linearization technique and introduces a low loss build-in linearizer based on HEMT process [6]. The operation principle is investigated. Based on the investigation, we propose a modification to the linearizer and give an intuitive explanation of its effectiveness. After a carefully examination, we find that there are three effects resulted from the modification. Examinations of the effects provide an instruction of selecting proper parameter of modification.

Chapter 4 presents the implementation process of a two-stage power amplifier with modified linearizer. Practical design process is provided and a bias optimization method of linearizer for specific power amplifier is proposed. A two-stage power amplifier is fabricated and measured to certify the effectiveness of linearizer. We then debug the negligence of simulation to make the measurement and simulation result to be similar.

The conclusions are drawn in Chapter 5.

Chapter 2 Linearity of MMW Power Amplifier

The chapter introduces the important component in transceiver system, called power amplifier. Important parameters and brief design flow will be introduced in the first section. However, since the objective of this literature is to improve the linearity of power amplifier, the resources of non-linear effect would be investigated.

Several linearization techniques have been developed to enhance the linearity of power amplifier and overcome the critical demand of linearity in communication system using complex digital modulation schemes. These linearization techniques including feedback, feed-forward, pre-distortion and post-distortion are introduced.

2.1 Introduction of Power Amplifier

2.1.1 Introduction

Power amplifier is one of the most challenged and important building blocks in RF communication system. As shown in Fig. 2.1, power amplifier is usually placed in the end of the active part of communication system. Therefore, it acts as the component that should provide largest output power, which should large enough overcome the loss of antenna and the free space.

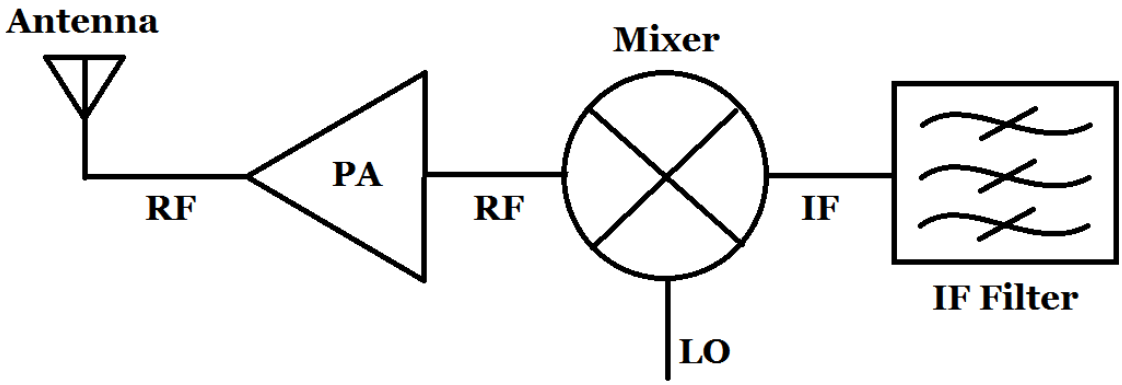


Fig. 2.1 Simplified building blocks of conventional communication system.

2.1.2 Important Parameters

Important design parameters of power amplifier include output power, gain, linearity, and power added efficiency (PAE). We should notice that the input power under which the parameters are described is important. Taking output power for example, the description of output power includes the output power at 1-dB-compression point and saturation output power, which are the output power described under different phenomena.

Moreover, the premise of the above mentioned parameters is to have a stable power amplifier. Therefore, we should ensure the power amplifier is stable. However, once the amplifier is stable, we don't have to pay much attention on it. Followings are the introduction of the parameters.

A. Output power

Needless to say, the main objective of power amplifier is to provide enough output power that can transmit RF signal to the distance we want and can overcome the loss introduced by free space and antenna. For the basic understanding, if we can use the device that is large enough and equipped with a good output matching network, we can provide no matter how much output power we want. The highest output power level that a power amplifier can provide is called the saturation output power (P_{sat}). The parameter can help us to measure the potential ability of the devices we use and also take the loss of output matching network into account.

However, power amplifier would encounter some non-ideal effect as the output power is getting larger. Those effects would make the gain of power amplifier to be reduced and the amplifier would have no gain at the largest output power. As a result, although it can provide high output power, we have to apply equal input power level to the PA, which means the power amplifier is nuisance of communication system.

In order to consider linearity and output power level simultaneously, we would consider the output power at which the gain has an 1-dB-compression. We call it 1-dB-compression output power (OP_{1dB}). In some cases, we would also consider the input power at which the output power is at OP_{1dB}. We call it input 1-dB-compression point (IP_{1dB}). The two parameters has the benefits of define the largest output power that power amplifier still have linear gain when considering the linearity issue of power amplifier.

B. Linearity

The linearity consideration includes the parameters like AM-AM distortion, IP3, IMD3, ACPR and EVM. They can be roughly categorized as the non-linearity resulted from one-tone, two-tone and n-tone input signal. The first parameter is under the first category. The second one and the third one are under the second category while the last two parameters are under the third category. The definition and the cause of the parameters will be introduced in next section.

C. Power-added-efficiency

The efficiency is the most suitable parameter to measure the trade-off between DC-consumption and output power level. There two methods for calculating the efficiency of power amplifier. The first one is called drain efficiency while another one called power-added efficiency, which are defined respectively as

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.1}$$

and

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}. \tag{2.2}$$

, where P_{out}, P_{in}, P_{DC} are output power, input power and DC consumption respectively.

The difference between the two definitions is the consideration of input power. The definition of drain efficiency only focuses on the ratio of transform dc power to output power. If the power amplifier has no gain but has large output power, we can still have high drain efficiency. This means the definition cannot honestly reflect the practicability of power amplifier. It only focuses on the ratio of signal current swing to dc current at output port of power amplifier.

On the other hand, power added efficiency calculates the ratio of the extra-added power to the dc consumption. The definition considers the amount of extra power the power amplifier can add on the input power. This perspective can rule out the possibility that the power amplifier has no gain and consider the signal power that power amplifier can contributes to whole communication system. The larger the PAE, more RF power is transformed from the dc power.

2.2 Linearity Consideration of Power Amplifier

2.2.1 Nonlinear Distortion Characterization

We usually approximate the characteristic of power amplifier to with a linear model when the amplitude of signal is small comparing to the dc value. However, when the amplitude is comparable to the dc value, the linear model is not suitable because the operation point on which the linear model depends on has been changed.

For consideration of linearity issue, we can use polynomial equation to describe the non-linear characteristic. Since the order more of three usually has small influence to the linearity issue, we would use the third order approximation, which is formulated as

$$y(t) \approx k_1 \cdot x(t) + k_2 \cdot x^2(t) + k_3 \cdot x^3(t) \tag{2.3}$$

, where k_i represents the coefficient for order i.

2.2.2 AM-AM Characteristic

When a sinusoidal signal, which is

$$x(t) = A\cos\omega t \tag{2.4}$$

, is fed to the input of power amplifier, the output signal will be

$$y(t) = k_1 A\cos\omega t + k_2 A^2\cos^2\omega t + k_3 A^3\cos^3\omega t\ . \tag{2.5}$$

Rewrite the equation and organize it according to its frequency, we can have

$$y(t) = \frac{k_2 A^2}{2} + \left(k_1 A + \frac{3k_3 A^3}{4}\right)\cos\omega t + \frac{k_2 A^2}{2}\cos 2\omega t + \frac{3k_3 A^3}{4}\cos 3\omega t\ . \tag{2.6}$$

The coefficient in equation (2.6) that is combined with the $\cos\omega t$ is the fundamental term of output signal. Other coefficients combined with other higher frequency signals $\cos n\omega t$ are the amplitudes of *n*th-order harmonics.

Divide the coefficient of fundamental term of output signal by that of input signal is the value of fundamental gain, which can be represented as

$$Gain = \frac{\text{Output Fundamental}}{\text{Input Fundamental}} = \frac{\left(k_1 A + \frac{3k_3 A^3}{4}\right)}{A} = k_1 + \frac{3k_3 A^2}{4} \tag{2.7}$$

The numerator has a term proportioning to A^3, which would have a relatively small value when A is small. Therefore, the gain would be a constant value at small input power, which is called linear gain. However, as the input signal with larger amplitude is fed, the term can hardly be neglected. Since the coefficient k_3 always has a negative value, the value of gain will be reduced and results in a compression of it.

For description convenience, we define the output power at which the gain has been reduced by 1dB as 1-dB compression output power (OP_{1dB}). The corresponding input power is called 1-dB compression input power (IP_{1dB}). As shown in Fig. 2.2, when the output power has departed from the expected output power by 1 dB, the output

power there is the OP_{1dB}.

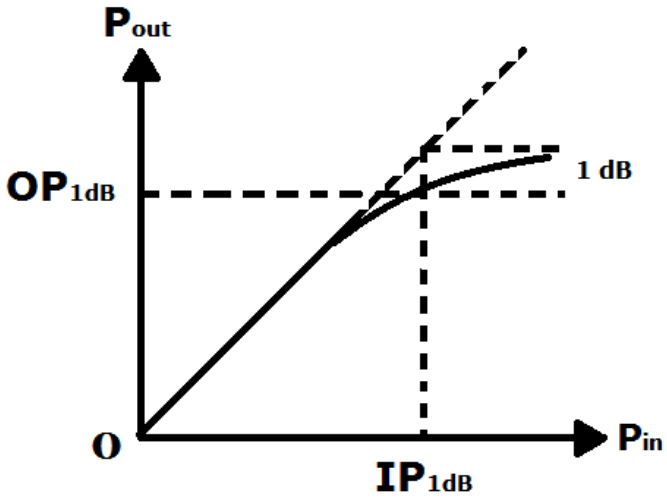


Fig. 2.2 Definition of input and output 1-dB compression point.

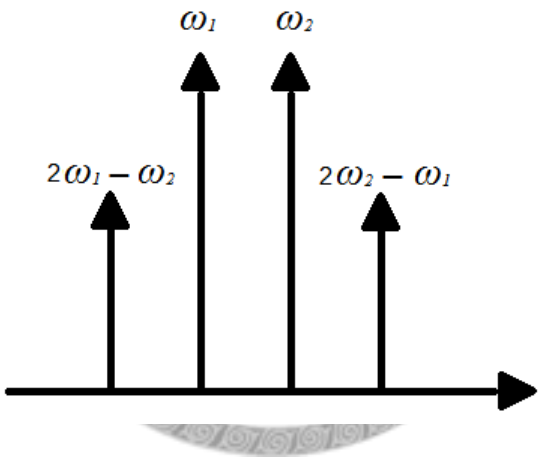


Fig. 2.3 Spectrum around fundamental tone after intermodulation.

2.2.3 Nonlinearity from two-tone input signal

Instead of feed the signal with single frequency to power amplifier, feeding two signals with slightly different frequencies can produce some mixing products called intermodulation (IM). The signal with two different frequencies but equal amplitude is

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)\,. \tag{2.8}$$

Apply the signal to equation (2.3) and expand the result according to different frequencies can have the spectrum with signals of different frequencies including ω_1, ω_2, $2\omega_1$, $2\omega_2$, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, $2\omega_2 \pm \omega_1$, $3\omega_1$, $3\omega_2$. However the frequency that influences

the fundamental tone ω_1 and ω_2 most, are the signals with frequency $2\omega_1 \pm \omega_2$, $2\omega_2 \pm \omega_1$. The spectrum around fundamental tone is shown in Fig. 2.3. The value of fundamental tone ω_1 and ω_2 is

$$k_1 A + \frac{9}{4} k_3 A^3 \tag{2.9}$$

, and the value of harmonics $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ is

$$\frac{3}{4} k_3 A^3 . \tag{2.10}$$

A. Third –order intermodulation ratio

The third-order intermodulation ratio (IMD3) is defined as the ratio of the amplitude of the third-order term of output signal to the linear fundamental term, which is

$$IMD3 = \frac{P_{fundamental}}{P_{IMD}} = \frac{P(\omega_1, \omega_2)}{P(2\omega_1 - \omega_2, 2\omega_2 - \omega_1)} = \frac{k_1 A}{\frac{3}{4} k_3 A^3} = \frac{4k_1}{3k_3 A^3} \tag{2.11}$$

The value can be calculated under different power level. For different power level, there is a corresponding IMD3. Specification of some communication standard would require the output power level to be measured under the IMD3 that is more than certain value.

B. Third-order intercept point (IP3)

Unlike IMD3, IP3 is a certain point that the value of third-order harmonics is the same to value of fundamental. The equation is given by

$$|k_1| A_{IP3} = \frac{3}{4} |k_3| A_{IP3}^3 . \tag{2.12}$$

When we refer the IP3 to input power and output power, it is called IIP3 and OIP3 and formulated as

$$IIP3 = A_{IP3} = \sqrt{\frac{3}{4}\left|\frac{k_1}{k_3}\right|} \tag{2.13}$$

and

$$OIP3 = k_1 A_{IP3} = \sqrt{\frac{3}{4}\left|\frac{k_1^3}{k_3}\right|} \tag{2.14}$$

,respectively.

If we draw the power of fundamental term and harmonic versus input power level respectively, the interception of the two curves is IP3, as shown in Fig. 2.4.

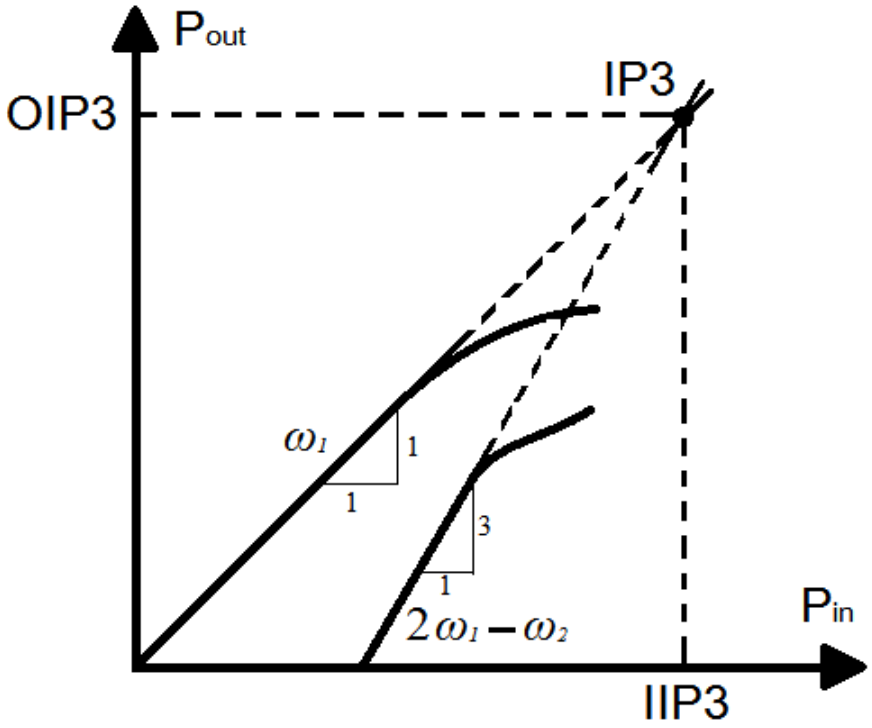


Fig. 2.4 Definition of third-order interception point.

Chapter 3 Cold-FET Linearizer with Delay Line

The objective of this chapter is to propose a modified low-loss build-in cold-FET linearizer for millimeter-wave CMOS power amplifier. Since the conductive substrate and severe parasitic effects of CMOS process will severely degrade the performance of conventional cold-FET linearizer in V-band, the modification is developed to overcome the difficulties.

Based on the modification, we successfully enhance the performance of the cold-FET linearizer and simultaneously maintain a low insertion loss even under the conductive substrate of CMOS process. To the best of our knowledge, this is the first demonstration of the pre-distortion technique to CMOS power amplifier for V-band.

The chapter first explains some general consideration of a pre-distortion linearizer, including the operation details, design criteria and the method to choose a proper linearizer for a specific power amplifier. Secondly, the operation details of the cold-mode linearizer will be introduced. The key point of exhibiting pre-distortion function is the saturation region of transistor. There are several difficulties to implement the conventional pre-distortion linearizer in CMOS technology for millimeter-wave frequencies.

In order to solve the difficulties, a modification to the cold-mode linearizer is proposed and gives an intuitive interpretation to its benefit. However, the modification has additional effects that need to be considered more carefully. Two major effects are assumed and described in detail. Mathematic equations are developed to find out the cause of the effects by observing the operation of the modified linearizer. Finally, more guide lines are proposed for choosing parameters of modified linearizer.

3.1 Pre-distortion Linearizer

This section will introduce the operation of the pre-distortion linearizer for a amplifier. Moreover, some important points about power performance curve of linearizer should be considered. Observing those points can help us to identity the performance of pre-distortion linearizer and to know whether the linearizer is suitable for a specific power amplifier. Finally, the method to place the linearizer on the best point of a multi-stage power amplifier will also be discussed.

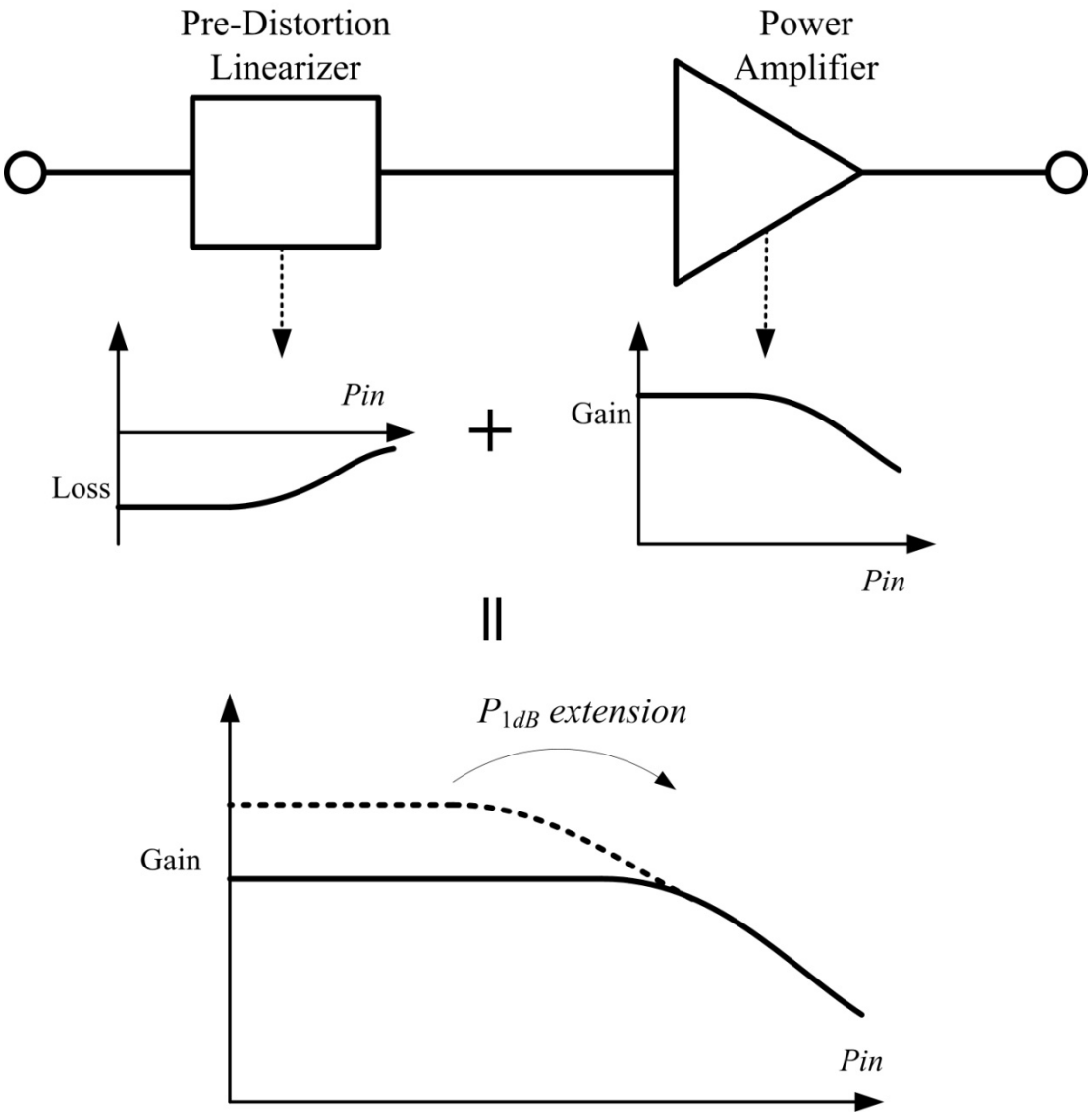


Fig. 3.1 Pre-distortion effect by cascading power amplifier with a linearizer.

3.1.1 Pre-distortion Technique

The principle of pre-distortion linearization technique is shown in Fig. 3.1. The power amplifier usually suffers from gain compression at high power level, which results in signal distortion. On the other hand, the pre-distortion linearizer has a constant loss at low input power level and has lower loss when input power level is high. After combining the two different tendencies of gain characteristic by cascading the two building blocks, we can have a power amplifier with larger linear output power region, which called gain extension.

Fig. 3.2 shows the comparison of the power performance of a power amplifier with and without pre-distortion linearization technique. The pre-distortion effect can postpone the gain compression point. Since the PAE increases more rapidly around 1-dB compression point, PAE at 1-dB compression point can be improved significantly. With the higher PAE, the power amplifier can have a higher output power under the same DC consumption.

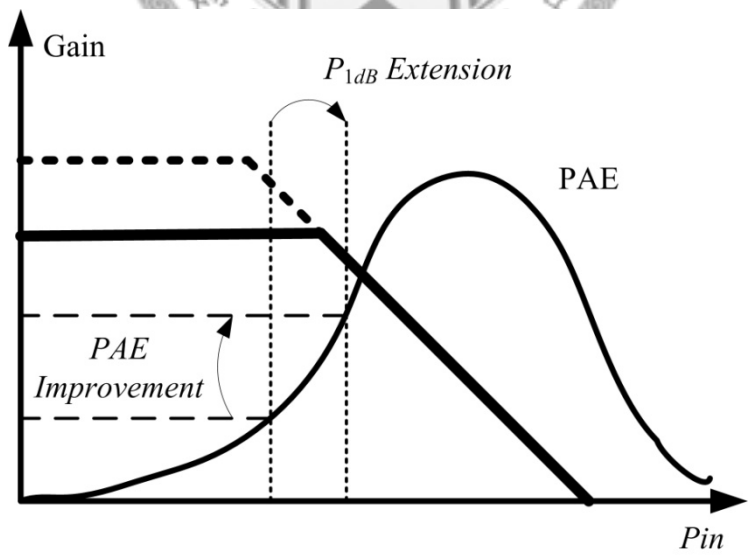


Fig. 3.2 Gain characteristics of power amplifier with and without pre-distortion technique.

3.1.2 Loss Characteristic of Pre-Distortion Linearizer

Different power amplifiers have different power performances. Therefore, it is impossible for a linearizer to be suitable for every power amplifier. Since the objective of a pre-distortion linearizer is to improve the power performance of power amplifier, we have to investigate the power performance of linearizer. The loss deviation of linearizer is the resource of pre-distortion effect. We should observe on the loss characteristic curve of linearizer.

Fig. 3.3 shows the loss versus the output power of a pre-distortion linearizer. The reason to define output power as x-axis will be introduced in following section. We should focus on three features which can be used to define the performance and specifications of a pre-distortion linearizer.

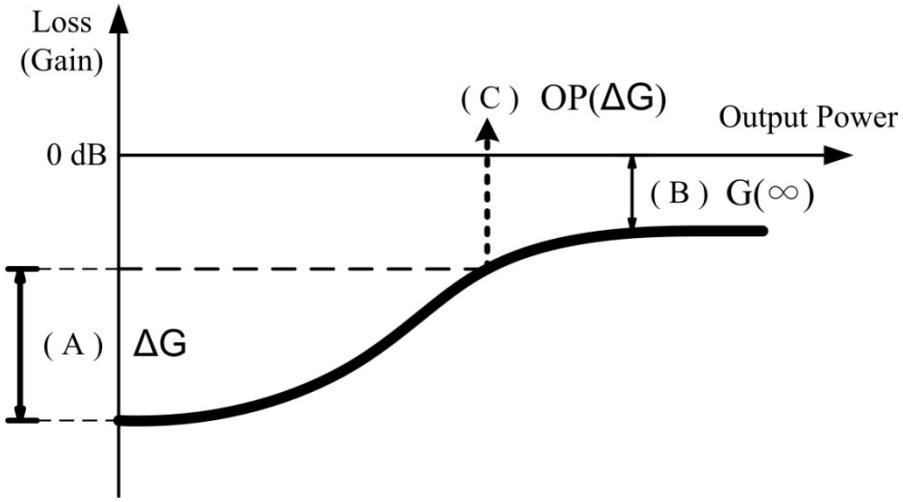


Fig. 3.3 Loss characteristic of a linearizer

A. Larger gain (loss) deviation:

A larger gain (loss) deviation can compensate more gain compression of a power amplifier. It means we can have stronger gain extension effect and make the power amplifier reach a higher OP_{1dB} and PAE. On the other hand, since the loss at high power level is decided by intrinsic factor, which cannot be changed by choosing device size or

control voltage, the small-signal loss is the high power loss minus loss deviation. Therefore, we should consider whether the gain of power amplifier is larger enough, and check whether the small signal loss is a burden to the link budget. The severe small-signal loss may need to be compensated by an extra gain stage, and degrade the PAE. Moreover, even though the loss deviation is large enough, the slope of loss deviation should not be too high. It is because the slope of loss deviation which is higher than that of the gain compression of power amplifier will result in a composite power performance curve that is not flat.

B. Lower loss at high input power level:

The application of pre-distortion linearizer will definitely introduce extra loss. The loss is an inevitable disadvantage when we want the loss characteristic of pre-distortion linearizer. Ideally, the loss of linearizer should be zero at the power level at which the cascaded power amplifier reaches its OP_{1dB}. However, because of the intrinsic operation process of linearizer, there must left some power loss at the high power level. Since the key object of introducing linearizer is to improve the linearity and make the value of OP_{1dB} higher, the loss at the high power level would reversely damage the goal. We can regard the phenomena as the loss of linearizer overwhelms the improvement of output power.

C. Low output power with enough gain (loss) deviation:

Since the linearizer is directly cascaded with a power amplifier, alike the link budget consideration of cascade multi-stage power amplifier, the output power of the linearizer should be at some adequate value that can support the operation of power amplifier. When the oscillation ability of a device is weak, linearizer can only reach enough loss deviation value at a high output power level. In this condition, the linearizer is only suitable for a large power amplifier. In addition, the amount of power consumed

by it will be relatively large.

In another condition that the linearizer can reach enough loss deviation at low power level, it can be suitable for a small power amplifier. If the size of power amplifier is larger, we can parallel several devices together to form a large linearizer which can provide enough power for power amplifier. For another solution, we can add another stage in front of power amplifier and put the linearizer at a low power level point.

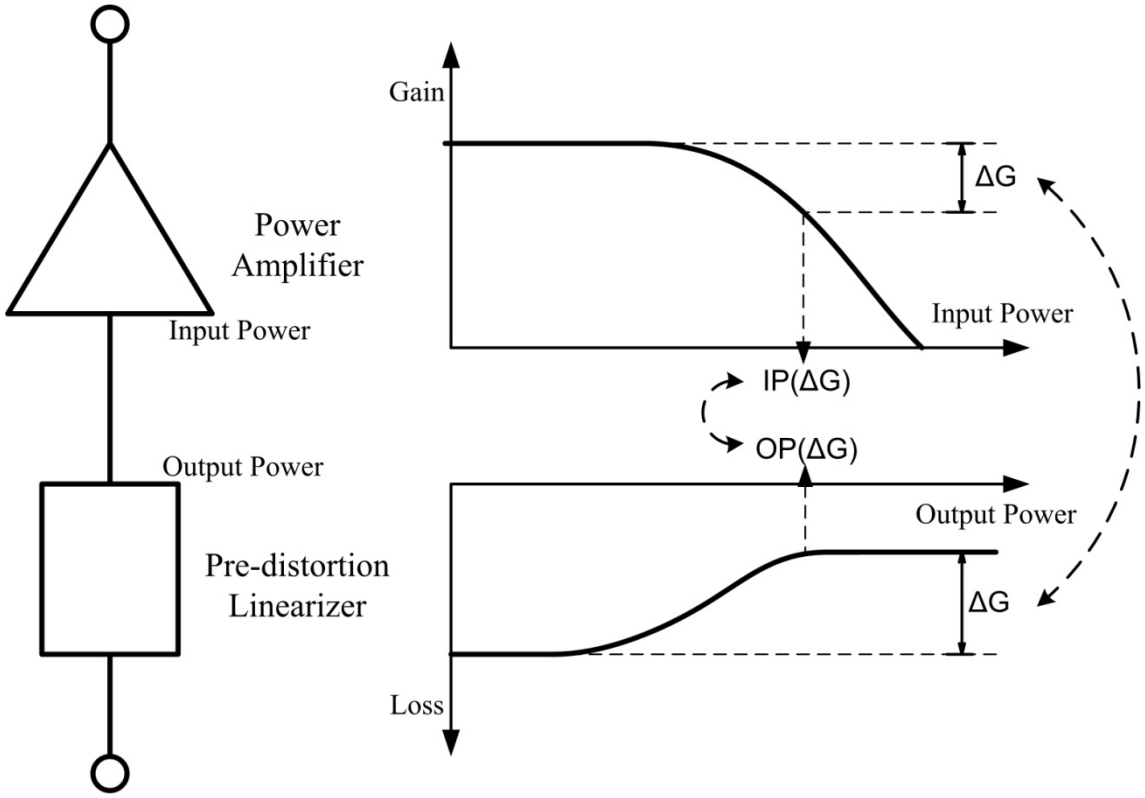


Fig. 3.4 Consideration of cascading a linearizer with a power amplifier.

3.1.3 Cascading with Power Amplifier

The influence of output power range of linearizer when cascading with a power amplifier has been discussed before. Here we will illustrate the guide line to cascade the two building blocks. There are two set of values of pre-distortion linearizer and power amplifier that should be the same simultaneously. The first set is the output power value of linearizer and input power value of power amplifier, and the second set is the loss

deviation value of linearizer and gain compression value of power amplifier. Fig. 3.4 clearly tells us the concept. The output power of pre-distortion linearizer when having enough loss deviation should be equal to the input power of power amplifier when have the same amount of gain compression.

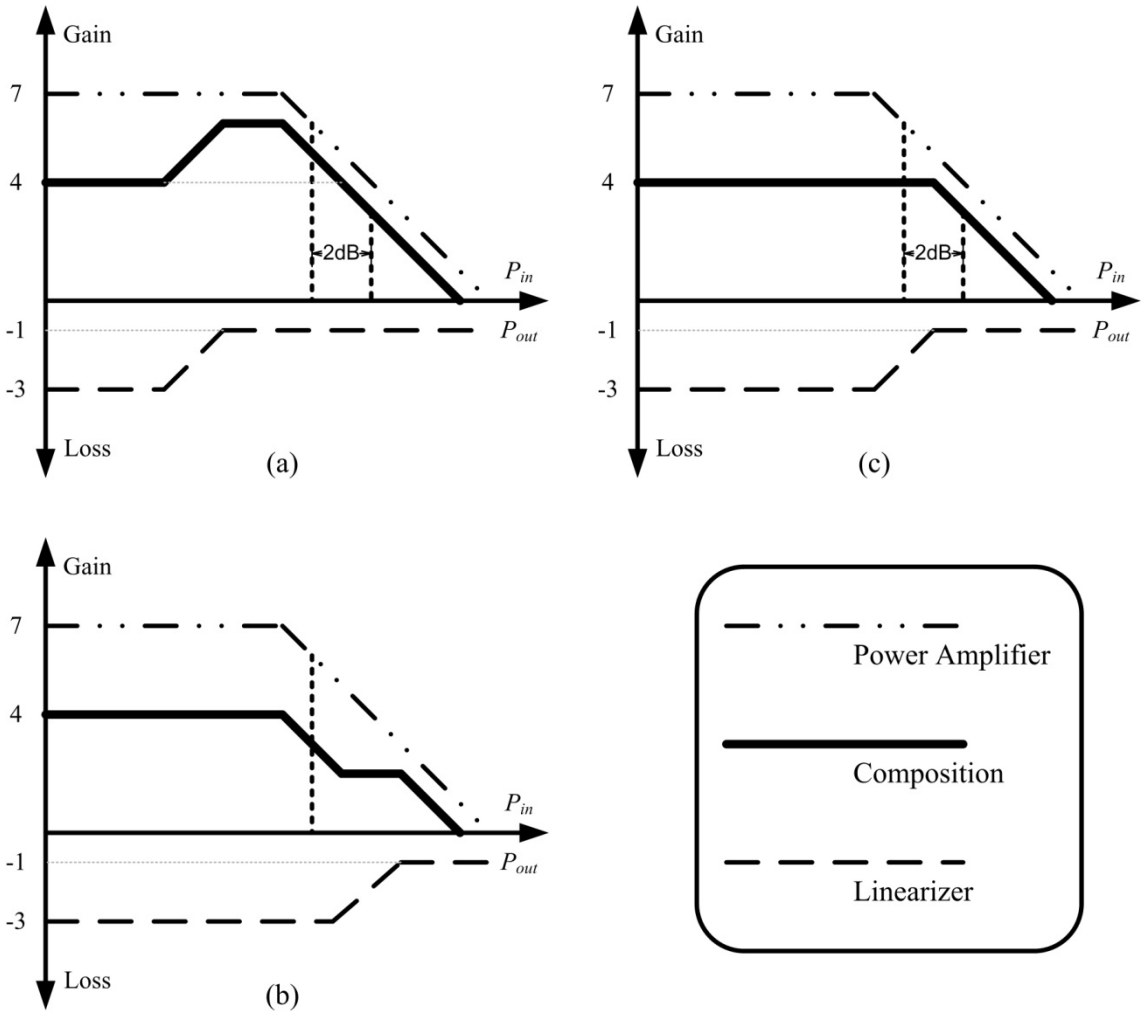


Fig. 3.5 Composite power performance for that the output power level of linearizer is (a) lower than (b) higher than, and (c) equal to the input power of power amplifier at 1-dB compression point.

Fig. 3.5 shows characteristics of the composite power performance for that for that the output power of linearizer is higher than, lower than and equal to the input power of the power amplifier at 1-dB compression point. At Fig. 3.5 (a), the early rising of loss deviation makes the composite power performance has a convex around the gain

compression point. The uneven curve has an improvement of IP_{1dB} when calculating the 1-dB compression point according to small-signal gain. However, some people will calculate it according to the peak gain value. This makes the point of OP_{1dB} unchanged.

On the other hand, as shown in Fig. 3.5 (b), if output power of linearizer is high, the linearizer provides enough loss deviation too late, hence has nothing benefit to power amplifier. The predicted gain extension effect would not happen. Finally, Fig. 3.5 (c) shows the adequate output power level of linearizer. When we want to improve the power performance of a specific power amplifier, we therefore should choose the linearizer that has the loss characteristic curve perfectly match to the gain curve of power amplifier.

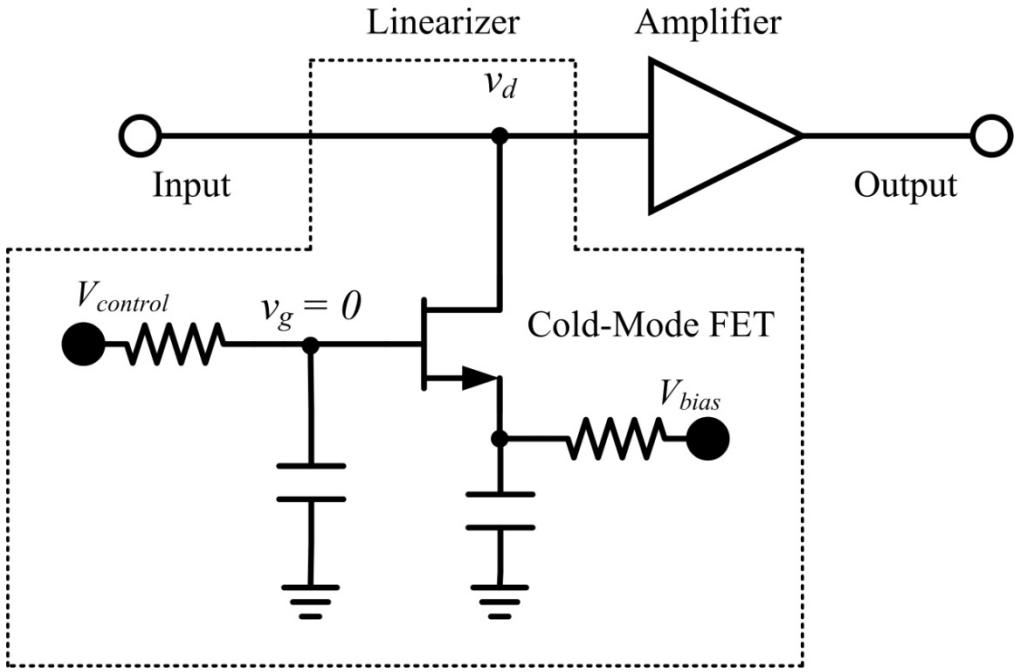


Fig. 3.6 Former proposed cold-FET linearizer [6].

3.2 Cold FET Linearizer

3.2.1 Introduction

In order to achieve the function of pre-distortion, we need to find a device that has a constant loss for low input power and a lower loss for higher input power. A MMIC low-loss built-in linearizer that has pre-distortion characteristic has been demonstrated by GaAs pHEMT, which is a parallel transistor operated in cold-mode [6]. The cold-mode means the transistor has zero drain-to-source voltage ($V_d = V_{bias}$), thus it requires zero dc consumption. The structure is shown in Fig. 3.6.

At large-signal operation, the cold-mode FET has gain expansion characteristic which can compensate gain compression of the power amplifier. In addition, since the gate bias of transistor exceeds the threshold voltage (V_{th}), the drain and source voltages are likely to be equal. Therefore, the bias voltage of the following cascaded amplifier can be fed directly through the linearizer. No additional bias circuit for next stage amplifier is needed.

3.2.2 Operation Principle

Thick line of Fig. 3.7 is the DC-IV curve of a transistor biased under some specific gate voltage. The bias point of a transistor biased under zero drain-to-source voltage condition is the point at the origin of Fig. 3.7. Considering the different characteristics between the triode region and the saturation region on the curve can help us to understand the operation of cold-FET linearizer.

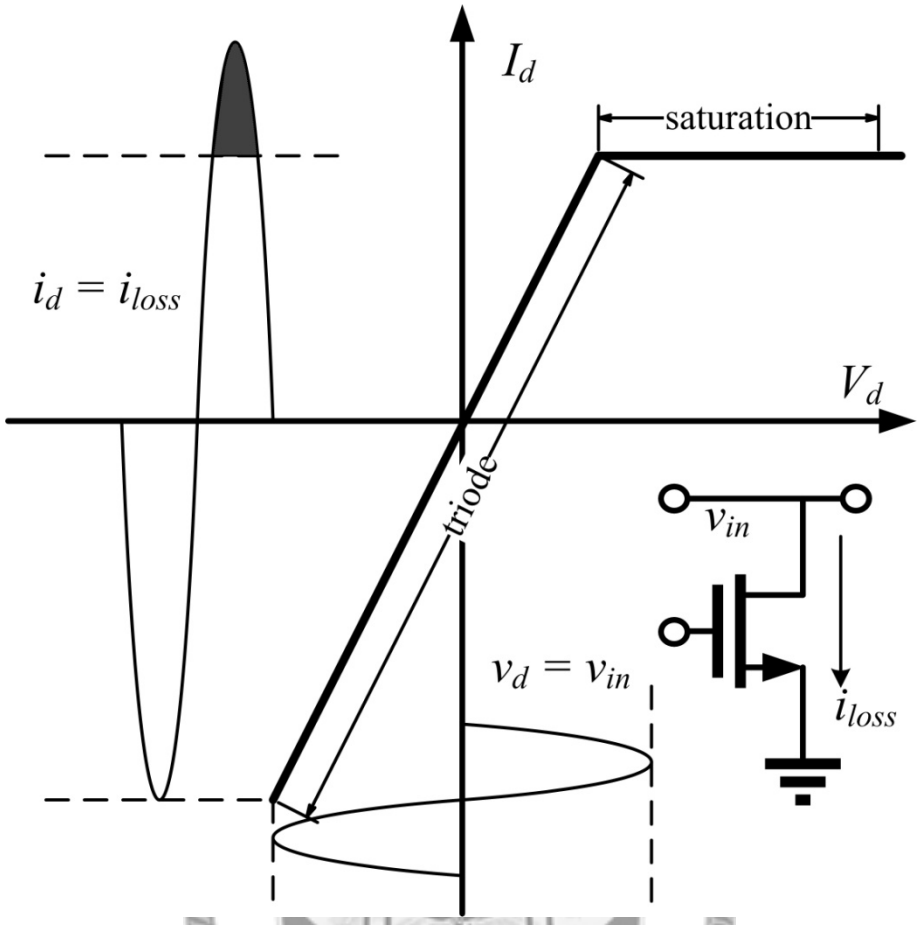


Fig. 3.7 Operation of linearizer along DC-IV curve

When the swing of signal voltage is small, the operation of the parallel transistor biased under cold-mode can be modeled as a resistor whose value is defined by its gate voltage. The value of the resistor value is

$$R_{ds} = \frac{1}{k \times (V_{GS} - V_{th})} \tag{3.1}$$

Since the gate voltage V_{GS} remains unchanged when input voltage signal is swinging, the drain resistor R_{ds} is always a constant value. Therefore, the amount of signal current flowing into the transistor will vary along a constant slope DC-IV curve at triode and deep-triode region, and exhibit a constant loss.

However, since the drain current of transistor is unlikely to change with drain voltage when transistor operates in saturation region, current flowing into linearizer will

not getting larger when input voltage swing over the saturation region. The voltage threshold for transistor to enter saturation region is

$$V_{ds} > V_{gs} - V_{th} \tag{3.2}$$

Based on the characteristic, the loss will become smaller when the input power level is high enough. It is because once the voltage value of the swing exceeds the saturation threshold, the linearizer cannot force more signal current to flow into it. Therefore, the cut-off part of current swing will occupy a larger ratio when the voltage swing at drain is getting larger. That means it will have smaller ratio of leakage current and exhibit smaller loss. We can call it cut-off effect, which is shown as the black part at the top of drain current swing in Fig. 3.7.

In conclusion, the saturation region provides a lower loss in high input power level while the triode region provides constant loss in low input power level. Since the cold-mode linearizer has a characteristic that meets the requirement of pre-distortion, it can help the power amplifier to have a larger linear output power region and a higher PAE at OP_{1dB}.

Moreover, since DC-IV curve of the transistor is asymmetry for positive and negative drain-to-source voltages, only positive voltage swing can really cause the gain extension effect when the transistor enter saturation region. Negative voltage swing can only force transistor to operate under deep-triode region, and provides a constant loss because of its similar slope comparing to operation under triode region.

3.2.3 Challenge of CMOS Process in V-band

The formerly introduced cold-mode linearizer was implemented on GaAs pHEMT technology has superior performance due to the higher electron mobility, higher breakdown voltage, and the availability of high quality-factor passive

components.

On the other hand, the CMOS technology is one of the most important and widely used processes today. It has advantages like small size, repeatability, productivity and high-level integration. Since the size and cost are important design issue, modern CMOS technology is really attractive for MMW applications. If we want to make the pre-distortion technique more applicable, to transplant the conventional linearizer from III-V technology to CMOS technology is a possible solution.

However, although CMOS technology has already widely used in several area, they are just applications in lower frequency, in which the performance of CMOS is good enough to meet the specifications. If we want to simultaneously take advantages of CMOS technology and maintain acceptable performance, followings are some issues we would encounter when trying to transplant the cold-mode linearizer concept from pHEMT technology to CMOS technology.

A. High loss of conductive substrate

The CMOS technology is fabricated on a conductive substrate. Comparing with the semi-insulating substrate of III-V technology, the lossy substrate of CMOS is really a hardship for a same design to have similar performance. For example, the loss of linearizer at high input power level is one of design criteria of linearizer, as the second criteria shown in Fig. 3.3. The lower loss, the higher loss deviation can be accomplished. The loss substrate will damage the performance of linearizer.

B. Low maximum oscillation frequency fmax

The CMOS technology has lower electron mobility than III-V technology, and hence has lower fmax. This means the oscillation ability at high frequency like V-band is weaker and also not good enough for the voltage swing to follow the expected curve of Fig. 3.7. The cut off function which make the loss deviation to be accomplished will

also be not obvious.

C. Severe parasitic effect

V-band is a millimeter-wave frequency that the fatal parasitic effect is relatively severe. The severe parasitic effect in V-band can highly detract the performance of linearizer because extra losses would overwhelm advantages introduced by linearizer and results in fewer output power and lower PAE.

All the above mentioned difficulties are the intrinsic problems that cannot be overcome by device selection or other design flow. We should otherwise try to improve the effectiveness of gain extension characteristic, which can be achieved by enhance the loss deviation ability and make the loss begin to decrease earlier. For the above mentioned purpose, a modification of cold-FET linearizer that can ensure the gain extension function is introduced in next section.

3.3 Modified Cold-Mode Linearizer Using Delay Line

In this section, we will propose the criteria for examining the performance of pre-distortion linearizer and provide the guide line to develop a modification that can effectively improve the performance of cold-mode linearizer. According to the guide line, we choose delay line as the solution and provide an intuitive interpretation to its benefit. However, we notice that the modification has extra benefit that can improve the pre-distortion function. Therefore, the mathematic equations of both advantages are formulated and their composite effect is analyzed. Finally, the figure that can best demonstrate performance of a linearizer is introduced. We will compare the conventional and modified linearizers by using the figure and hence verify the effectiveness of the proposed modified linearizer.

3.3.1 Guideline to Develop a Modified Linearizer

The modification for the linearizer is based on the knowledge that if the transistor is more likely to reach saturation region while input signal is getting larger, it can have a sharper gain deviation slope and earlier up-rising curve, hence more effectively compensates the gain compression slope of power amplifier. The condition that transistor should satisfy at saturation region has been shown at equation (3.2).

The conventional linearizer only utilizes drain-to-source voltage V_{ds} to force the transistor into saturation region [6]. However, as we can see in the equation (3.2), the gate-to-source voltage V_{gs} is also effective to force the transistor into saturation region. We can rewrite equation (3.2) as

$$V_{ds} - V_{gs} > -V_{th}. \tag{3.3}$$

If we want the saturation region to be reached earlier, we can otherwise increase the term faster while the power level is getting higher. Therefore, the linearizer will have a sharper loss characteristic and reach enough gain deviation at lower power level.

3.3.2 Modified Cold-Mode Linearizer

Based on the guideline, a pre-distortion linearizer with an effective modification is proposed. Fig. 3.8 shows the schematic of the modified linearizer. The proposed linearizer is modified by adding an extra delay line connecting drain and gate of the core transistor. The delay line can provide a phase delay of θ, and produce a voltage signal swing at gate, unlike the signal ground of conventional linearizer at gate. Comparing with Fig. 3.6, the modified linearizer does not need extra passive component except the delay line. We can consider the modification as a trade-off between performance and chip size.

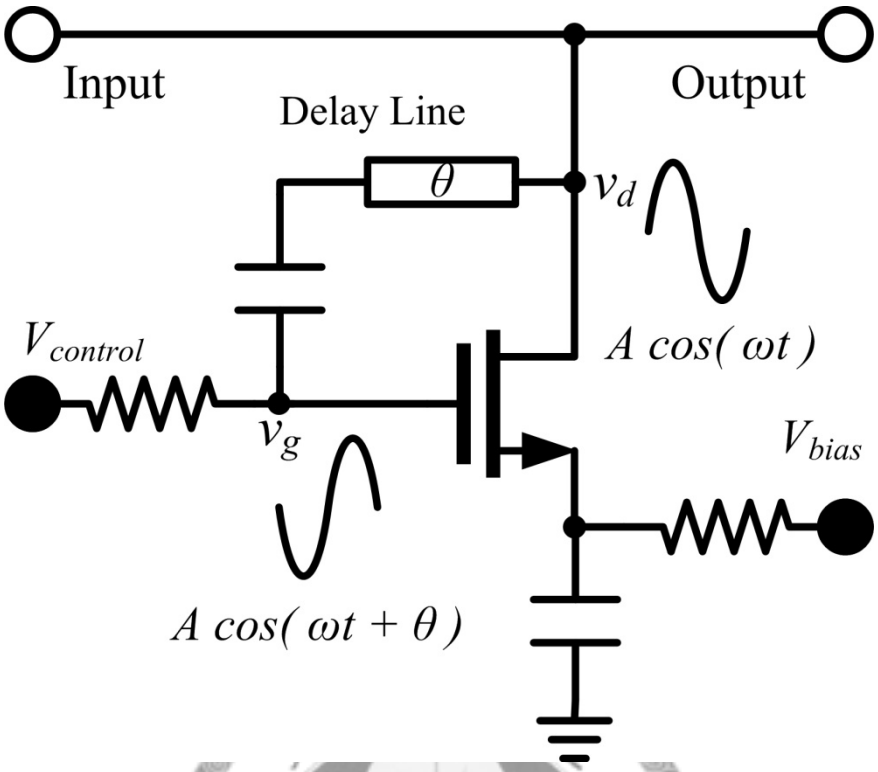


Fig. 3.8 Linearizer adding a delay line with phase difference θ .

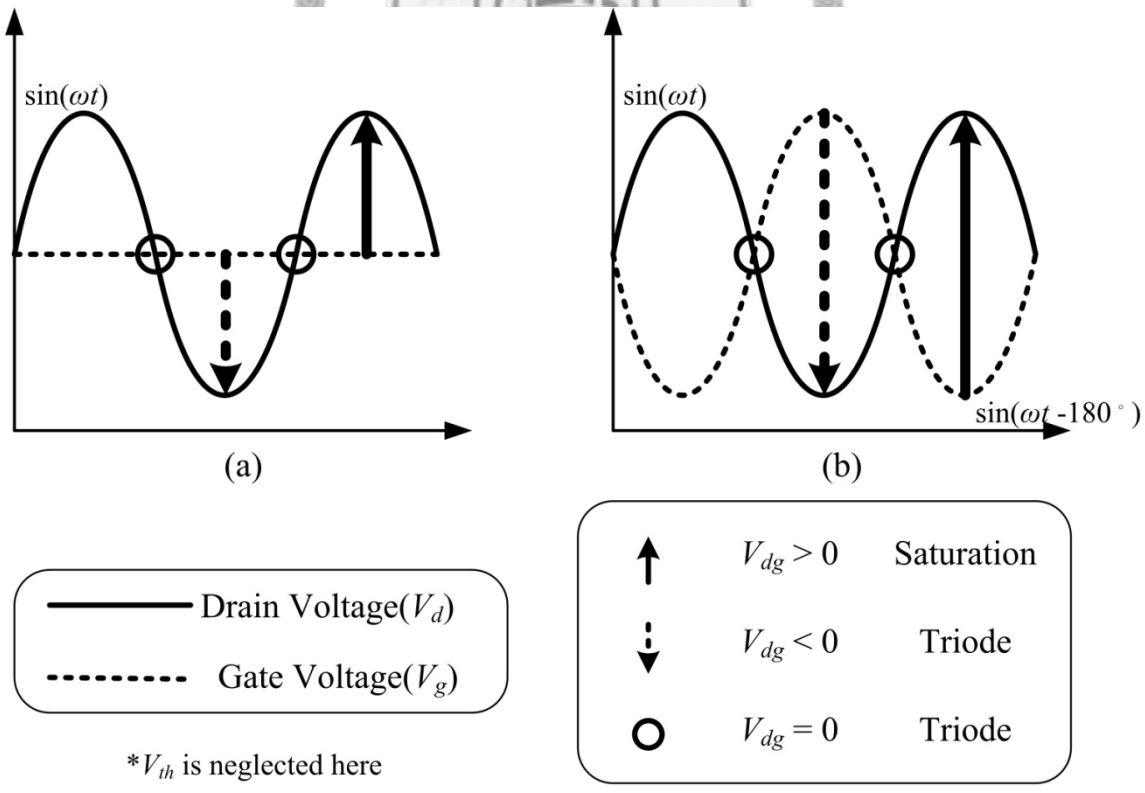


Fig. 3.9 The saturation condition of transistor of linearizer when the gate an drain are connected by (a) no delay line, and (b) a 180 degree delay line.

If the delay line provides a 180 degree phase delay, it can produce out-of-phase signals at the drain and the gate of the linearizer. The term ($V_{ds} - V_{gs}$) will therefore be increased twice faster than that of conventional linearizer, and make the saturation condition equation (3.3) be satisfied earlier. In addition, even when the delay line cannot produce a 180 degree signal, the term can still change faster than no delay line.

3.3.3 Intuitive Interpretation of the Modification

Fig. 3.10 can provide us an explanation to the effect of extra delay line. The solid line in the figure is the voltage swing at drain while the dash line represents the voltage swing at gate. The vector pointing upward means drain-to-gate voltage ($V_{ds} - V_{gs}$) is getting larger, hence easier to enter the saturation region. On the other hand, a circle or a vector pointing downward means ($V_{ds} - V_{gs}$) remains unchanged or getting lower, which keep the linearizer remaining in triode region or being forced into deep triode region. Followings are the discussion of the operation when a 180 degree delay lines is applied or not.

A. No delay line

It is a normal cold-FET linearizer which has no signal at gate of linearizer. Since only the vector pointing upward can enter the saturation region, we can observe from the figure that only half period of time has the possibility to enter saturation region.

B. 180 degree delay line

The gate voltage signal will have a negative swing while positive signal swing appears at drain. Since the voltage difference between drain and gate will therefore be twice, the transistor will be more likely to enter saturation region. Moreover, it would have an earlier loss deviation. In terms of the loss characteristic, it can produce earlier rising loss curve than no delay added, which means a lower output power for loss

deviation is needed.

We should notice that the delay line can also produce extra negative drain-to-gate voltage period. However, the linearizer will still in triode region when suffering a negative drain-to-gate voltage, and having similar loss as in normal triode region. Therefore, the phenomena will not damage the effect of loss deviation. The linearizer can still be better because it can enter saturation region easier.

3.4 Operation Detail of Modified Linearizer

3.4.1 Analysis of Possible Effects during Operation

In order to give a systematic analysis of the proposed linearizer, we should investigate the large signal operation of the modified linearizer, and focus on the influence of the delay line to the power flowing into linearizer. The method of investigating the effect is based on comparing the amount of power produced by the both linearizer when a voltage signal swing is at drain. The power flowing into the linearizer can be formulated as

$$P_{loss} = I_d \times V_d \tag{3.4}$$

The drain voltage V_d is a sinusoidal wave. It is the same for linearizer with and without delay line. However, the current flowing into the linearizer is different in both conditions. Therefore, the comparison of power loss can be simplifies as comparison of the current flowing into linearizer with and without delay line.

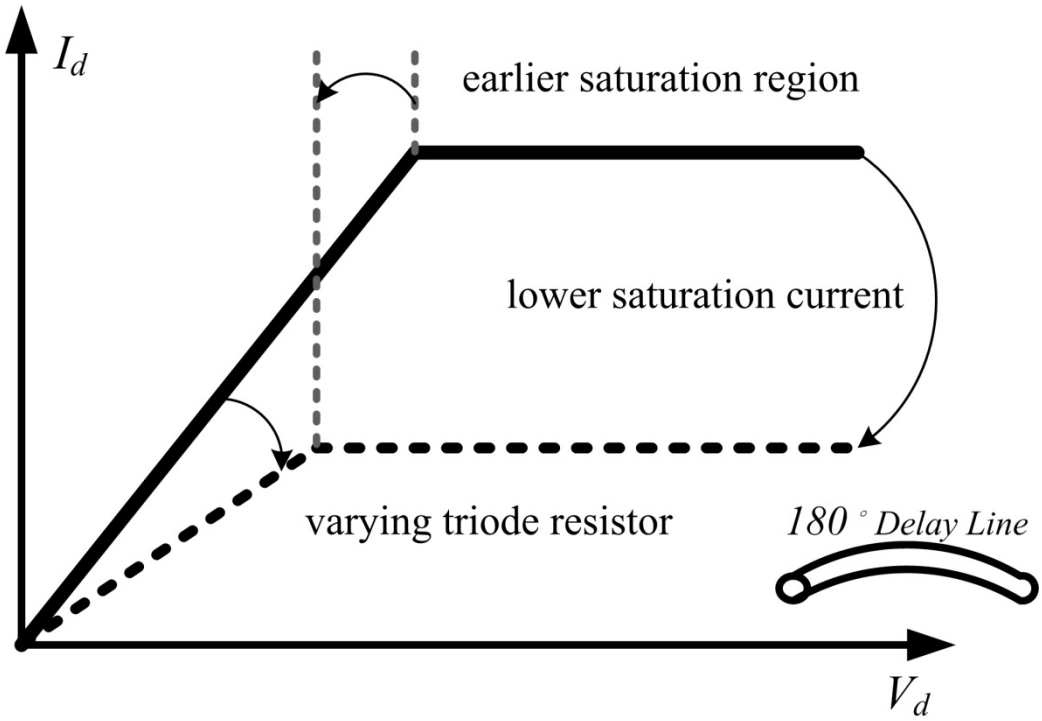


Fig. 3.10 Large signal operation of cold-FET linearizer with delay line.

Fig. 3.10 illustrates the change of DC-IV curve when the gate of transistor has an adversely swinging signal, which is the result of adding a 180 degree delay line. The change of DC-IV curve is described under the up swinging of input voltage signal. Therefore, the voltage swinging at the gate is swinging downward.

There are three effects we can observe from Fig. 3.10. The first one is that the linearizer will be more likely to enter the saturation region, because the saturation region is reached simultaneously by increasing drain voltage and decreasing gate voltage. The second one is the continuously decreasing current under the saturation region. This is a major difference comparing to the unchanged drain current of the conventional linearizer without delay line, which can reduce the current flowing into the transistor instead of passively remain no increment. The third one is the varying slope of the DC-IV curve in triode region which results from the voltage swing at gate of transistor. According to equation (3.1), the value of the resistor is defined mainly by the value of gate voltage.

The former two effects are both related to the saturation region of transistor. However, the first one is focused on the timing for the transistor to enter the saturation region. The second one focuses on the current variation when the transistor has already been in the saturation region. The third one are just discuss the effect at triode region.

We will investigate the reasons of the effects and give the mathematic equations which can properly describe these characteristics. For convenience, we should define some variables which will be used in the math equations. The definitions of variables are listed in Table 3.1.

Table 3.1 Definitions of variables regarding DC bias and signal voltage.

Variable	***Definition***
V_{DS}	*DC bias voltage at drain*
V_{GS}	*DC bias voltage at gate*
$v_{ds} = A\sin(\omega t)$	*AC signal voltage at drain*
$v_{gs} = A\sin(\omega t - \theta)$	*AC signal voltage at gate*
$V_{DS} + A\sin(\omega t)$	*Total voltage at drain of both linearizer*
$V_{GS} + A\sin(\omega t - \theta)$	*Total voltage at gate of new linearizer*
V_{GS}	*Total voltage at gate of conventional linearizer*

The θ results from the delay line that creates a phase difference of θ. Through the θ degree delay line, drain signal $A\sin(\omega t)$ of the linearizer will produce a equal amplitude but different phase signal $A\sin(\omega t - \theta)$ at the gate of the linearizer. Following section will separately discuss the influence of the effects to loss characteristic. When one effect is discussed, the other two effects will be assumed the same as no delay line on

linearizer.

3.4.2 Earlier Saturation Region

A. Function evaluation

We first consider the effect called earlier saturation region presented in Fig. 3.10. Using the equation (3.2) of transistor and applying the variables listed above, the saturation condition for a cold-FET linearizer with and without delay line can be formulated as

$$A\sin(\omega t) > -V_{th} - (V_{DS} - V_{GS}) \tag{3.5}$$

and

$$A\sin(\omega t) - A\sin(\omega t - \theta) > -V_{th} - (V_{DS} - V_{GS}) \tag{3.6}$$

, respectively. We can further simplify equation (3.6) to

$$2A\sin\left(\frac{\theta}{2}\right)\cdot\sin\left(\omega t + 90^{\circ} - \frac{\theta}{2}\right) > -V_{th} - (V_{DS} - V_{GS}) \tag{3.7}$$

B. Larger amplitude

Comparing equation (3.5) and (3.7), we will find that the term of both equations at left-hand-side have different coefficients. The coefficients are A in equation (3.4) and $2A\sin(\theta/2)$ in equation (3.7) for conventional and modified linearizer respectively. If the phase θ is larger than 60 degree, the coefficient $2A\sin(\theta/2)$ will be larger than A. Therefore, when amplitude of input signal is increasing, the left-hand-side of equation (3.7) will increase faster than that of equation (3.5), which means equation (3.7) is more likely to be satisfied and to enter saturation region.

As shown in Fig. 3.7, the saturation region of transistor will result in a cutoff waveform of drain current, which results in the pre-distortion function. According to Fig. 3.3, one of the criteria of pre-distortion linearizer is the output power at which the loss

deviation is enough. In order to achieve the criteria, we can otherwise make the loss begin to decrease at lower output power.

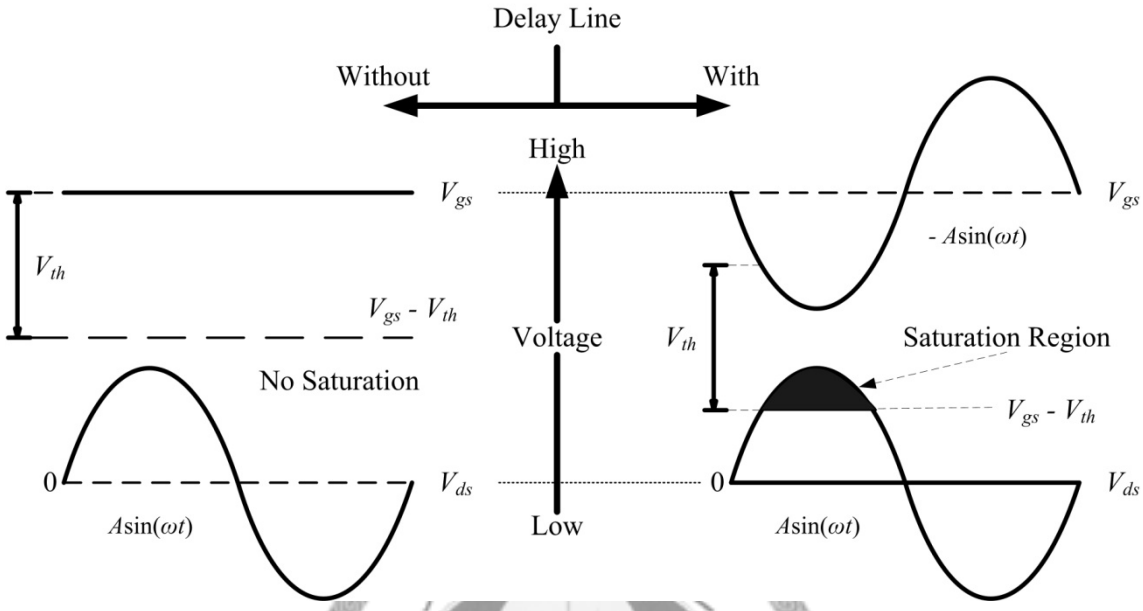


Fig. 3.11 Negative voltage swing at gate makes linearizer to enter saturation region easier.

The earlier saturation region effect can meet the requirement. Fig. 3.11 shows the benefit of the delay line. The left and the right represent voltage condition of linearizer with and without 180 degree delay line. The higher of the curve means a higher voltage. Since the gate is biased at a higher voltage, we place the DC value of gate voltage higher than that of drain voltage.

Drain voltage signal in both conditions are the same. Both are signal swings with a zero DC value. The drain voltage signal in the left-side figure is not large enough to reach the saturation threshold when the gate voltage remains unchanged. However, if the delay line is added, the gate would have an out-of-phase voltage swing to the drain voltage. When the voltage difference between drain and gate is smaller than V_{th}, the saturation condition is satisfied. As we can be observed from the figure, the linearizer with delay line can reach saturation region while the linearizer without delay line

cannot.

Equation (3.7) shows once the phase of delay line is larger than 60 degree, it is more likely to enter saturation than the linearizer without delay line. In conclusion, the line with more than 60 degree phase delay can make the transistor to enter saturation at lower input power, and result in an early-rising-up loss curve at which the linearizer has low output power.

C. Phase shift of saturation region

From equation (3.7), we can observe not only the amplitude of the left-hand side can influence the possibility of saturation region and influence the current flowing into linearizer, but also the phase difference $\left(90^{\circ}-\theta/2\right)$ of the composite term is also influential.

Fig. 3.12 demonstrated the influence of the phase difference. Fig. 3.12 (a) shows the voltage swings at gate and drain in different conditions. Subtracting the gate voltage by drain voltage results in the waveform in Fig. 3.12 (b). The waveforms are the value of left-hand-side of equation (3.7) that represents the possibility of entering saturation region. The waveform for the condition with delay line has a phase difference of $\left(90^{\circ}-\theta/2\right)$ comparing to the drain voltage wave. For the conventional linearizer, saturation always occurs when drain voltage has positive value. However, the phase difference $\left(90^{\circ}-\theta/2\right)$ makes linearizer to enter saturation region in different period. The region labeled “new” and “old” in Fig. 3.12 (b) are the saturation region of linearizer with and without delay line, respectively.

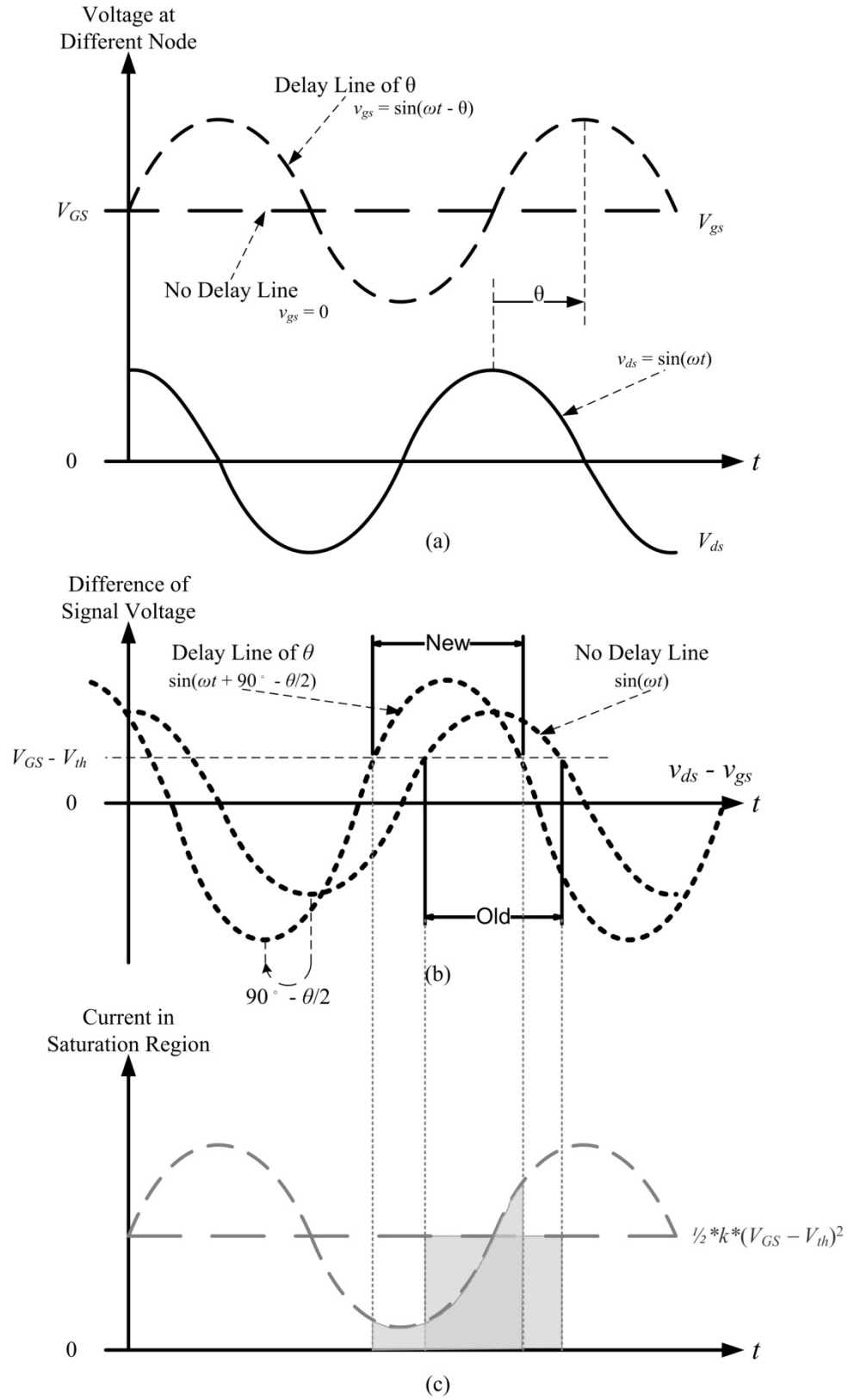


Fig. 3.12 The value of (a) gate voltage and drain voltage, (b) left-hand-side of equation (3.7), and (c) current in saturation region of linearizer with and without delay line.

The phase shift of saturation will result in lower drain current, enhancing the ability of loss deviation. Considering the equation

$$I_d = k_n \times \left[\frac{1}{2} \left(V_{gs} - V_{th} \right)^2 \right] \tag{3.8}$$

, where I_d is the drain current and k_n is a constant. The drain current of transistor in saturation region is totally defined by the gate voltage. The marked part of Fig. 3.12 (c) represents the amount of current flowing into linearizer in saturation region. Slash and back-slash region represents the condition that linearizer has delay line and not. The gray horizontal and sinusoidal dash lines are gate voltages that are used for calculating the drain current.

The current remains unchanged in the old saturation, following the constant gate voltage V_{GS} of linearizer without delay line. However, the gate voltage V_{gs} in the new saturation region is more likely to be larger than its DC value V_{GS} and form a smaller area, as shown by slash region in Fig. 3.12 (c). Therefore, "average" current in the new saturation region is smaller than in the old saturation region, which means the power flowing into the transistor will be reduced more rapidly.

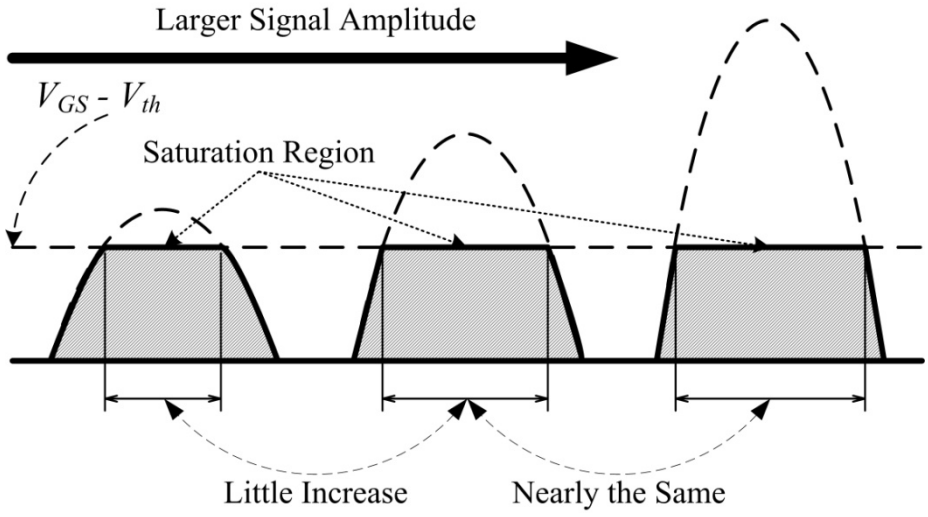


Fig. 3.13 Constant up-swinging current after entering saturation region.

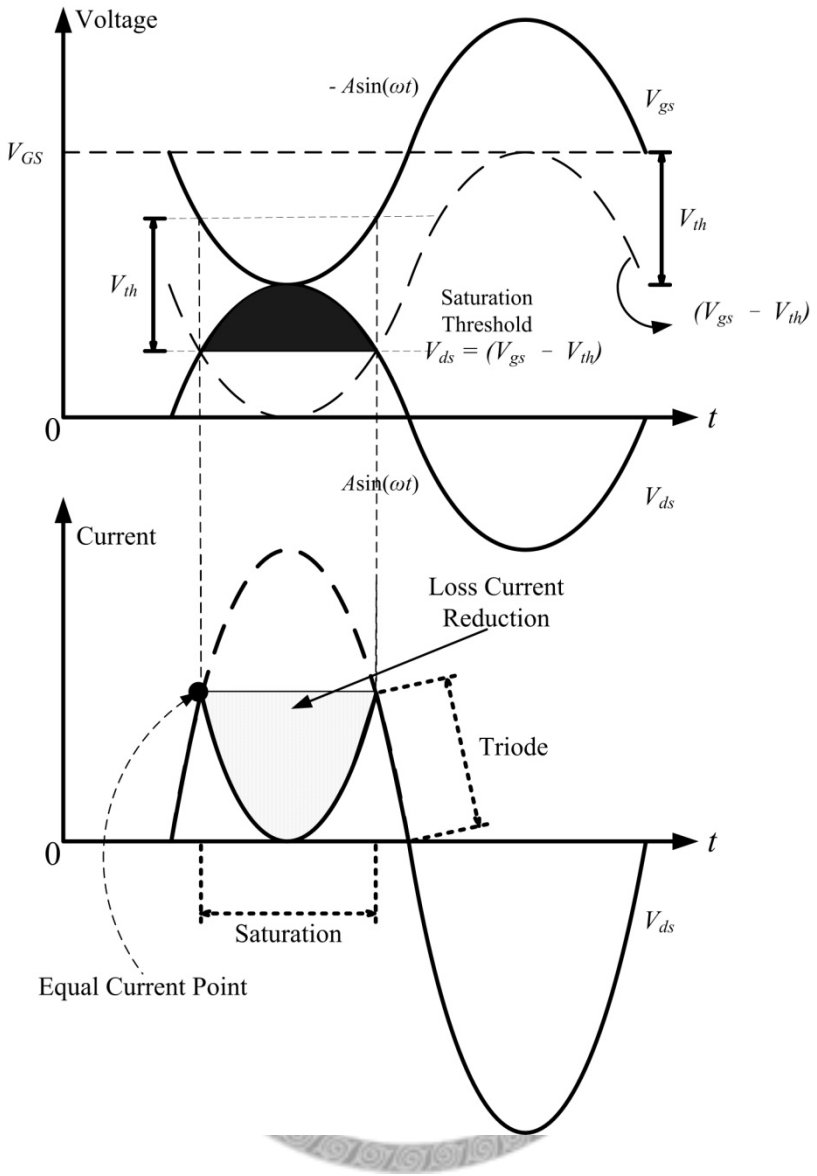


Fig. 3.14 Current reduction after entering saturation region.

3.4.3 Lower Current Loss at Saturation Region

Sinusoidal dash line in Fig. 3.13 represents the left-hand-side of equation (3.5), which are for conventional linearizer. The conventional linearizer has a constant gate voltage, making the current of it keep unchanged when entering saturation region, as depicted by the drain current equation in equation (3.8). The threshold after which the linearizer would enter the saturation region is shown by horizontal dash line in Fig. 3.13. As the input power is getting larger, transistor will enter the saturation region quickly at the first of the operation cycle. This means the current of transistor will soon reach

constant value of drain current and then remains unchanged.

Since the current in saturation region is the largest in the whole period, the larger saturation period would results in a larger average current. However, the ultimate length of saturation period is the half cycle of whole period. As shown in the middle of Fig. 3.14, when the amplitude of signal is large enough, nearly whole up-swinging period is saturation period. The average current will therefore remains nearly unchanged at high power level, even when the power is still getting larger.

The pre-distortion function can still work under the phenomena because the current fed to next stage is still getting larger. The loss which represented by ratio of the current flowing into linearizer to the current fed to next stage will therefore still getting smaller, and exhibits pre-distortion effect. However, the constant current flowing into linearizer will results a certain amount of loss when the power level is high, which is the loss in criteria (B) of Fig. 3.3.

After adding the delay line, the gate voltage V_{gs} is always changing. According to equation (3.8), the current in the saturation will totally defined by the gate voltage. Since the gate voltage is still getting lower in the saturation region, the loss current should also get smaller in the saturation region. Fig. 3.14 provides the concept of decreasing loss current in saturation region. Unlike the constant loss current, the current of transistor with delay line can ensure a lower loss at high output power level. By the way, the still decreasing current can form a loss characteristic that is still rising up even the input power is large enough to oversee the saturation threshold. This characteristic can extend the loss deviation curve, producing more loss deviation which can meet the criteria (A) in Fig. 3.3.

In addition, we have to discuss the point which the transistor just enters saturation region. Comparing the drain current equation in triode region

$$I_d = k_n \times \left[\left(V_{gs} - V_{th} \right) \times V_{ds} - \frac{1}{2} \times {V_{ds}}^2 \right] \tag{3.9}$$

with equation (3.7) which is in saturation region, they are two totally different equations. However, at the point which the transistor just enters the saturation region, the two equations are conjoined together and should have the same current value.

Since the point entering saturation region should satisfy equation (3.2), the term $\left(V_{gs} - V_{th} \right)$ will be the same to the term V_{ds} at the point. Fortunately, after putting the equilibrium into equation (3.8) and (3.9), we will find that the current provide by two equation will be the same. Therefore, the final curve will be dominated by equation (3.9) at first when the drain voltage begins to rise up. After the same current point, the current value otherwise dominated by equation (3.8), and the current value begin to decrease.

3.4.4 Varying Resistor Effect

The effect called varying resistor presented in Fig. 3.10 is resulted from the swinging signal voltage at gate. The swinging gate voltage will cause the slope of DC-IV curve in triode region to change according to the signal.

A. Evaluation of admittance equation

In order to find out the influence of voltage swing in triode region, we have to apply the voltage in Table 3.1 to equation (3.8). Since the DC-current of linearizer is zero, the formulated equation will be the signal current flow into the linearizer. By setting V_{DS} to be zero, the signal current flowing into linearizer with and without delay line are formulated respectively as

$$i_{d1} = k_n \times \left[\left(V_{GS} - V_{th} \right) \times A \sin\left(\omega t \right) + A^2 \sin\left(\omega t - \theta \right) \times \sin\left(\omega t \right) - \frac{1}{2} A^2 \sin^2\left(\omega t \right) \right] \tag{3.10}$$

and

$$i_{d2} = k_n \times \left[\left(V_{GS} - V_{th} \right) \times A \sin\left(\omega t \right) - \frac{1}{2} A^2 \sin^2\left(\omega t \right) \right] \tag{3.11}$$

Dividing equation (3.10) and (3.11) by input voltage signal $A\sin(\omega t)$ can get

$$Y_{d1} = k_n \times \left[\left(V_{GS} - V_{th} \right) + A \sin\left(\omega t - \theta \right) - \frac{1}{2} A \sin\left(\omega t \right) \right] \tag{3.12}$$

and

$$Y_{d2} = k_n \times \left[\left(V_{GS} - V_{th} \right) - \frac{1}{2} A \sin\left(\omega t \right) \right] \tag{3.13}$$

,which are admittances of linearizer with and without delay line respectively.

Observing equation (3.12) and (3.13), we will find that they are in the form

$$Y_{dx} = Y_0 \times \left[1 - k_x \times \sin\left(\omega t - \varphi_x \right) \right] \tag{3.14}$$

,where Y_0 is the small signal admittance

$$Y_0 = k_n \times \left(V_{GS} - V_{th} \right) \tag{3.15}$$

, when the drain-to-source DC voltage is equal to zero.

For example, when the phase delay is 180 degree, equation (3.13) will be

$$Y_{d1} = k_n \times \left[\left(V_{GS} - V_{th} \right) - \frac{3}{2} A \sin\left(\omega t \right) \right] \tag{3.16}$$

,where

$$k_1 = \frac{3}{2} \times \frac{A}{\left(V_{GS} - V_{th} \right)}$$

and

$$\varphi_1 = 0 .$$

According to equation (3.13), we will find that the admittance have a lower value when input voltage is swinging upward and have a higher admittance when input voltage is swinging downward. Since the equation (3.12) also has the term

$-\frac{1}{2}\times A\sin(\omega t)$ that produces the phenomena, it is the intrinsic characteristic of transistor. Therefore, we should focus on the effect of extra term $A\sin(\omega t-\theta)$ introduced by delay line. For example, equation (3.16) shows a more severe admittance variation by setting the degree θ to be 180.

B. Effect of varying admittance

The current of linearizer is a multiple of admittance and drain voltage. However, the current value would be constant after entering the saturation region. In the following discussion, we neglect the influence of changing gate voltage of linearizer with delay line to current in saturation region. We assume the current in saturation region is always the same. We would focus on the effect of the varying admittance to the current in triode region.

Fig. 3.15 shows the process of calculating the drain current I_d, and provides the result of the drain current under constant admittance and varying admittance. We take the delay line with 180 degree phase delay for example. Fig. 3.15 (a) is the drain voltage for linearizer in all condition. The current of linearizer is shown as Fig. 3.15 (c) and Fig. 3.15 (d) when the drain voltage is multiplied by a constant admittance or a varying admittance shown in Fig. 3.15 (b), respectively. Thick dash line in Fig. 3.15 (c) and thin dash line in Fig. 3.15 (d) represent the drain currents I_d of linearizer under the condition that admittance is a constant and saturation region is not considered. The thick dash line in Fig. 3.15 (c) and Fig. 3.15 (d) are the current that only the effect of admittance is considered. The solid line in Fig. 3.15 (c) and Fig. 3.15 (d) are final current which is a constant value in saturation region.

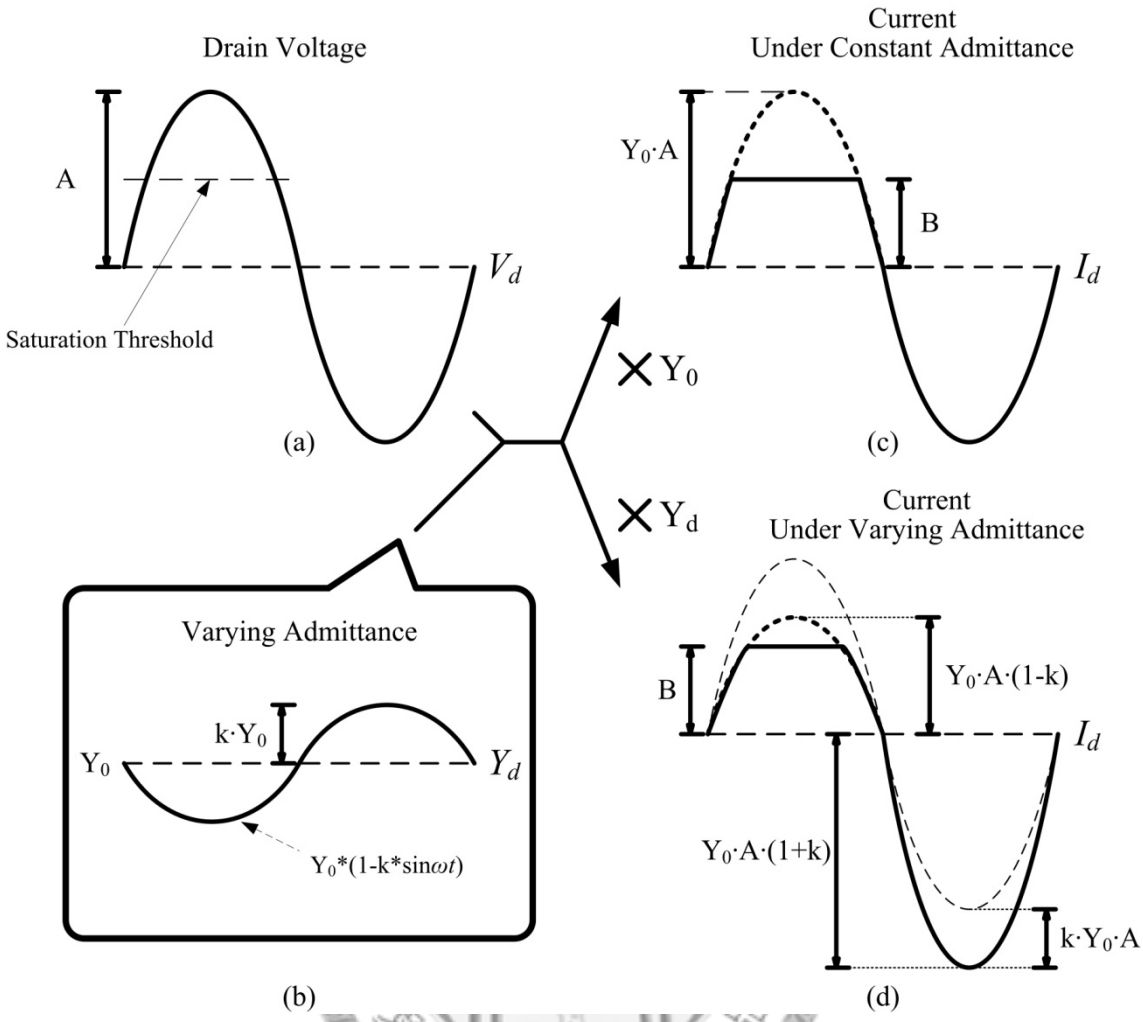


Fig. 3.15 Effect of varying admittance. Multiply (a) voltage at drain with constant admittance or (b) varying admittance to form current of linearizer under (c) constant admittance or (d) varying admittance.

If we only compare the thick dash line in Fig. 3.15 (c) and Fig. 3.15 (d), which does not consider saturation region, we will find that the current under varying admittance has a lower current in upward swinging period and has a higher current in downward swinging period. Since the waveform is not affected by the saturation region at which the current has a constant value, the decreasing admittance that produce lower current loss in upward swinging period, which is the amount of $Y_0 \times A \times (1-k)$, will be compensated by the increasing admittance that produce higher current loss in the downward swinging period, which is the amount of $Y_0 \times A \times (1+k)$.

When considering the constant current in saturation region, we would assume the total current in upward swing period are the same when the amplitude is larger enough, as the concept shown in Fig. 3.13. That means the admittance variation has no influence to the current in the up-swinging period, as shown by the solid line of Fig. 3.15 (d). However, the current will still be higher in the downward swinging period because the admittance is higher there. We do not have to consider constant current of saturation region in the downward swinging period.

Since the pre-distortion function is achieved by the lower loss when signal amplitude is getting higher. The higher loss of the admittance variation will degrade the performance of modified linearizer. Although the conventional linearizer also has the varying admittance effect, the effect is more severe when adding a delay line. Equation (3.11), which is the admittance of linearizer with delay line, has an additional term $A\sin(\omega t-\theta)$ comparing with equation (3.12). The θ of 180 degree would produce a most varying admittance, and degrade the performance of linearizer most..

C. Select 90˚ delay line

Since the admittance variation is fatal to the modified linearizer, we should try to minimize the effect. The key point is the term $A\sin(\omega t-\theta)$ in equation (3.11). If we can make the term has no contribution to increase the loss, the admittance variation will only have the same degree of effect as conventional linearizer.

Since the varying admittance is a sinusoidal wave, which is odd-symmetry around the point that has the average value of it, the admittance would be larger before the point and be smaller after the point. The difference can be compensated by each other around the point. The extra term $A\sin(\omega t-\theta)$ in equation (3.11) has the same characteristic. The position of the point intercepts average value can be decided by the

θ of term $A\sin(\omega t-\theta)$ in equation (3.11).

Since the saturation effect only occurs in upward swinging period, we have to consider the method that makes the effect of extra term $A\sin(\omega t-\theta)$ to be eliminated in upward and downward swinging period. The objective can be achieved by placing the average-value point of the wave at the center of upward and downward swinging period. Since the value around the point can be compensated by each other, the current in downward swinging period will not have a larger average value. It can be achieved by setting the value of θ to be 90 degree.

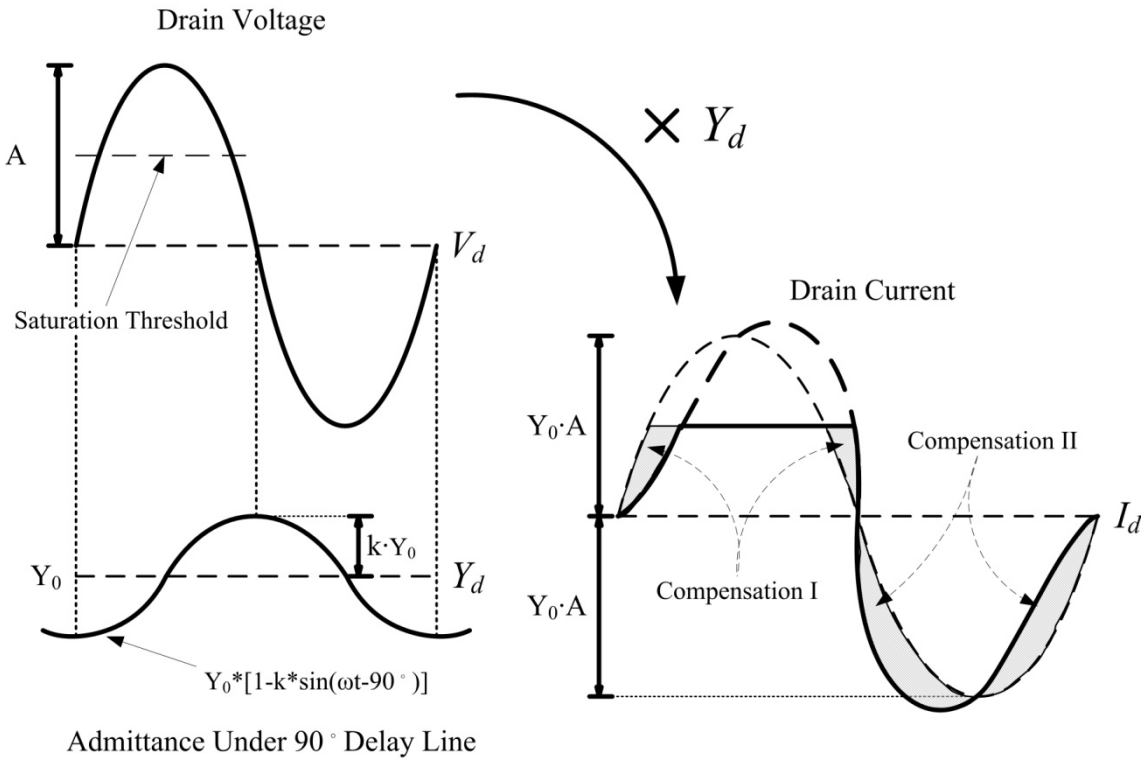


Fig. 3.16 Self-compensation under 90° admittance variation.

When linearizer has a 90 degree delay line, the extra admittance term $A\sin(\omega t-\theta)$ would be like the curve shown in left-down of Fig. 3.16. It produces an admittance variation that is an odd function around the peak value of voltage swing. Therefore, the higher admittance and the lower admittance in one up-swinging or

down-swinging period will compensate by themselves. The compensation I and compensation II are the example of self-compensation in up-swinging period and down-swinging period.

Since we have known the 180 degree phase delay will produce more loss and 90 degree phase delay will not, the trend is to produce more loss when the phase delay is increasing from 90 degree, and produce less loss when phase delay is decreasing from 90 degree. It can also be understood by consider the symmetry around peak value.

3.4.5 Verification of the modified linearizer

From above discussion, we find that delay line is beneficial to the pre-distortion function of conventional linearizer. The question left is to choose a phase delay of delay line that is practical for on-chip linearizer and can also exhibit the expected function.

Investigation of three possible effects provides us the answer. The first and second effects are effective to linearizer with 90 and 180 degree delay line. However, the third effect would damage the function of 180 degree delay line more. Therefore, the 90 degree delay line may have comparable effectiveness to 180 degree delay line.

The simulation is set up as Fig. 3.17 to verify the effectiveness of linearizer with 90-degree-delay-line. The part of linearizer will be placed with the modified linearizer and conventional linearizer in Fig. 3.8 and Fig. 3.6, respectively. We use the device size of 20x1 μm choose in section 4.4 for simulation because it will be further verified by measurement. For the same reason, we use power stage of the final power amplifier in Chapter 4 to be the part of amplifier. All the reflection losses are subtracted from the loss curve presented below.

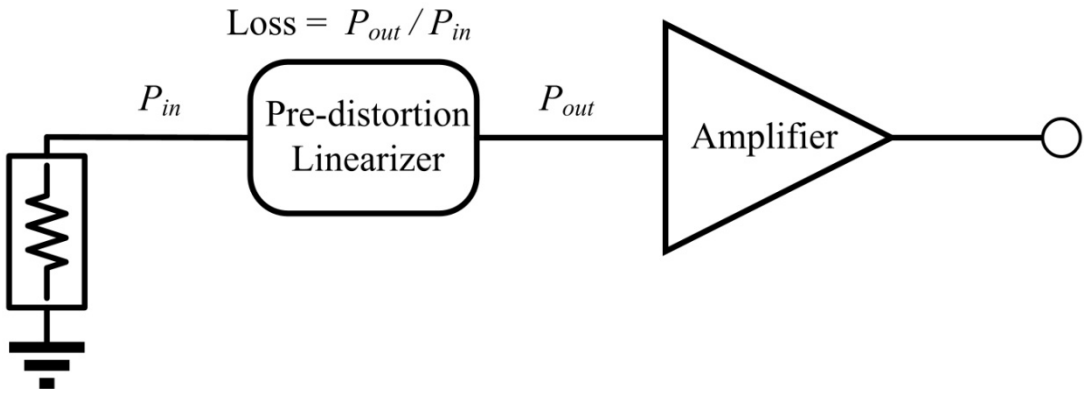


Fig. 3.17 Simulate the loss characteristic of pre-distortion linearizer.

We first compare the loss curve of modified linearizer and conventional linearizer, as shown in Fig. 3.18. The modified linearizer provides a larger loss deviation and can reach 1-dB loss deviation at a lower output power. Moreover, the modified linearizer also has a lower loss at the high output power. By the combination of the above two features, the modified linearizer has a sharper loss curve and is much possible to compensate the sharp gain compression curve of power amplifier.

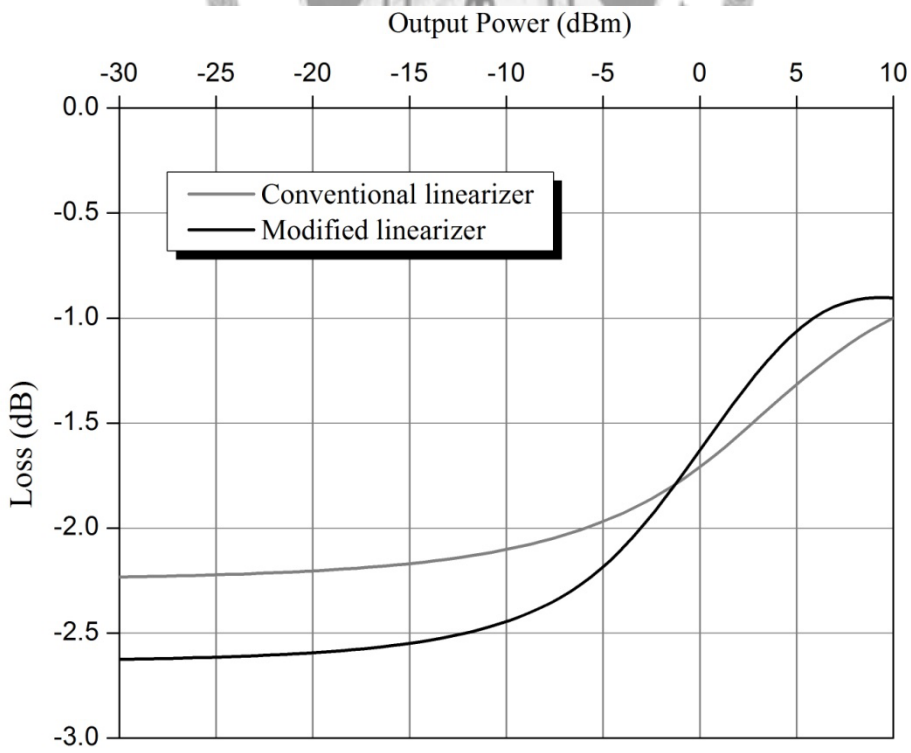


Fig. 3.18 Loss curves of conventional linearizer and modified linearizer.

Secondly, we will compare between the loss curves of modified linearizer with different phase delays. As shown in Fig. 3.19, the loss curve of the linearizer with 30-degree delay line has similar small-signal loss with other loss curves. However, it cannot provide larger loss deviation at higher output power. The 90-degree and 180-degree delay line have similar loss curves while the 120-degree and 150-degree curves are also similar. The linearizers with 120-degree and 150-degree delay lines present a lower loss than 90-degree and 180-degree delay line at small signal. However, the losses are similar for the four delay line below 5-dBm output power. This means the 90-degree and 180-degree delay line can provide higher loss deviation below 5-dBm output power. Even above the 5-dBm output power, the linearizer cannot provide equal loss deviation until 10 dBm. Since the input P_{1dB} of power amplifier we want to design is lower than 5 dBm, the 90-degree and 180-degree delay lines are more suitable.

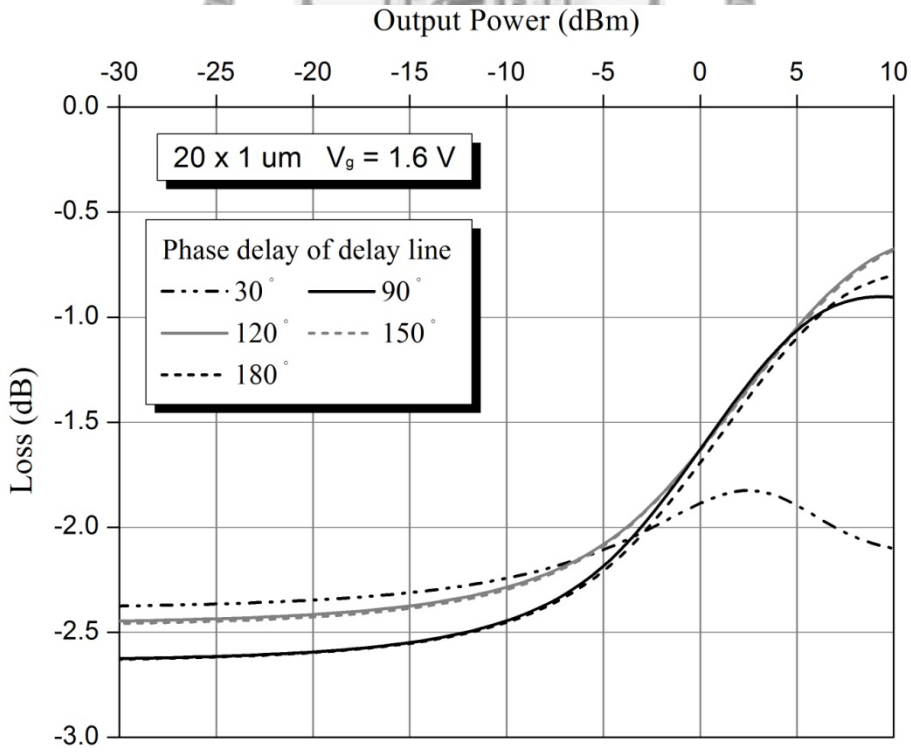


Fig. 3.19 Loss curves of linearizer with 90 and 180 degree delay line.

Finally, we have to choose between the 90-degree and 180-degree delay line. Obviously, the 90-degree delay line will occupy less area than the other one. Since the 90-degree delay line shows the best loss characteristic and maintains a small area, it is a better choice. The result also verifies the discussion of the previous sections.

3.5 Conclusion

This chapter proposes a modified linearizer that has better pre-distortion effect than conventional linearizer. The modification is achieved by adding an extra delay line connecting drain and gate of transistor. It can produce a different phase voltage wave at gate. From the analysis, we find that the modification can really help the linearizer to have better performance. The earlier entering saturation region effect can help the linearizer to provide enough loss deviation at low output power. The decreasing current in saturation region can help the linearizer to achieve higher loss deviation. The two effects both meet the criteria we proposed in the chapter.

However, the changing gate voltage would make the admittance in triode region to vary. It would produce more loss into linearizer and degrade the performance of linearizer. By choosing the phase delay of delay line to be 90 degree, we can eliminate the extra admittance variation introduced by delay line. Therefore, we can ensure the modified linearizer to have a better performance than conventional linearizer.

In conclusion, the 90 degree delay line is a choice that has comparable performance to the delay line with more phase delay. Moreover, it need smaller chip size to implement the 90 degree delay line. By considering the chip size and the performance simultaneously, the modified linearizer can be equipped with a delay line with 90 degree phase delay.

Chapter 4 A 60GHz Cascode Power Amplifier with Modified Linearizer

4.1 Introduction

4.1.1 Motivation

Power amplifier is an important building block in a wireless communication transmitter. Every time we want to transmit electric-magnetic wave signal into the free-space, we need a large enough output power to overcome the loss introduced by air and the long distance. However, its nonlinear characteristic due to large signal operation is a main limitation of the output power. The nonlinearity problem will be even more severe when the transmitter needs to transmit complex digital modulation signal.

Pre-distortion linearization technique is a solution to the problem, and many circuits are designed to implement the technique. The cold-mode linearizer is one of the best linearizer that effectively improves the linearity of power amplifier in pHEMT technology around 40 GHz [6]. A modification to the linearizer has been introduced and carefully discussed in the former chapter. From the equations and simulation results, we can find that the modified linearizer will help us to overcome the difficulties of V-band. An effective pre-distortion effect can therefore greatly improve the power added efficiency at OP_{1dB}, making the power amplifier using CMOS technology more practical in V-band.

Besides the solution to the poor linearity, we still have to find a topology of power amplifier that can meet the specifications for the application in V-band, like a large enough output power and high gain. Even though cascode device has poor linearity, it is

a good choice because of its high gain and high output power. In addition, the poor linearity can be compensated by the linearizer and help to best present the effectiveness of our modification. Extra loss introduced by linearizer will be neglected because the cascode device has far more gain. Although the common source topology which has good linearity is another regular choice for power amplifier, the common-source topology in 90 nm CMOS process only has 6 dB gain around 60 GHz. The low gain will be exhausted when adding the pre-distortion linearizer. Since the cascode device and the modified linearizer can mutually compensate each disadvantage, the cascode topology is the only choice.

4.1.2 Objective

The design process of inserting a linearizer into the power amplifier is rarely discussed in the published literatures. If we can clearly understand the effect of the design parameters, no matter the design process will be more efficiency, the real potential of the linearizer and amplifier can also be stimulated. Therefore, the objective of this chapter is to develop a clearly process of designing a power amplifier with linearizer.

In the perspective of the specification, the most important parameter we consider is the PAE at OP_{1dB}. Since the OP_{1dB} is the amount of output power that is usable under nonlinear effect and the PAE is the efficiency considering DC consumption, the parameter can best represent the trade-off between linearity and efficiency of power amplifier. Our objective is to improve the parameter as much as possible.

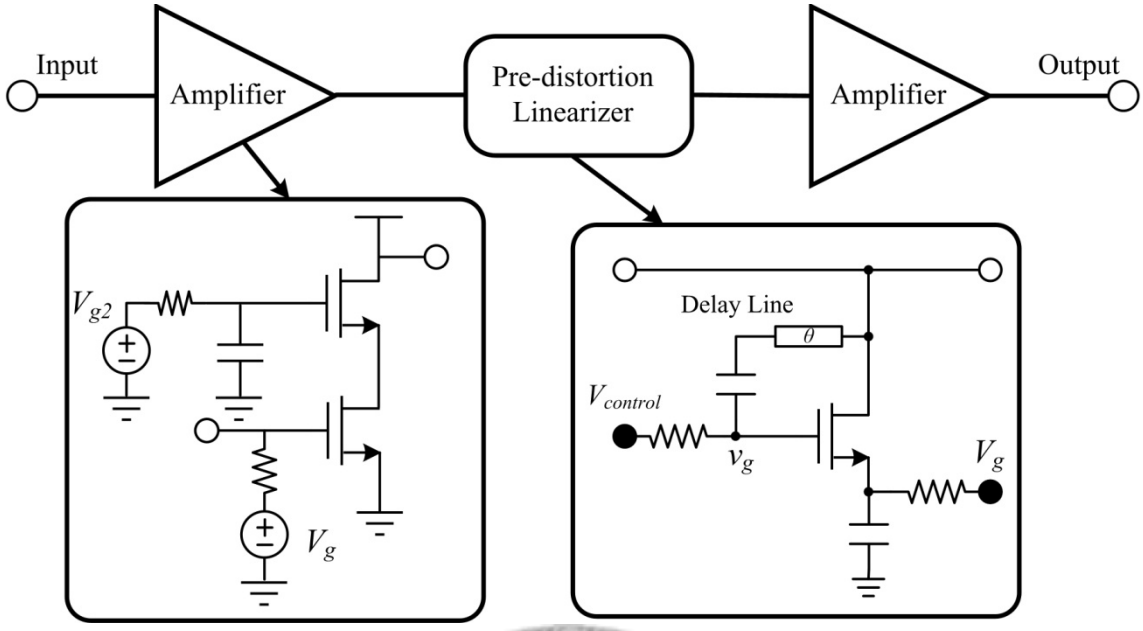


Fig. 4.1 Block diagram of the two-stage power amplifier with linearizer inserted in front of the power stage.

4.1.3 Design Flow

Fig. 4.1 is the block diagram of the two-stage power amplifier with a linearizer between the two amplifier stages. We should notice that the linearizer is not always at the position.

Fig. 4.2 is the design flow of the proposed amplifier. According to the figure, we will first design a conventional two-stage power amplifier following the process introduced before. Subsequently, first stage and the inter-stage matching network will be removed, remaining the second stage cascode device and the output matching network. Using the remaining part, the device of linearizer will be selected according to the design criteria presented in the former chapter. Important variables like the $V_{control}$, total gate width and the number of finger have different influences to the loss characteristic. We try to define the influences independently and make the design process can be finish without recursive tuning. Since the modification is regarded as the core part of the linearizer, the 90 degree delay line will always be added during the process of selection.

After the selection, we now have a power stage composited of a cascode amplifier and a modified pre-distortion linearizer. We have two choices for the following step. We can reuse the output matching network designed in the first step or follow the design process of two-stage power amplifier again. The latter choice would need an extra load-pull simulation and a new output matching network. No matter which method we take, inter-stage and input matching network will be redesigned again.

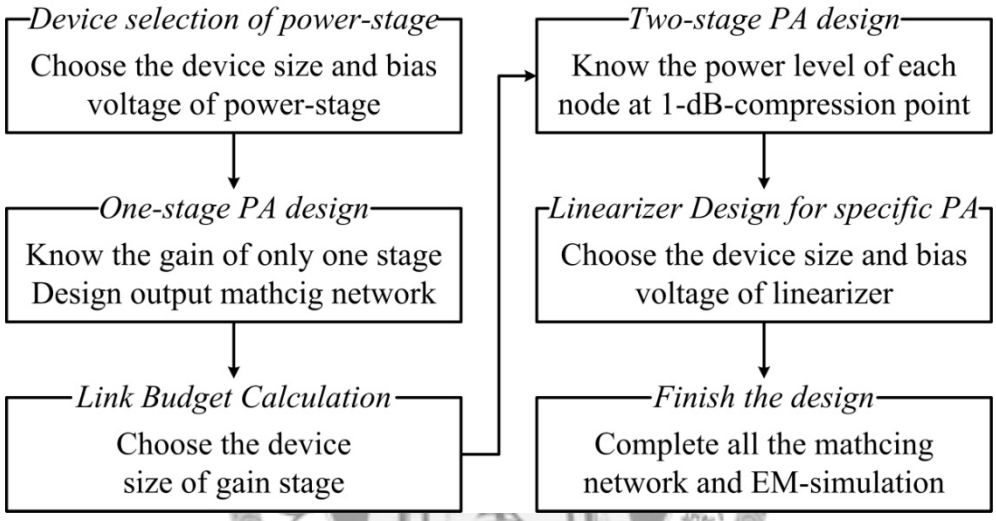


Fig. 4.2 Design flow of a two-stage power amplifier with linearizer.

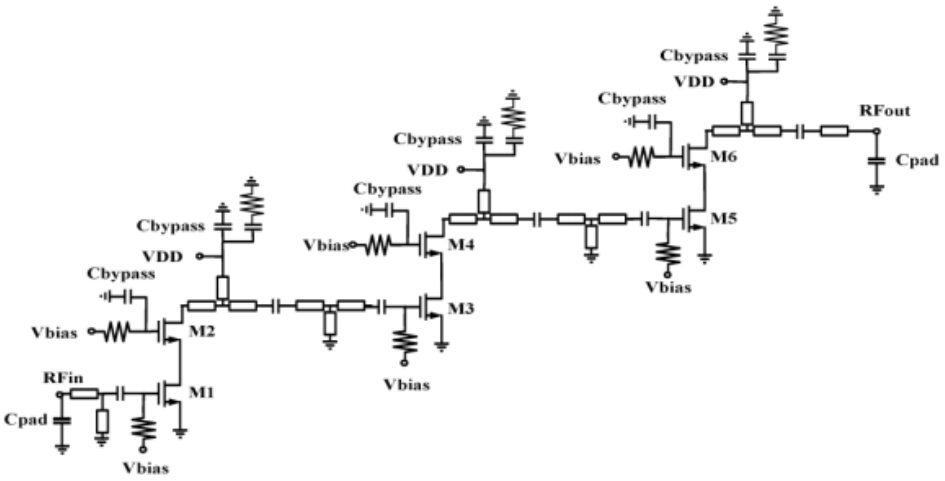


Fig. 4.3 Schematic of a three-stage cascode power amplifier [7].

4.2 Previous Published Literatures

4.2.1 Cascode Device and the Proposed Power Amplifier

A wideband power amplifier using RF 90-nm GP CMOS process is proposed in 2009 [7]. This PA demonstrates a measured P_{sat} of 18 dBm, P_{1dB} of 12 dBm, peak PAE of 12.6% and linear gain of 30 dB at 60 GHz under a 3 V supply voltage. Schematic of the circuit is shown in Fig. 4.3. The cascode device can really provide high gain and high output power.

However, the cascode device is poor in linearity. The difference between saturation power and OP_{1dB} is 6 dB, which means the amplifier has saturated when the amplifier have not demonstrate its highest PAE. The gain provided by the amplifier has been reduced by 10 dB before the power amplifier delivers saturation power.

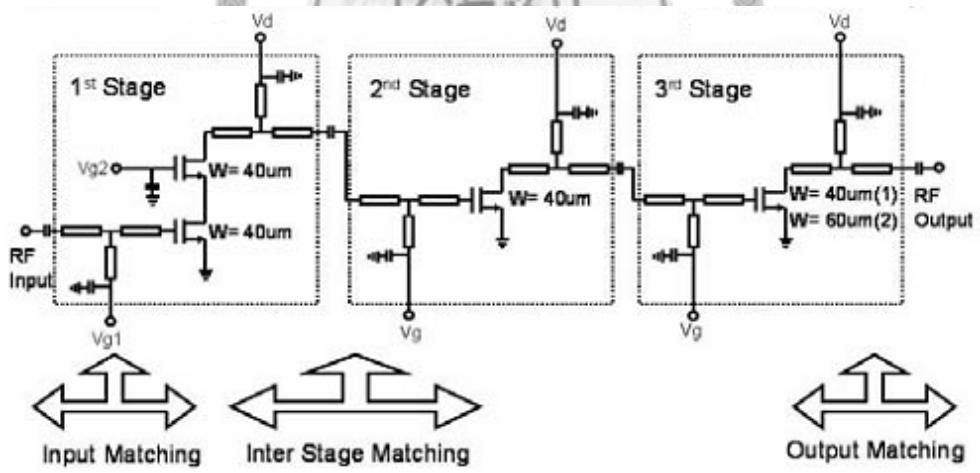


Fig. 4.4 Circuit schematic of three-stage 60GHz CMOS power amplifiers with the cascode device in first stage [14].

Another 60 GHz power amplifier is also fabricated by 90nm CMOS process in 2008 [14]. It uses a special structure that place a cascode stage in front of two common source stages. The PA has a 17 dB linear gain, 8.4 dBm P_{sat} and OP_{1dB} of 5.1 dBm. Since the DC consumption is 54 mW, its PAE has a peak value of 12.6 % and is 6 % at

OP_{1dB}. The difference between saturation power and OP_{1dB} is just 3 dB, which is a better linearity than the former circuit. The reason of the better linearity is the common source topology of output stage. Common source device can provide far better linearity than cascode device. The circuit takes advantage of the cascode device and common source device by placing the common source device at output stage and cascode device at the input stage, as shown in Fig. 4.4.

4.2.2 Amplifier with Linearizer

A power amplifier with pre-distortion linearizer using pHEMT technology is proposed in 2006 [6]. The operation detail was introduced in former chapter. The literature is the first attempt to apply pre-distortion linearization technique in millimeter-wave band. It effectively extends the point of OP_{1dB} and improves the linearity of power amplifier.

Another pre-distortion linearizer was proposed at 2.4 GHz using 0.18 μm CMOS process in 2009 [15]. The linearizer helps the PA extending OP_{1dB} point to 20.6 dBm and reaches 24.6 % PAE at the point. This is an attempt to apply the pre-distortion linearization technique to CMOS process. The schematic is shown in Fig. 4.5.

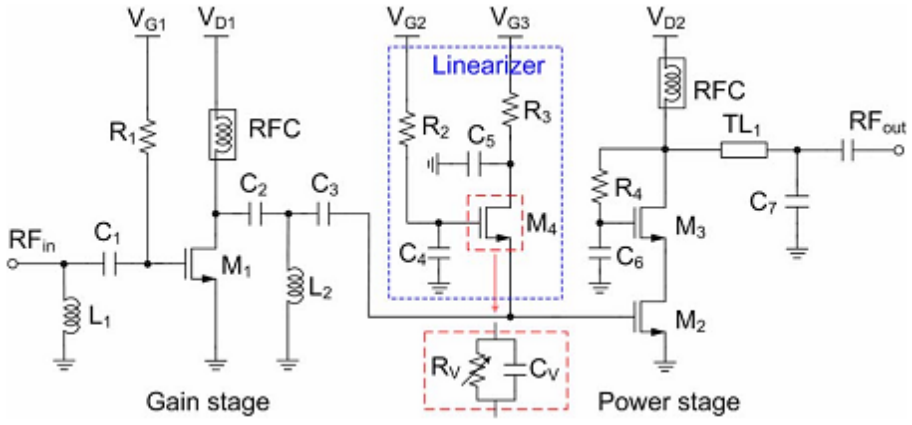


Fig. 4.5 Circuit schematic of a 24GHz CMOS power amplifiers with a built-in linearizer in 0.18 μm CMOS process [15].

4.2.3 High PAE Power Amplifier

A 60 GHz power amplifier with really high power-added-efficiency using 90 nm CMOS process was proposed in 2008 [9]. The PA has a 15 dB small-signal gain, a 12 dBm saturation power and a best peak PAE of 20%. The OP_{1dB} of it is about 10.5 dBm with a 12.5 % PAE. Although only one chip has the state-of-art performance, other chips still have peak PAE of 15 %. To our best knowledge, this is the power amplifier that presents the best PAE in V-band.

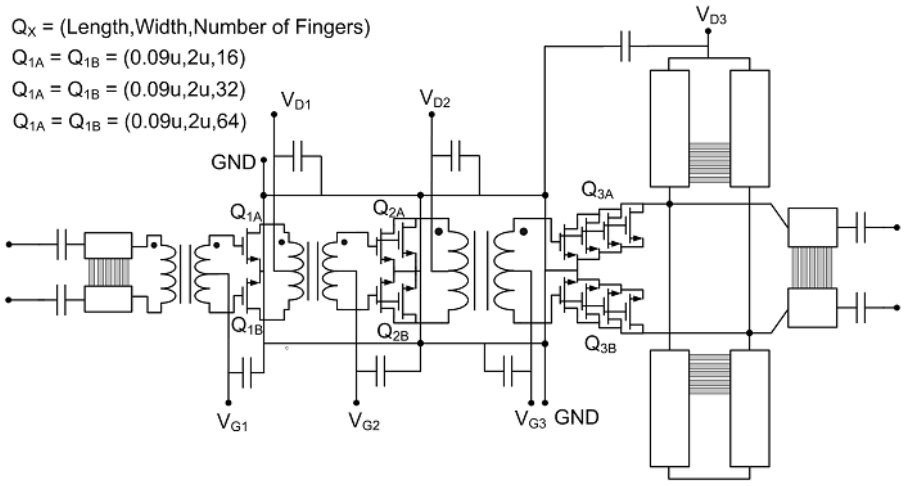


Fig. 4.6 Circuit schematic of differential, transformer coupled CMOS PA [9].

4.3 Pre-Design a Two-Stage Power Amplifier

This section is the first step of the whole design flow. We will design a two stage power amplifier and propose the process of linearizer design. Since we want to have extra gain to compensate the loss introduced by linearizer, the cascode device will be the device topology, as shown in Fig. 4.7. Fig. 4.8 shows the comparison of maximum gain between cascode and common source device. The cascode device can provide extra 7 dB gain than common source device.

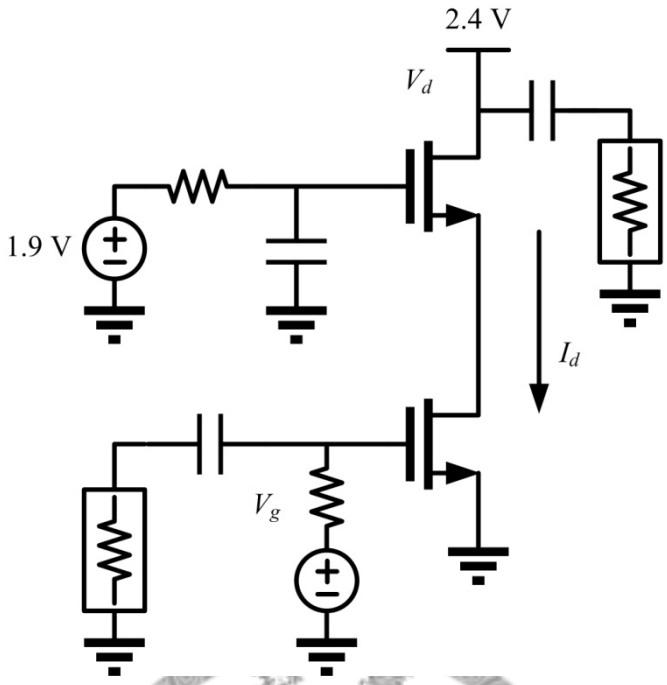


Fig. 4.7 Circuit schematic of cascode device.

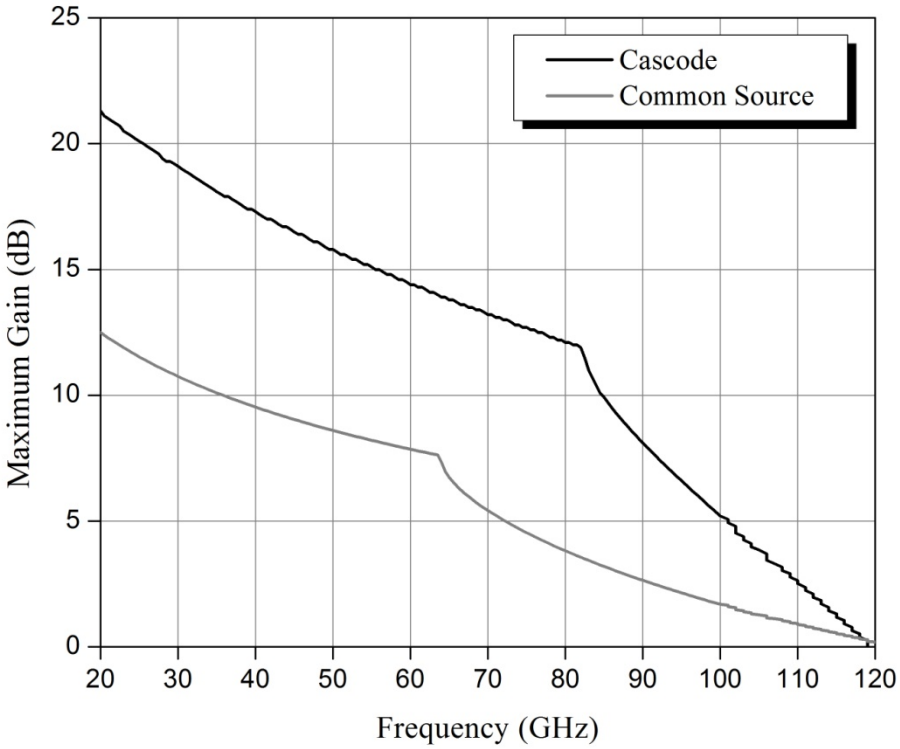


Fig. 4.8 Comparison of maximum gain between common-source and cascode device.

4.3.1 Device Selection

The objective of device selection is to decide the parameters of total gate width, gate bias and number of finger of a device. In order to select a device that has good power performance, three key factors should be considered. The following step will first investigate the relationship between the parameters and the key factors, then try to find out a way that can decide each parameters independently.

A. Gate voltage and efficiency

The efficiency of device is mainly decided by the gate bias voltage. The device with lower conduction angle will have a better efficiency performance. Since a lower gate bias voltage means a lower conduction angle, the amplifier will have a higher efficiency when the gate bias is slightly lower. However, if the bias voltage is too small, the gain of the device will be too low. The output power will also be too low under a low bias voltage.

The amount of conduction angle is decided by the threshold voltage and gate bias voltage of transistor. Since total gate width of transistor does not affect the threshold voltage, it will not affect the conduction angle. It only relates to the amount of current because the current of transistor is directly proportion to the total gate width in the behavior equation of CMOS device.

Although the gate bias will also affect the amount of current, we should choose the gate bias voltage first. It is because a lower current resulted from the low gate bias can be adjusted by other factor like total gate width. We should only make sure that the gate bias is not too low to be adjusted. The output power level we want will form an important limitation.

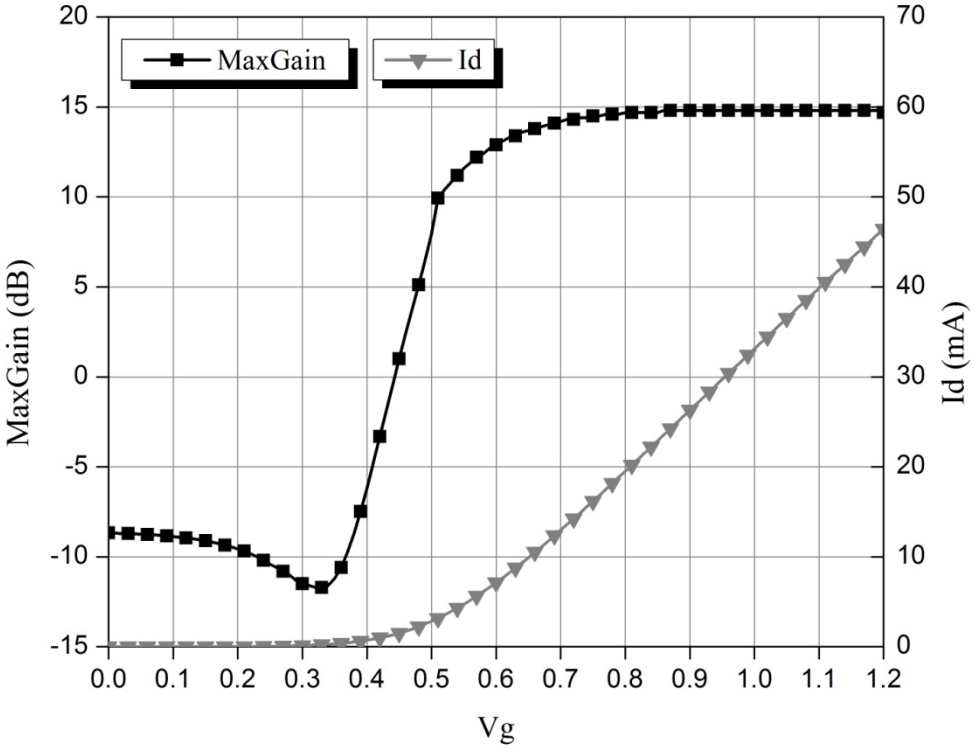


Fig. 4.9 Maximum gain at 60 GHz and drain current versus gate bias voltage.

Fig. 4.9 shows the maximum gain and drain current versus gate bias voltage. Maximum gain can help take the parasitic effect into account in high frequency. The current curve can help us to observe the output power level simultaneously. The curve shows the largest maximum of 15 dB is around 0.9 V, which can be regarded as the bias of class A. Decreasing the gate voltage does not result in a degradation of maximum gain more than 1dB until 0.65 V. Finally, we chose the 0.7 V to be the gate bias of our device, because it can provide larger gain and can deliver larger power.

B. Output power and DC consumption

The consideration of output power is controlled by total gate width. We plan to have a power amplifier with an OP_{1dB} of 10 dBm with a 10% PAE. Therefore, the DC power consumption should be 100 mW under the specifications. The cascode device is constructed by placing two transistors in series, so it can suffer two times drain voltage.

Since the standard drain-to-source voltage of a device in 90 nm LP CMOS process is 1.2 V, the supply voltage of the cascode device should be 2.4V. Under the supply voltage, the DC drain current is about 40 mA.

However, the current is the total current instead of just for one device. We have to know the device size ratio of power stage and gain stage to help us deciding the current of each device. Although device size ratio is decided by link budget calculation, we still cannot calculate it because the gain of the power stage is still uncertain before introducing the loss of matching network. For a power amplifier, the size ratio should be considered according to the gain of the power stage. Since the linearizer will introduce extra loss, we conservatively choose the ratio to be 2. We can investigate whether the choice is proper after some further design.

If the device size ratio is 2, the current of power stage is two thirds of the 40mA, which is 26 mA. Fig. 4.10 is the drain current of transistor with different total gate width. As we can see, the gate width of 90 μm can provide 13 mA and the gate width of 180 μm will provide 26 mA. However, since device with larger gate width is more stable and provides lower gain, we should also observe the maximum gain curve of device with different total gate width. Fig. 4.11 shows the maximum gain of device with total gate width from 90 μm to 120 μm. Since the transitional point (K = 1) of 120 μm device is at 67 GHz, device with larger total gate width will be more stable and provide lower gain. Therefore, we use two 90 μm devices to form the power stage. Details of the consideration of maximum gain will be introduced in next section.

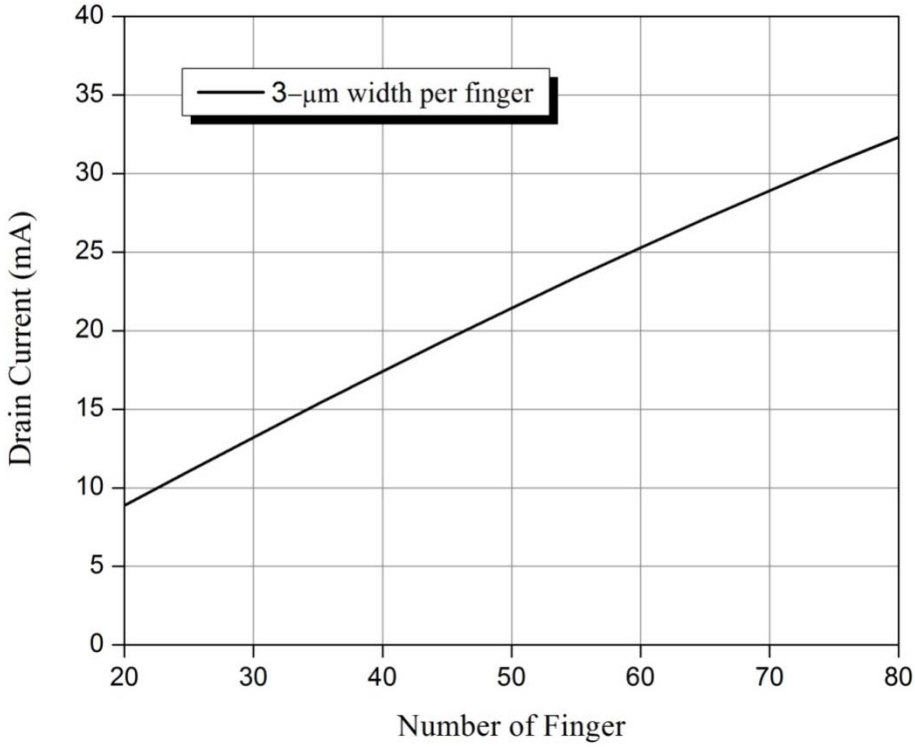


Fig. 4.10 Drain current of device with different total gate width and 0.7-V V_g.

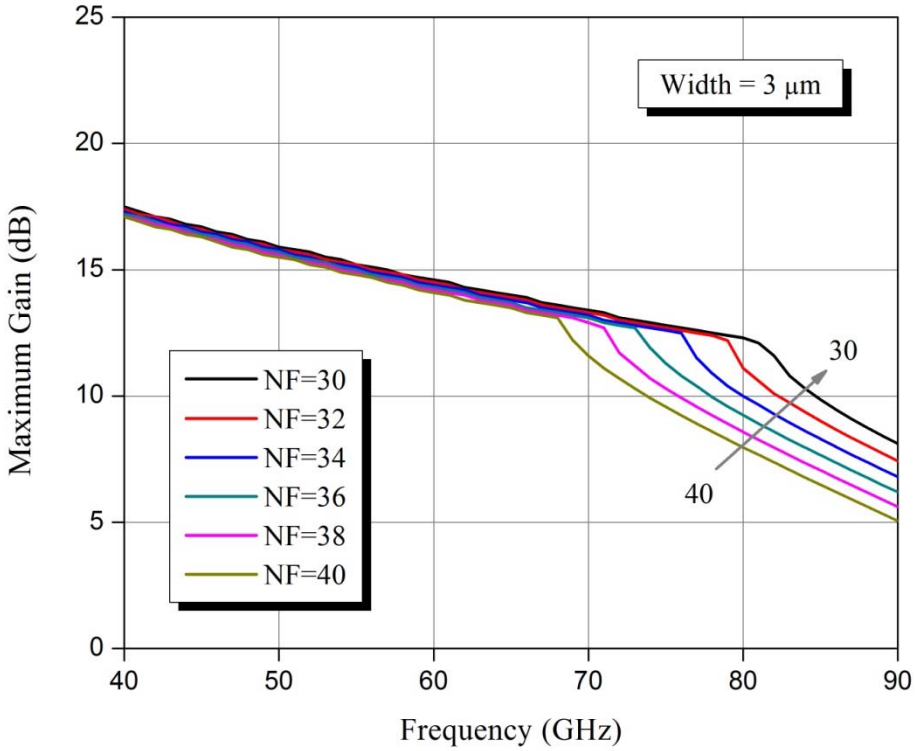


Fig. 4.11 Maximum available gain of device with different total gate width.

C. Gain consideration

Since the conductive substrate of CMOS process will introduces severe loss, we can select a device that is more unstable. If we choose a stable device at first, the loss of matching network will make the amplifier too stable and have a lower loss. A potential unstable device can provide more gain. The stability problem will be solved by the loss of matching network.

As we can observe from Fig. 4.11, the maximum curves are not continuous. All the curves have an obvious transitional point. The point separates the frequencies that the device is stable and unstable. Before the point, the flat parts of curves are the frequencies at which the device is unstable. We have to make sure the unstable part can cover the band we want, which is 57 GHz to 66 GHz. For the sake, we will make the transitional point at the frequency that is 10 GHz higher than the desired frequency band. This is the reason we choose the device with 90 μm gate width in Fig. 4.11.

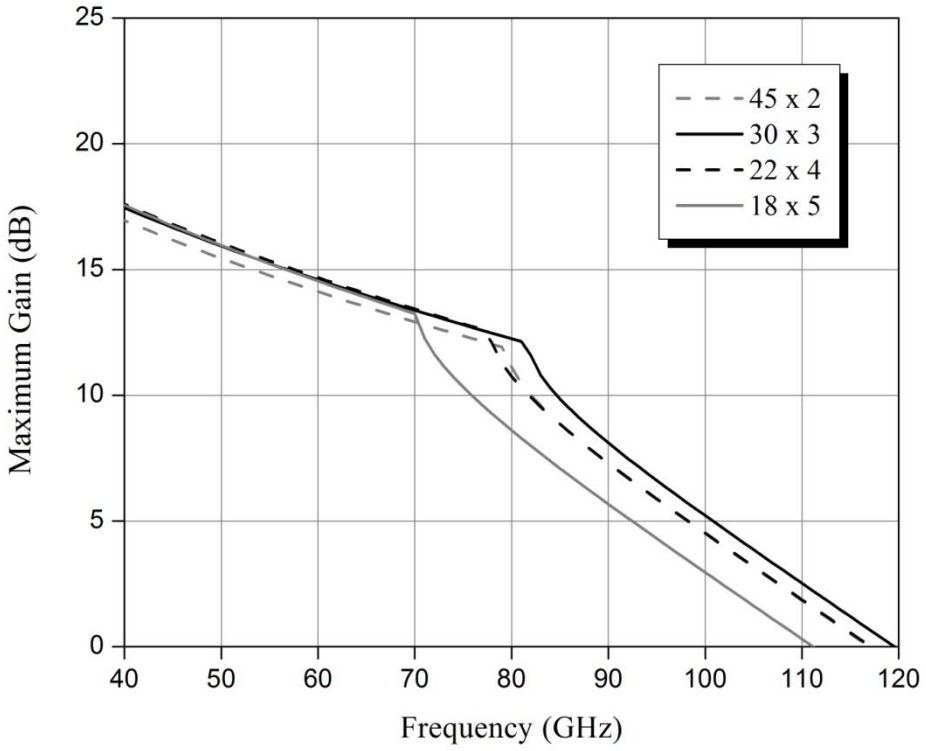


Fig. 4.12 Maximum gain of 90 μm device with different number of finger.

Beside the total gate width, we still have to decide the number of fingers. Fig. 4.12 shows the maximum gain curve of device having same total gate width but with different number of finger. We can observe that different choice of fingers will results in different stability and maximum gain. The 3 μm width per finger can provide a highest gain. We finally choose the device with 2.5-μm gate width per finger. The choice would be a 36 fingers 90-μm device.

In order to make sure the selected finger number is optimum for PAE, we can simulate the ideal power performance of the power stage with different number of finger but same total gate width, as shown in Fig. 4.13. In this simulation, the devices are 36 and 18 fingers with unit gate width of 2.5 and 5 μm respectively. From the figure, we can see the 36-finger device has a higher peak PAE, which is more efficient.

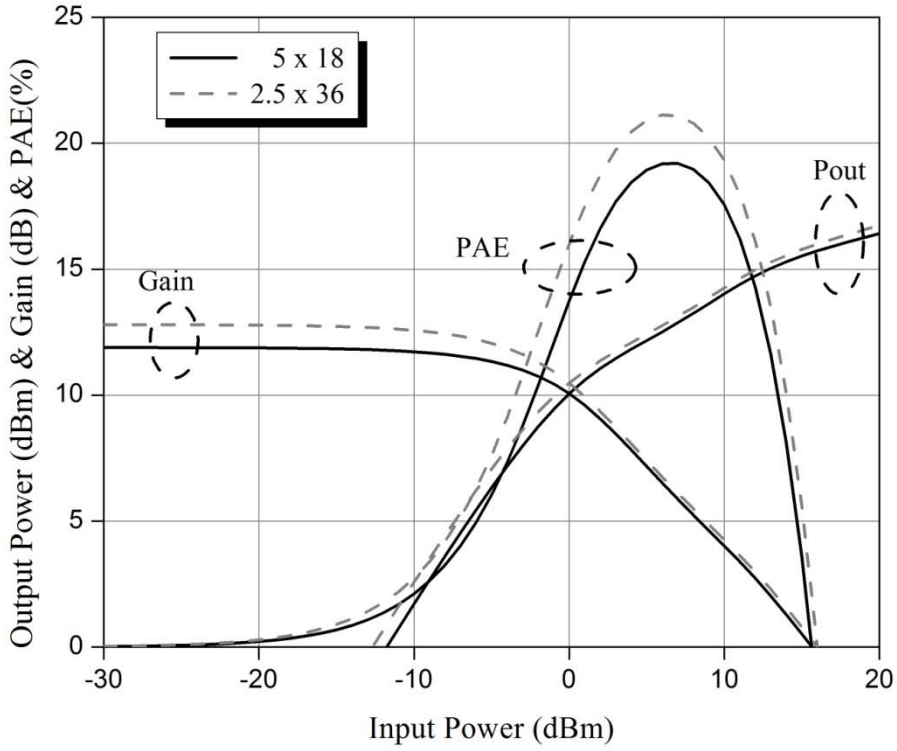


Fig. 4.13 Comparison of power performance of same total gate width power stage with different finger.

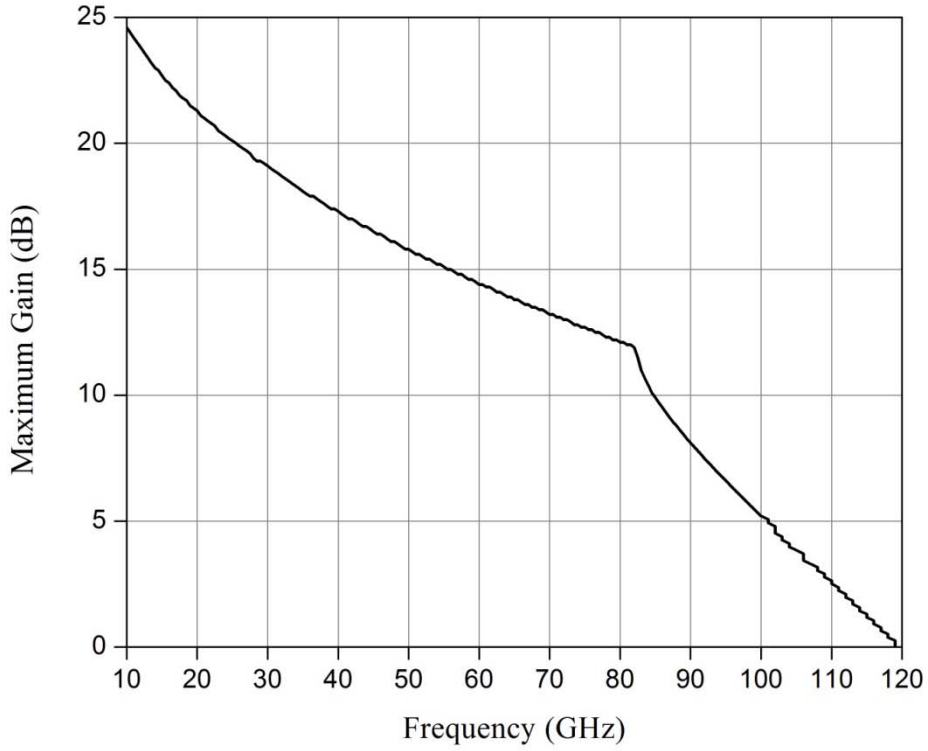


Fig. 4.14 Maximum Gain of 36 fingers 90-μm device from 10 GHz to 120 GHz.

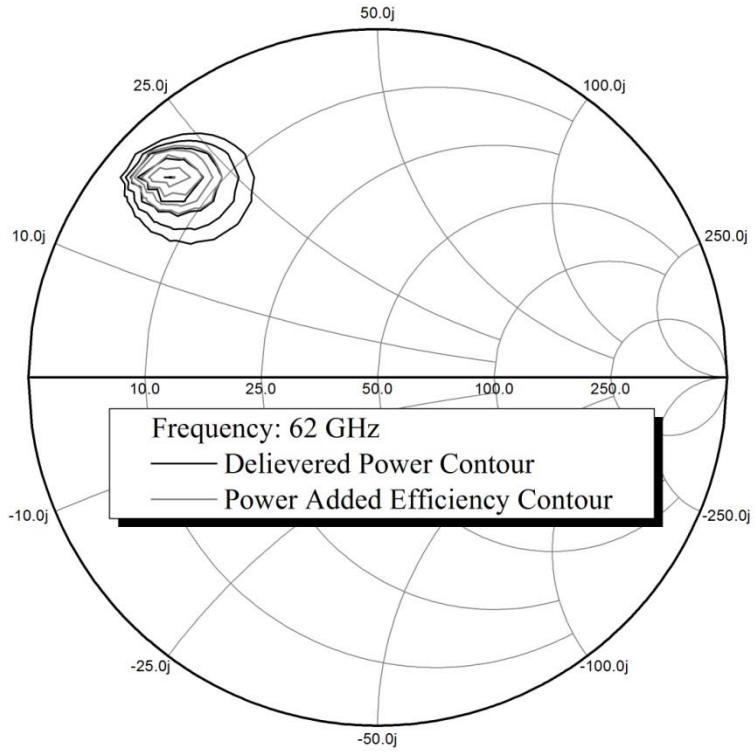


Fig. 4.15 Load-pull simulation of 36 fingers 90-μm device at 62 GHz.

D. Selection result

We finally choose a 36 fingers 90-μm device. Fig. 4.14 and Fig. 4.15 show the maximum available gain and load-pull simulation results of the device. This device can achieve f_{max} of 120 GHz and G_{max} of 14 dB at 60 GHz, as shown in Fig. 4.14. The ideal power performance has been presented in Fig. 4.13. This device with ideal matching network can provide 21 % peak PAE and 11 dBm saturation power. Fig. 4.15 provides the impedance for the maximum output power.

4.3.2 One -Stage Power Amplifier

Designing a one-stage power amplifier first can help us to understand the peak PAE and gain when the loss of the CMOS technology is considered. The matching networks are realized by thin-film micro-strip lines composed of metal 9 and metal 1 as signal line and ground, respectively. The micro-strip line is 5-μm wide and has characteristic impedance of 60 Ω.

Fig. 4.16 shows the process we design output matching network. The number represents the sequence of transmission line we transform 50 Ω to the impedance for the maximum output power. The matching network composed of five lines, blocking capacitance and RF-pad. Since the block capacitance and RF-pad is the necessary part of circuit, we should consider them to design the matching network. The lines of matching network are consisted of three series lines, one open stub and one short stub.

The configuration can make the load impedance of different frequency to form a little circle on smith chart, as shown in Fig. 4.16. The small circle means impedances of different frequencies are gathering together. It is because open stub and short stub have converse tendency of impedance shift when frequency varies. Since, the load-pull contours of device in neighboring frequency are very close, we can have a wideband

power performance when the circle of load impedance is circle around the load-pull contour in center frequency, which is presented in left-side of Fig. 4.16.

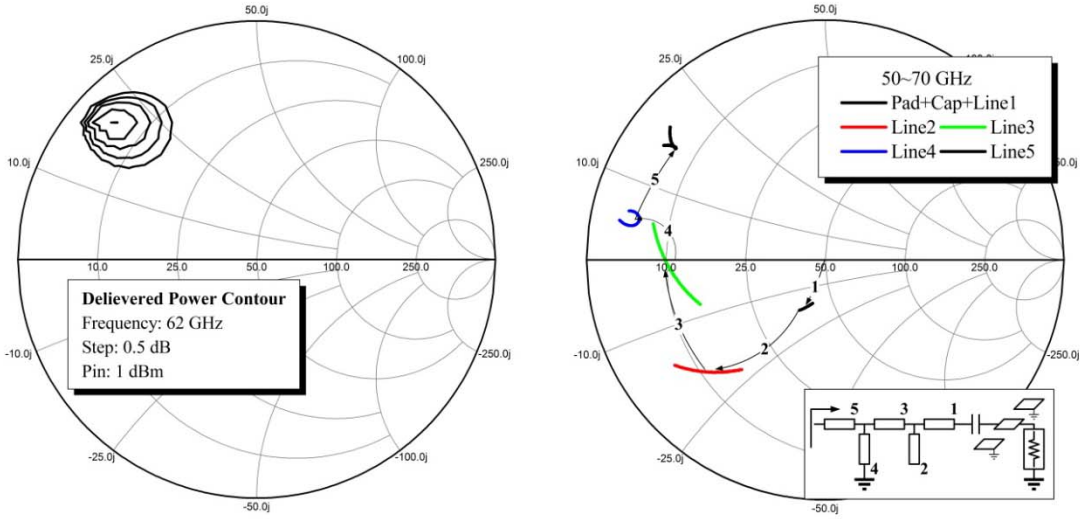


Fig. 4.16 Compare load impedance provided by output matching network with power contour of power stage.

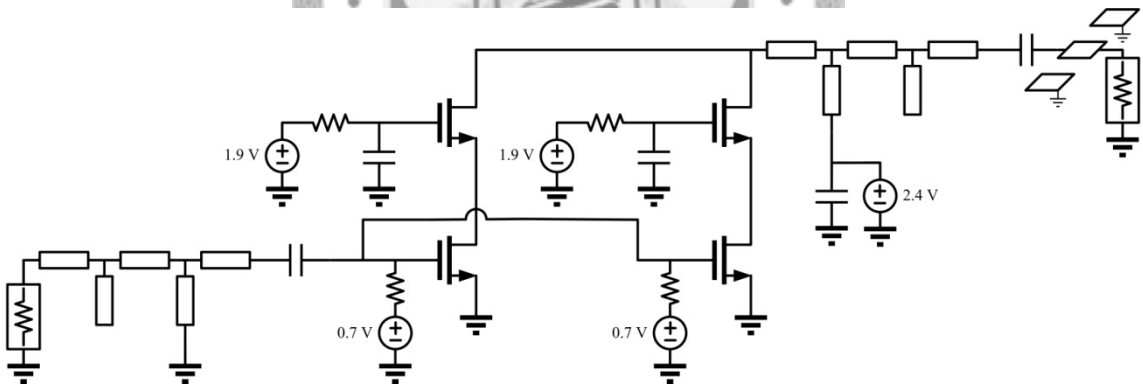


Fig. 4.17 Circuit schematic of one-stage power amplifier.

After finishing the output matching network, we should design input matching network to form a complete power amplifier. The conventional input matching network should provide conjugate impedance for input impedance of building block it connected with. The building block here is the power stage device with the output matching network designed before. However, the method would result in a bad output return loss.

Since we want to have a flat gain performance, we have to use the method of iteration tuning. After the tuning, we can have a flat gain curve and acceptable return loss. The output matching network is now a network that can simultaneously provide good power performance and acceptable output return loss.

S-parameter simulation result of the one stage power amplifier is presented in Fig.4.18, it can provide nearly 8 dB small-signal gain and have a bad output return loss. Fig. 4.19 is the power performance of the one-stage power amplifier. The peak PAE is 12 % and the OP_{1dB} is about 8 dBm. We can use the gain provided by the one-stage power amplifier to calculate the link budget in next section. The output matching will be reused after the linearizer is inserted.

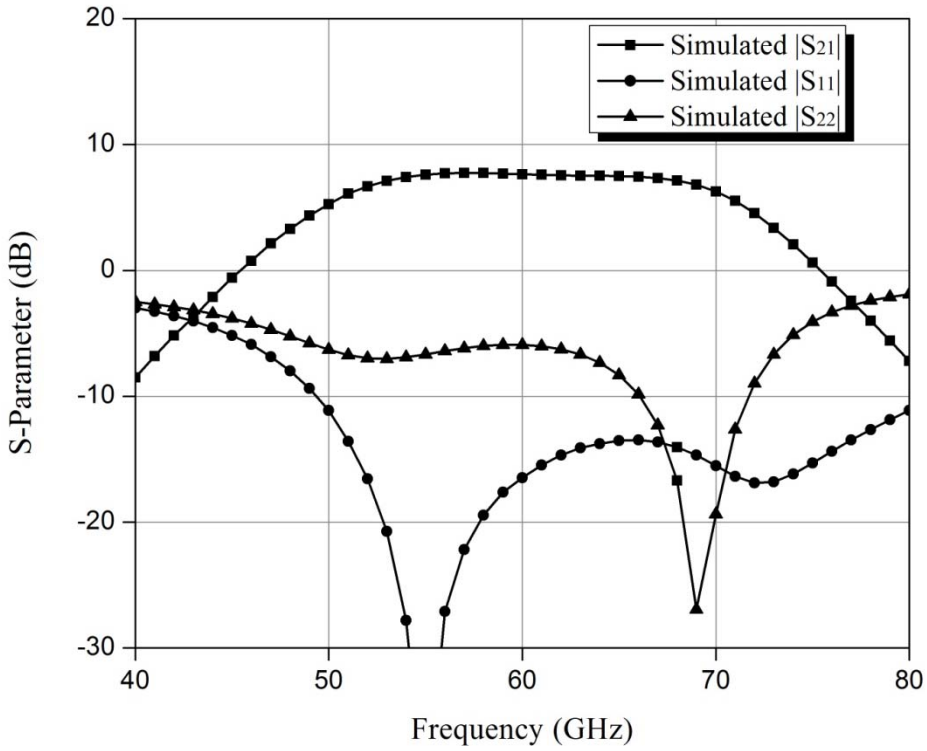


Fig. 4.18 S-parameter of the one-stage power amplifier.

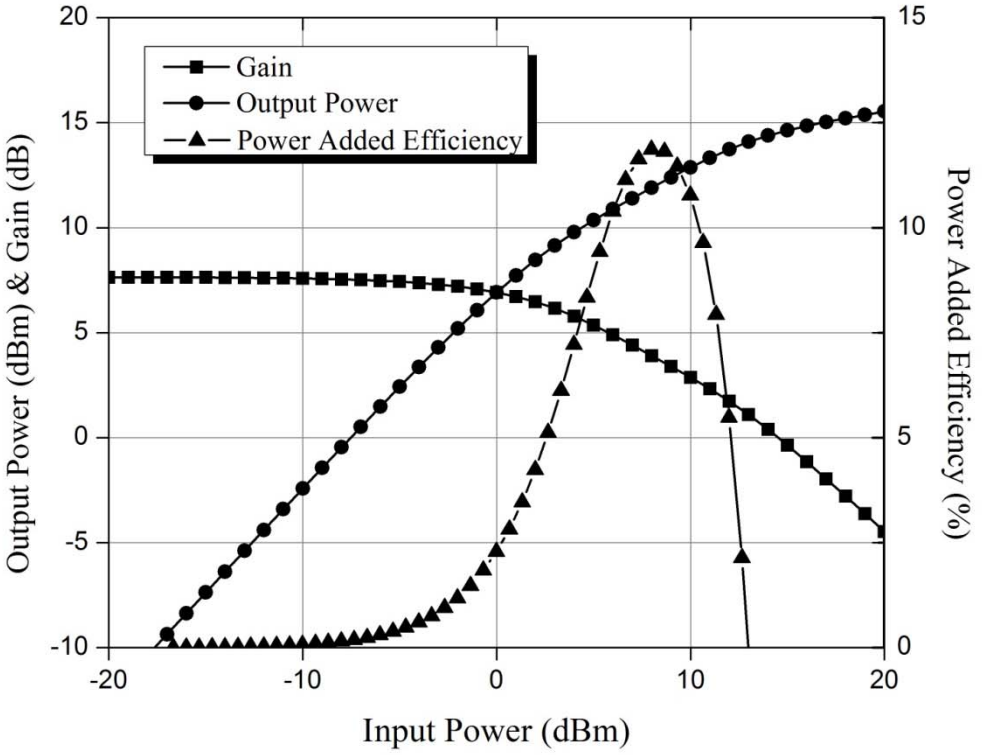


Fig. 4.19 Power performance of the one-stage power amplifier

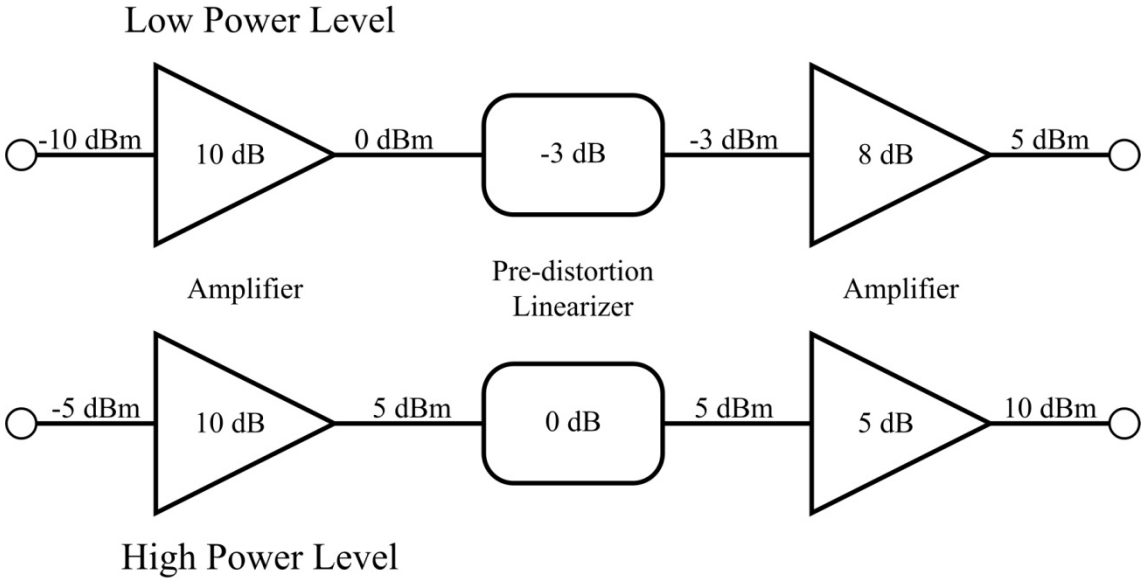


Fig. 4.20 Link budget of two-stage power amplifier with linearizer.

4.3.3 Link Budget

If we want to design a two-stage power amplifier, we should carefully calculate the device size ratio of the power stage and gain stage. A parameter that we should know is

the gain provided by power stage. The calculation to decide the device size ratio is called link-budget. After the design of one-stage power amplifier, we have known the gain that one stage can provide under the loss of CMOS process. Therefore, we have enough information for the link-budget calculation. The main objective of line-budget is to ensure the output power of gain stage is large enough to drive the power stage until the power stage saturates. The notation can be formulated as

$$OP_{1dB,gain} > IP_{1dB,power} \tag{4.1}$$

, which $OP_{1dB,gain}$ is the OP_{1dB} of gain stage and $IP_{1dB,power}$ is the IP_{1dB} of power stage. Since the output power of the device is proportion to its device size, we also have

$$\frac{OP_{1dB,power}}{OP_{1dB,gain}} = \frac{w_{power}}{w_{gain}} \tag{4.2}$$

, which w_{power} and w_{gain} mean the total gate width of power and gain stage.

There are two possible nodes we can put the linearizer. The first one is the node before power stage. The second one is the node before gain stage. No matter which node we place linearizer; the device size ratio would be the same. Fig. 4.20 is a calculation example of inserting the linearizer at node before power stage. We expect the linearizer to provide a 3 dB loss at low power level and no loss at high power level. Consider Fig. 4.19, the new OP_{1dB} of power stage after adding a linearizer with 3 dB loss should be at the old output power of 4-dB compression point (OP_{4dB}). This is because the linearizer will extend the gain curve by reducing the gain at low power level. The new $OP_{1dB,power}$ is about 10 dBm.

At the new $OP_{1dB,power}$, the gain of power stage is about 5 dB and the loss of linearizer is zero. Therefore, the new $IP_{1dB,power}$ is about 5 dBm. In order to guarantee the power can deliver without saturation, we make $OP_{1dB,gain} = IP_{1dB,power} + 2(dB)$. The extra 2 dB is the margin for the guarantee.

Since the $OP_{1dB,gain}$ will be 7 dBm with a 10-dBm new $OP_{1dB,power}$, the device size ratio is 2, which is about 3 dB. The power stage should be two times larger than the gain stage. Since we have choose a device with 16 mA dc current, we can make the power stage to be composed of two device, and the gain stage to have only one device.

On the other hand, if the linearizer is placed in front of gain stage, the device size ratio should also be 2. Consider the function of linearizer is to compensate the gain compression of power stage, the gain stage should not saturate before the new gain compression point. However, the gain that power stage can provide at the new gain compression point is 5 dB, which means the circumstances is similar to the former condition. Therefore, we also should have a device size ratio of 2.

4.3.4 Conventional Two-Stage Power Amplifier

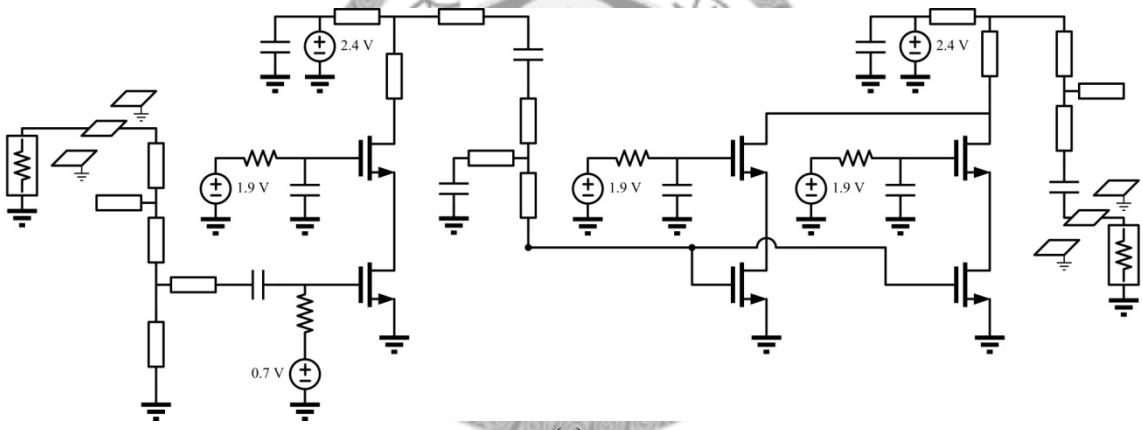
Since we have designed a one-stage power amplifier that has broad-band performance, we can use the output matching network of the amplifier for the output matching network of two-stage power amplifier. This is because the power stages are the same for the two amplifiers.

The major difference of the one-stage and two-stage design is the inter-stage matching network between the gain stage and power stage. We have to use the matching network to transform the input impedance of power stage to the power deliver contour of gain stage. The network is composed of two short stubs and three series lines, as shown in the center of Fig. 4.21 (a). Since the requirement of power matching is not as important for the gain stage, we can trade-off between the return loss and the power performance of the whole circuit by parameter tuning.

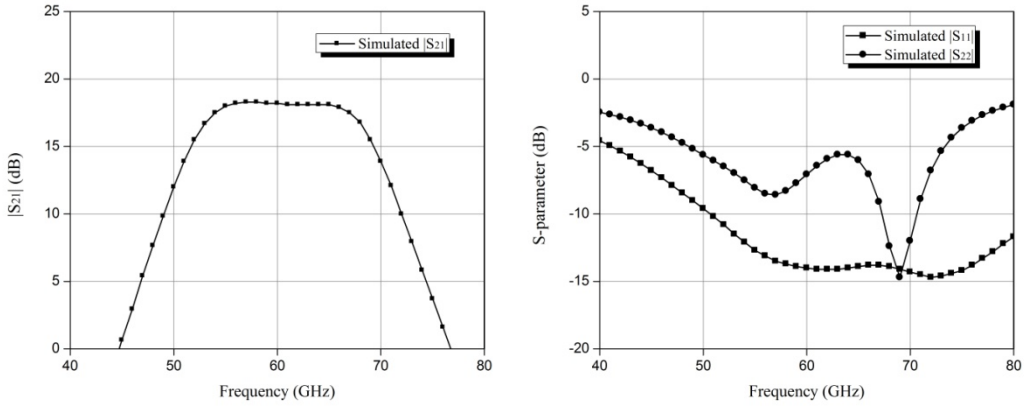
Finally, input matching network should be added in front of gain stage. The only requirement is to make the input return loss of whole circuit be more than 10 dB. The S-

parameter simulation result is presented in Fig. 4.21 (b). The circuit can provide 18 dB small-signal gain can have input and output return loss more than 10 dB and 5 dB respectively.

The power performance is presented in Fig. 4.22. The circuit can provide OP_{1dB} of 7.5 dBm with a 6 % PAE. The peak value of PAE is 12.5 % and the P_{sat} is 14 dBm. The circuit is a standard cascode power amplifier with poor linearity but high output power because the difference between OP_{1dB} and P_{sat} is more than 6 dB and the difference between IP_{1dB} and input power at peak PAE is about 11 dB. Since the peak PAE is high, the power amplifier has the potential to have great power performance after the linearizer is added.



(a)



(b)

Fig. 4.21 (a) Circuit schematic and (b) S-parameter simulation result , of conventional two-stage power amplifier.

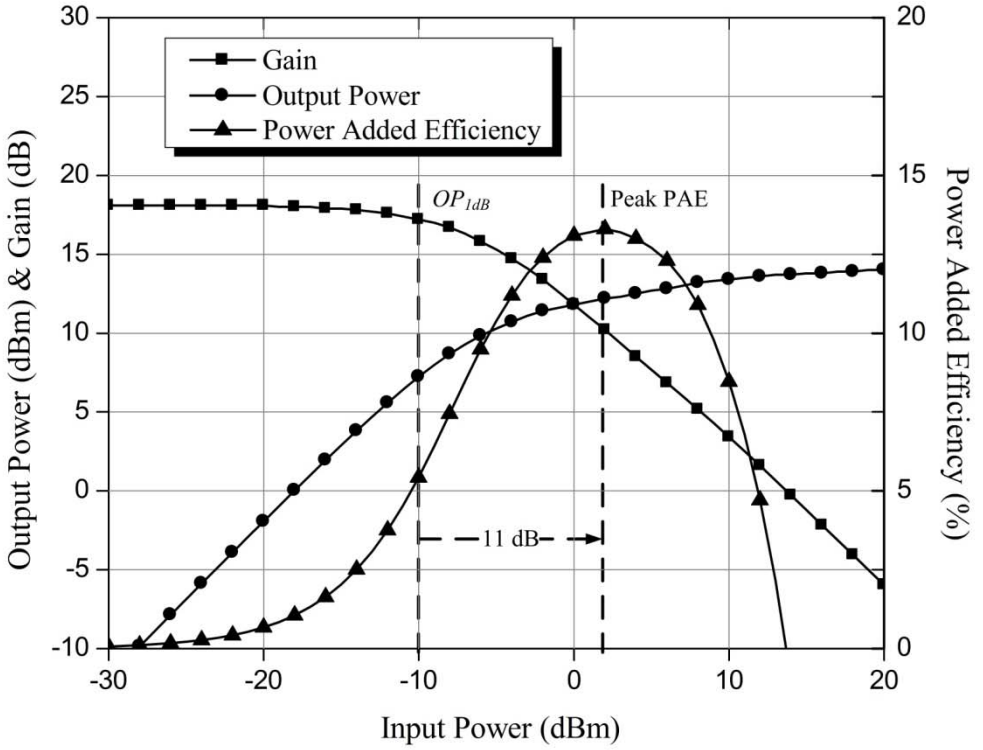


Fig. 4.22 Power performance of conventional two-stage power amplifier.

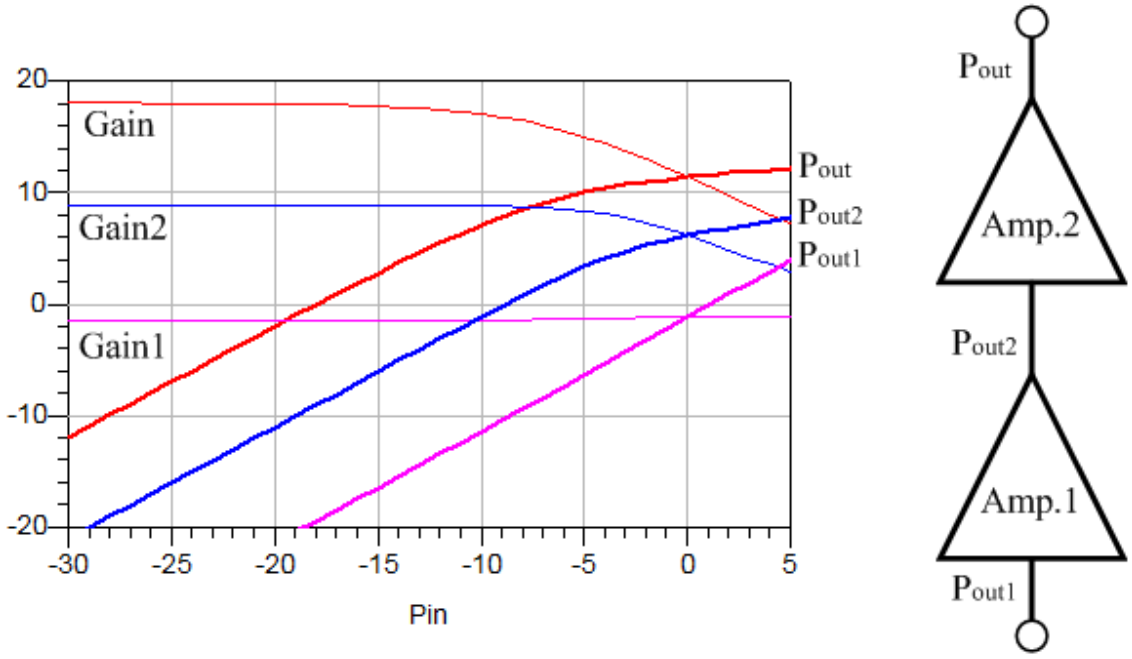


Fig. 4.23 Gain curve and output power of conventional two-stage power amplifier at different node of the circuit.

4.3.5 Power Performance at Different Node of Power Amplifier

Since we have to decide which point to insert linearizer in a two-stage power amplifier, the required power at different node of the circuit should be known. By comparing the normal output power of linearizer that can provide enough loss deviation with the power at each node, we can match the loss deviation and gain compression at the same power level.

Fig. 4.23 shows the gain curve and power curve of conventional two-stage power amplifier at different node of the circuit. The power of each node at the OP_{1dB} should be read out. The node in front of gain stage has a power of -10 dBm and the node in front of power stage has a power of -1 dBm at the IP_{1dB}. We do not consider the node at the output port of power stage because the power level is too high to sever a severe power wasting.

4.4 Integration of Linearizer to Power Amplifier

After the two-stage power amplifier is designed, we are going to insert a linearizer into the amplifier. Admittance of amplifier can be used to find out the admittance of linearizer that can result in the amount of loss we want. Based on the admittance requirement, several loss curves are provided for reading out the output power that can provide enough loss deviation. We finally decide to insert the linearizer before the power stage device because it is the node that the output power of linearizer and input power of amplifier are similar. Power stage of the two-stage amplifier is then used to choose the device size and the control voltage of the linearizer.

The selection process of device size would be the same for the linearizer with and without delay line. Since we have discussed the phase of the delay line in the former chapter, the phase delay of the delay line will not be changed in the design process. The

phase of the delay line is fixed at 90 degree during the design process. The design process will be focused on other parameters, including total gate width and control voltage of the transistor.

After the device size of the linearizer is selected, we will composite the power stage and the linearizer together to be the new power stage. Conventional design process will be applied to the new power stage and form a new power amplifier with the delay line linearizer. Simulation results before and after the electrical-magnetic simulation will be presented.

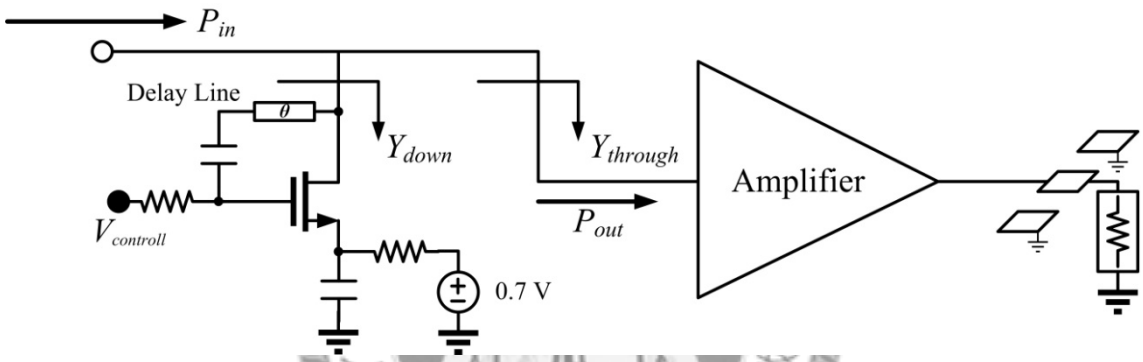


Fig. 4.24 Input power is divided by the admittance of amplifier and linearizer.

4.4.1 Power Division and Gain compensation

The object of this section is to propose a practical process of device size selection. We will introduce a simulation figure that can help us to know the compensation ability of a linearizer for specific power amplifier. The curve is practical because it provides a way to directly read out the value we need. Based on the curve, we can know the best control voltage of a linearizer with specific total gate width. Moreover, the envelope of loss deviation curve for a linearizer under different control voltage can provide us the maximum reachable loss deviation under different output power, which can help us to know the limitation of specific linearizer. We can also compare the envelope curve of different device size to select the most proper total gate width.

A. Power division

Based on Fig. 4.24, we will investigate the method of calculate the loss of linearizer. In the linearizer design, we highly concern the loss and its variation. If we want to find a linearizer that can achieve the loss we expect, we have to know what factor will affect the amount of loss. In the former chapter, we have known the reason of better loss deviation. But we should also consider the loss in low power level to understand the effect of linearizer to the gain of power amplifier. We can understand the power division concept from following equation.

Input power can be separated as

$$P_{in} = P_{through} + P_{down} \tag{4.3}$$

The power flows into the power stage and the linearizer are formulated as

$$P_{through} = \mathrm{Re}\left(V_d \times I_{through}\right) = \mathrm{Re}\left(V_d \times Y_{through} \times V_d\right) = \left|V_d^2\right| \times \mathrm{Re}\left(Y_{through}\right) \tag{4.4}$$

and

$$P_{down} = \mathrm{Re}\left(V_d \times I_{down}\right) = \mathrm{Re}\left(V_d \times Y_{down} \times V_d\right) = \left|V_d^2\right| \times \mathrm{Re}\left(Y_{down}\right) \tag{4.5}$$

, respectively.

Neglect the power reflection resulted from the mismatching, the loss of the linearizer can be defined as

$$Loss = \frac{P_{through}}{P_{in}} = \frac{P_{through}}{P_{through} + P_{down}} = \frac{\mathrm{Re}\left(Y_{through}\right)}{\mathrm{Re}\left(Y_{through}\right) + \mathrm{Re}\left(Y_{down}\right)} \tag{4.6}$$

Therefore, if we have known the input admittance of power stage, we can choose the admittance of linearizer to know the loss introduced by it. As the input power is getting larger, the admittance of linearizer will be smaller. The value of equation (4.6) will increase and results in a lower loss.

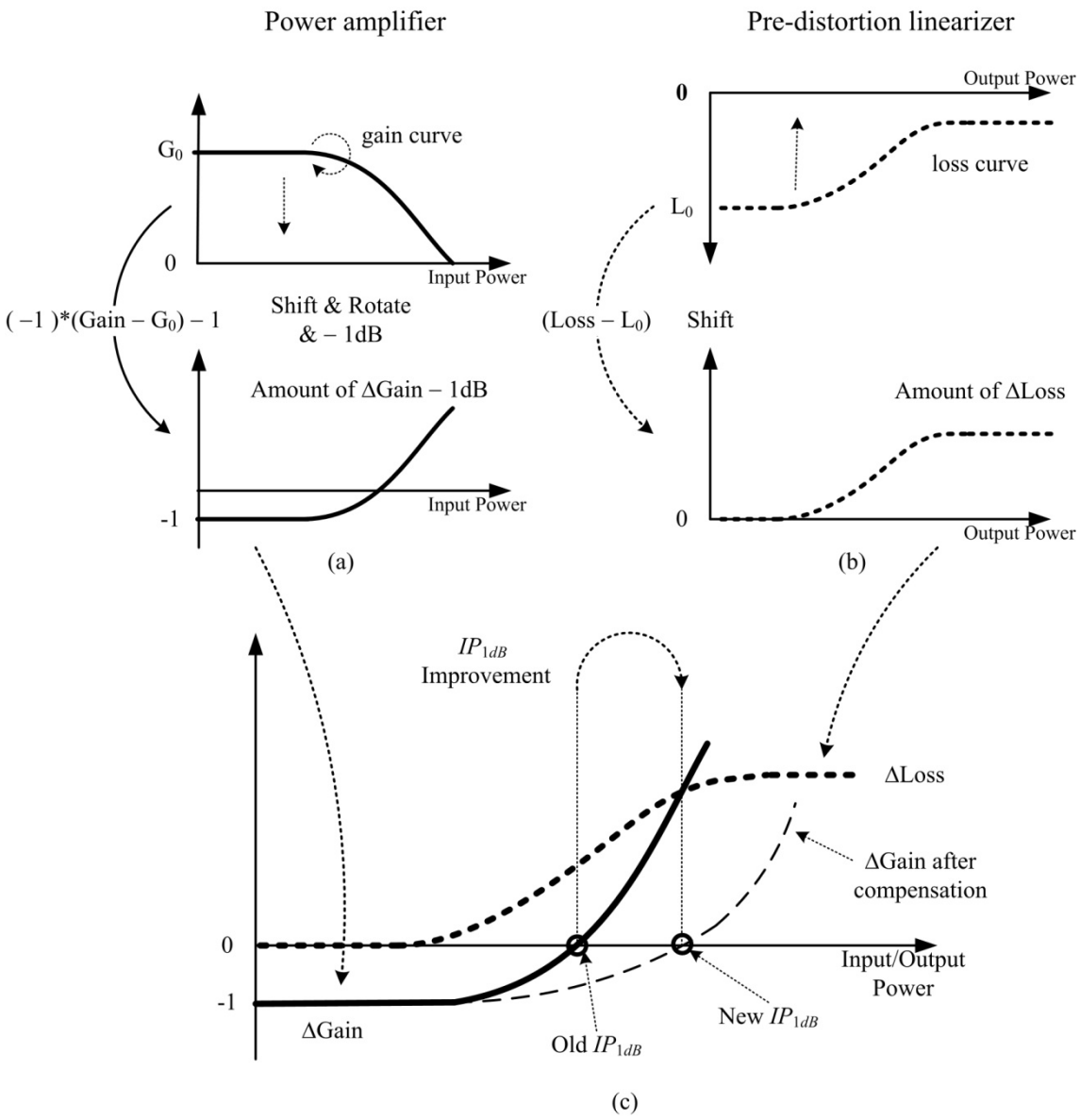


Fig. 4.25 Methods of producing curves that represents amount of (a) gain compression, and (b) loss deviation. Place the two curves together to form the (c) compensation curve.

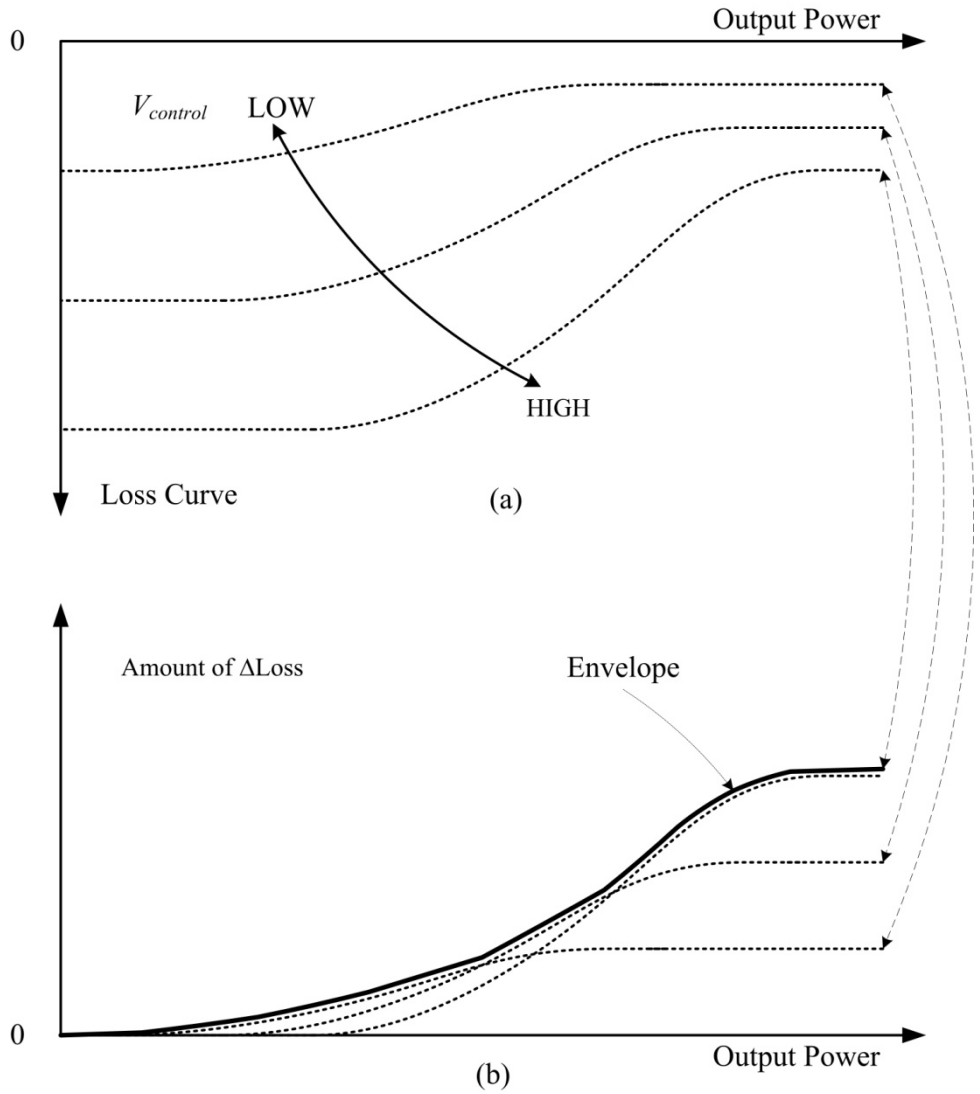
B. Compensation curve for a better OP_{1dB}

In Fig. 4.25 (a), we transform the gain curve of power amplifier to be a curve that represents the amount of gain compression under different input power. In order to focus on the IP_{1dB} point, we then shift the gain compression curve by -1 dB. The interception of the curve with x-axis is the point of IP_{1dB}. The curve that is larger than 0 dB is the amounts of gain-compression that must be compensated by linearizer to form

an extension of IP_{1dB}.

Similarly, as shown in Fig. 4.25 (b), the loss curve of linearizer should also be shifted to represent the loss deviation of it. The shift can help us to recognize the amount of gain compression it can compensate under different output power.

Placing the two new curves together will be helpful to know the improvement of IP_{1dB}, as shown in Fig. 4.25 (c). Since the gain compression curve is minus by 1 dB, the interception of the two new curves means the new position of IP_{1dB}.



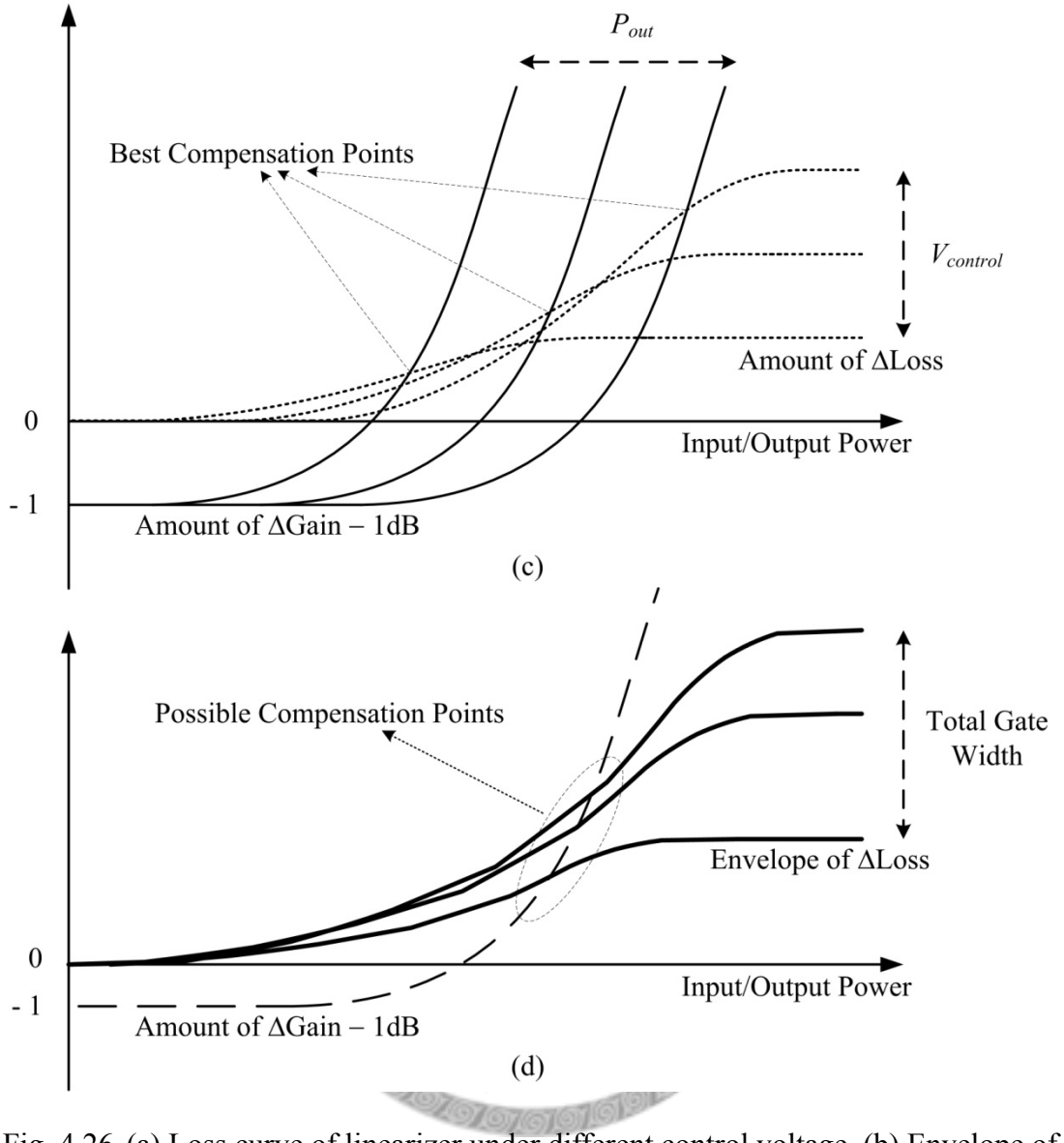


Fig. 4.26 (a) Loss curve of linearizer under different control voltage. (b) Envelope of loss deviation curve for specific total gate width. (c) Interception of loss deviation curves and gain compression curves. (d) Choose adequate total gate width by using envelopes of loss deviation curves with different total gate width.

C. Envelope of loss curve

Fig. 4.26 (a) is the loss curve of linearizer under different control voltage. We shift the loss at small output power to the position of 0 dB and define the curves as loss deviation curve. The loss deviation curves are shown in Fig. 4.26 (b). We then portray the envelope of them that represent the highest ability of loss deviation for a device with specific total gate width. The envelope can help us to compare the ability of device with

different total gate width and choose the one that can meet our requirement.

When the device size of linearizer is fixed, Fig. 4.26 (c) shows the method to choose control voltage for different gain compression curve. When the power level of power amplifier is low, we may want to use the low control voltage that can have a loss rising up earlier. If the power level is high, we can choose high control voltage that can provide high loss deviation and compensate more gain compression. In conclusion, the objective of this figure can help us to find the largest IP_{1dB} improvement that a device with specific total gate width can reach.

Fig. 4.26 (d) shows the points at which gain compression curve and envelopes of loss deviation curves intercept. The envelops are derived from the process presented in Fig. 4.26 (a). There are different envelopes of linearizers with different total gate width. The figure can help us to find out the adequate total gate width. Linearizer with large gate width will have a higher loss deviation curve because a large device is a multiple of small device. A three times larger device can provide three times loss deviation. However, the large device will also introduce higher loss and make the loss rising up too late. Therefore, we should select the smallest device that provides enough loss deviation.

4.4.2 Linearizer Size and Control Voltage Selection

A. Node to insert linearizer

The best node we want to insert is the node before gain stage. Since same loss will consume lower signal power when the power level is low, we would like to place the linearizer at the node that power level is low. Since the node before the gain stage device is the node with lowest power level, we will first examine the possibility of placing the linearizer at the node.

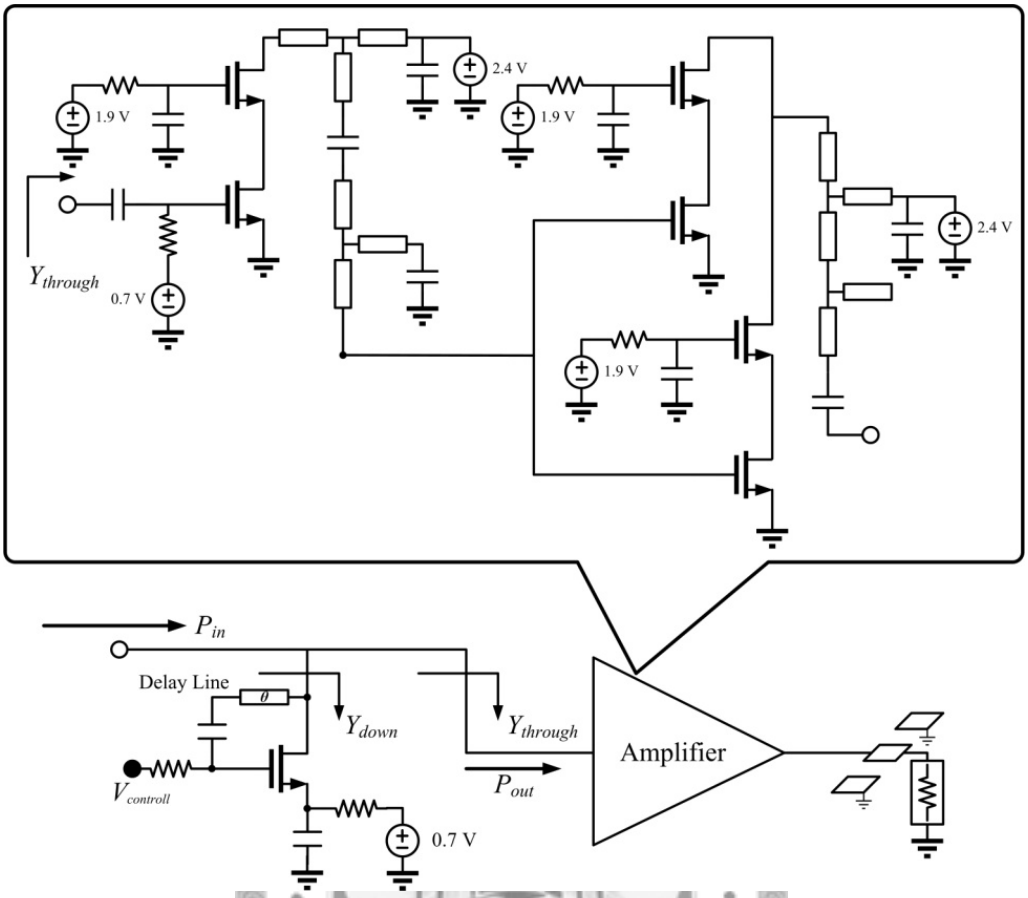


Fig. 4.27 Cascade linearizer with gain stage.

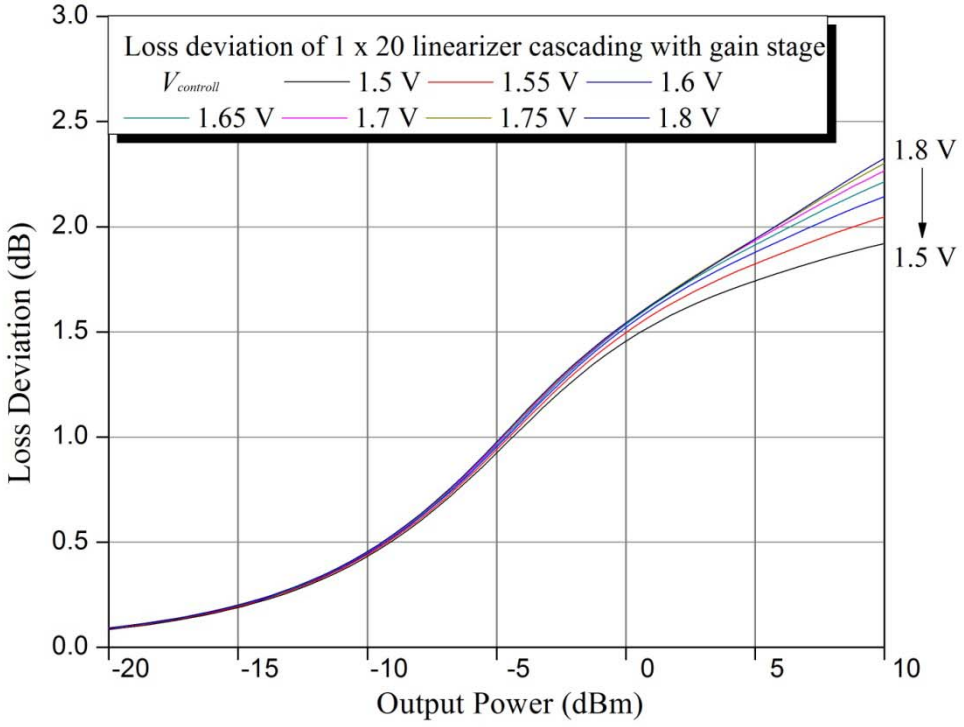


Fig. 4.28 Loss deviation curve of 20-μm-gate-width linearizer cascading gain stage.

As shown in Fig. 4.27, we cascade the linearizer with the gain stage. Fig. 4.28 shows the loss deviation curves of the 20-μm gate width linearizer when cascading the gain stage. Since we have known the output power level at the node is about -10 dBm from Fig. 4.23, we should notice the loss deviation that linearizer can provide around -10 dBm. As shown in Fig. 4.28, the linearizer can only provide 0.5 dB loss deviation around -10 dBm. Even though under a higher control voltage, the loss deviation cannot increase anymore. We may expect linearizer to have a smaller output power when it has smaller size. However, if we choose the linearizer with smaller gate width, we can only have a smaller loss deviation. We will not have a larger loss deviation around – 10 dBm. Therefore, the node before gain stage is not a good position for placing linearizer.

However, as we can observe from the loss deviation curve presented before, the loss deviation can reach 1dB around 0 dBm. This means the node before power stage may be an adequate place to insert linearizer. Fig. 4.29 shows the schematic that we will use to simulate the linearizer in the following paragraph.

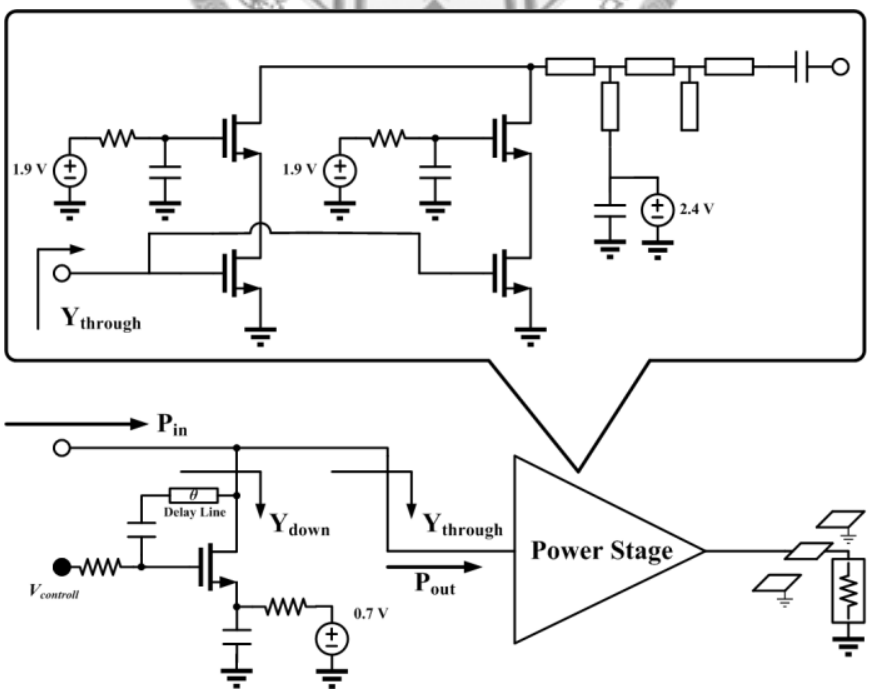
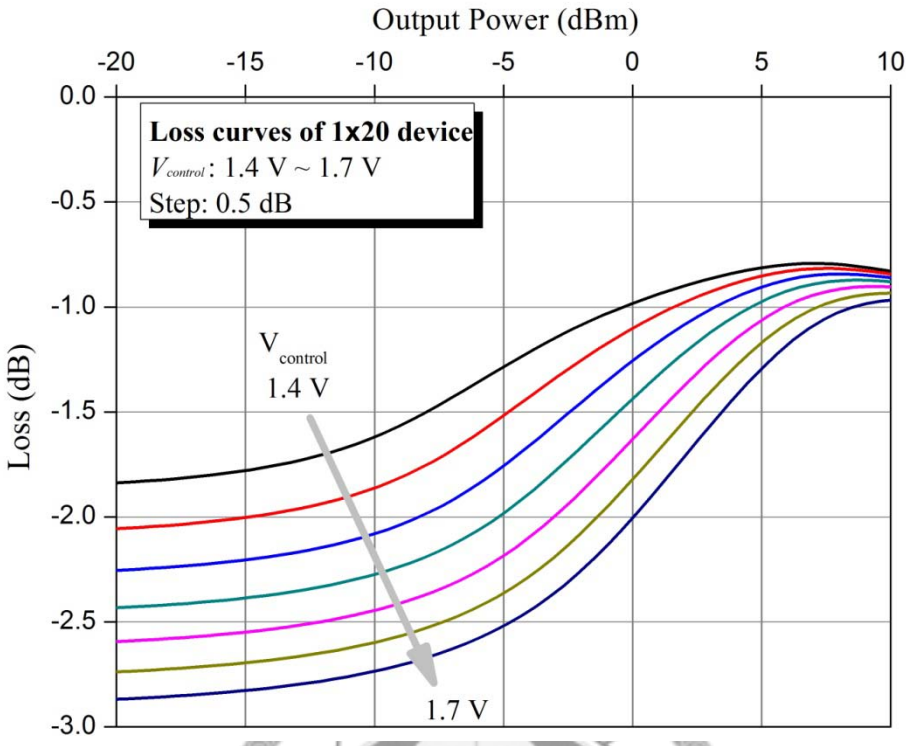
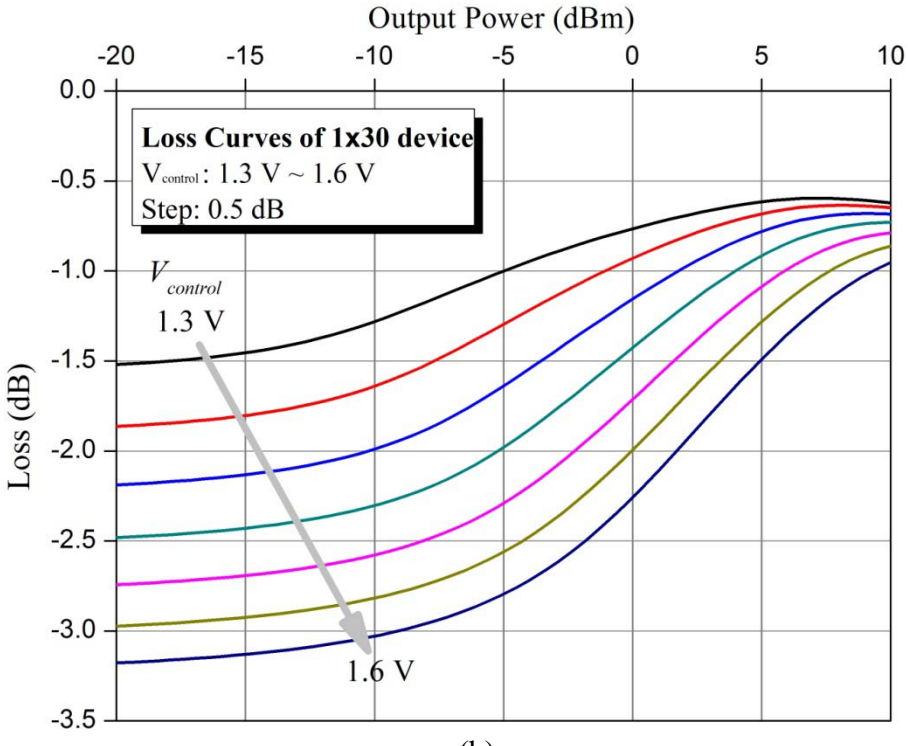


Fig. 4.29 Cascade linearizer with power stage.

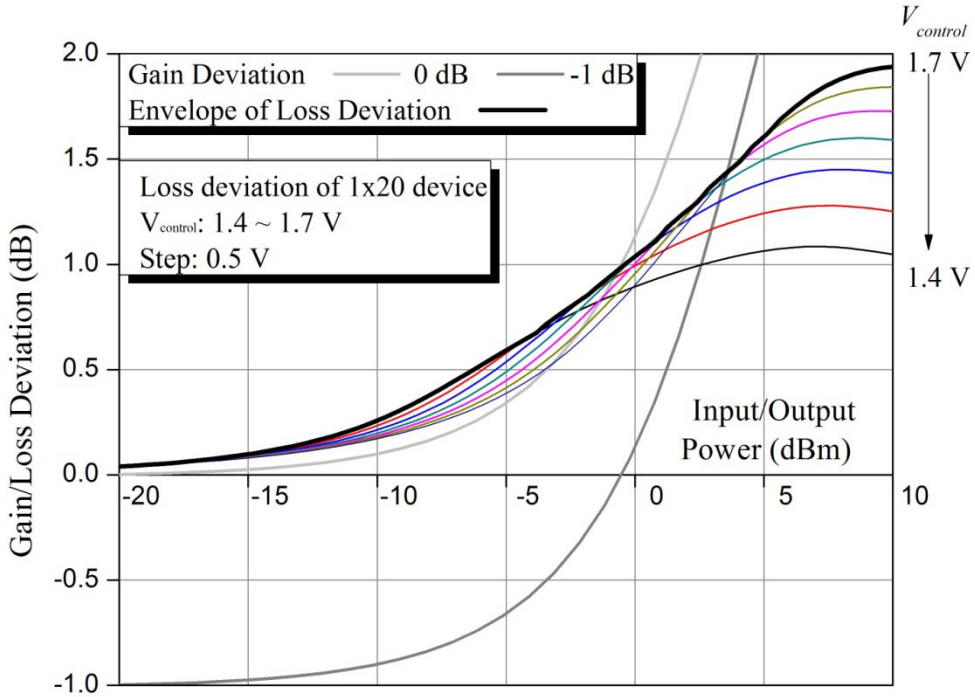


(a)

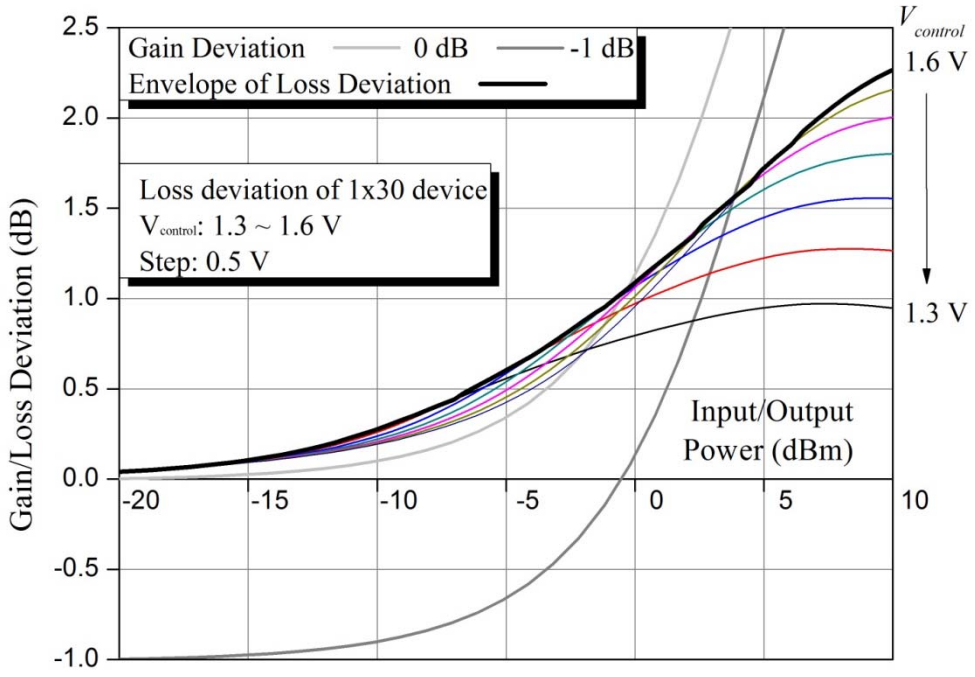


(b)

Fig. 4.30 Loss curves of linearizer with (a) 20-μm (b) 30-μm total gate width under different control voltage.



(a)



(b)

Fig. 4.31 Loss deviation curve of linearizer with (a) 20-μm (b) 30-μm total gate width under different control voltage and the envelope of them.

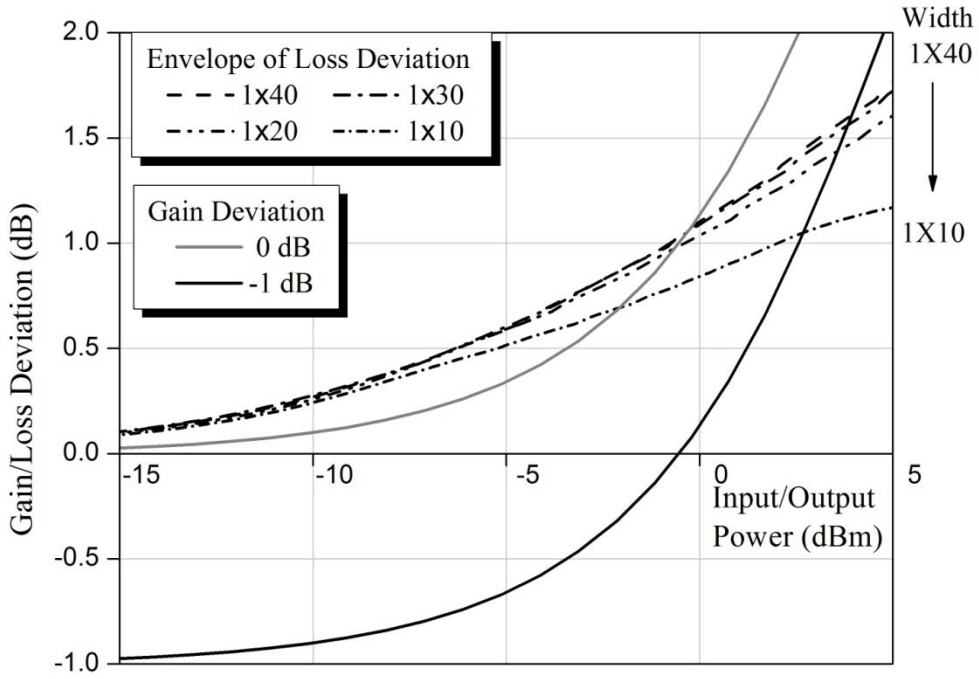


Fig. 4.32 Envelopes of loss deviation curves with different total gate width.

B. Total gate width selection

Fig. 4.30 presents the loss curve of linearizer with 20-μm and 30-μm total gate width. Following the step presented in Fig. 4.25 (a), we can get the loss deviation curve of them in Fig. 4.31 (a) and (b). The envelopes of them are also plot on the figure. Following the same steps, we can get envelopes of loss deviation curve of linearizer with other total gate width. All the envelopes are placed plot in Fig. 4.32 with the gain compression curve of the power stage.

As can be observe in Fig. 4.32, we can find the interception points of the envelopes with the gain compression curve. The interception point of 10-μm envelope can compensate the gain compression curve by 1 dB at the 3-dBm power. However, other envelopes can compensate about 1.5 dB at a higher power level. Even the large device can provide more compensations, it will also introduce more loss. Therefore, we will choose the envelopes that exhibit comparable compensation but has the smallest size.

Comparing the 40-μm envelope and 30-μm envelope, two curves are nearly the

same before the interception point with gain compression curve. Since the linearizer with 30-μm gate width is smaller, we will choose it for the lower small-signal loss

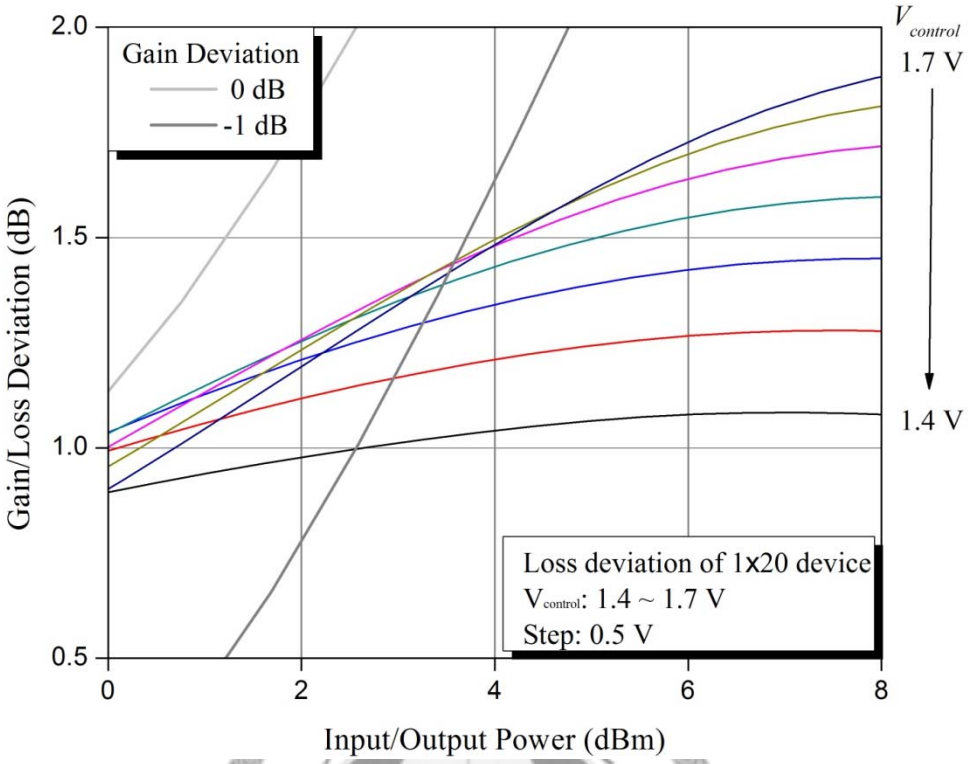
However, it is hard for us to choose between 30-μm and 20-μm envelope. The 30-μm envelope can provide slightly larger gain compensation while the 20-μm envelope will have lower small-signal loss. Since we have known the 30-μm envelope can provide about 0.1 dB more gain compensation from Fig. 4.32, we should know how large is the difference between small-signal gain of the two total gate width under their idea control voltage.

C. Control voltage selection

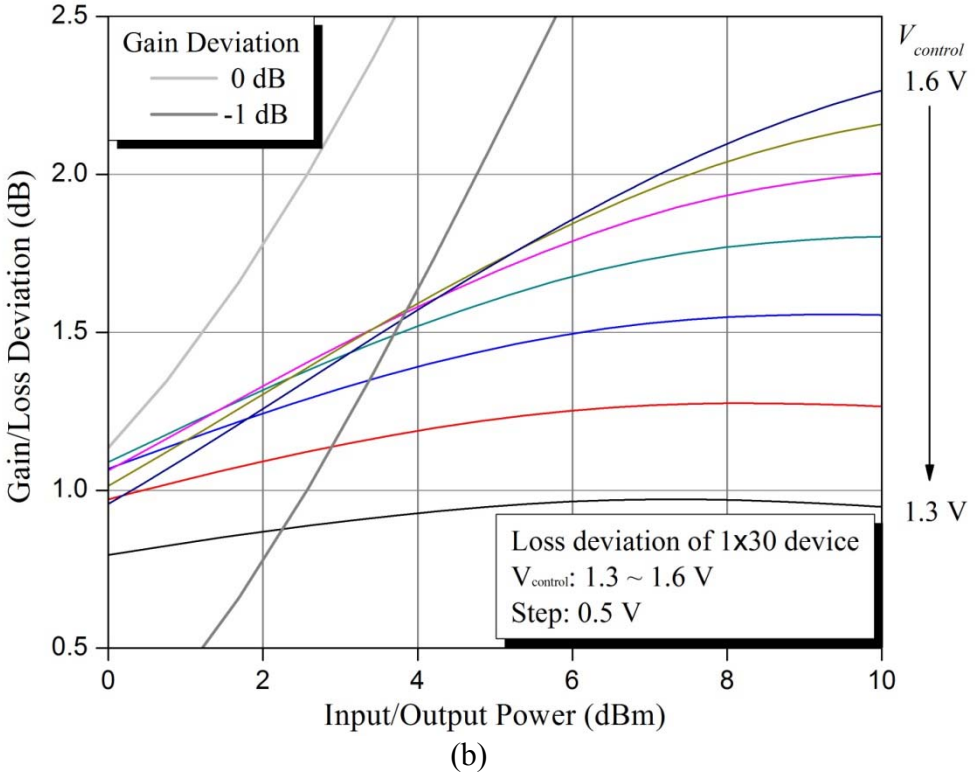
After knowing the linearizer with 20-μm and 30-μm to be the appropriate choice, we should know their ideal control voltage, and then compare their small-signal loss. Fig. 4.33 shows the loss deviation curve of linearizer with 20-μm and 30-μm gate width under different control voltage. The adequate control voltage should be the curve that forms the segment of envelope that intercepts with gain compression curve.

In Fig. 4.33 (a), the gain compression curve intercept with loss deviation curves of 20-μm that represents different control voltage. Among all the interception point, 1.6-V loss deviation curve has the largest value. Therefore, the ideal control voltage of 20-μm linearizer is 1.6 V. Similarly, Fig. 4.33 (b) is the loss deviation curve of 30-μm linearizer. The control voltage of 1.5 V can reach larger loss deviation than other control voltage.

Read the small-signal loss in Fig. 4.30 (a) and (b) for 1.6 V and 1.5 V respectively, we can find the small-signal losses are 2.6 dB and 2.75 dB for 20-μm and 30-μm device. The loss difference is 0.15 dB. Since we want to have a linearizer with smaller loss at small-signal, we finally choose total gate width of linearizer to be 20 μm. The ideal control voltage is 1.6 V.



(a)



(b)

Fig. 4.33 The detail figure of loss deviation curve of linearizer with (a) 20-μm (b) 30-μm total gate width under different control voltage.

4.4.3 Two-stage Power Amplifier with Modified Linearizer

Fig. 4.34 is the final circuit schematic includes DC bias circuits. The gain stage is formed by one cascode device with the size selected before while the power stage is formed by two cascode devices and the modified linearizer. Since the output port is still the original power stage, we can use the output matching network design before. Subsequently, the inter-stage and input matching network is designed through ordinary design process to ensure the power can flow forward. Followings are the simulation results of the power amplifier.

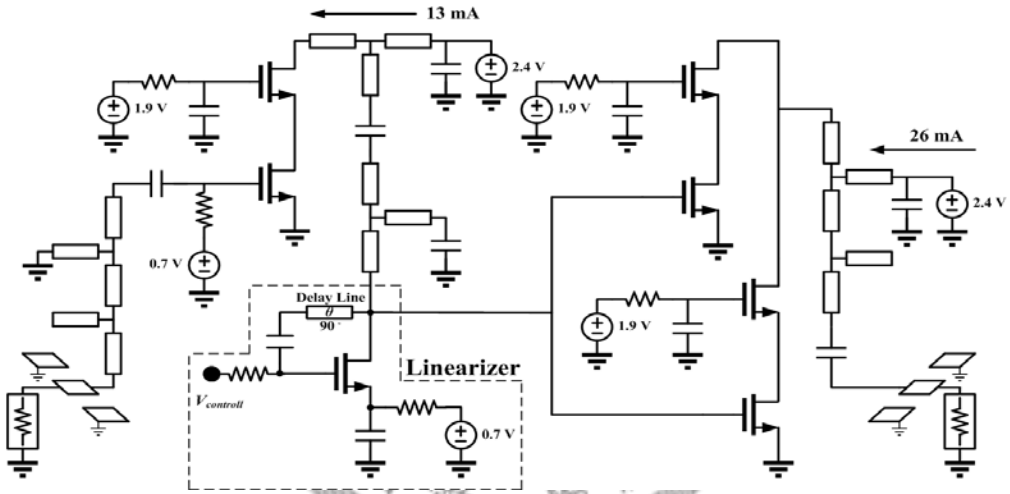


Fig. 4.34 Circuit Schematic of two-stage power amplifier with modified linearizer.

A. S-parameters and power performance

Figures Fig. 4.35 to Fig. 4.37 are simulated result of the complete circuit. The simulated $|S_{21}|$ can achieve nearly 15 dB from 57-66 GHz under 2.4 V power supply and 0.7 V gate bias voltage, as shown in Fig. 4.35. Form Fig. 4.36, the simulated $|S_{11}|$ is larger than 14 dB from 57 GHz to 66 GHz. However, the simulated $|S_{22}|$ is has a smallest value of 4 dB. The output return loss is sacrificed for the power performance. The simulated power performances are provided in Fig. 4.37. The power amplifier can deliver a saturated power (P_{sat}) of 12.5 dBm and output 1-dB compression power (OP_{1dB}) of 12 dBm with power consumption of 100 mW. The simulated peak PAE can

achieve 12.5% while the PAE at $OP_{1dB.}$ is 10.5%.

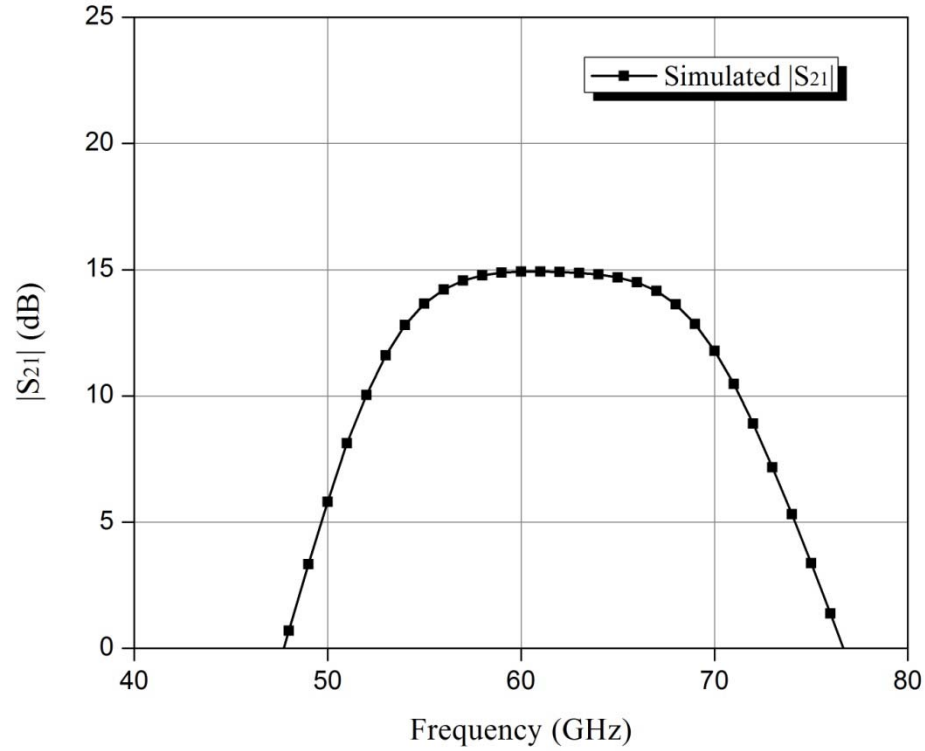


Fig. 4.35 Final simulated result of $|S_{21}|$ from 40-80 GHz.

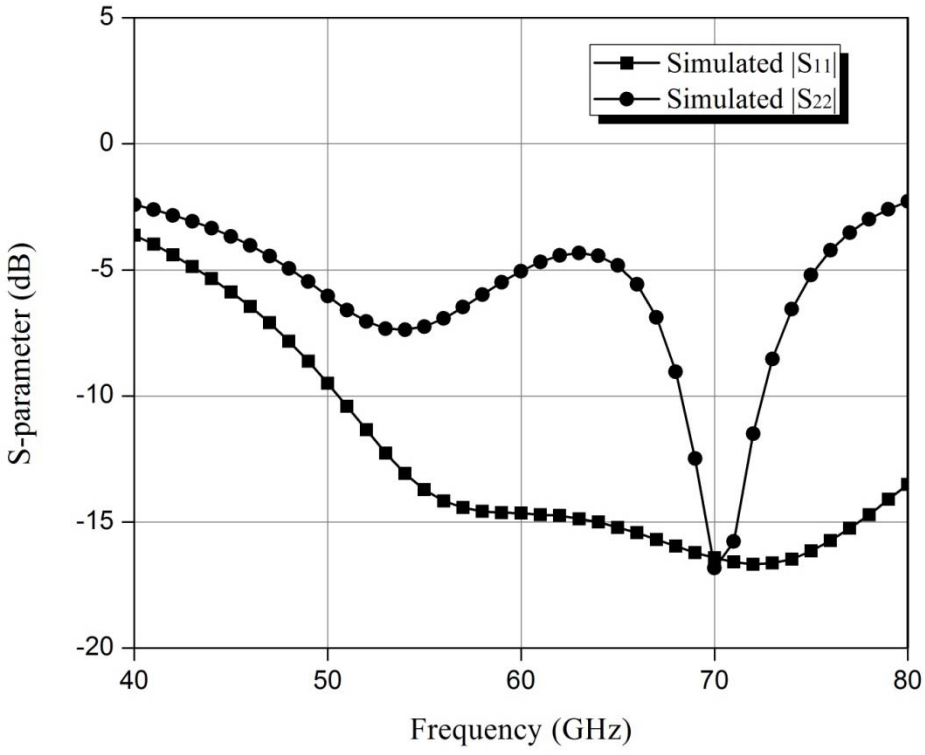


Fig. 4.36 Final simulated result of $|S_{11}|$ and $|S_{22}|$ from 40-80 GHz.

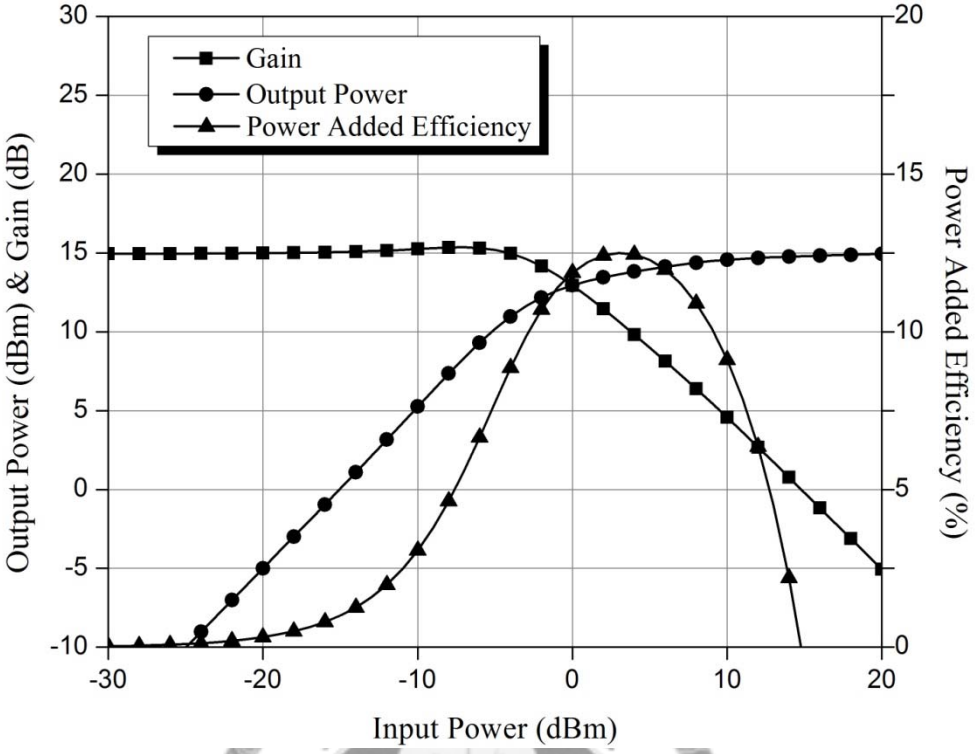


Fig. 4.37 Final simulated power performance.

B. AM-AM and AM-PM characteristics

On the other hand, Fig. 4.38 shows the gain curve of power amplifier with modified linearizer and that of conventional power amplifier without linearizer. The former one shows an extension of P_{1dB} point, which means the linearity in word of AM-AM characteristic, is improved. As shown in Fig. 4.38, the P_{1dB} is extended from -10 dBm to -5 dBm at least.

The AM-PM characteristic is also improved, as shown in Fig. 4.39. We can simulate the improvement of AM-PM characteristic by considering the point which the curves have a value of -5 degree. The input powers of the -5-degree points on two curves are about -5 dBm and -10 dBm respectively. The power amplifier with the modified linearizer shows an extension of the -5-degree point, which means a better AM-PM characteristic.

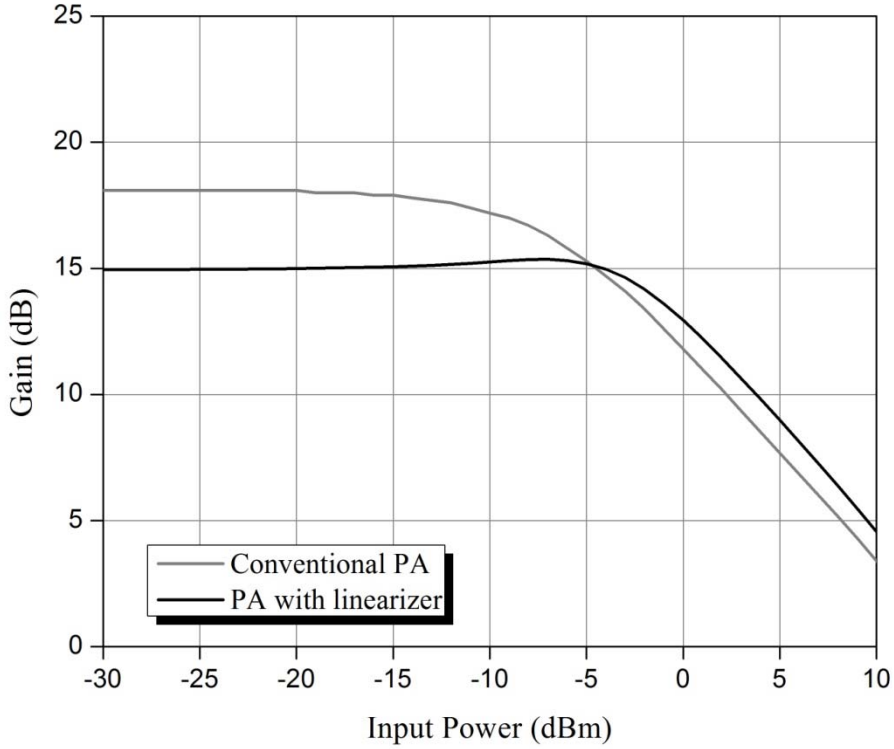


Fig. 4.38 Comparison of AM-AM characteristics of power amplifier with modified linearizer and conventional power amplifier without linearizer.

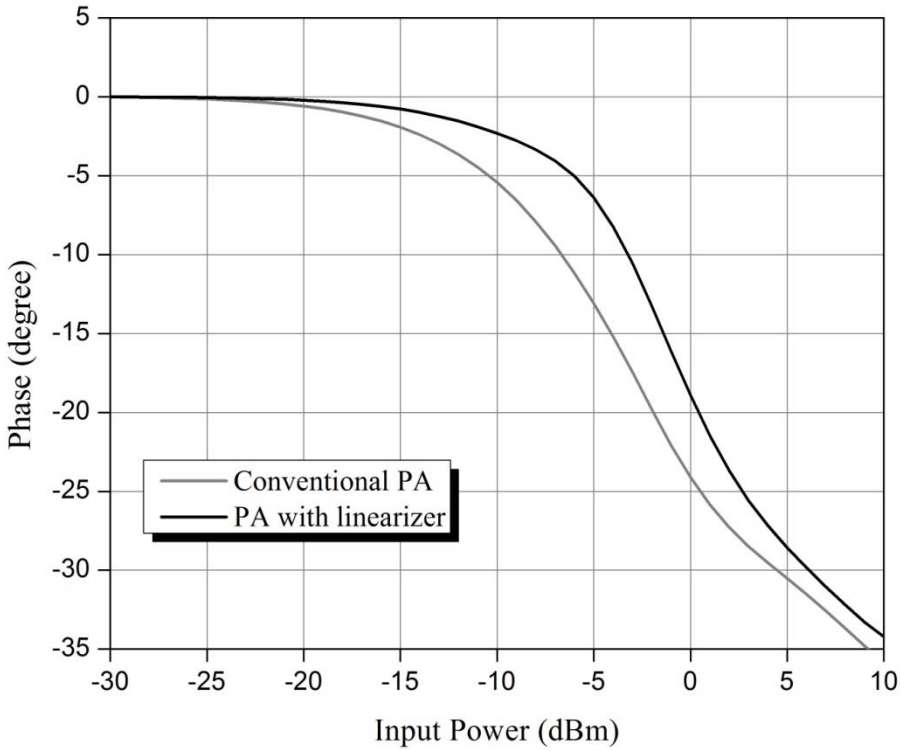


Fig. 4.39 Comparison of AM-PM characteristics of power amplifier with modified linearizer and conventional power amplifier without linearizer.

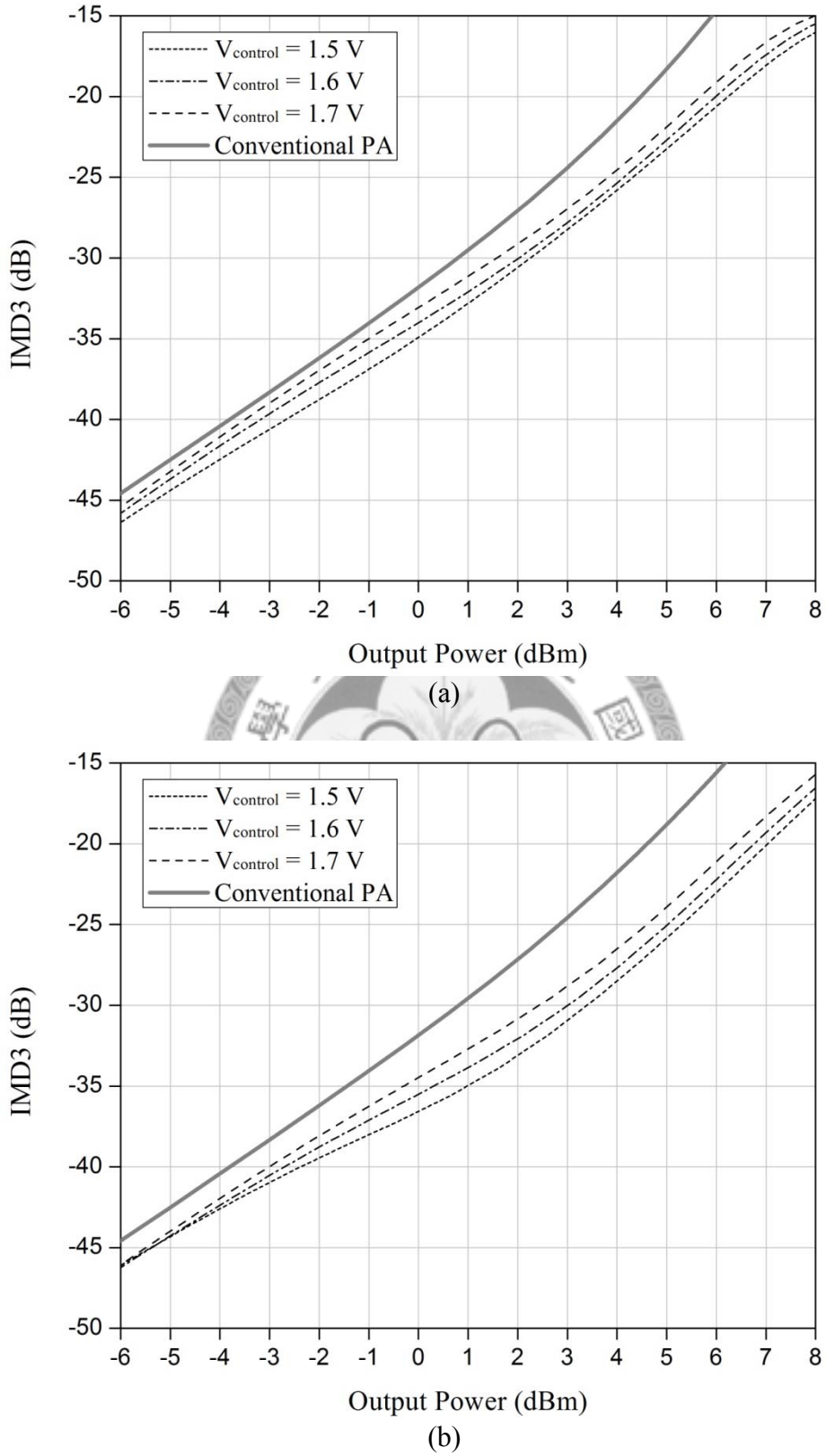
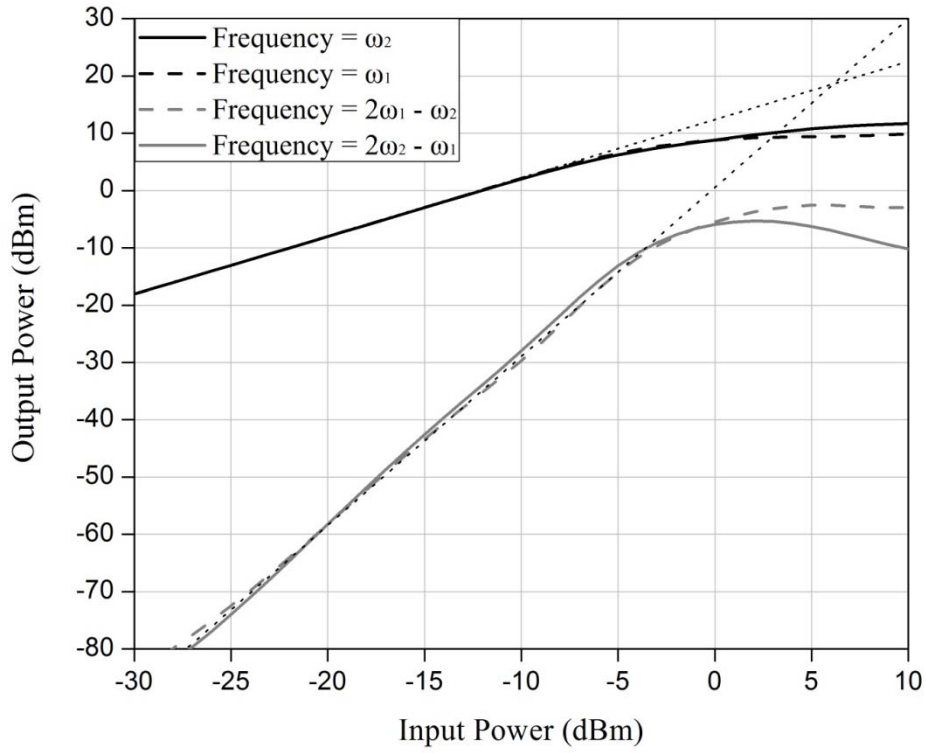


Fig. 4.40 (a) Upper-side-band and (b) lower-side-band IMD3 of conventional power amplifier and power amplifier with modified linearizer under different control voltage.

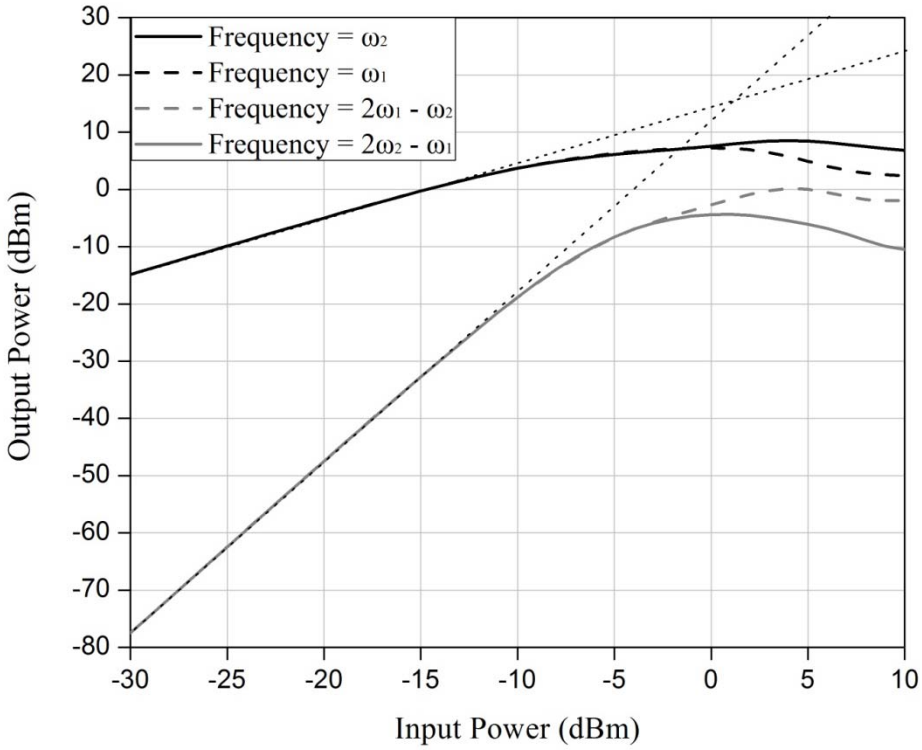
C. Third-order modulation

Instead of AM-AM and AM-PM characteristics, the linearity of power amplifier can also be measured by the two-tone test. The two-tone test is applied by driving the power amplifier by two frequencies that are separated by a little frequency difference. It can provide two kind of value for estimation of linearity. The first one is third-order intermodulation ratio (IMD3) and the second one is input power of third-order intercept point (IIP3).

The upper-side-band and lower-side-band IMD3 are provided in Fig. 4.40. The frequencies in the simulation are 59.9 and 60.1 GHz. We simulate the values under different conditions. The power amplifier with modified linearizer does provide better IMD3s in both figures. When comparing the performance under different control voltage, changing the control voltage has little influence to the IMD3 value.



(a)



(b)

Fig. 4.41 IIP3 of (a) power amplifier with modified linearizer under 1.6-V control voltage and (b) conventional power amplifier without linearizer.

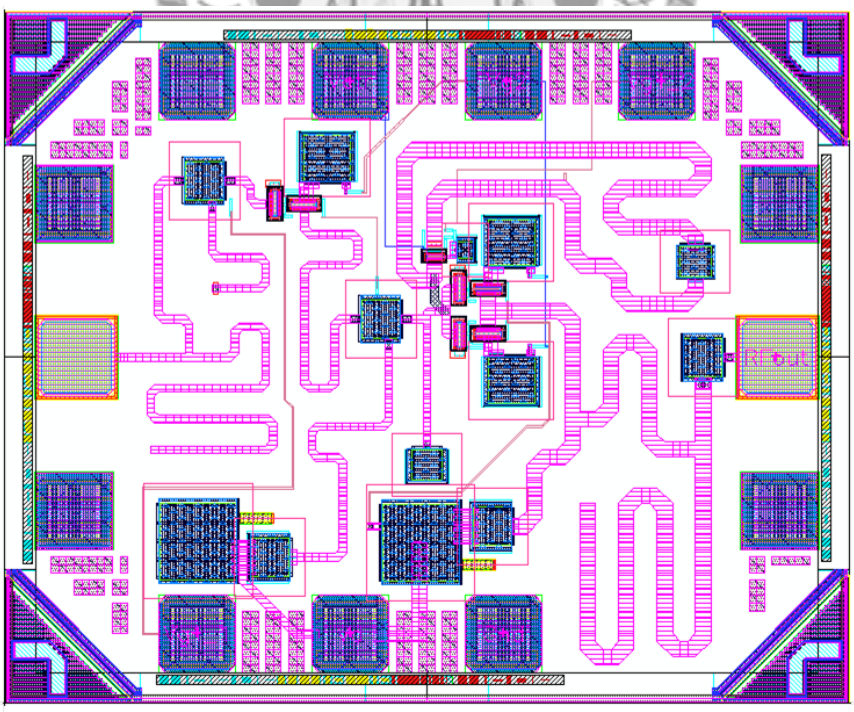


Fig. 4.42 Layout of the 57-66 GHz power amplifier with size of 0.45 x 0.55 mm^2.

IIP3s of power amplifier with modified linearizer under 1.6-V control voltage and conventional power amplifier are provided in Fig. 4.41. The value is improved from 1 dBm to around 6 dBm comparing the interception points of dash lines in Fig. 4.41 (a) and Fig. 4.41 (b). The layout of the circuit is shown in Fig. 4.42. The layout is plotted by Cadence and have the size of 0.45 x 0.55 mm^2 including all DC and RF pads.

4.5 Measurement Results

Fig. 4.43 is the chip photo of the complete circuit. The input port is at the left-hand side while the output port is at the right side. The voltages are biased through the DC pad at the top and bottom of the chip. This chip is measured by on wafer probing. A pair of 3-pin RF probes, a 3-pin DC probe and a 6-pin DC probe is used. The measurement results include *S*-parameters, IP_{1dB}, OP_{1dB} and P_{sat}.

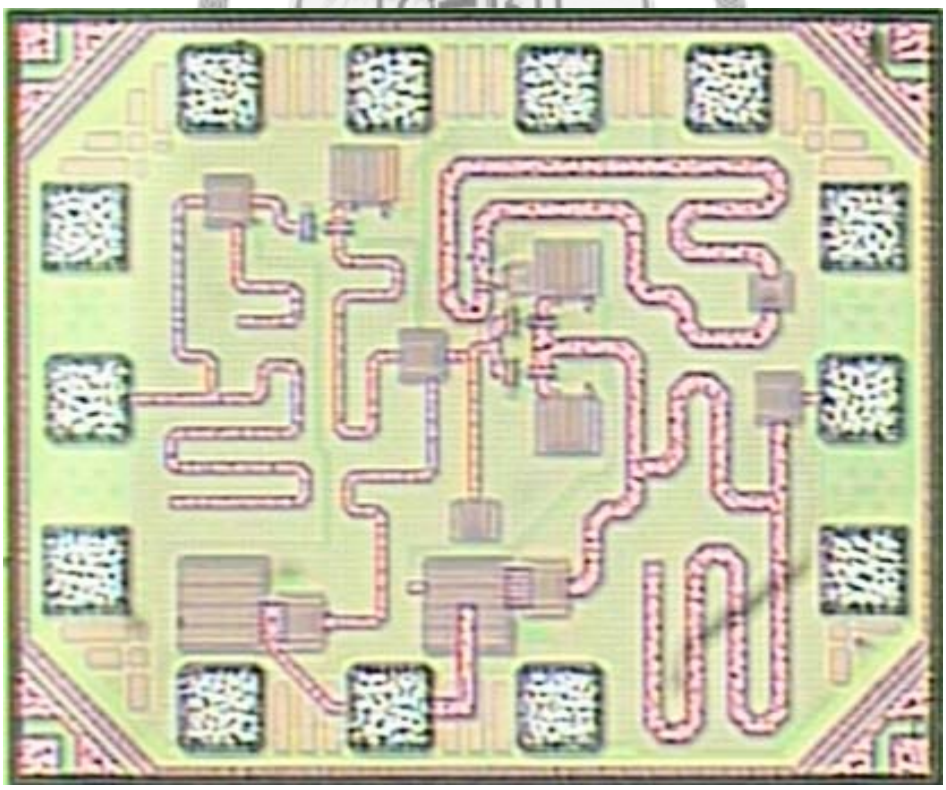


Fig. 4.43 Chip photo of the 57-66 GHz power amplifier chip with size of 0.45 x 0.55 mm^2 including all the testing pads.

4.5.1 *S*-parameter

Fig. 4.44 to Fig. 4.46 shows the simulated and measured S-parameters of this power amplifier. The cascode device of this circuit should be biased under 2.4 V power supply and has total drain current of 40 mA. The measurement results are similar to the simulated results but have a little frequency shift to higher frequency. Small-signal gains are higher than simulated value over 55 GHz, and is larger than simulated result by 2 dB at 67 GHz. The measured linear gains are increase from 15 dB to 17 dB from 55 to 67 GHz. Output return loss is higher than 7 dB and input return loss is higher than 9 dB from 57 to 66 GHz.

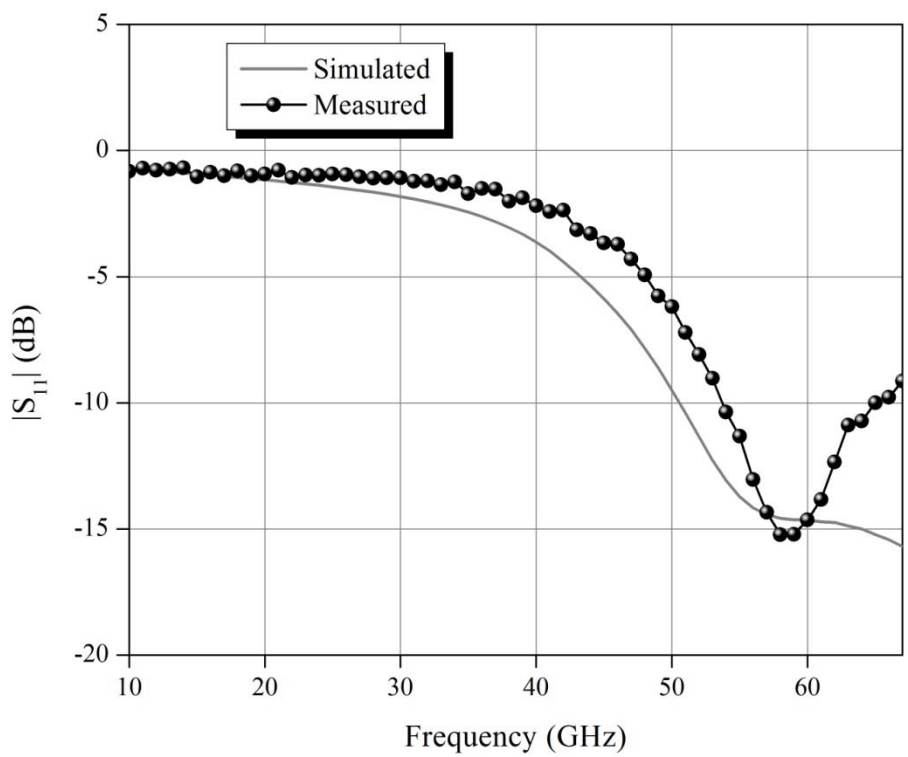


Fig. 4.44 Simulated and measured $|S_{21}|$ of the power amplifier from 30-67 GHz.

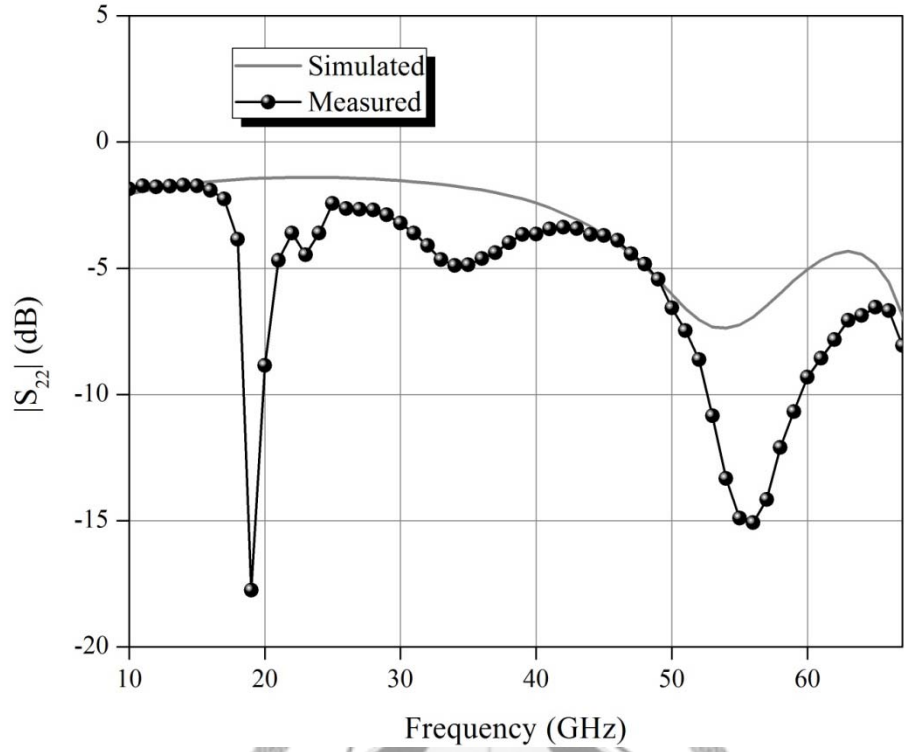


Fig. 4.45 Simulated and measured $|S_{22}|$ of the power amplifier from 30-67 GHz.

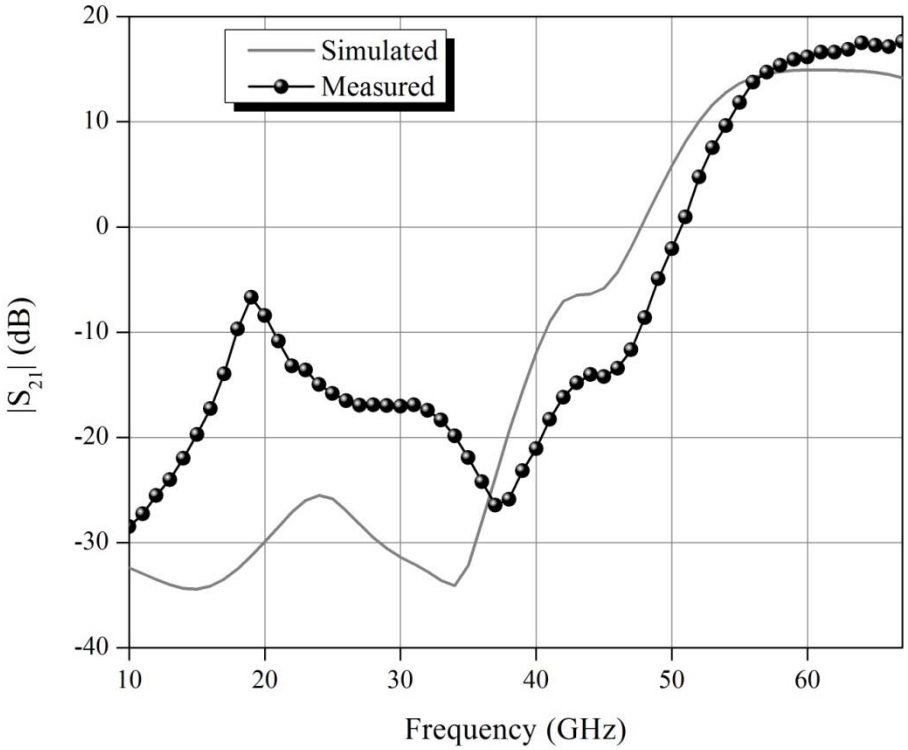


Fig. 4.46 Simulated and measured $|S_{21}|$ of the power amplifier from 30-67 GHz.

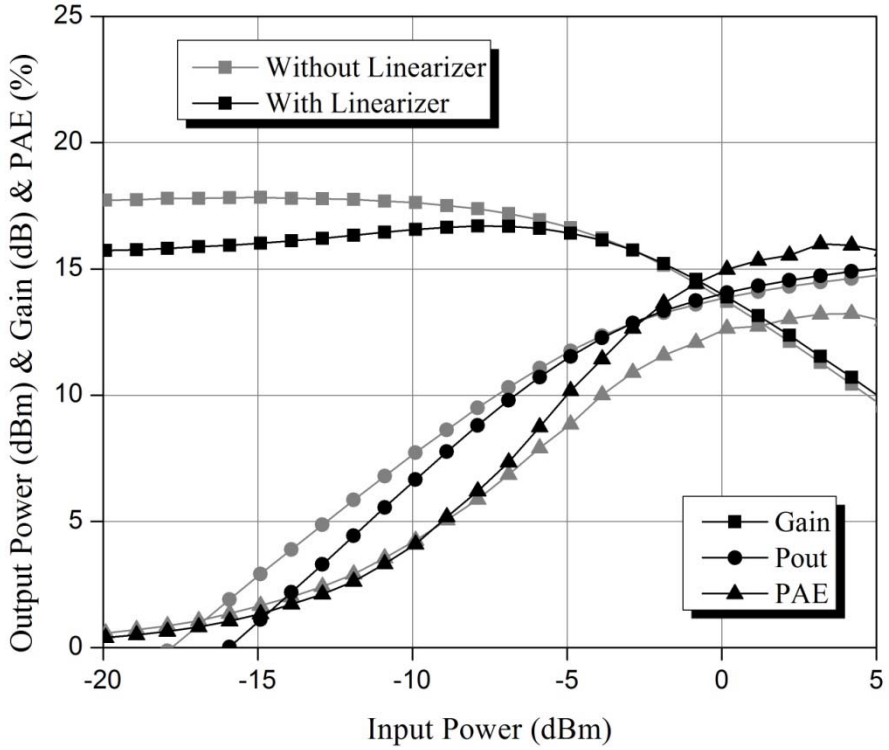


Fig. 4.47 The measured P_{out}, Gain, and PAE versus P_{in} when the linearizer of power amplifier is turn-on and turn-off at 60 GHz.

4.5.2 Power Performance

In Fig. 4.47, the measured output powers are plotted versus input power at 60 GHz. The gray line and the black line are the results that control voltage of linearizer is turn on and turn off. For a turn on linearizer, the power amplifier can deliver a saturated power of 15.4 dBm and achieve measured OP_{1dB} of 13.7 dBm. The PAE has a peak value of 16 % and a value of 14.3 % at OP_{1dB}.

Comparing the two curves in the figure, the linearizer does demonstrate a pre-distortion effect. The turn-on mode of power amplifier has a gain that is smaller by 2 dB than the turn-off mode. However, the gains are similar at larger power level which is the same to our expectation.

Table 4.1 lists important power parameters of power amplifier for different chips and different frequencies. As can be observed from the table, the power amplifier can

provide excellent power performance for 57 GHz, 60 GHz and 64 GHz. Moreover, power amplifiers can provide saturation powers more than 14-dBm under different frequencies. Since the saturation output power is totally decided by the output matching network, the table certifies the effectiveness of broadband power matching network.

The difference of P_{sat} and OP_{1dB} has smallest value at 57 GHz, which is 1.4 dB, and has the largest value at 64 GHz, which is 2.2 dB. The phenomena means the linearizer is more effective at lower frequency. Higher frequency is really a challenged factor of designing pre-distortion linearizer. The modification of linearizer does help the pre-distortion function of conventional linearizer.

Table 4.1 Power performance of different chips for different frequencies.

P_{in}		Chip 1			Chip 2		
Frequency		57 GHz	60 GHz	64 GHz	57 GHz	60 GHz	64 GHz
Low	Gain (dB)	13.66	15.34	15.75	13.98	15.66	15.97
1dB-compression	OP_{1dB} (dBm)	12.8	13.5	11.8	13	13.7	12.1
	PAE (%)	10.5	13.7	11.2	11.1	14.3	11.9
High(peak)	P_{sat} (dBm)	14.2	15.1	14	14.3	15.4	14.3
	PAE (%)	11.1	14.9	13.2	11.9	16	13.9

4.5.3 IMD3

Fig. 4.48 provides measured upper-side-band and lower-side-band IMD3 of power amplifier with modified linearizer biased by different control voltage. The 0.7-V control voltage means the linearizer is turn-off. When the linearizer is turn-on, the IMD3 is improved in upper-side-band but remains unchanged in lower-side-band. However, the IMD3s are not improved in high power level. The output power at which the IMD3 is

improved by at least 5 dB is about 3 dBm for one tone.

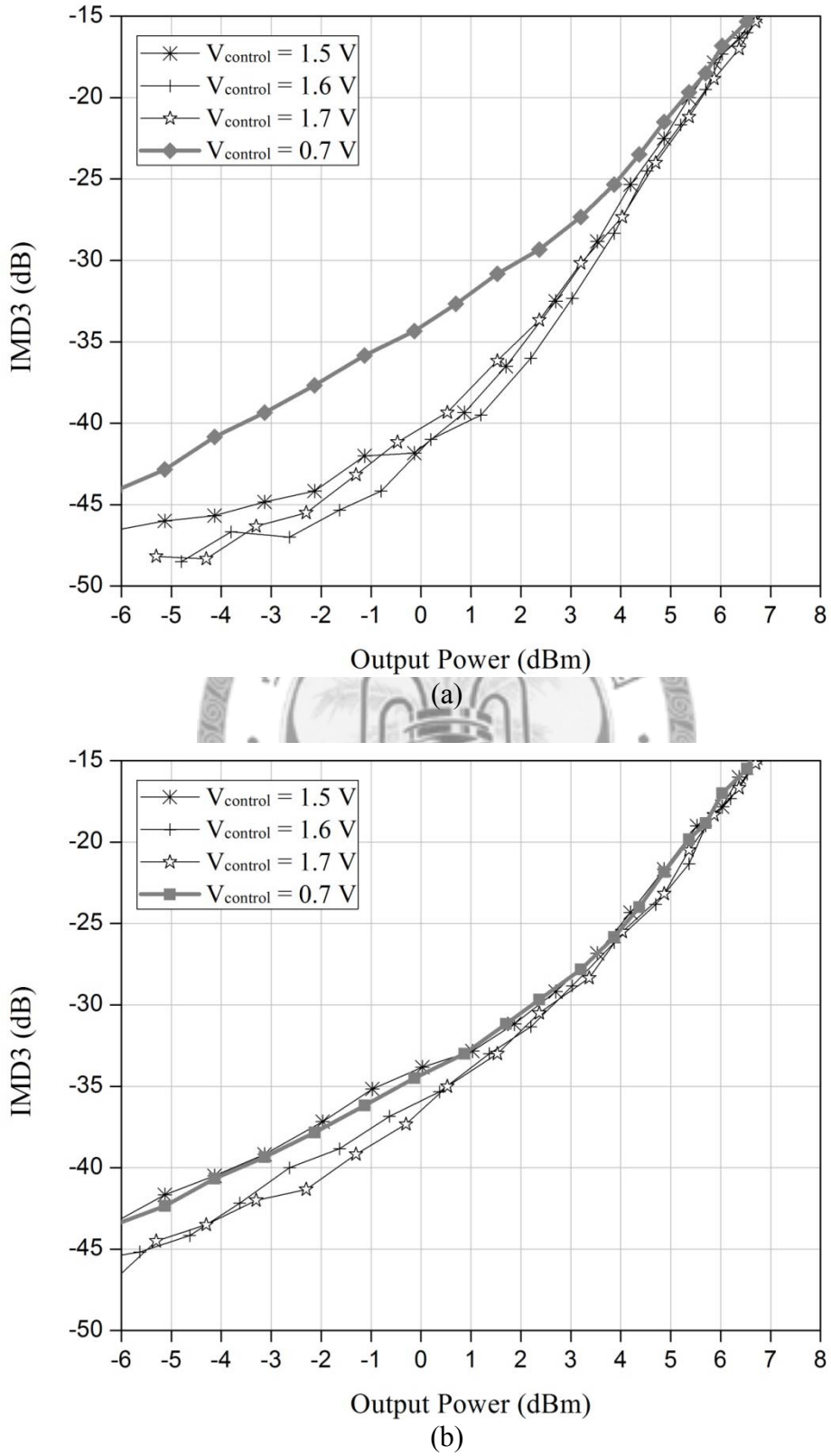


Fig. 4.48 Measured (a) upper-side-band and (b) lower-side-band IMD3 of power amplifier with modified linearizer biased by different control voltage.

4.5.4 Debug and Discussion

S-parameters of measurement and simulation result exhibits a frequency shift at lower frequency. We want to find the cause of the mismatch between simulation and measurement. After the carefully investigation, we found that the simulation of structure after the bypass circuit is neglected. The structure we neglected in simulation process is shown within rectangle of Fig. 4.49 (a). Subsequently, we simulate it by EM-simulation tool, as shown in Fig. 4.49 (b).

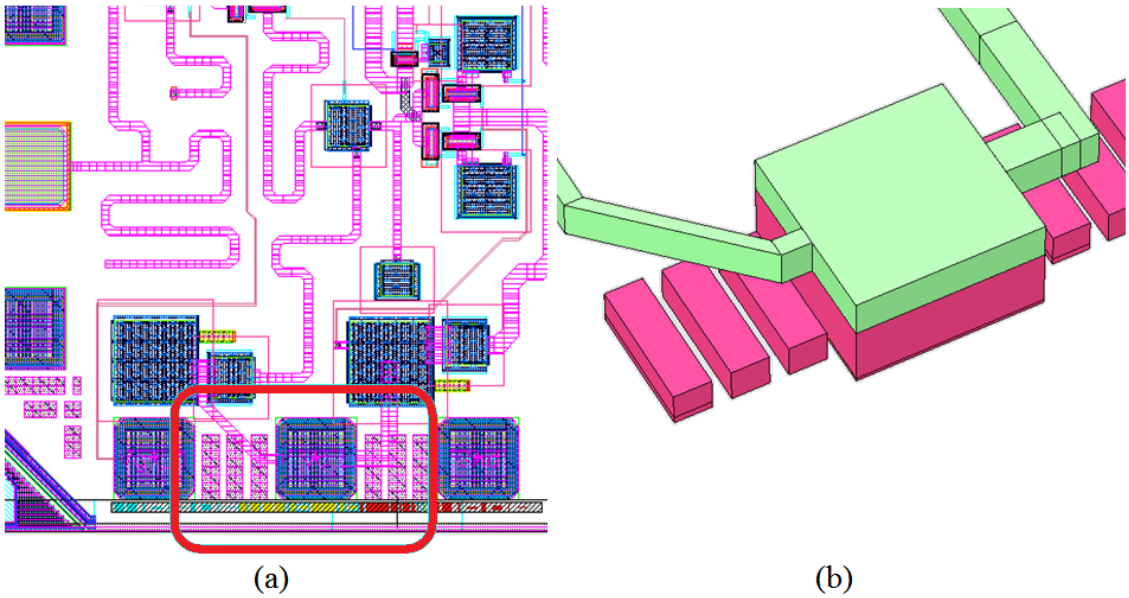


Fig. 4.49 (a) Layout and (b) EM-simulation of DC-pad for V_{dd}.

Fig. 4.50 to Fig. 4.52 shows the *S*-parameters of measurement results and simulation results after debug. The degree of coincidence is improved after taking the structure into simulation, especially for the reduction of gain at frequency around 50 GHz. Even though the input and output return losses are still slightly mismatch, the tendency of the curves are similar.

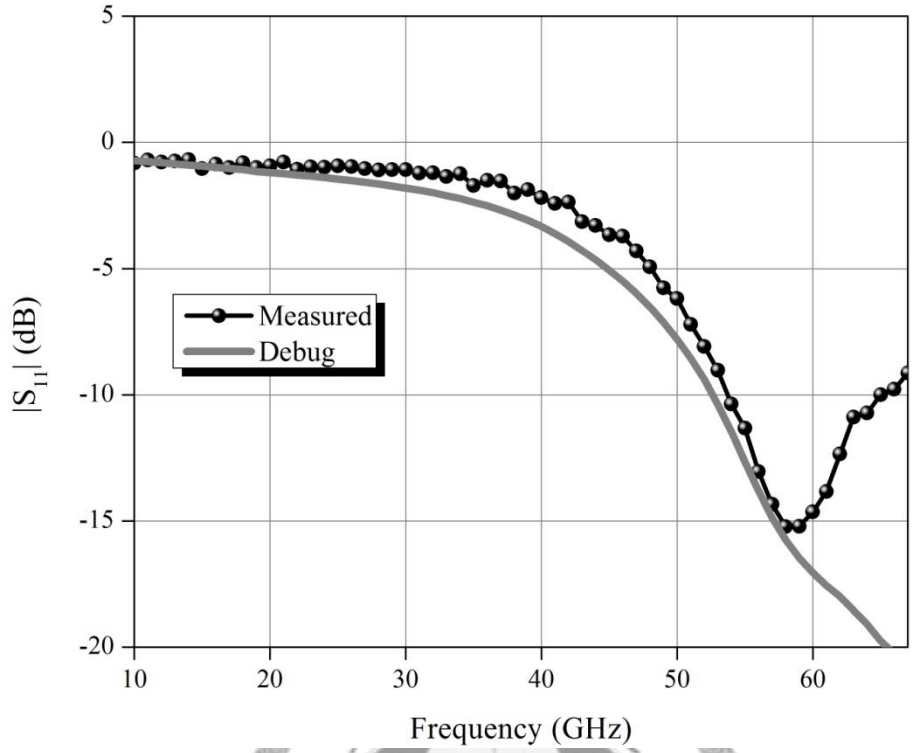


Fig. 4.50 Debug and measured $|S_{11}|$ of the power amplifier from 10-67 GHz.

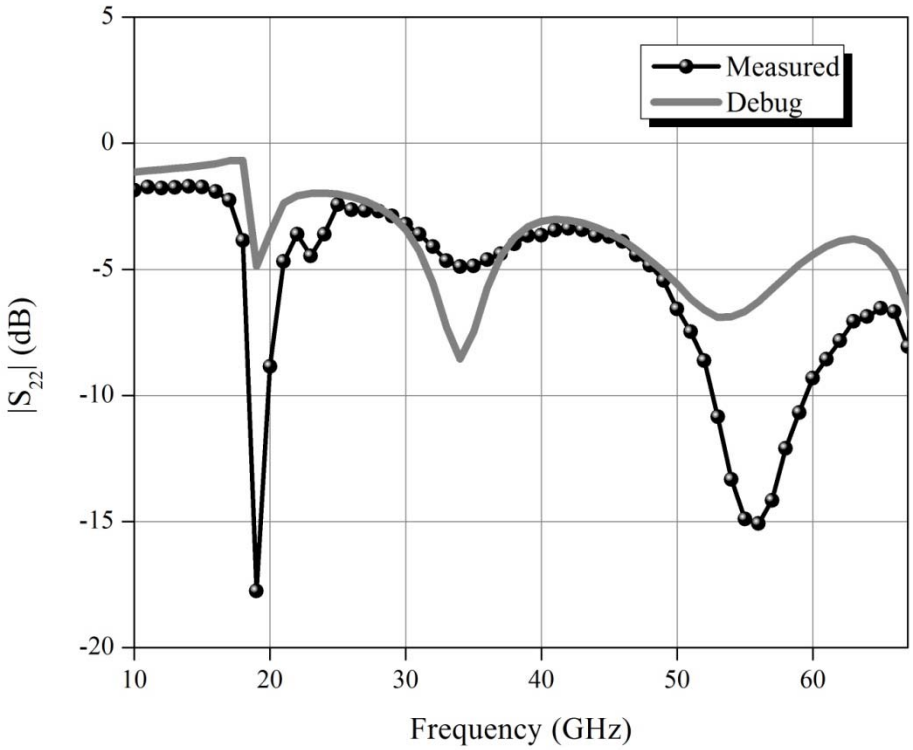


Fig. 4.51 Debug and measured $|S_{22}|$ of the power amplifier from 10-67 GHz.

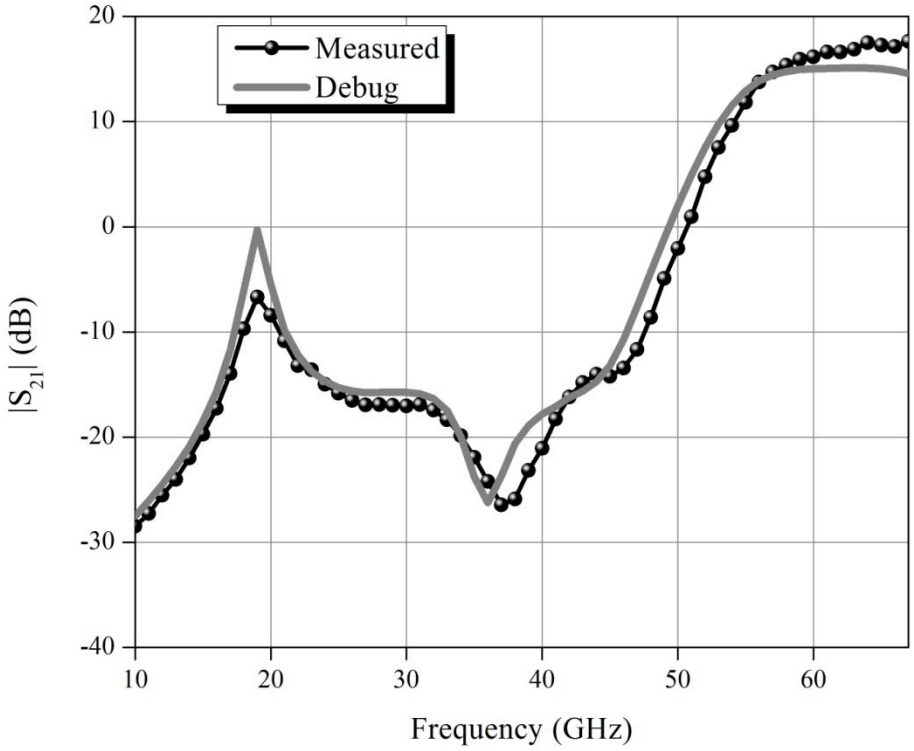


Fig. 4.52 Debug and measured $|S_{21}|$ of the power amplifier from 10-67 GHz.

The reason that the structure severely changes the performance can be explained through Fig. 4.53. The structure in Fig. 4.49 (b) connects the bypass circuits of inter-stage and output matching networks together through their connections to DC-pad respectively. The relationship between the two bypass circuits and DC-pad is shown in Fig. 4.53. The bypass circuit connecting short stub of output matching network is at the right side while that of inter-stage matching network is at left side.

We always premise in simulation process that the bypass circuits can prevent the performance change from off-bypass impedance variation. However, there is a limitation for the off-bypass impedance value that bypass circuit can prevent. Bypass circuit achieves its function through its first stage capacitors, which can provide small impedance value. Any off-bypass impedance value that is larger than the small impedance value can be neglected through the parallel with first-stage capacitor. On the

other hand, if the off-bypass impedance has a smaller value, the impedance seen by short stub will be dominated by the off-bypass impedance. We should notice not to connect object with small impedance with the bypass circuit.

There are two extra resources of small impedance. The first one is the DC pad formed by metals from metal 9 to metal 2 with via connected together. Since we use metal 1 to be the ground of whole circuit, small distance between metal 2 and metal 1 makes the DC-pad as a large capacitor connected with ground. The second one is the bypass circuit in another matching network.

We take the bypass circuit in output matching network for example in Fig. 4.53. The short stub of output matching network originally sees the small impedance of capacitor in bypass circuit. However, the structure we not simulate connects the bypass circuit with DC-pad and bypass circuit of inter-stage matching network. The two extra small impedances provided by the structure makes the impedance seen by short stub of output matching network to be lower and depart from the original value. Since we didn't simulate the structure before, the measurement result is different with our original simulation. After the debug, the simulation result is similar to measurement result.

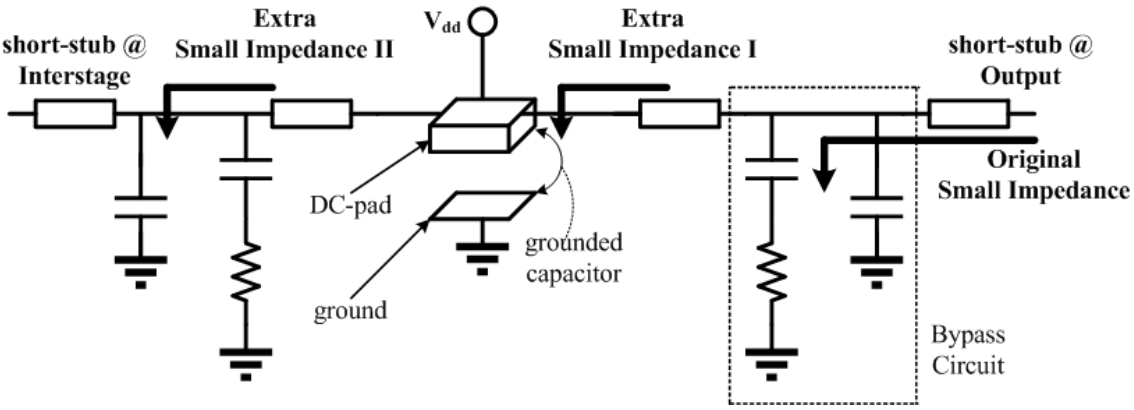


Fig. 4.53 Connecting bypass circuits of inter-stage and output matching networks back-to-back through DC-pad of V_{dd}.

Table 4.2 Comparison of this work with excellent power amplifier in V-band on CMOS process.

Ref.	Topology	Process	Freq. (GHz)	Gain	OP_{1dB}	P_{sat} (dBm)	Peak PAE (%)	Vdd (V)	Area (mm^2)	Power (mW)	OP_{1dB} PAE (%)
[27] 2010 ISSCC	4-stage CS	65nm CMOS	60	19.2	15.1	17.7	11.1	1	0.83	N/A	7.8
[29] 2010 JSSCC	3-stage CS (diff.)	65nm CMOS	62	15.5	4	11.5	15.2	1	0.05※	50	4.8
[32] 2010 JSSCC	2-stage Cascode	65nm SOI CMOS	60	16	12.7	14.5	25.7	1.8	0.04※	77.4	23
[30] 2010 RFIC	3-stage Cascode	45nm CMOS	60	20	11.2	14.5	14.4	2	0.04※	180	7
[24] 2009 RFIC	3-stage CS	90 nm CMOS	60	4.4	12.1	14.2	5.8	1	1.2	N/A	N/A
[22] 2010 ISSCC	4-stage CS	90 nm GP CMOS	60	20.6	18.2	19.9	14.2	1	3.25	N/A	N/A
[7] 2009 MWCL	3-stage Cascode	90 nm GP CMOS	50-70	31.3	11.7 (60G)	16.2	14	2.4	0.33	290	N/A
[8] 2008 CSICS	3-stage DAT Cascode	90nm GP CMOS	57-69 (Gain)	26.1	10.5	14.5	10.5 (60 G)	1.8	0.64	N/A	N/A
			57-69 (Gain)	26.6	14.5	18	12.2 (60 G)	3**		N/A	N/A
[9] 2008 RFIC	3-stage CS (diff.)	90nm LP CMOS	58-63	15	10.2	12.5	19.3* (15%)	1.2	0.15※	84	N/A
This Work	2-stage Cascode	90nm LP CMOS	57-67	15.5	13.7	15.4	16	2.4	0.25	100	14.3

※DC/RF pads are neglected *for only one chip **2.4 V is nominal value

4.6 Conclusion

A 57 to 66 GHz power amplifier using TSMC LP 90-nm CMOS process has been simulated, fabricated, and measured in this chapter. This power amplifier is equipped with a low loss built-in modified linearizer, which provides an effective pre-distortion function. The amplifier achieves linear gain more than 15 dB from 57 to 68 GHz and

delivers 13.5 dBm OP_{1dB} and 15 dBm P_{sat}. In addition, the measured result demonstrates the effectiveness of the modified linearizer. This is the first amplifier that applies the pre-distortion linearizer using CMOS process in V-band.

The performances of the amplifier are concluded in Table 4.3. Table 4.2 demonstrates reported performances of 60 GHz power amplifiers. To our best knowledge, it is the CMOS power amplifier that has highest PAE at OP_{1dB} in V-band. Besides its good linearity, the power amplifier can also provide comparable peak PAE and saturation power to other power amplifiers using better technologies.

Table 4.3 Performance of this work.

	Simulation	Measurement
Frequency (GHz)	57 ~ 66	57 ~ 66
Gain (dB)	15	15 ~ 17
Input return loss (dB)	> 14	> 9
Output return loss (dB)	> 4	> 7
peak PAE (%)	12.5	16
P_{sat} (dBm)	15	15.4
PAE@P_{1dB} (%)	> 10.5	> 14
OP_{1dB} (dBm)	12	13.7
Size (mm^2)	0.45 × 0.55	
DC power (mW)	100mW	

Chapter 5 Conclusions

This dissertation presents the research on the pre-distortion linearization technique for power amplifier in V-band using silicon-based 90-nm LP CMOS process. Based on the conventional cold-mode HEMT linearizer in 0.15-μm GaAs HEMT MMIC process, a modification to the linearizer is proposed and carefully investigated in chapter 3. The simulation result shows that the modified linearizer can provide a better per-distortion function.

In chapter 4, we try to apply the modified linearizer in CMOS process for 60 GHz CMOS power amplifier. Even though the CMOS is a weaker process than HEMT and the frequency we want to apply is a higher frequency that is more challenged, the great performance of modified linearizer can still help the power amplifier to have a better power performance. The cascode device is selected for its high gain and high output power. It is the suitable device to compensate with pre-distortion linearizer mutually.

The measurement result demonstrates a great power performance. It can provide P_{sat} of 15.4 dBm and OP_{1dB} of 13.7 dBm with an acceptable gain of more than 15 dB. It also has peak PAE value of 16% and 14% at OP_{1dB}. To our best knowledge, it is the CMOS power amplifier that has highest PAE at OP_{1dB} in V-band. Besides its good linearity, the power amplifier can also provide comparable peak PAE and saturation power to other power amplifiers using better technologies.

In conclusion, the modification of conventional linearizer makes pre-distortion technique possibly to be implemented on chip in CMOS process. The resulted power amplifier do exhibits a great performance.

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