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採用眼圖監測技術之 8Gb/s 時脈資料回復電路

An 8Gb/s Clock and Data Recovery Using Eye-Opening Monitor Technique

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本論文係洪慧雯君（R96943039）在國立臺灣大學電子工程學系、所完成之碩士學位論文，於民國 99 年 12 月 16/17 日承下列考試委員審查通過及口試及格，特此證明

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（指導教授）

系主任、所長

An 8Gb/s Clock and Data Recovery Using Eye-Opening Monitor Technique

By

Hui-Wen Hung

THESIS

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誌謝

終於要離開台大了，這個我待了將近八年的地方。這一路，在別人眼中看可能走得過於緩慢，但我總算是用我的速度，一步步的走過來了。看著手上這本論文，有滿滿的感動，這是用好多眼淚還有日出換來的。雖然碩士班的生涯，算是走到了一個句點，但我知道要學的東西還很多，不管是電路的設計、系統的考量、量測的經驗，還是如何將研究的成果寫成吸引人的論文，這些知識都還要學習。這只是一個階段性的句點，前面還有更長的路要走，希望我能堅持的往下走。

首先要謝謝我的指導教授汪重光博士，帶給實驗室這麼多的資源，照顧著我們大家，並且鼓勵著我要出國念書，在留學深造方面給我許多建議。接著謝謝口試委員們撥冗參加我的口試，給了許多寶貴的意見，讓我的論文內容能夠更充實、更完備。

研究所這三年多，在 333 實驗室生活真的很開心。謝謝照勳學長，要不是學長一路很耐心的提供我研究的方向、回答我愚笨的問題，偶爾還要鼓勵監督我，我可能怎麼都畢不了業。謝謝華錦學長，除了平常會很認真給我電路上的意見，在量測那好幾個月，都是學長慢慢教會我很多量測要注意的事，還有幫我解決很多量測上的問題。謝謝富謙學長，當我遇到不知道怎麼解決的人生問題時，謝謝學長總是第一時間就會給我意見。還有當我有任何需要別人修改的文件時，學長也總是會細心看過，提出很多很寶貴的建議。謝謝志峰學長，總是會提供系統研究上的想法跟方向，還會找資料給我看，幫助我解決問題。謝謝隔壁實驗室的季昀學姐，總是會陪我聊東聊西，然後也會鼓勵我。在這個幾乎是男生的地方，有一個可以談心說話的妳在，我真的覺得很開心。謝謝之前畢業的學長們：松翰、志憲、坤達、文頤、宜賢、芳立還有柏強，總是給實驗室帶來很多歡笑，也提供

我很多電路上的意見。謝謝我同屆的同學道堯，從修課到研究的東西，總是不吝嗇的提供我很多很多的幫助跟想法，謝謝你這幾年的幫忙。謝謝小我一屆好笑又可愛貼心的學弟們：明業、昕翰、宗澤還有宜宏，有你們加入後，實驗室又變得好熱鬧，來實驗室都很開心有人可以聊天。謝謝其他的學弟們：崑印、書緯、耿裕還有辰修，都會跟我講話，然後我有甚麼困難也都會幫忙。我很感謝進了333這個實驗室!!

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我終於畢業了。謝謝我身邊的所有人，有你們才有現在的這個我。

洪慧雯

2011.02.13

摘要

本篇論文將探討應用於高速有線系統之時脈資料回復電路設計。首先，傳統的時脈資料回復電路，根據它的架構基本上可以分做兩類。一種是鎖相迴路構成的時脈資料回復電路。這架構主要是利用相位偵測器，慢慢的讓時脈對準資料的正中央來做取樣的動作。另一種架構是超取樣構成的時脈資料回復電路。這電路是利用不同相位的時脈，同時對輸入的訊號做取樣，再從這一堆資料裡面，找出最好的訊號。不管是哪一種架構，都有一個共通的問題跟缺點，就是時脈取樣的位置，皆固定在資料的正中央。但根據誤碼率 (BER) 的分析，由於信號在通道傳送過程中會受到雜訊 (noise)、符元干擾 (Intersymbol Interference, ISI) 及時間軸的抖動 (timing jitter) 等因素的影響，信號誤碼率 (BER) 最低的位置並不是資料的正中央，而是跟著外在因素影響而變動。因此傳統的時脈資料回復電路並不適用於任何的情況。

因此，本篇論文提出一個使用眼圖監測機制的時脈資料回復電路。傳統的眼圖監測機制主要是監測輸入信號的品質，然後調整等化器 (equalizer) 的係數，來更改等化器需要補償的增益。這裡將眼圖監測機制應用在時脈資料回復電路。不管信號在通道傳輸時受到甚麼非理想效應的影響，採用眼圖監測機制的時脈資料回復電路都可以找出某個時脈位於信號誤碼率 (BER) 較低的位置去做取樣，因而得到較好的回復信號。

最後，我們在 90 奈米 CMOS 數位製程裡實現這個採用眼圖監測機制之 8Gb/s 的時脈資料回復電路。這個電路的核心面積為 $0.7*0.8mm^2$。在 1 伏特的電壓供應狀態下，當眼圖監測機制在判斷哪個時脈位於信號誤碼率 (BER) 較低的位置時，整個電路消耗 254mW。當做完判斷後，為了節省能量消耗，眼圖監

測機制將被關掉，此時整個電路只消耗 61mW。在沒有任何等化器的情況下，輸入 2^{31}-1 PRBS 信號，而且信號經過長度 30cm FR-4 材料的通道的情況下，這個採用眼圖監測機制之 8Gb/s 的時脈資料回復電路依然可以將回復資料的誤碼率 (BER) 降低到小於 10^{-12}。

Abstract

Traditional CDR circuits can be categorized as PLL-based CDR and oversampling CDR based on its architecture. The sampling position of these CDR circuits is always fixed in the middle of the received data. However, when data is transmitted in channel, it is distorted by some non-ideal factors such as noise, ISI and timing jitter. Therefore, the best sampling position is not at the middle of the received data by BER analysis. In order to apply in different channel conditions and reduce the complexity of the front equalizer, an eye-opening monitor (EOM) CDR circuit is proposed based on the oversampling architecture. In different channel conditions, the EOM CDR circuit can select one clock phase to recover data at the position where has low BER. Furthermore, the EOM is turned off after having selected the most appropriate sampling clock to save the power consumption of CDR circuit.

This EOM CDR circuit is implemented with 90nm CMOS technology, and the core is occupied an area of $0.7^{*}0.8mm^{2}$. Moreover, this circuit consumes 254mW from 1.0V supply when the EOM turns on, and only costs 61mW after having selected one appropriate sampling clock. Without any pre-equalizer or pre-emphasis circuit, this proposed EOM CDR circuit can recover the 8Gb/s data, which is passing through 30cm FR-4 channel with BER $< 10^{-12}$.

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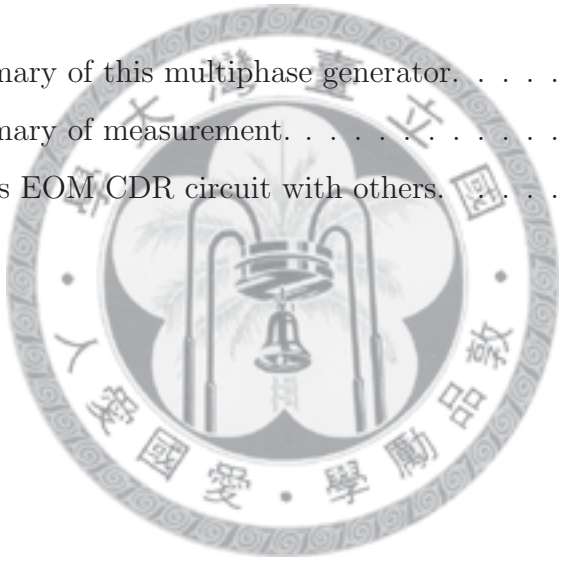

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Chapter 1

Introduction

1.1 Motivation

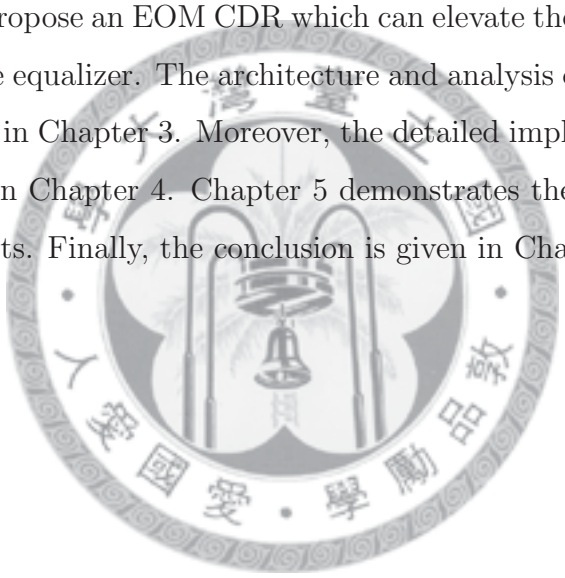
Clock and data recovery (CDR) is a critical component in the receiver end of wired communication system. Because the clock is not transmitted directly, the timing information should be acquired from the received data to allow synchronous operations. Moreover, the data received in the receiver is noisy, so the data should be sampled again to eliminate the noise. Hence, CDR is demanded to recover data and clock, and the received data can be read precisely.

Traditional CDR circuits can be categorized as PLL-based CDR and oversampling CDR hinging on its architecture. There are some limitations in typical CDR circuits. The presupposition of designing CDR circuits is that the optimal sampling position is at the middle of input signal and all CDR circuits attempt to recover data at this position. Nevertheless, this premise only occurs when data is transmitted in the front circuits with bandwidth of 0.7 data rate according to the analysis of bit error rate(BER). Due to the channel loss such as ISI and noise, an equalizer in the receiver is demanded to compensate the received data. If utilize conventional CDR circuit, the equalizer should extend the bandwidth to 0.7 data rate at least. This is because the sampling position is fixed at the middle of received data in typical CDR circuits. This thesis proposes an eye-opening monitor(EOM) CDR based on oversampling CDR architecture to eliminate this drawback. The EOM CDR circuit can adjust sampling position according to various input data and recover data at position with low BER. Hence, the requirement of

equalizer is relaxed and not so strict as that in employing conventional CDR.

1.2 Thesis Overview

This thesis presents the design and implementation of an eye-opening monitor (EOM) clock and data recovery (CDR). Because this proposed EOM CDR circuit is applied to high speed serial-link, the basic concepts of this system is introduced in Chapter 2. In Chapter 3, traditional clock and data recovery circuits are classified and illustrated first. Then according to the bit error rate analysis of recovered data, interpret the obstacles of typical CDR and propose an EOM CDR which can elevate the drawbacks and reduce the requirements of the equalizer. The architecture and analysis of the proposed EOM CDR are also illustrated in Chapter 3. Moreover, the detailed implementation and simulation results are shown in Chapter 4. Chapter 5 demonstrates the testing environments and the measured results. Finally, the conclusion is given in Chapter 6.



Chapter 2

High Speed Serial-Link Receiver

2.1 Introduction of High Speed Links

High speed links operating at multi-Gb/s are demanded not only in standard computer systems like the memory, storage or component interfaces, but also in specialized applications such as Internet routers or large multi-process systems. Since that devices operate at high speed in standard IC processes is difficult, the high speed links and chip-to-chip interfaces are considered as a design challenge.

Traditionally, high speed links use single link. However, when the semiconductor technology progresses, the on-chip speed is increased enormously and much greater than off-chip bandwidth. Hence, the single link whose speed is restricted to the on-chip bandwidth is inadequate, and the employment of parallel links is required. High speed link with parallel-link technology for input-output (I/O) interface is depicted in Fig. 2.1(a) [1]. As the data rates increase much quickly, some issues in parallel links become significant. One is that the processing in the front transceiver to multiplex various channels is increased. Another is the channel mismatches cause signal skewing, and the synchronization between clock and data becomes much difficult. Because of these obstacles, the requirement at circuit level to implement parallel links changes into tight. After all, the cost of parallel links increases greatly as the data rates reach Gb/s range.

While the parallel transmission becomes expensive, serial high-speed links are demanded to replace parallel links. Fig. 2.1(b) [1] shows the block diagram of this tech-

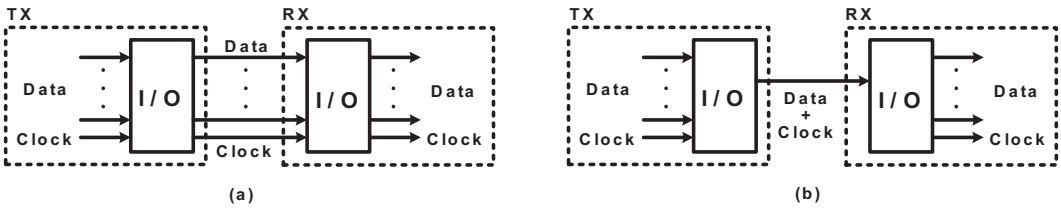


Figure 2.1: (a)Parallel link and (b)serial link.

nology. In the serial link transmission, the clock information is embedded in the data and carried with data. Additionally, serial links applied in chip-to-chip and inter-board communications can operate at high speed with lower I/O counts and greater flexibility of the kind of used material. This trend is clearly illustrated in the development of the personal component interconnect (PCI), gigabit ethernet and the gigabit backplane interconnect. Therefore, this thesis focuses on the serial high-speed links, and this chapter mainly references to [1].

2.2 Serial High-Speed Links

Fig. 2.2 illustrates the block diagram of a typical front-end in the serial link which is also called serializer-deserializer system (SERDES). In the transmitter, the multiplexer converts the parallel data into serial data, and then the driver processes these serial data. In various application or standard, the design of driver is different, and there is generally pre-emphasis to compensate the loss which is going to be generated as passing the channel. Furthermore, the phase-locked loop (PLL) supplies high frequency clock using a reference clock with lower operating frequency. This clock synchronizes the data in the serialization and transmission processes.

As the data is transmitted in channel, it is distorted by the frequency-dependent loss of channel. Hence, an equalizer is required to compensate the non-ideal phenomena, such as ISI and noise caused by the channel in the receiver. When the output of equalizer is accurate enough for the clock and data recovery (CDR) circuit, the CDR circuit recovers the data and clock. Finally, the demultiplexer deserializes the recovered data back to the original data in parallel style.

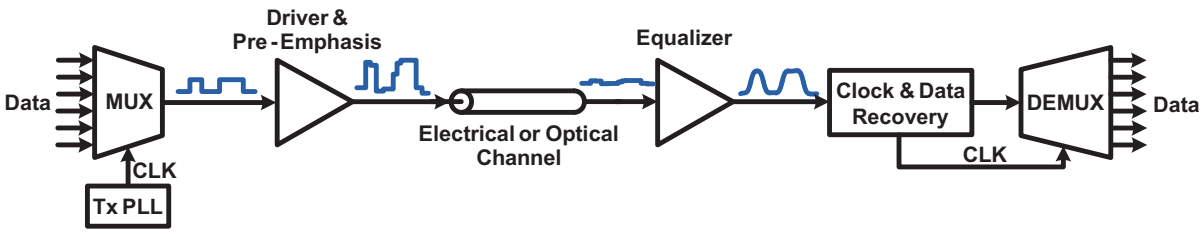


Figure 2.2: Front-end of a high-speed serial link.

Because the data transmitted in the high-speed serial links covers a large range of frequency, one of the design issues in this system is whether this electrical channel has uniform frequency response. The non-uniform frequency response of the channel seriously influences the integrity of signal transmitted in the high-speed serial links, and can increase the bit error rate of the recovered data. This undesirable phenomenon primarily comes from the channel's physical characteristics such as skin effect, dielectric loss and radiation loss which will be introduced in the next section.

2.3 Channel Characteristics

The electrical channel used in serial high-speed links is implemented by transmission line for the reason of less distortion. Microstrip line and stripline are two of the most popular planar transmission line categories, since they can be easily fabricated on printed circuit board (PCB) and integrated with other active or passive devices. Fig. 2.3 shows the cross-sections of these lines. In this thesis, the microstrip line is used as the electrical channel in the experiment. Therefore, following discussions mainly concentrate on this type of transmission line.

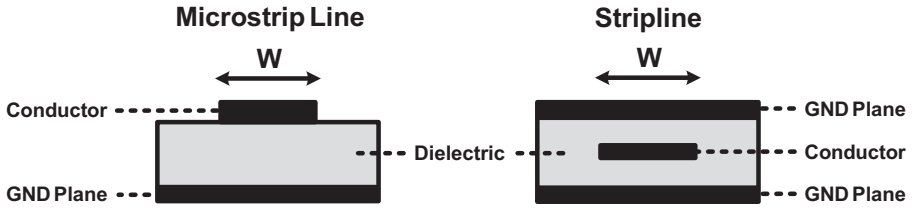


Figure 2.3: Cross-sections of various transmission lines.

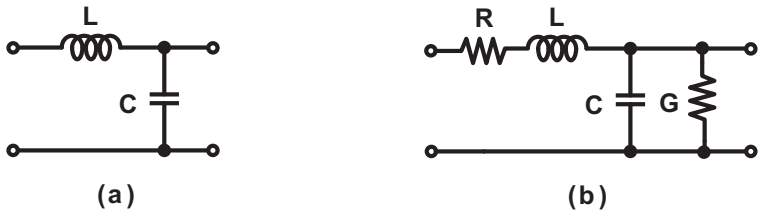


Figure 2.4: Line model (a)without loss (b)with loss.

If the channel is an ideal transmission line, it can propagate signal without any distortion. Fig. 2.4(a) illustrates the per-unit length model of this ideal transmission line. The signal in this figure is transmitted from one LC unit to the next without any loss. If the ideal transmission line is terminated properly, it can be written as

$$Z_o = \sqrt{\frac{L}{C}}. \tag{2.1}$$

However, real transmission line has undesirable physical characteristics such as skin effect, dielectric loss and radiation loss, and its per-unit length model should be modified as Fig. 2.4(b). Only skin effect and dielectric loss are considered in this model, and the radiation loss is neglected. This is because the radiation loss is comparatively smaller than that from skin effect and dielectric loss. In this figure, the resistance R represents the skin effect, and the conductance G models the dielectric loss. Hence, the characteristic impedance of this transmission line is

$$Z_o = \sqrt{\frac{j\omega L + R}{j\omega C + G}}. \tag{2.2}$$

If the frequency is high enough, the impedance can be rewritten as

$$Z_o = \sqrt{\frac{L}{C}}, \tag{2.3}$$

which is identical with Eq.(2.1).

The physical characteristics (i.e.skin effect and dielectric loss) of the channel are particularly interpreted in the following subsections, because these factors play important roles in the high speed data transmission.

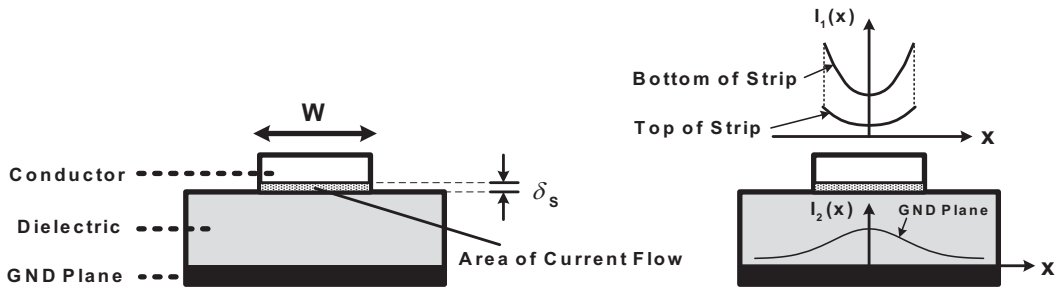


Figure 2.5: Skin effect of microstrip line.

2.3.1 Skin Effect

The skin effect is caused by the distribution of current and magnetic field in a conductor altering with various frequency. When the signal is DC, the current density is uniform across the conductor. However, if the frequency of signal becomes higher, the current tends to concentrate on the conductor surface. The approximate distributions of current at high frequency in the microstrip line is depicted in the Fig. 2.5 [2].

W and δ_s in Fig. 2.5 respectively represent the width and the skin depth of the transmission line. The skin depth is the effective depth of signal current which conducts on the conductor surface. This skin depth can be written as

$$\delta_s = \sqrt{\frac{\rho}{\pi \mu f}}, \tag{2.4}$$

where μ is magnetic permeability of the conducting material and expressed in Henries per unit length. Additionally, ρ represents the resistivity of the conducting material and its unit is ohms per length. The surface resistivity R_s of the conductor is

$$R_s = \frac{\rho}{\delta_s} = \sqrt{\pi \rho \mu f}, \tag{2.5}$$

and the attenuation caused by the skin effect is written as

$$\alpha_{skin} = \frac{R_s}{Z_o W} = \frac{\sqrt{\pi \rho \mu}}{Z_o W} \sqrt{f}. \tag{2.6}$$

From this equation, α_{skin} increases when the frequency becomes higher. Moreover, this result can be explained in intuitive. Since the current of higher frequency flows through a smaller cross-section than that with lower frequency, the resistance increases when the frequency becomes higher and the loss does as well.

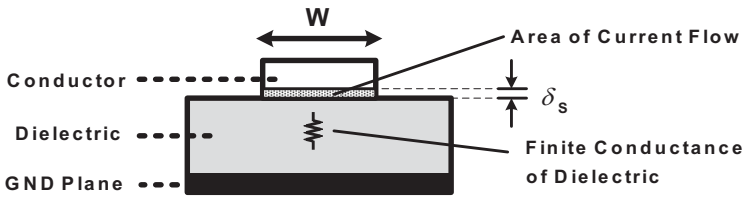


Figure 2.6: Skin effect and dielectric loss of microstrip line.

2.3.2 Dielectric Loss

When atoms and molecules move or rotate for being subjected to the changing electric field, the electric energy is dissipated as heat. Fig. 2.6 respectively shows the skin effect and dielectric loss of the microstrip line.

The property of material that quantifies the dielectric loss is known as the dielectric loss tangent or $\tan\delta$. The parameter, $\tan\delta$, varies with different dielectric material and is typically constant with frequency, at least up to 10GHz. α_d is the attenuation constant due to dielectric loss, and is written as

$$\alpha_d = \frac{\pi\sqrt{\epsilon_r}\tan\delta}{c} f, \tag{2.7}$$

where c is the speed of light and ϵ_r represents the relative permittivity of the dielectric. From Eq.(2.7), the dielectric loss also increases with the frequency. Furthermore, the channel is preferable to use low loss dielectric material for minimizing loss. The most common material used in today's backplanes is FR-4 board whose loss tangent is less than 0.02.

The total loss of the channel comprising both the effects caused by skin effect and dielectric loss is

$$\alpha = \left(\frac{\sqrt{\pi\rho\mu}}{Z_o W}\sqrt{f} + \frac{\pi\sqrt{\epsilon_r}\tan\delta}{c} f\right) l, \tag{2.8}$$

where l is the length of the channel. Because the dielectric loss linearly increases with frequency, it dominates the overall channel loss at high frequency.

2.3.3 FR-4 Board Simulation

The channel employed in this work is FR-4 microstrip line which is extensively used in high speed serial-link. In order to comprehend the characteristics of FR-4 microstrip line, utilize software to simulate FR-4 traces of various lengths.

While consider both the skin effect and dielectric loss, the conventional model in Fig. 2.4(b) is not sufficient for broadband design. [2] proposes a broadband model depicted in Fig. 2.7 for a 1-in FR-4 trace. The characteristics of required channel length can be obtained by cascading this model. Fig. 2.8 shows the comparison of the results of this broadband model and the software simulation.

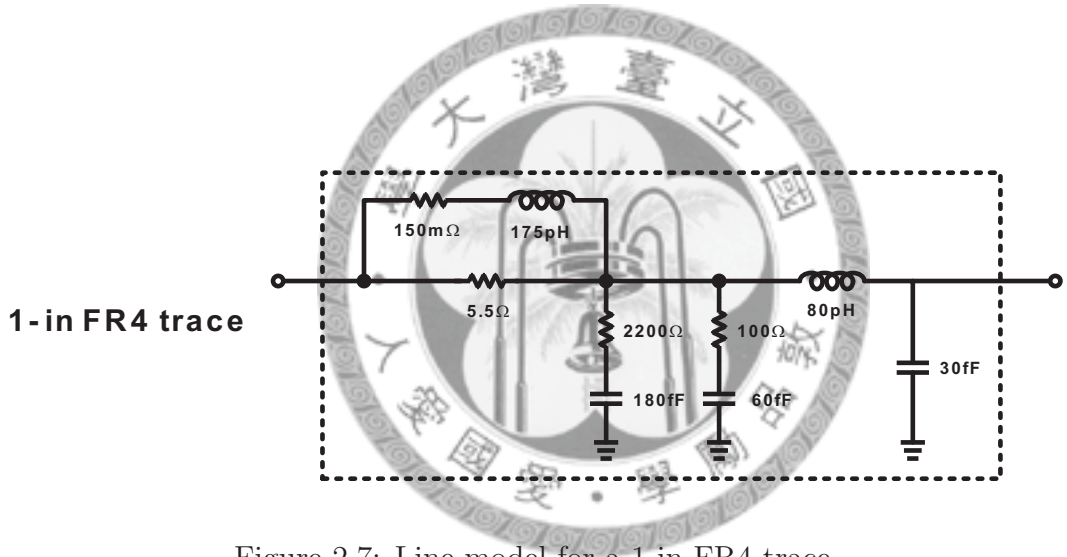


Figure 2.7: Line model for a 1-in FR4 trace.

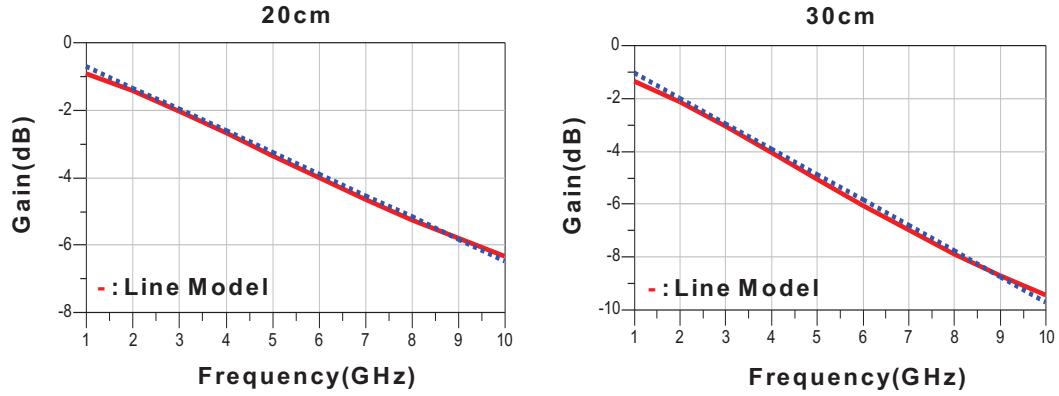


Figure 2.8: Comparison of actual channel loss (dashed line) and line model (solid line).

Chapter 3

Clock and Data Recovery

When the receiver in serial link receives data stream that is noisy and asynchronous, it should first process the data with equalizer to compensate the loss caused by channel, and then use clock and data recovery (CDR) circuit to extract clock embedded in the received data. After all, a decision circuit composed of d flip-flop retimes the received data and generates recovered data which is synchronous with the recovered clock. Moreover, the jitter and noise of data accumulating during transmission can also be eliminated after data being recovered. The operating principle of CDR circuit is depicted in Fig. 3.1. The input signal is non-return to zero (NRZ) random bit stream.

Since CDR circuit is a critical component in the receiver end of wired communication system, here focus on this component. First, introduce the traditional CDR circuits. Secondly, illustrate the obstacles of traditional CDR circuits according to the analysis of the bit error rate (BER). Finally, propose an eye-opening monitor (EOM) CDR which can not only select one phase clock to sample data where the received data has low BER, but also relax the bandwidth and group delay requirements of the receiver front-end in

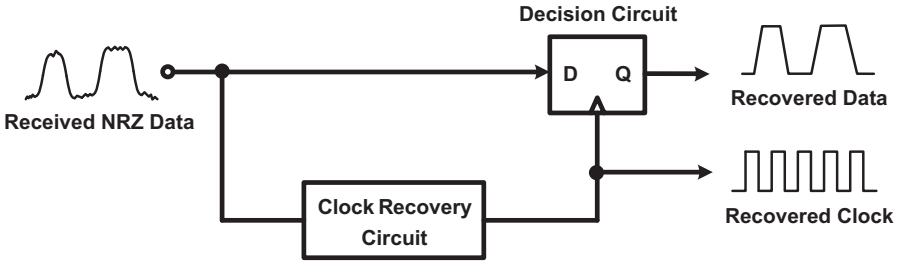


Figure 3.1: Operating principle of CDR circuit.

the high-speed links.

3.1 Traditional Clock and Data Recovery

In this section, various traditional clock and data recovery circuits are introduced. Moreover, these circuits are categorized by their architectures and characteristics roughly.

3.1.1 Phase-Locked Loop Based CDR

The block diagram of traditional CDR based on phase-locked loop is demonstrated in Fig. 3.2. This circuit consists of phase detector, charge pump, low-pass filter, VCO and decision circuit. PLL-based CDR circuits can be categorized by many types depending on the rate of recovered clock, or various kinds of phase detector, or if the reference clock exists or not. Here only discuss a full rate CDR circuit with a reference clock.

In the PLL-based CDR, the phase detector is used to detect the phase difference between input data and the output of the VCO. This phase detector can be simply implemented by an XOR and a d flip-flop, and its operation is illustrated in Fig. 3.3. If there is phase difference, the average voltage of node Y will alter, and modify the operating frequency of the VCO. Finally, the recovered clock that comes from the output of VCO can exactly sample the received data at the center position.

In traditional CDR circuits, the optimal sampling position is always considered at the middle of input data where the data is thought to have low bit error rate. Hence, most designs of CDR circuits follow this premise. However, from the bit error rate

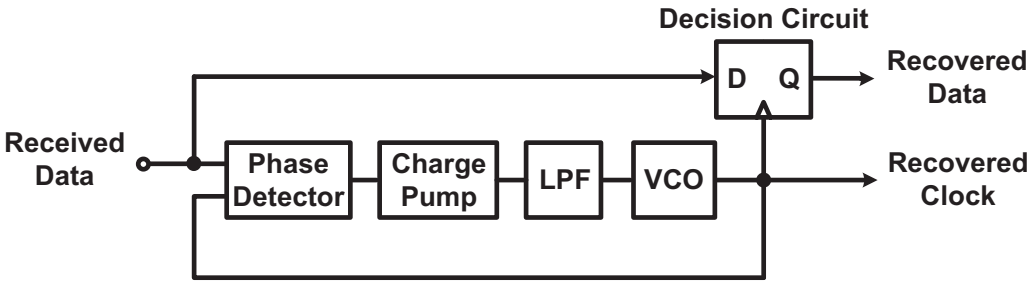


Figure 3.2: Architecture of PLL-based CDR.

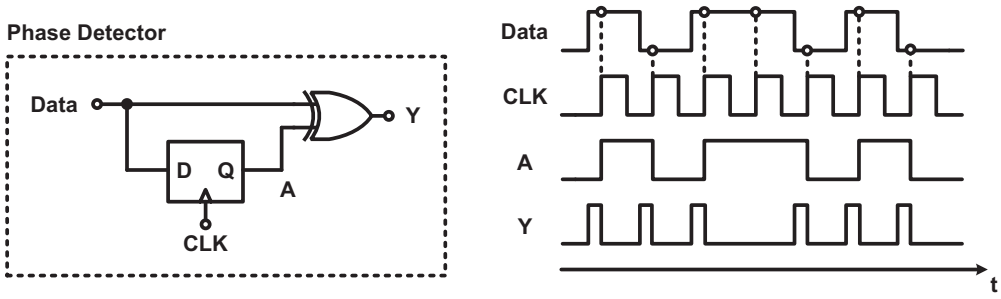


Figure 3.3: Operation of PLL-based CDR.

analysis discussed in Section 3.2, the optimal sampling position is not always at the middle of input data, but varies according to the bandwidth of or noise from the front circuits. Therefore, traditional CDR circuit is not suitable in every situation.

3.1.2 Blind Oversampling CDR

Unlike the PLL-based CDR which always recovers data at the half of one bit period ($T_b/2$), this CDR circuit blindly samples the received signal with M clocks simultaneously and selects one clock which is approaching the position , $T_b/2$, the most to recover data. Block diagram of a blind oversampling CDR circuit [3] is depicted in Fig. 3.4. The principle of traditional blind oversampling CDR circuit is to detect bit boundary and choose one of the sampling clocks that is farthest from the bit boundary. In other words, select the sampling clock which approaches middle of the input data. Fig 3.5 shows the operation.

Because of the premise that sampling data at center of one bit interval can acquire low bit error rate, the worst case is two sampling clocks straddle the center position of one bit period, and result in the maximum sampling time offset ($T_{os,max}$) which is

$$T_{os,max} = \begin{cases} \dfrac{T_b}{2M} & \text{if } M \text{ is odd integer} \\ \dfrac{T_b}{M} & \text{if } M \text{ is even integer} \end{cases}, \tag{3.1}$$

where T_b represents each bit period. From this equation, the sampling time offset is smaller when the number of clocks M is odd. Hence, M is normally odd integer in place

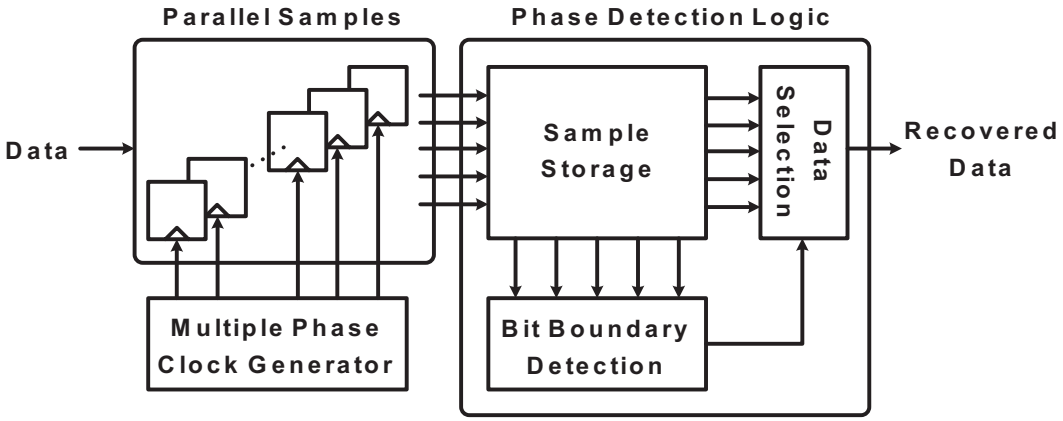


Figure 3.4: Block diagram of traditional blind oversampling CDR.

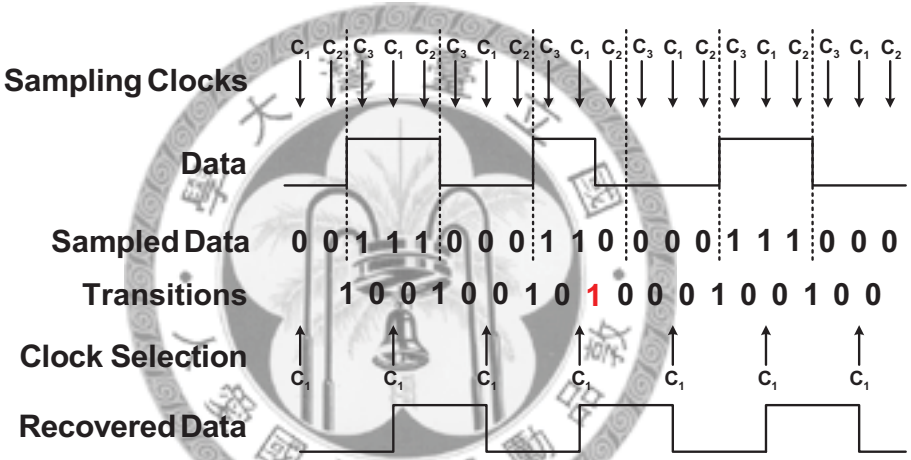


Figure 3.5: Operating principle of traditional blind oversampling CDR.

of even one. When M is larger, the sampling position is closer to the center of data, and the recovered data has less jitter. Nevertheless, it consumes more power than the traditional CDR circuits stated in 3.1.1.

One advantage of this architecture is that it is a feed-forward system without feedback loop like that in the PLL-based CDR circuit. Therefore, this CDR circuit is much appropriate in some wireline system such as EPON system which requires short settling time. Although the architecture of blind oversampling CDR circuit has this advantage, it can not recover data just at the middle of input data and has sampling time offset which causes jitter. Hence, the jitter of recovered data in this architecture is more serious than that in the PLL-based CDR circuit.

3.2 Bit Error Rate Analysis

The criteria to determine the quality of received data is to detect its amplitude noise, inter-symbol interference or jitter. These properties all impact the bit error rate (BER) of recovered data. BER is a general performance to describe a CDR circuit.

The BER is defined as the ratio of the number of errors to the total number of received data, and can be written as

$$BER = P(0) \cdot P(1|0) + P(1) \cdot P(0|1). \tag{3.2}$$

P(0) and P(1) are the probabilities of transmitted bit being ZERO and ONE respectively. Here assume the probabilities are equal (i.e.P(0)=P(1)=0.5). P(1|0) represents the probability which the bit is sampled as ONE but it is actually ZERO in transmission. On the other hand, P(0|1) is the probability that the bit is read as ZERO but it is ONE being delivered. In the following sections, various elements causing BER will be illustrated.

In this section, analyze the relations between the characteristics and the BER. This BER analysis mainly references to the Chapter 2 in the thesis [4].

3.2.1 Noise

Noise is one of the primary causes that results in the BER. When data transmits through channel to receiver, it can be influenced by the noise. The noise leads to amplitude fluctuations at the sampling point and bring errors in detecting the signal. Fig. 3.6 shows BER calculation from the area of noise distribution. Assume the noise is Gaussian distribution with standard deviation of σ_n. From Fig. 3.6 and Eq. (3.2), if the BER is just influenced by noise, it can be written as

$$BER = \frac{1}{2} \cdot Q\left(\frac{V_{TH} - 0}{\sigma_n}\right) + \frac{1}{2} \cdot Q\left(\frac{1 - V_{TH}}{\sigma_n}\right), \tag{3.3}$$

where $Q(\cdot)$ represents the cumulative distribution function.

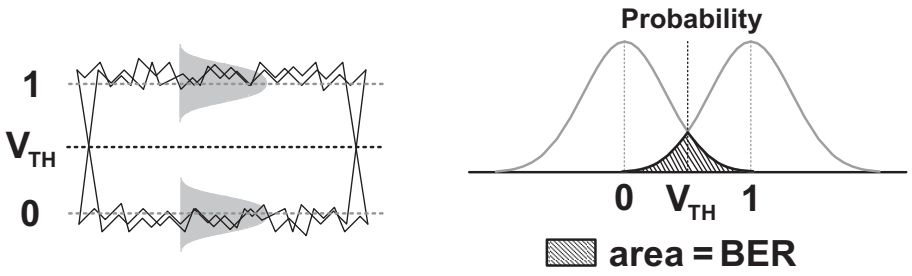


Figure 3.6: The relation between BER and noise.

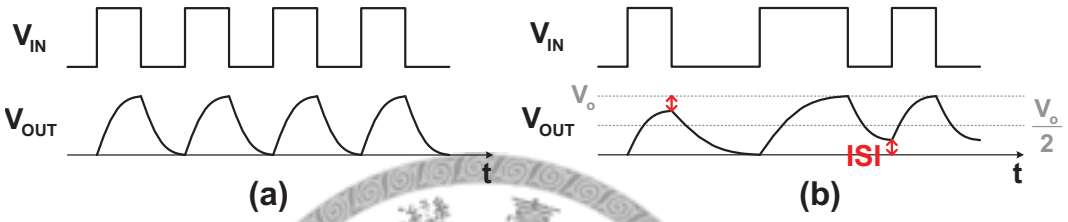


Figure 3.7: Influence of ISI on (a)periodic data and (b)random data.

3.2.2 Inter-Symbol Interference (ISI)

In reality, the noise is not the only cause of amplitude fluctuation to increase the BER. Before reaching the CDR circuit, the received data passes through other circuits with limited bandwidth. If the received data is NRZ signal, it can be seen as being consisted of various pulses. In other words, every bit of the data is a pulse. Because of the bandwidth restriction, the tail of each bit can last longer than a bit period (T_b), and hence impacts on the amplitude of its neighboring bits. This influence is called "inter-symbol interference"(ISI) and is depicted in Fig. 3.7.

An ideal NRZ signal, $x(t)$, composed of pulses can be written as

$$x(t) = \sum_{k=-\infty}^{\infty} a_k \cdot p_i(t - kT_b) \qquad (a_k \in \{0, 1\}\ ) \tag{3.4}$$

where $p_i(t)$ represents the function of unit pulse and is defined as

$$p_i(t) = \begin{cases} 1 & 0 \le t \le T_b \\ 0 & \text{otherwise} \end{cases}. \tag{3.5}$$

Furthermore, the the kth bit of the NRZ signal decides the coefficient a_k.

From Eq. (3.4), the received data, $r(t)$, influenced by ISI can be modified as

$$r(t) = \sum_{k=-\infty}^{\infty} a_k \cdot p_o(t - kT_b) + n(t) \qquad (a_k \in \{0, 1\}\ ). \tag{3.6}$$

$p_o(t)$ represents the received pulse shape, and n(t) is the noise produced in transmission. If $r(t)$ is sampled at $t = T_s + mT_b$ to recover data, the received data at this time is

$$r(T_s + mT_b) = a_m p_o(T_s) + \underbrace{\sum_{k=-\infty, k\neq m}^{\infty} a_k \cdot p_o(T_s + (m-k)T_b)}_{\text{ISI term}} + n(T_s + mT_b), \tag{3.7}$$

where m is an integer, and T_s is the sampling time offset from 0 and $0 < T_s < T_b$. Owing to this equation, the ISI term impacts on the decision of recovered data.

Assume the system is first-order linear time invariant (LTI) with time constant τ, and the received pulse shape can be written as

$$p_o(t) = \begin{cases} 0 & t \leq 0 \\ 1 - e^{-\frac{t}{\tau}} & 0 \leq t \leq T_b \\ \left(\frac{1}{\alpha} - 1\right) \cdot e^{-\frac{t}{\tau}} & T_b \leq t \end{cases} \tag{3.8}$$

in which define $\alpha \equiv e^{-T_b/\tau}$.

Replace $p_o(t)$ of the ISI term in Eq.(3.7) with Eq.(3.8). In this system, suppose the received data is only influenced by front data. The ISI term at $m = 0$ can be written as

$$ISI = \sum_{k=-\infty}^{-1} a_k \cdot p_o(T_s - kT_b) = \alpha^{\frac{T_s}{T_b}} \sum_{k=-\infty}^{-1} a_k \cdot (1-\alpha) \cdot \alpha^{-k-1}. \tag{3.9}$$

The sum is just accumulated to $k = -1$. When the impact of the prior one bit (a_{-1}) is significant, the ISI term is concentrated around two value, ISI_0 and ISI_1. These values are calculated from the expected value of ISI in Eq. (3.9) and illustrated below.

$$ISI_0 = E\{ISI | a_{-1} = 0\}\ = \frac{1}{2}\alpha^{\frac{T_s}{T_b}} + 1. \tag{3.10}$$

$$ISI_1 = E\{ISI | a_{-1} = 1\}\ = \alpha^{\frac{T_s}{T_b}} \left(1 - \frac{\alpha}{2}\right). \tag{3.11}$$

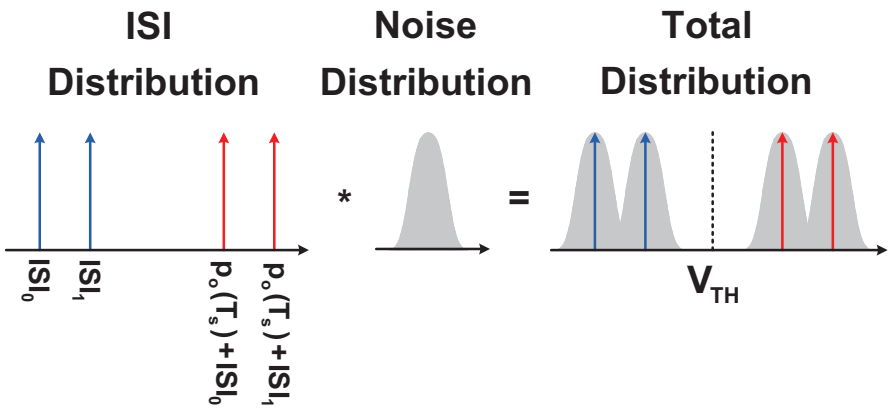


Figure 3.8: Amplitude distribution from noise and ISI.

These ISI terms impact on the amplitude of received data at sampling time, and represented by two delta functions whose values are ISI_0 and ISI_1, respectively with probability p and $(1-p)$. p is the probability of $a_{-1}=0$ and $(1-p)$ is the probability of $a_{-1}=1$. In order to simplify the calculation, let $p=(1-p)=0.5$.

The total amplitude distribution including the effects from noise and ISI is shown in Fig. 3.8. It is obtained by the convolution of noise and ISI distribution. The valuse of ISI and $p_o(T_s)$ in this figure are acquired above, and then calculate the parameter of noise distribution.

The frequency response of a first-order LTI system is

$$H(f)=\frac{1}{1+\tau s}=\frac{1}{1+j(2\pi\tau f)}. \tag{3.12}$$

Moreover, the relation between the power spectral densities of input and output in the frequency domain can be expressed as

$$S_{out}(f)=|H(f)|^2\,S_{in}(f)=\frac{1}{1+(2\pi\tau f)^2}S_{in}(f). \tag{3.13}$$

If the additive white noise of the input in receiver has double-sided power spectral density $\frac{N_0}{2}$, the total noise power can be calculated from Eq.(3.13) and written as

$$P_{total}=\sigma^2\cdot T_b=\int_{-\infty}^{\infty}\frac{\frac{N_0}{2}}{1+(2\pi\tau f)^2}\,df=\frac{N_0}{4\tau} \tag{3.14}$$

where σ is the noise variance.

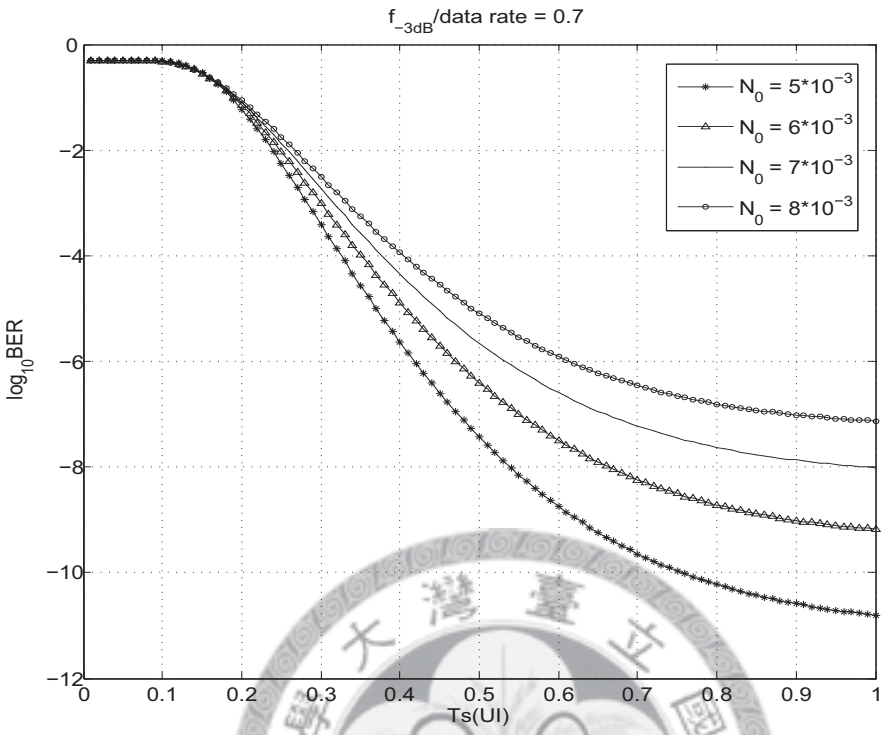


Figure 3.9: The BER with various sampling time.

Total BER shown in Fig. 3.8 is

$$BER = \frac{1}{4}\left[Q\left(\frac{0.5 - ISI_0}{\sigma_n}\right) + Q\left(\frac{0.5 - ISI_1}{\sigma_n}\right) + Q\left(\frac{p_o(T_s) + ISI_0 - 0.5}{\sigma_n}\right) + Q\left(\frac{p_o(T_s) + ISI_1 - 0.5}{\sigma_n}\right)\right]. \tag{3.15}$$

From this equation, it can be comprehended that BER is related to sampling point (T_s), bandwidth of the system (τ) and noise power spectral density (N_0).

Use MATLAB to simulate the BER with various parameters. Fig. 3.9 shows the relation of BER and sampling point in a first-order LTI system with equal N_0 and bandwidth. According to Fig. 3.9, this system obtains lower BER when the sampling point (T_s) is closer to T_b. This conclusion also can be explained based on the formula of received data. From Eq. (3.8), the amplitude of received data at sampling time can be written as

$$p(T_s) = 1 - \alpha^{\frac{T_s}{T_b}}. \tag{3.16}$$

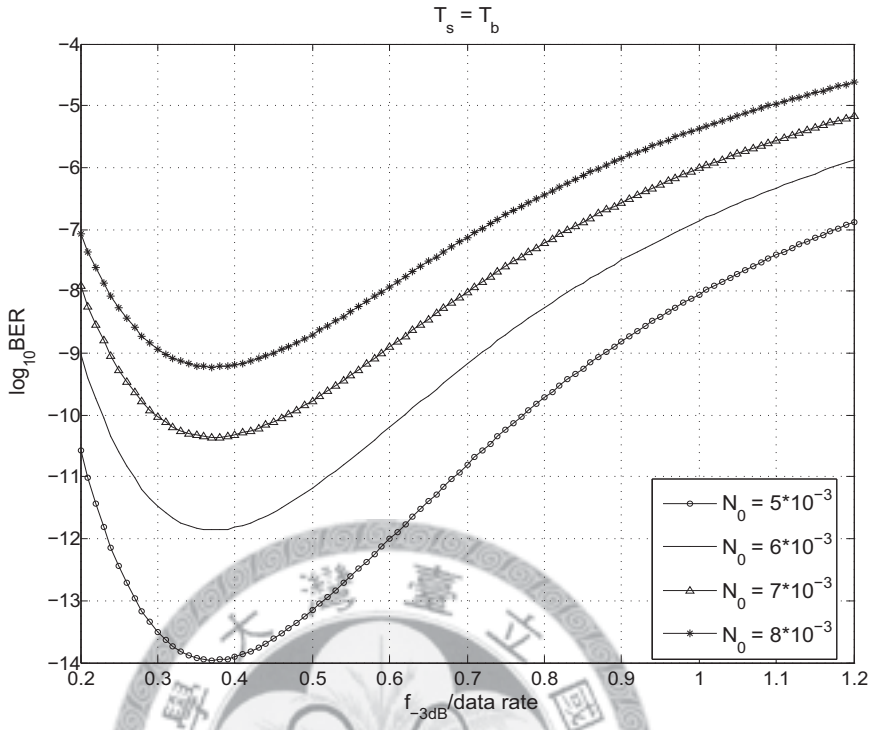


Figure 3.10: The BER with various bandwidth at $T_s = T_b$.

The amplitude reaches maximum at $T_s = T_b$ and the BER in Eq. (3.15) is going to be minimum if N_0 and bandwidth are identical.

From Fig. 3.9, the optimal sampling point in the LTI system is at $T_s = T_b$. In order to find the bandwidth with lower BER, simulate the BER with various bandwidth at $T_s = T_b$, and the result is demonstrated in Fig. 3.10. From this figure, it depicts there is a trade-off between the noise and the ISI influence. When the bandwidth becomes boarder, the noise injects into the receiver and causes higher BER. However, if the bandwidth is excessively small, the impact of ISI is significant and limits the BER. At $T_s = T_b$, it exists an optimal bandwidth to acquire minimum BER and the value is 40% of the data rate.

Although the optimal sampling point is at $T_s = T_b$ based on above simulation results, the typical sampling point is in the middle of the received data (i.e.$T_s = 0.5T_b$) in traditional CDR circuits. The simulation result is in Fig. 3.11. Therefore, the bandwidth is designed to about 70% of the data rate in the receiver with traditional CDR circuits.

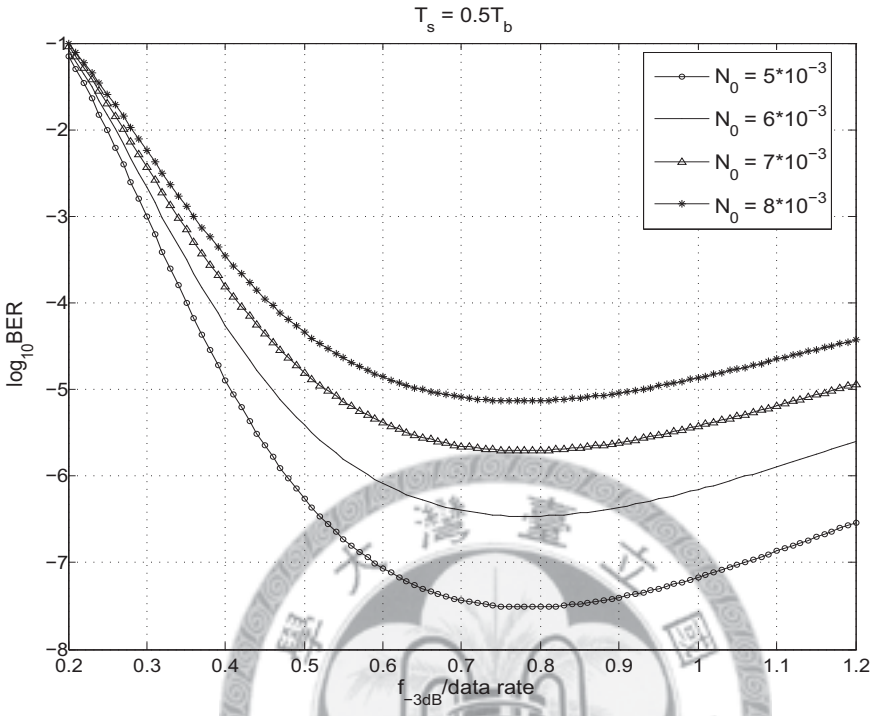


Figure 3.11: The BER with various bandwidth at $T_s = 0.5T_b$.

3.2.3 Timing Jitter

Timing jitter is also one of the factors influencing the BER, and is mainly caused by two sources. One is data jitter and the other is the uncertainty of the sampling clock. These two causes will be respectively illustrated later.

In previous sections, assume the data transitions defined as the time of the data crossing the decision threshold (V_{TH}) occur at mT_b ($m \in$ integer), and the amplitude fluctuation dominates the BER. However, the actual time of data transition deviates from the expected value thanks to the non-ideal effects mentioned before, e.g. noise and ISI. This phenomenon is called data jitter and leads to timing jitter depicted in Fig. 3.12(a). The data jitter reduces the eye diagram of received data on the horizontal direction. Fig. 3.12(b) shows this appearance. When the data jitter alters larger, the sampling window where the BER can achieve the target becomes smaller. Furthermore,

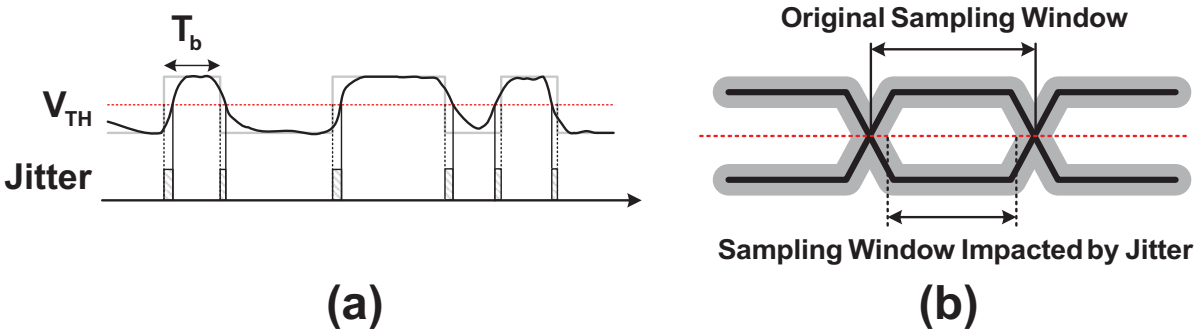


Figure 3.12: (a)The timing jitter and (b)sampling window of received data.

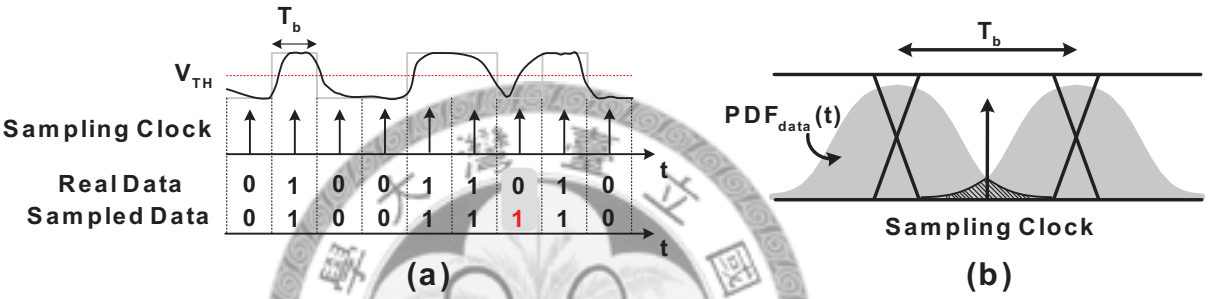


Figure 3.13: The BER caused by the data jitter.

if the sampling point is fixed, the BER increases due to the error detection caused by the data jitter. Fig. 3.13 shows the BER from jitter which is the area under the tail of $PDF_{data}(t)$. $PDF_{data}(t)$ is the probability distribution of total jitter, and σ_d represents the variance of the data jitter. If there are no noise and ISI, and sampling clock is ideal, the BER only influenced by data jitter is written as

$$BER(T_s) = \frac{1}{2}\left[\int_{T_s}^{\infty} PDF_{data}(t)\,dt\right] + \frac{1}{2}\left[\int_{-\infty}^{-T_b+T_s} PDF_{data}(t)\,dt\right]. \tag{3.17}$$

Additionally,

$$PDF_{data}(t) = \frac{1}{\sqrt{2\pi}\sigma_d} \cdot e^{-\frac{(t-T_s)^2}{2\sigma_d^2}}. \tag{3.18}$$

The errors induced by data jitter are independent of those from amplitude fluctuations that come from noise and ISI. Use MATLAB to simulate the BER caused by data jitter and demonstrate the result in Fig. 3.14. Based on this figure, if the received data is only influenced by the data jitter, the optimal sampling point is in the middle of the data. Therefore, the traditional CDR circuits can acquire recovered data precisely.

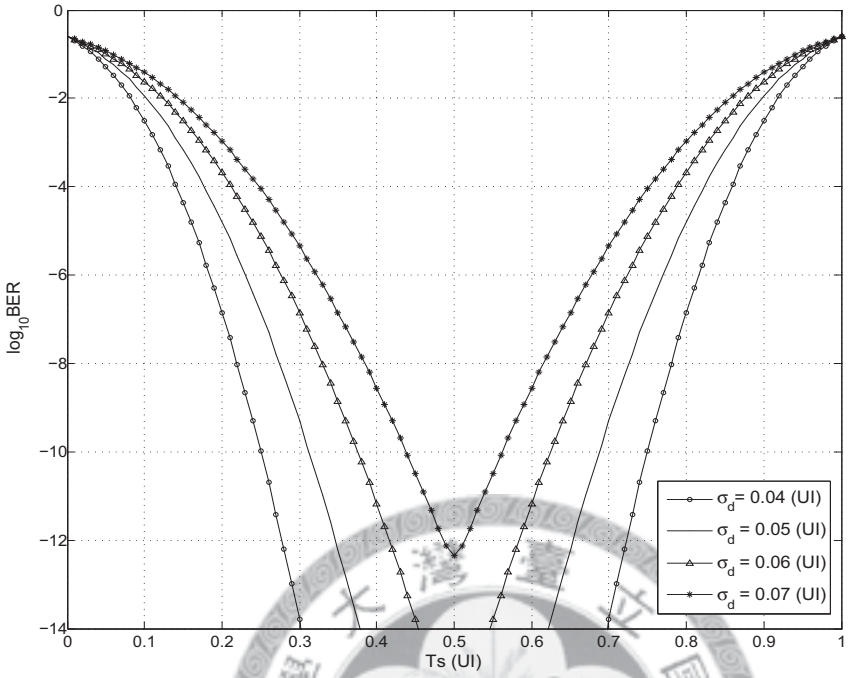


Figure 3.14: The simulation result of BER with various the data jitter.

Another source to impact on the BER is clock jitter. The probability distribution function of clock jitter, $PDF_{clk}(t)$, in various CDR is distinct. In the traditional CDR, the $PDF_{clk}(t)$ is related to not only the jitter from clock generator, but also the data jitter. Because the clock of these architectures is regenerated by some logic gates which received data control, the data jitter impacts on the clock jitter as well. σ_c represents the variance of the clock jitter, and the $PDF_{clk}(t)$ is written as

$$PDF_{clk}(t) = \frac{1}{\sqrt{2\pi}\sigma_c} \cdot e^{-\frac{(t-T_s)^2}{2\sigma_c^2}}. \tag{3.19}$$

Because the clock is not regenerated in the blind oversampling CDR, the clock jitter does not relate to data jitter. The sampling time is not at $0.5T_b$ similar to that in the typical CDR, but has an offset from the middle of one bit period. Therefore, the $PDF_{clk}(t)$ of oversampling CDR is consisted of the jitter generated from clock generator and the sampling time offset. The probability distribution function of the sampling time

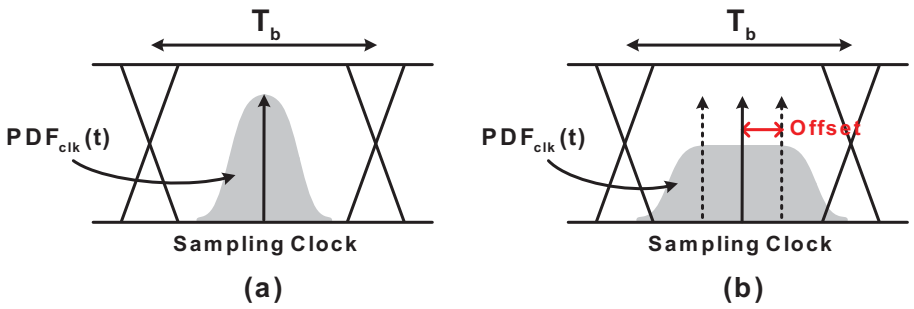


Figure 3.15: The PDF of data jitter in (a)typical CDR, and (b)oversampling CDR.

offset is

$$PDF_{os}(t) = \begin{cases} M & \frac{-1}{2M} \leq t < \frac{1}{2M} \quad (M \in \text{odd integer}) \\ 0 & \text{otherwise} \end{cases} \tag{3.20}$$

where M is the number of clocks to sample data and has been mentioned in Section 3.1.2. Finally, combine the original clock jitter from the oscillator and this sampling time offset, and the $PDF_{clk}(t)$ is written as

$$PDF_{clk}(t) = \begin{cases} \frac{M}{\sqrt{2\pi}\sigma_c} \cdot e^{-\frac{(t-T_s)^2}{2\sigma_c^2}} & \frac{-1}{2M} < (t - T_s) < \frac{1}{2M} \\ 0 & \text{otherwise} \end{cases}. \tag{3.21}$$

Fig. 3.15(a) and (b) separately demonstrate the probability distribution function of clock jitter in traditional CDR and blind oversampling CDR.

3.2.4 Overall BER and Comparison

From previous sections, the noise, jitter and ISI all impact on the BER independently. Combine all the causes to discuss the BER in this section. The BER related to noise and ISI terms has been illustrated in Eq.(3.15). Now add the timing jitter into this equation and temporarily assume that the sampling clock is ideal. According to [4], the

BER without clock jitter at sampling time (T_s) is

$$BER(T_s) = \frac{1}{4}\Bigg[Q\left(\frac{0.5 - ISI_0(T_s)}{\sigma_n}\right) \cdot \left(1 + Q\left(\frac{T_s - T_b}{\sigma_d}\right)\right) + \left(\int_{-\infty}^{T_s} PDF_{data}(t) \cdot Q\left(\frac{0.5 - ISI_1(T_s - t)}{\sigma_n}\right) dt \right) \cdot \left(1 + Q\left(\frac{T_s - T_b}{\sigma_d}\right)\right) + Q\left(\frac{T_s}{\sigma_d}\right) + Q\left(\frac{T_b - T_s}{\sigma_d}\right) \Bigg]. \quad (3.22)$$

The simulation result of MATLAB is depicted in Fig. 3.16. Here supposes the bandwidth of previous circuit is 70% of data rate and vary N_0 to demonstrate the relation between BER and the sampling point. It can be seen from this figure that the finally optimal sampling point is not in the middle of the received data. If the data influenced more seriously by noise and ISI, the optimal sampling point is closer to T_b in the LTI system. Otherwise, if the data impacted more critically by timing jitter, the optimal sampling point is closer to middle of the data ($0.5T_b$).

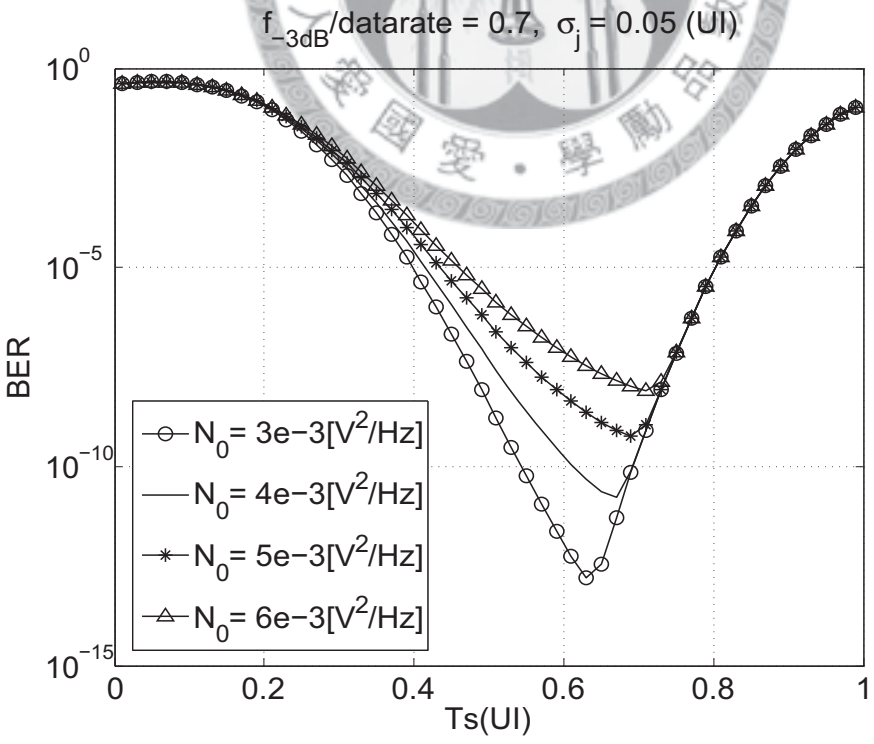


Figure 3.16: The relation between BER and T_s with various N_0.

Additionally, when N_0 is fixed and the bandwidth of previous circuit is 70% of data rate, the jitter(σ_j) is altered to observe the relation between BER and sampling point. This simulation result is shown in Fig. 3.17. It can be seen that the optimal sampling point is not identical with various jitter.

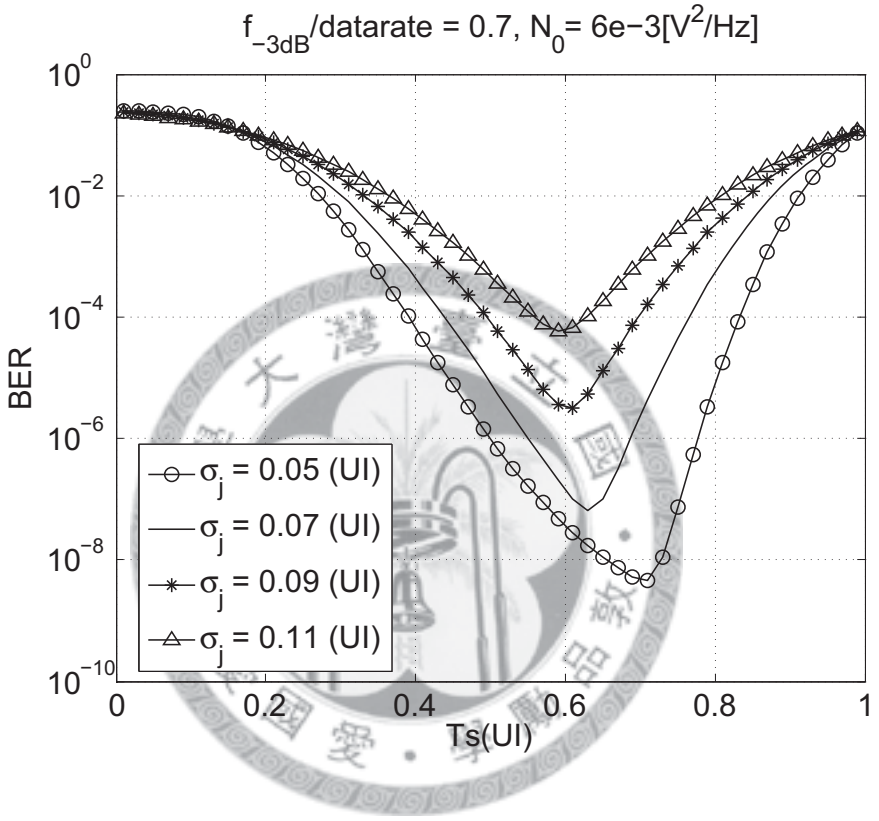


Figure 3.17: The relation between BER and T_s with various jitter.

Based on Fig. 3.16 and Fig. 3.17, the optimal sampling point is not at $0.5T_b$, but alters dependent on various situations. Therefore, traditional CDR circuits which always sample at the middle of received data can not recover signal with lower BER. In order to improve this drawback, an eye-opening monitor CDR is proposed in this thesis and introduced in the later section.

If the sampling clock is not ideal and has jitter like that modeled in Eq.(3.21) and Eq.(3.19), the actually total BER at sampling time (T_s) is derived as

$$BER = \int_0^{T_b} PDF_{clk}(Ts) \cdot BER(T_s)\, dT_s. \tag{3.23}$$

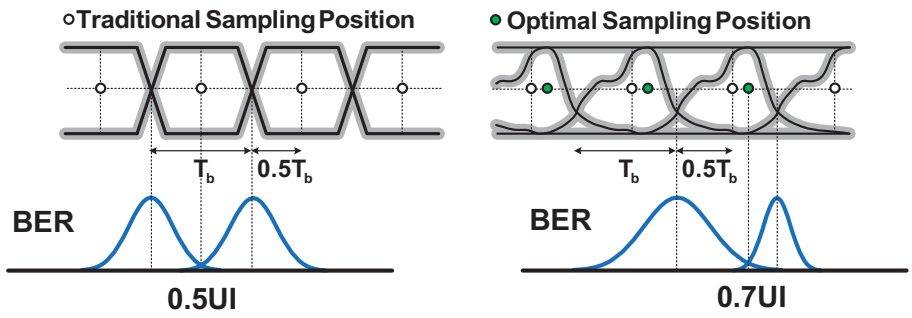


Figure 3.18: (a)Ideal received data, and (b)received data in reality.

3.3 Proposed Eye-Opening Monitor CDR

No matter what kind of CDR it is, the sampling time is perferably at middle of one bit period ($T_s = 0.5T_b$) to recover data. Nevertheless, when data is transmitted, it is impacted by channel loss and the received data is not looked like that in Fig. 3.18(a) but in Fig. 3.18(b). Hence, the optimal sampling point is not at $0.5T_b$, but alters dependent on distinct received data. This conclusion is obtained from BER analysis discussed in preceding sections. From Fig. 3.16 and Fig. 3.17, the lowest BER is not at $0.5T_b$. Thus, propose an architecture based on the oversampling CDR including an eye-opening monitor technique. It has not only the advantages of oversampling CDR, but also the additional capability that can select a more appropriate sampling clock when channel loss exists.

3.3.1 Eye-Opening Monitor

In communication system, the received signal quality is related to its eye diagram. Therefore, eye-opening monitor (EOM) technique is normally used to extract information from the received signal. For instance, a "window monitor" and a "window counter" are implemented to inspect optical signal quality in [5]. The "window monitor" uses two reference levels overlapped with the eye diagram of input signal and finds the signal falling between the two reference levels. Furthermore, the "window counter" counts the number of bits inside the window. When the number exceeds a threshold, it means that the signal quality in working fibre degrades and then the system is switched to receive

signal from a standby fibre. In [6], the eye-opening monitor can adaptively adjust the decision threshold level of the receiver and the clocks recover the input data at half a clock period in the receiver. Moreover, the eye-opening monitor is used in feedback of adaptive transversal filter equalizers in [7]. The eye diagram monitor evaluates output data of the filter and adjust its coefficients. This EOM circuit architecture maps not only the vertical (amplitude) opening of the eye diagram but also the horizontal (temporal) opening and is called two-dimensional(2-D) EOM. [8] has used the eye-opening monitor technique to implement CDR circuit, but it needs off-chip PC-based algorithm to find out the optimal sampling position. In addition, it consumes large power and area.

3.3.2 Proposed EOM CDR Architecture

Propose a CDR circuit including a two-dimensional eye-opening monitor to detect the input signal and select proper sampling clock to recover data with low BER. Firstly, use two reference levels, $V_{REF,H}$ and $V_{REF,L}$, to form a window overlapping on the eye diagram of input signal, and find the part of signal which does not fall in this window. The signal out of this window is more appropriate to be read than other parts, because it has more open eye diagram and lower bit error rate. Moreover, determine the size of window by adjusting the reference voltage.

Secondly, use multiphase clocks to sample those signals, and process the results with logic gates. After the majority voting mechanism, the most adequate sampling clock is selected in the end. The architecture of this EOM CDR is depicted in Fig. 3.19. No matter how the received data is impacted by noise, ISI and jitter, this EOM CDR can recover data at more proper position.

The reference voltage can decide the size of window. When the window gets larger, the sampling clock is closer to the position where data has the lowest BER. The relation between selected sampling clock and window size is demonstrated in Fig. 3.20.

Moreover, use MATLAB to simulate the BER analysis related to the sampling clocks and various reference voltage (i.e. distinct window size). In Fig. 3.21, it can be seen

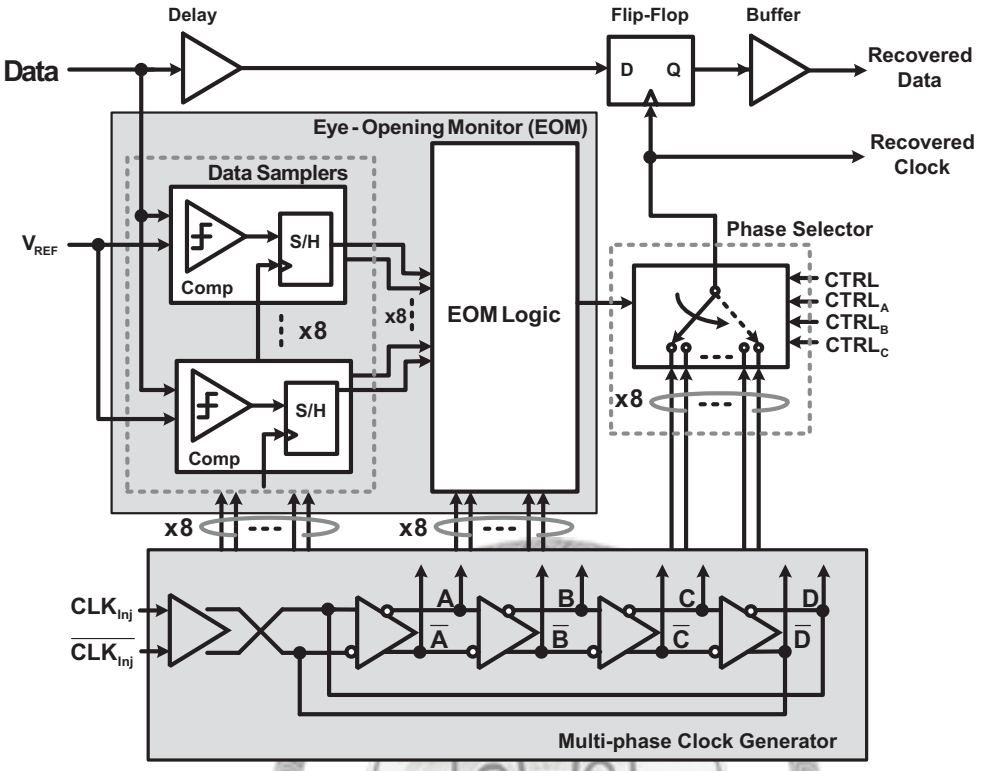


Figure 3.19: The block diagram of the EOM CDR.

if the system asks the BER of recovered data should be lower than a specific value (assume 10^{-12} here), the EOM CDR can achieve this request by modifying the reference voltage. Here, assume the amplitude of input data is 0.2V peak-to-peak and the dc value is 0.6V. From this simulation result, if the reference voltage is set at 0.66V, the BER of recovered data is only gauranteed to achieve lower than 10^{-8}. However, adjust the reference voltage to 0.68V, the recovered data with BER lower than 10^{-12} can be attained.

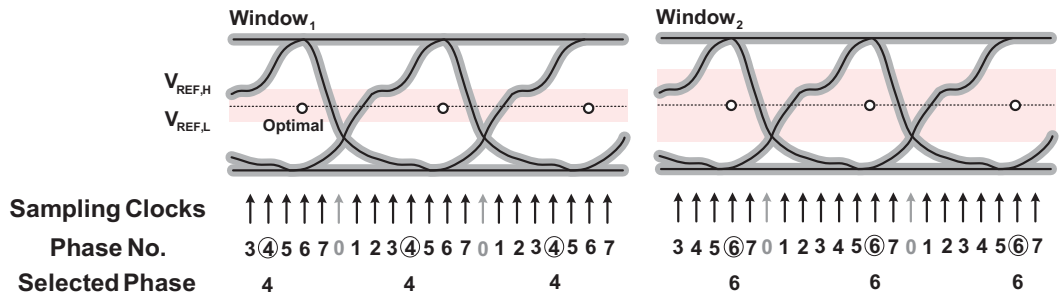


Figure 3.20: The relation between window size and selected sampling phase.

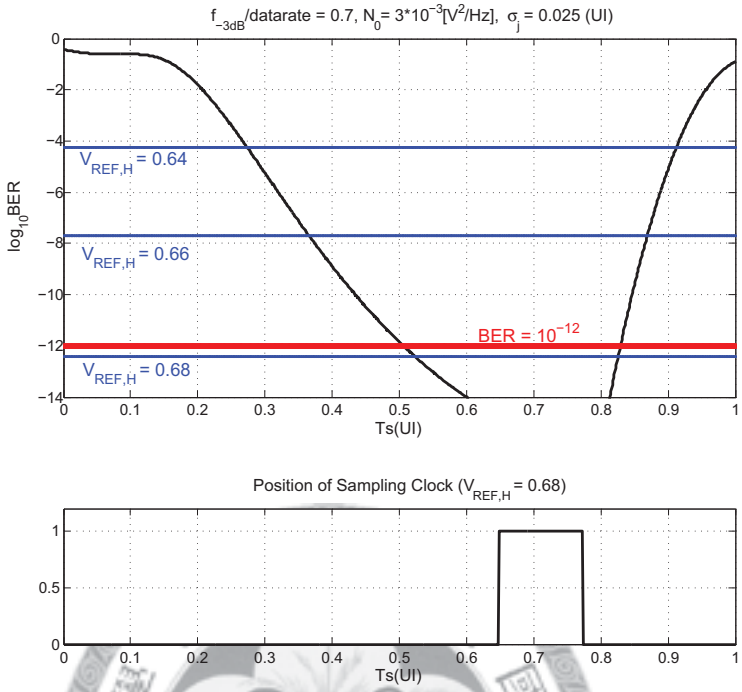


Figure 3.21: The relation between reference voltage and BER, and sampling position.

In high speed serial-link receiver, an equalizer is demanded to compensate the channel attenuation. The channel used here is FR4 trace. The compensating ability of equalizer limits the transmission length. The equalizer ordinarily boosts the gain, and the combined bandwidth of channel and equalizer should be at least 0.7 of data rate. Only when the bandwidth is 0.7 of data rate, the optimal sampling position is at $0.5T_b$ which is the premise of designing typical CDR circuit. However, if use the EOM CDR, the sampling position is not fixed and varies with received data, and the bandwidth of channel and equalizer need not to achieve 0.7 data rate.

The requirement of equalizer in using conventional CDR and EOM CDR is illustrated with AC response in Fig 3.22. From this figure, the bandwidth of equalizer used with EOM CDR is only demanded to compensate to 0.5 data rate instead of 0.7 data rate in using traditional CDR. The restriction of equalizer in employing EOM CDR is rougher.

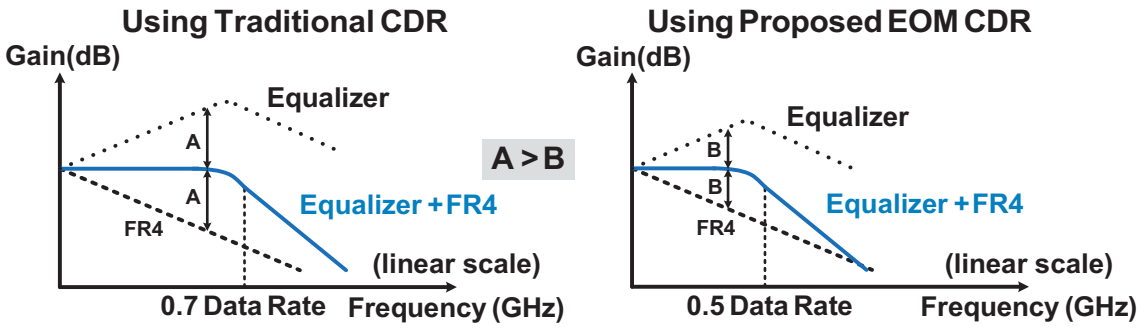


Figure 3.22: Responses of FR4 and equalizer using various CDR circuits.

3.3.3 Extended Application

Since the EOM CDR is based on the blind oversampling architecture, it has the advantage such as quick settling time. This is because blind oversampling CDR does not require feedback loop to decide the position of sampling clock like that in traditional CDR. Because of the fast settling time, EOM CDR can also be used in burst-mode CDR which is employed in optical communication system such as EPON. In addition, it eliminates the obstacles of traditional burst-mode CDR circuits.

The block diagram of traditional CDR using gated-VCO is depicted in Fig. 3.23 [9]. The circuit consists of two matched gated oscillators($GVCO_A$ and $GVCO_B$), a NOR gate, a D latch and a phase-locked loop.

$GVCO_A$ and $GVCO_B$ are respectively started and stopped oscillating by Data and $\overline{\text{Data}}$. The schematic circuit of GVCO is shown in Fig. 3.24. The operating frequency of these oscillators is controlled by the voltage, V_{CTRL}, determined by the PLL. This PLL locks at the rate of transmission data, and uses a duplicate $GVCO_C$ to acquire V_{CTRL}. If these three oscillators are matched, they all operate at the frequency that equals to the data rate. Finally, combine the outputs of $GVCO_A$ and $GVCO_B$ with a NOR gate, and obtain the recovered clock to sample data using D-Latch at the positioin which is in middle of one data interval if the clock generated by GVCO has 50% duty cycle. Fig. 3.25 demonstrates the timing diagram of this circuit.

Though, this circuit has advantages such as simple architecture and elimination of phase error, it has some drawbacks. The operating frequency of $GVCO_A$ and $GVCO_B$ is

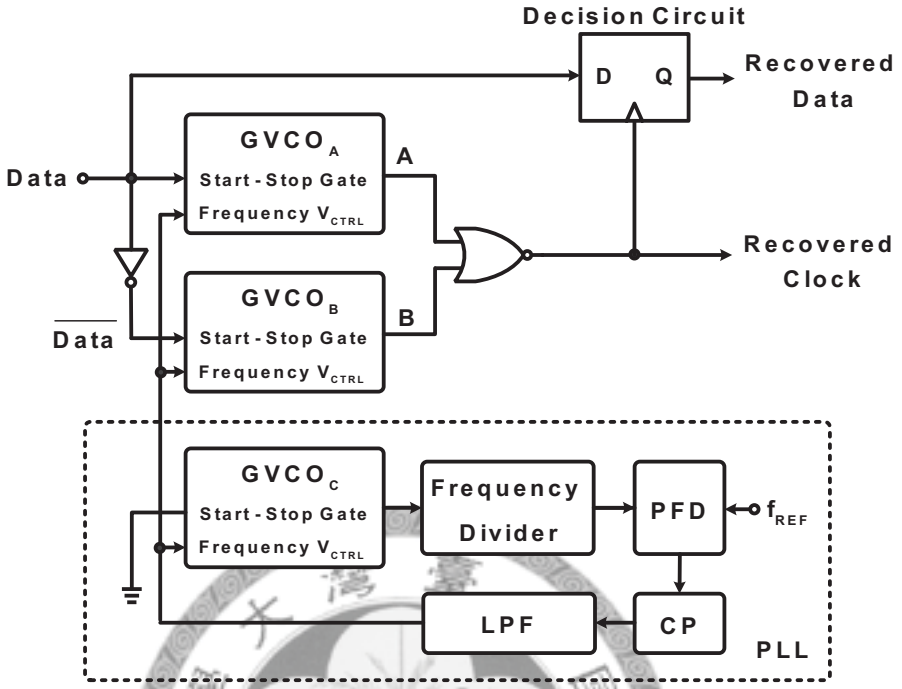


Figure 3.23: Block diagram of GVCO CDR.

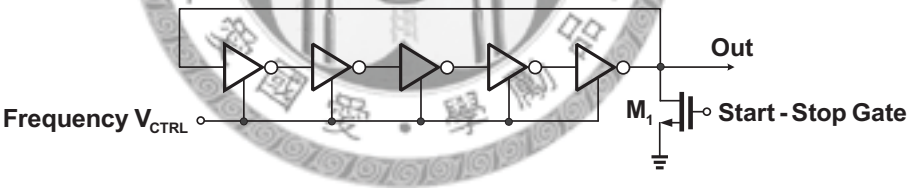


Figure 3.24: Schematic of gated voltage-controlled oscillator (GVCO).

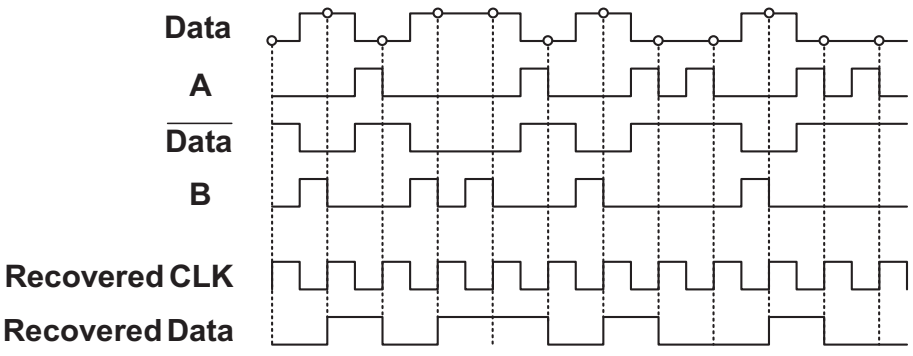


Figure 3.25: Operation of GVCO CDR.

merely controlled by V_{CTRL} instead of a PLL, and it may exist deviations with data rate. Therefore, the phase error will accumulate when consecutive identical digits (CIDs) are received. Moreover, the mismatch between various oscillators can also cause external phase error. These appearances may incur undesired jitter to increase the bit error rate of the recovered data, and also diminish the tolerance to CIDs. In addition to the drawbacks illustrated above, the switched action of the GVCO causes variation on the recovered data and deteriorates the jitter as well.

Compared with traditional CDR, the recovered clock of EOM CDR is the output of multiphase oscillator. However, the recovered clock of typical CDR is regenerated with logic gates controlled by input data. As a result, the recovered data of conventional CDR circuit may be influenced by the jitter of input signal, but that of EOM CDR does not be impacted. In addition, no matter how the received data is impacted by noise, ISI and jitter, this EOM CDR can recover data at more proper position.

3.4 Behavior Simulation

In this section, implement this EOM CDR with MATLAB and verify the function. The diagram is demonstrated in Fig. 3.26. In order to conform to actual situation, this behavior simulation adds extra noise and the influence of ISI on the received data instead of ideal input signal. The input signal is shown in Fig. 3.27.

From the MATLAB simulation, the EOM CDR can select one phase clock to recover data. In order to justify whether the selected clock conforms to the result of analysis mentioned in previous sections, measure the BER of recovered data. Calculate the bit

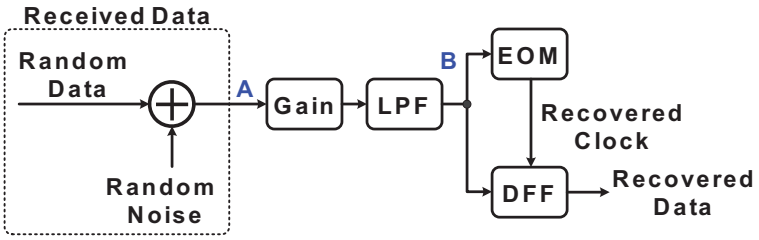


Figure 3.26: The architecture of EOM CDR implemented by MATLAB.

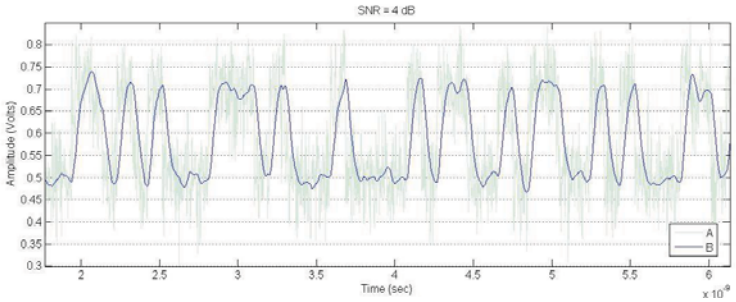


Figure 3.27: The noise and ISI added on the received data.

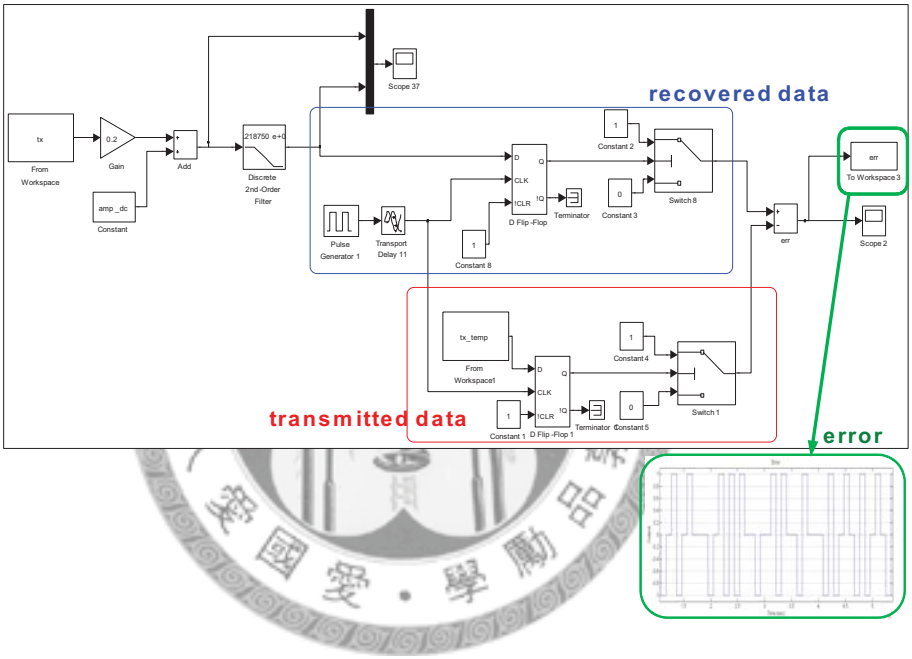


Figure 3.28: Block diagram to calculate the BER of the EOM CDR.

error rate of this implemented EOM CDR using the block diagram in Fig. 3.28.

Firstly, use eight phase clocks to recover data individually and plot the BER curve of various clocks. Then, compare the result of simulation in Fig. 3.30 with that of BER analysis in Fig. 3.29. The trades of these curves are consistent. Finally, to evidence the relation between reference voltage and the selected sampling clock. From the simulation result of Fig. 3.26, this EOM CDR selects Phase_6 when the high reference voltage is 0.65V, and Phase_7 when the high reference voltage is set at 0.67V. These are identical to the analysis result.

The objective in this behavior simulation is just to verify if the EOM CDR can

operate correspondingly with the analysis in previous sections. In order to save the spending time on the simulation, decrease the SNR and increase the BER of this system.

The detailed design and implementation of this EOM CDR are illustrated in the next chapter.

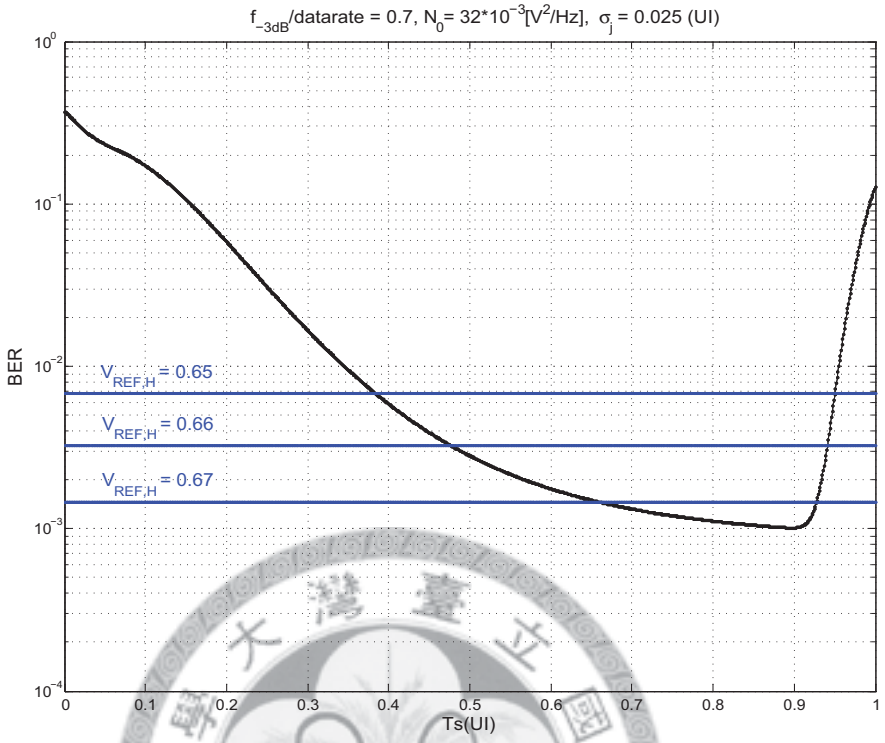


Figure 3.29: The simulation results of analysis.

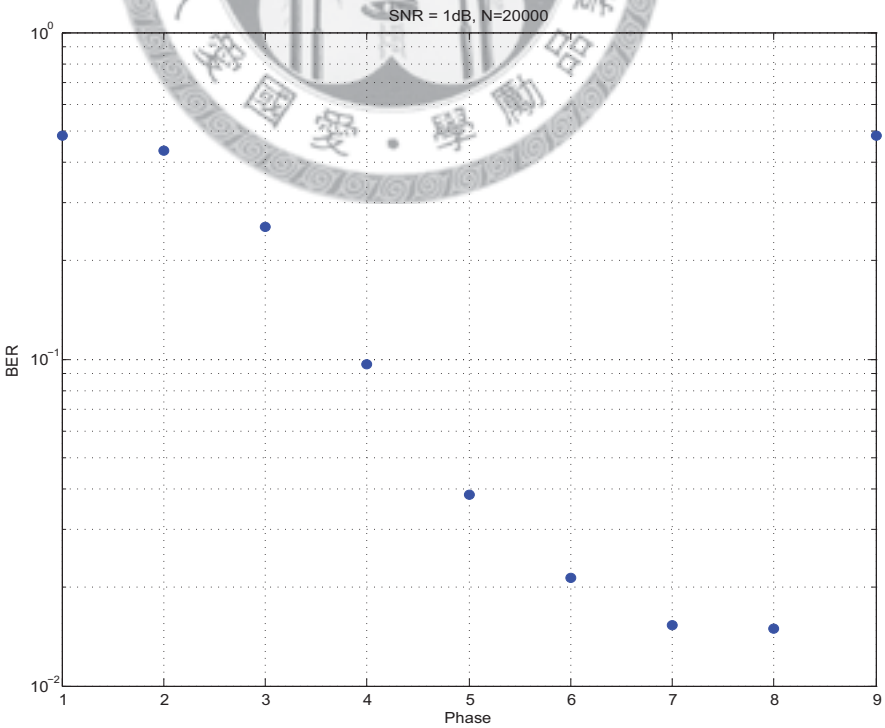


Figure 3.30: The simulation results of behavior simulation.

Chapter 4

Implementation of Eye-Opening Monitor CDR

Fig. 4.1 shows the complete block diagrams of the proposed eye-opening monitor (EOM) CDR. In Chapter 3, the advantages of the EOM CDR have been illustrated, and then in this chapter, demonstrate the design and implementation of this EOM CDR in detail. First, introduce the implementation of the eye-opening monitor which is used to detect input signals and find the optimal sampling phase clock. Secondly, illustrate the multiphase clock generator demanded to provide various sampling clocks for EOM. At the last, a phase selector and output D flip-flop to recover data and clock are included.

4.1 Eye-Opening Monitor

The block diagram of the proposed eye-opening monitor is demonstrated in Fig. 4.2. EOM uses the data samplers to detect received data, and then processes these results with EOM logic to decide the secondly most reliable sampling clock to recover data.

4.1.1 Operating Principle of the EOM

This EOM can be categorized into three modes, ON, OFF and RESET. In RESET mode, it represents that the next pattern is coming and the sampling clock selected based on previous pattern should be reset. No matter which mode the EOM is in, once

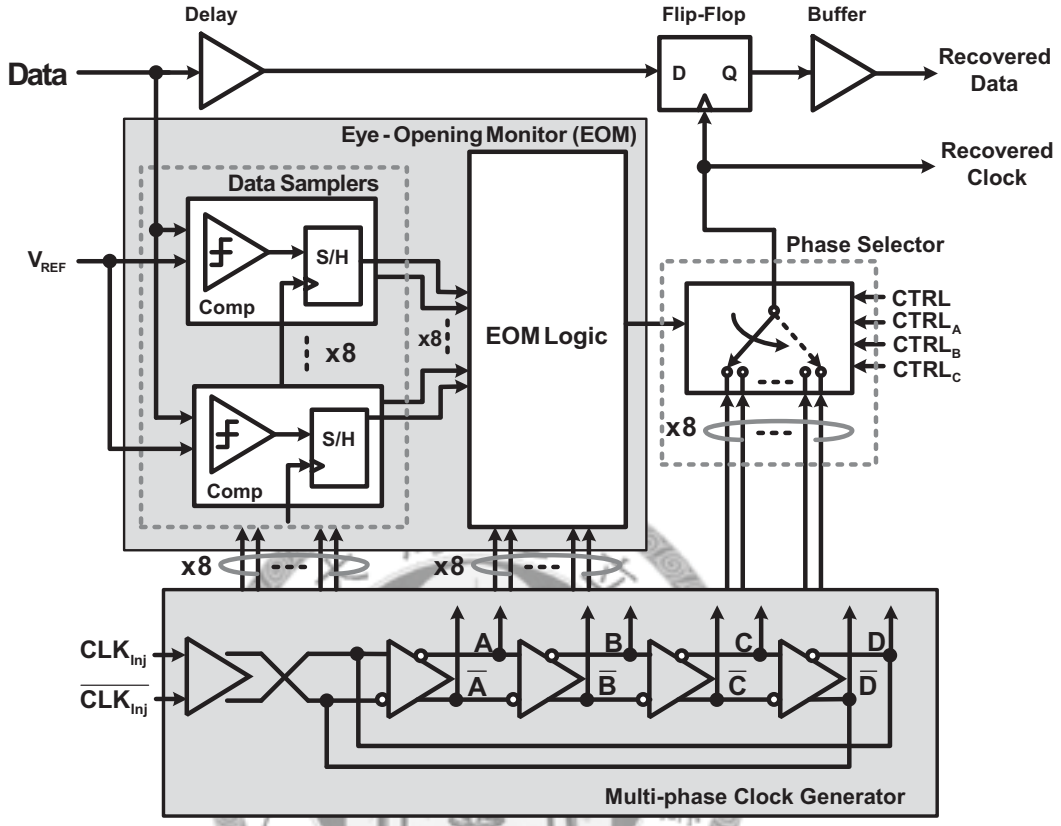


Figure 4.1: The block diagram of the EOM CDR.

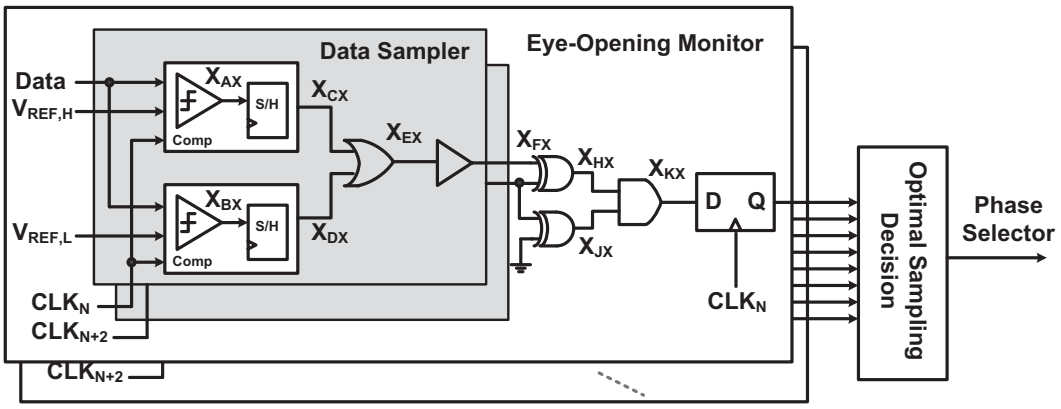


Figure 4.2: Block diagram of the proposed eye-opening monitor.

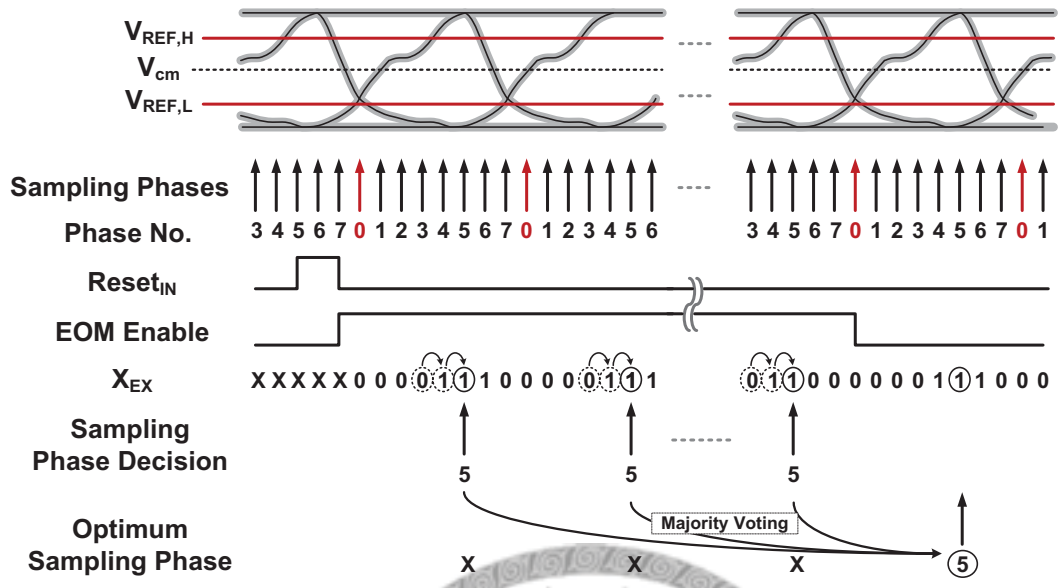


Figure 4.3: Timing diagram of the EOM.

the reset signal (Reset_{IN}) is ONE, the EOM is immediately changed to RESET mode. When the EOM is enable (i.e. EOM in ON mode), it is turned on to choose a proper phase clock. After the EOM has selected and stored one sampling phase clock, it is switched to OFF mode for decreasing power consumption. At this time, the output D flip-flop in Fig. 4.1 starts reading data and exports the recovered data and clock.

Fig. 4.3 shows the timing diagram of this EOM. The node X_{EX} represents the detection result of received data by sampling clock. If V_{EX} is ONE, it is said that the sampling clock can recover data precisely. For the reason to avoid choosing sampling clock closer to the data edge, the EOM selects the secondly reliable clock instead of the first one in this CDR. When the identical sampling clock is chosen repeatedly over 16 times, it is decided the optimal sampling phase and then the EOM is shut down.

4.1.2 Data Sampler

When data is transmitted in optical network, it will be disturbed by noise or ISI. Therefore, the amplitude of received data is not completely V_o or 0, and can be looked like Fig. 4.4. In this EOM CDR, clock can only sample data at the position where the eye diagram is opened large enough and the BER is low. Use $V_{REF,H}$ and $V_{REF,L}$

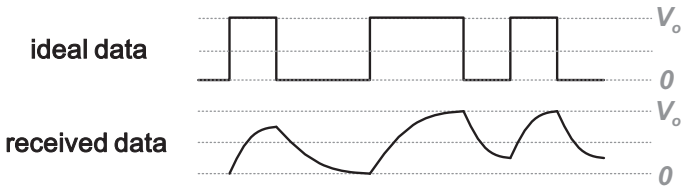


Figure 4.4: Ideal data and received data.

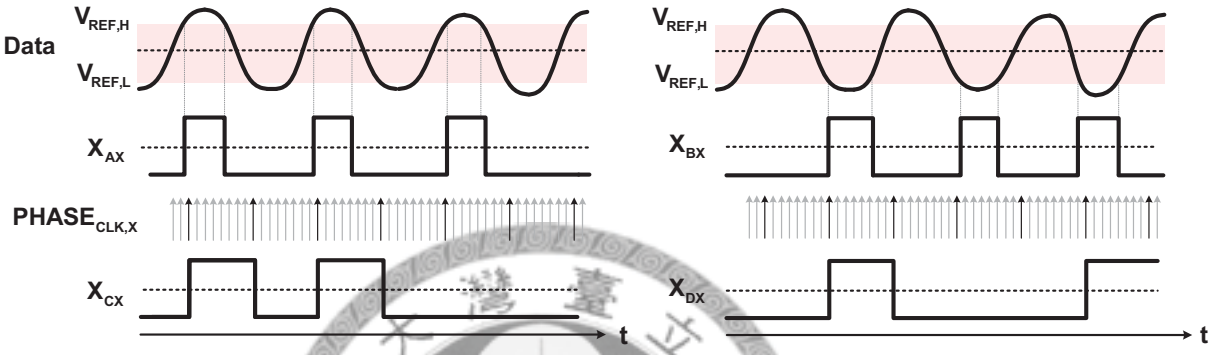


Figure 4.5: Operation of the data sampler.

forming a window to find the part of signal out of the window. In other words, detect input signal whose amplitude is larger than $V_{REF,H}$ or smaller than $V_{REF,L}$. These two reference voltages are decided according to the BER requirement that has been analysed in Chapter 3.

In the data sampler, two comparators are needed to detect which part of input signal during one bit interval achieves desirable amplitude. One decides whether the amplitude of signal ONE is larger than $V_{REF,H}$, and the other compares the amplitude of signal ZERO with $V_{REF,L}$. After comparators have detected which part of input signal has desirable amplitude, use sample and hold circuit with eight phase clocks to sample the outputs, X_{AX} and X_{BX}, of these comparators. Finally, combine the outputs of sample and hold circuit, X_{CX} and X_{DX}, by an OR gate. If the output, X_{EX}, of data sampler is ONE, it represents the phase clock can read data at proper position. The timing diagram of this data sampler is shown in Fig. 4.5.

Fig. 4.6 demonstrates the comparators used here. They are similar but only the positions of two reference voltages and output are opposite. The comparator consists of two parallel source-coupled pairs [7]. Transistors M_3 and M_4 are added to be switches

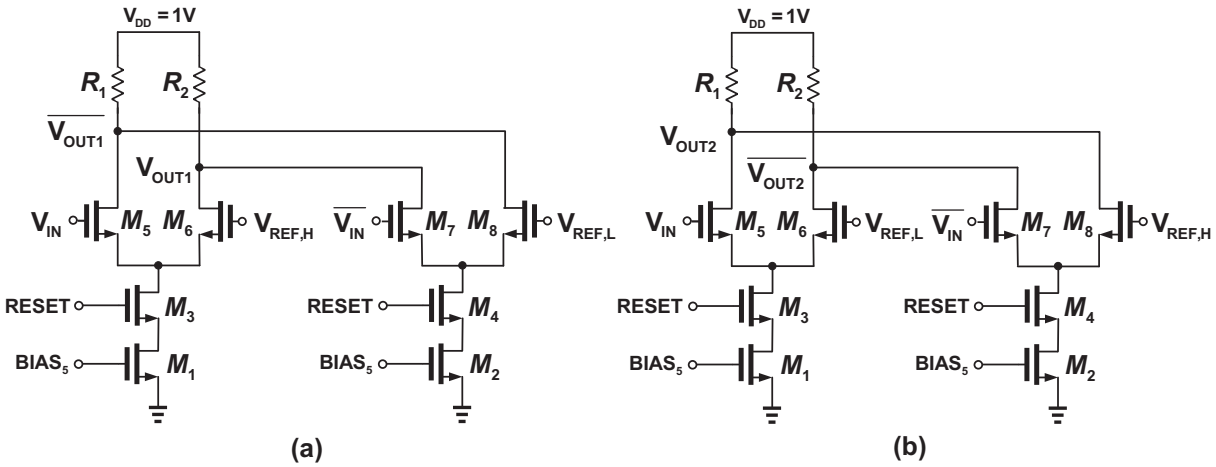


Figure 4.6: (a) Comparator for signal ONE, (b) Comparator for signal ZERO.

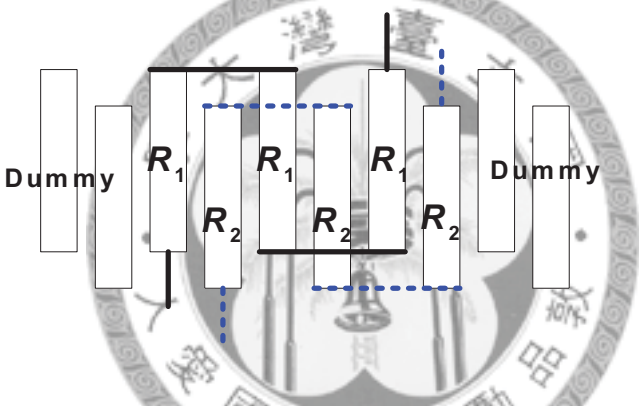


Figure 4.7: Diagram of resistors' placement to avoid mismatch.

that when EOM is turned off, the node RESET is connected to ground to shut off the comparator for saving power. Transistors M_5, M_6, M_7 and M_8 have same size and their transconductances equal g_m. Furthermore, resistors R_1 and R_2 also have identical value, R. Because of the probably serious mismatch between the resistors, the layout of R_1 and R_2 is placed as Fig. 4.7. The outputs of the comparators in Fig. 4.6 are

$$V_{OUT1} = g_m R[(V_{IN} - V_{REF,H}) - (\overline{V_{IN}} - V_{REF,L})] \tag{4.1}$$

$$V_{OUT2} = -g_m R[(V_{IN} - V_{REF,L}) - (\overline{V_{IN}} - V_{REF,H})], \tag{4.2}$$

which can be rewritten as

$$V_{OUT1} = g_m R[(V_{IN} - \overline{V_{IN}}) - (V_{REF,H} - V_{REF,L})] \tag{4.3}$$

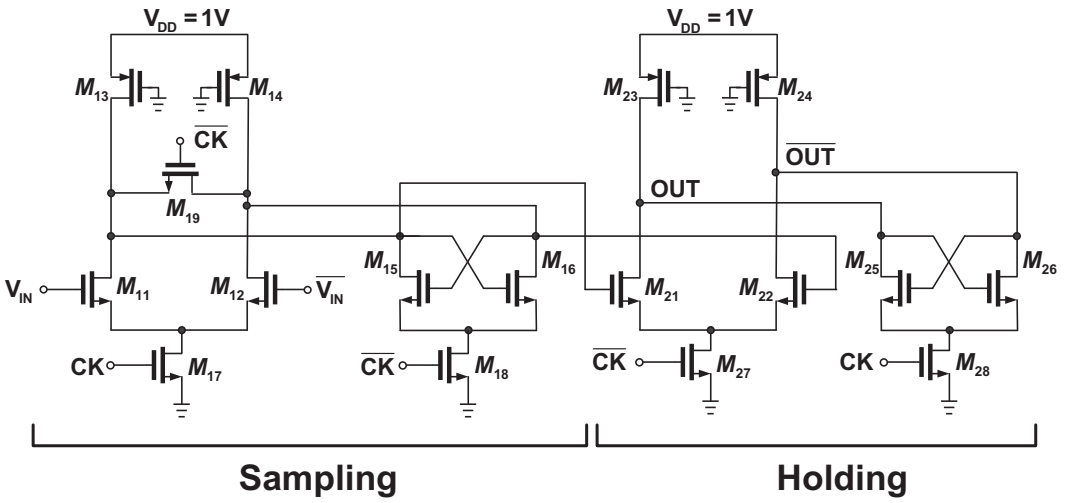


Figure 4.8: Schematic circuit of sample and latch.

$$V_{OUT2} = g_m R[(\overline{V_{IN}} - V_{IN}) - (V_{REF,H} - V_{REF,L})]. \tag{4.4}$$

From Eq. (4.3), when the amplitude of differential input signal exceeds the determined voltage ($V_{REF,H}$-$V_{REF,L}$), the differential output is larger than zero and can be considered as logic 1. On the other hand, the output is thought of logic 0.

After comparators, use sample and hold circuit to sample the output of comparator. The schematic is shown in Fig. 4.8. If the output of this circuit is ONE, it represents the phase clock is proper to recover data.

4.1.3 Eye-Opening Monitor Logic

From Section 4.1.2, there is at least one phase clock which can sample data at appropriate position. If there is only one phase clock conformed to expectation, the only one is selected. However, more than one desired clock may exist. At this situation, the secondly reliable phase clock is chosen. Eye-opening monitor logic uses some logic gates to find the most appropriate sampling clock.

The operation of this EOM logic is illustrated in Fig. 4.9. If X_{EX} in Fig. 4.2 is positive, it represents that the sampling phase clock of the path can recover data with low BER. The Buffer in Fig. 4.2 just amplifies the output of OR, and the results of X_{EX} and X_{FX} are same.

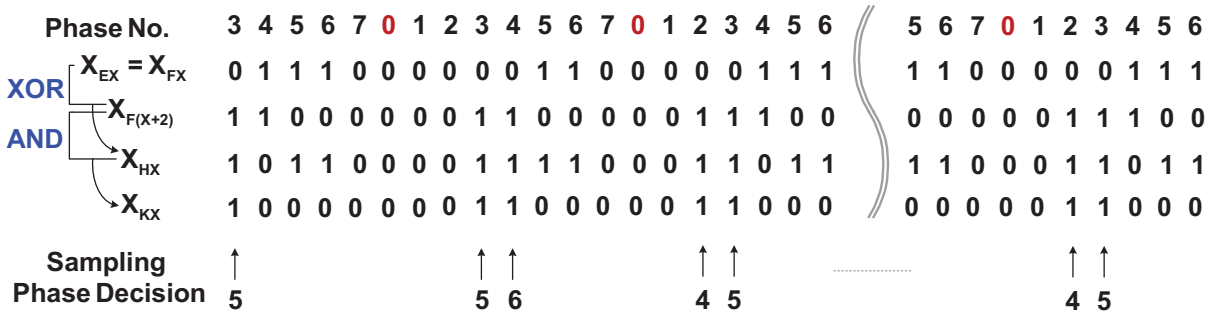


Figure 4.9: Operation diagram of EOM logic.

In order to find in which path X_{FX} is one, use XOR gate and AND gate. A XOR gate first processes X_{FX} and $X_{F(X+2)}$ to find the edge which X_{FX} changes from ZERO to ONE or ONE to ZERO, and outputs ONE at node X_{HX}. Here use $X_{F(X+2)}$ instead of $X_{F(X+1)}$, because the EOM logic is designed to select the secondly proper phase clock. After the transforming edge has been detected, use an AND gate to find out the edge changing from ZERO to ONE. Since there is delay between X_{HX} and $X_{F(X+2)}$, add a dummy XOR to generate matching delay. This delay makes X_{HX} and X_{JX} changing at the same time to avoid undesirable glitch. After all, X_{KX} only outputs ONE when X_{FX} transforms from ZERO to ONE, and it represents the sampling clock of the path (X+2) is desirable.

These logic gates used in EOM logic should be operated at half of the clock frequency, so static CMOS logic is not suitable here. Therefore, use current-mode logic topology to meet this requirement. Fig. 4.10 demonstrate the schematics of current-mode logic circuits (OR, AND and XOR) used here.

In each path, a differential output can be obtained through preceding stages, but a single signal with full swing, 0 V or V_{DD}, is needed to control the switches which decide the counter operating or not in optimal decision circuit. Therefore, the differential signal at node X_{KX} has to be transformed to single one. The circuit is depicted in Fig. 4.11.

In Fig. 4.11, the transistors M_1, M_2, M_3 and M_4 transform differential signal to single one. When $(X_{KX} - \overline{X_{KX}})$ is positive, there is mirrored current charging point A and output a single high signal. On the other hand, a current flows to ground via M_2 and pulls point A to a single low signal.

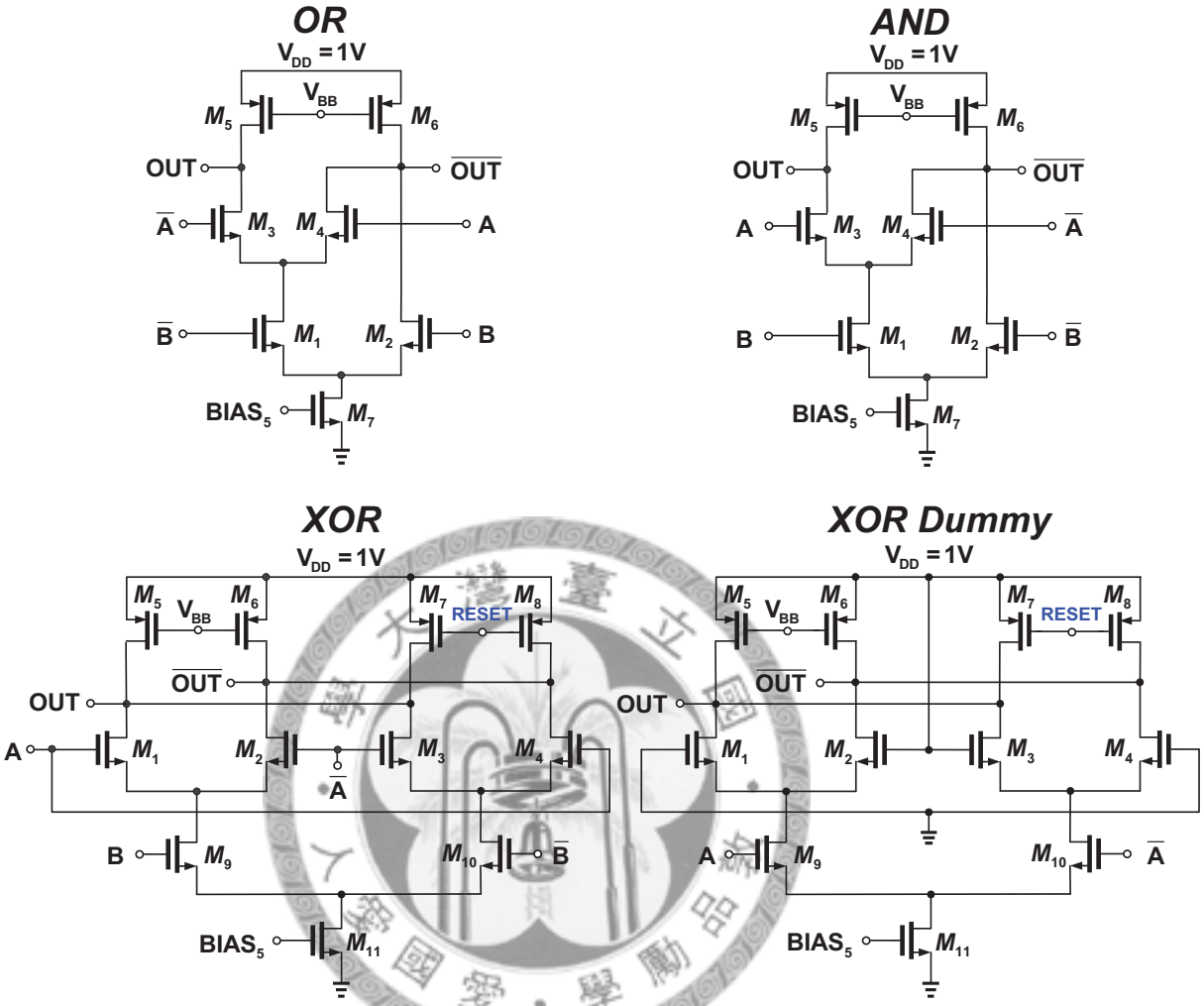


Figure 4.10: Schematics of current-mode logic circuits used.

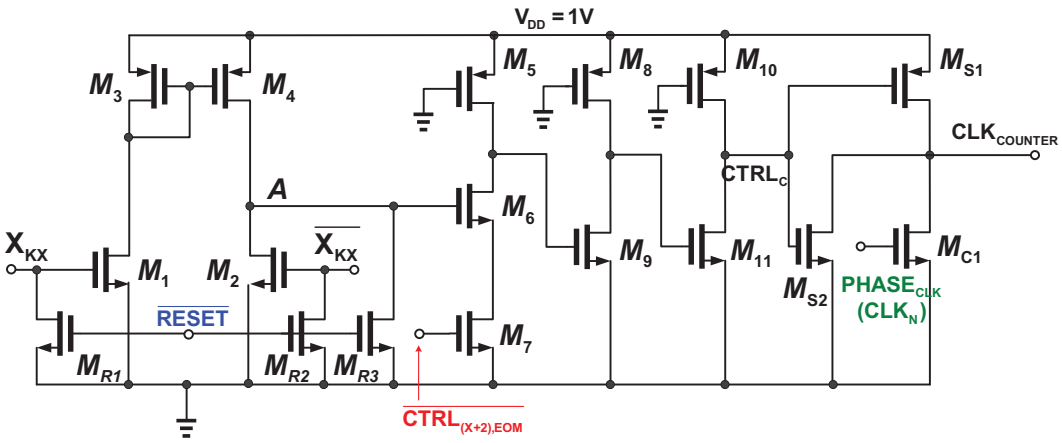


Figure 4.11: Differential to single circuit

Only when $\overline{\text{CTRL}_{(\text{X+2}),\text{EOM}}}$ is high, the result generated by proceeding circuits can control the counter. If $\overline{\text{CTRL}_{(\text{X+2}),\text{EOM}}}$ is low, it represents the EOM has selected proper phase clock, and is in OFF or RESET mode that the EOM does not operate. An AND gate consists of transistors M_5, M_6 and M_7 to implement this function.

The inverters composed by M_8, M_9, M_{10}, and M_{11} amplify the signal to full swing for completely turning on or turning off the switches, M_{S1} and M_{S2}. These switches decide whether the next stage, counter, operates or not. When CTRL_C is high, the counter cannot receive PHASE_CLK and does not count. The counter starts to operate during CTRL_C being low.

4.1.4 Optimal Decision Circuit

In the preceding subsections, there must be at least one of eight phase clocks considered more proper to sample data. Hence, majority voting technique is used to select the optimal sampling phase clock. In spite of making decision by just one bit, the final chosen phase clock is determined after the same phase clock picked over several times.

The times needed of majority voting to select final sampling clock are determined by probability analysis. If one identical phase clock is selected repeatedly over n times, it is chosen as the optimal phase clock and the EOM is turned off. The probability of selecting this phase clock every time is assumed as p. On the contrary, the probability of selecting unsuitable phase clock is $(1-p)$. The probability of choosing correct phase clock is discussed as follows. In this discussion, we assume that the EOM can always select one phase clock every bit. One situation here is that the optimal phase clock is continuously selected, and the probability of this situation is written as

$$X_0 = \underbrace{p \cdot p \cdot p \cdot p \cdot \cdots \cdot p}_{total\ number\ of\ p\ =\ n} = p^n. \tag{4.5}$$

The undesirable phase clock can also be chosen m times. However, since the optimal phase clock is still decided finally, the most number, m, of selecting every undesirable phase clock should be smaller than n. Therefore, the probability of choosing correct

phase clock in this situation is

$$X_m = \overbrace{p \cdot p \cdot \cdots \cdot \underbrace{\cdots (1-p) \cdot (1-p)}_{total\ number\ of\ (1-p)\ =\ m} \cdots p}^{total\ number\ of\ p\ =\ n} = p^n \cdot C_m^{(m+n-1)} (1-p)^m. \tag{4.6}$$

All the cases mentioned above should be considered, and the total probability of selecting optimal sampling clock is represented as

$$X_{sum} = X_0 + X_1 + \cdots\cdots + X_m = \sum_{k=0}^{m} X_k \qquad (\ m\ =\ 7(n-1)+n\ ). \tag{4.7}$$

The probability of selecting the optimal phase clock every time, p, relates to the value of reference voltage. The input signal is assumed as sine wave, and the amplitude of signal ONE is 0.7 and the amplitude of signal ONE is 0.5. If the reference voltage is 0.65V, the probability of selecting optimal phase clock, p, can be written as

$$p = \frac{\frac{\pi}{8}}{\frac{5\pi}{6} - \frac{\pi}{6}} = \frac{3}{16}. \tag{4.8}$$

In this situation, the relation between the times needed of majority voting, n, and the correct rate is demonstrated in Fig. 4.12. From this figure, when the n reaches sixteen, the correct rate is over 99%. Therefore, in this implementation, the times of majority voting are determined as sixteen. When reference voltage becomes higher, the probability of selecting optimal phase clock is also larger and p gets higher. Therefore, the times needed of majority voting can be reduced. Fig. 4.13 demonstrates the relation between p and n.

In this optimal decision circuit, a counter is demanded to count how many times the same phase is selected, and output ONE at the right path. The architecture of counter and decision part is depicted in Fig. 4.14, including an asynchronous 5-bit counter, two D flip-flops and some logic gates.

The asynchronous 5-bit counter consists of D flip-flops shown in Fig. 4.15 with various MOS size. In each D flip-flop, the node Q is connected to $\overline{\text{D}}$, and the node $\overline{\text{Q}}$ is connected to D. When EOM is turned off, OFF and $\overline{\text{RESET}}$ are high. At this situation, the D flip-flop is shut off and its outputs, Q and $\overline{\text{Q}}$, are pulled down to ground. One of the reasons for using asynchronous counter is that only the clocks, CK and $\overline{\text{CK}}$, of DFF_{C1}

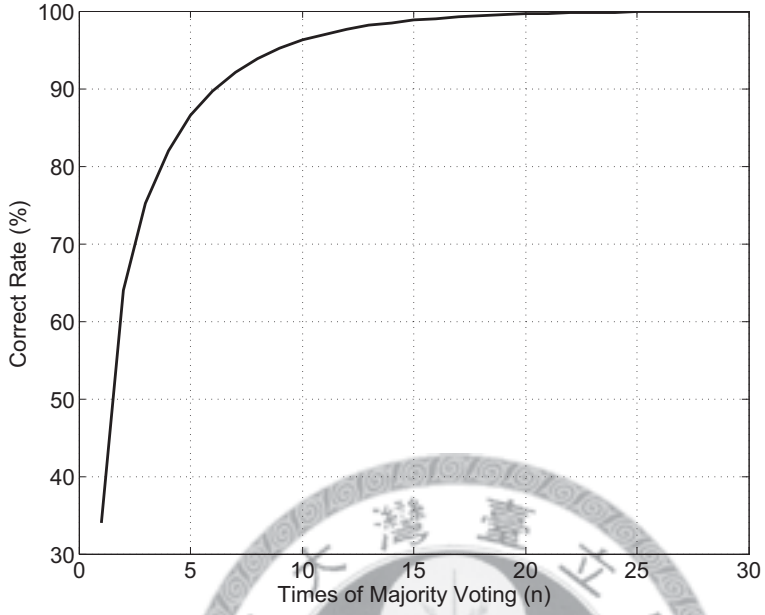


Figure 4.12: The relation between correct rate and the times of majority voting.

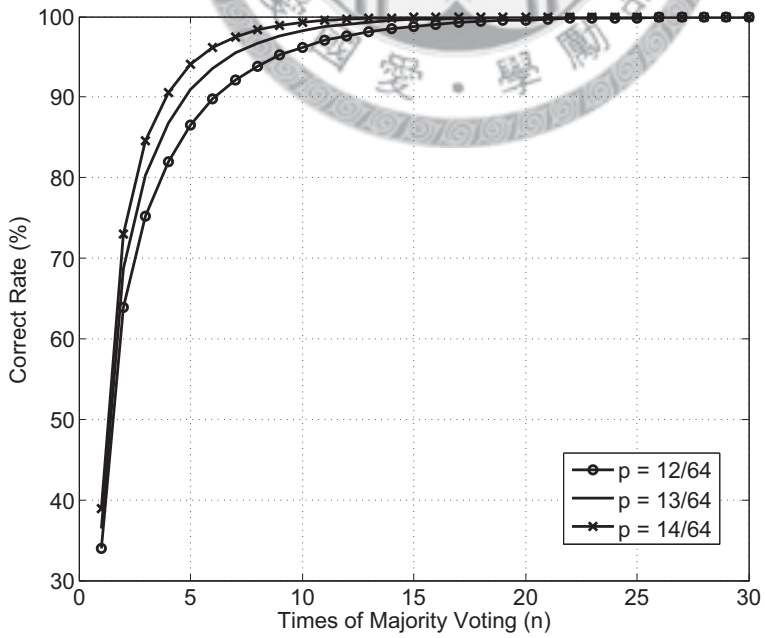


Figure 4.13: The relation between p and the times of majority voting.

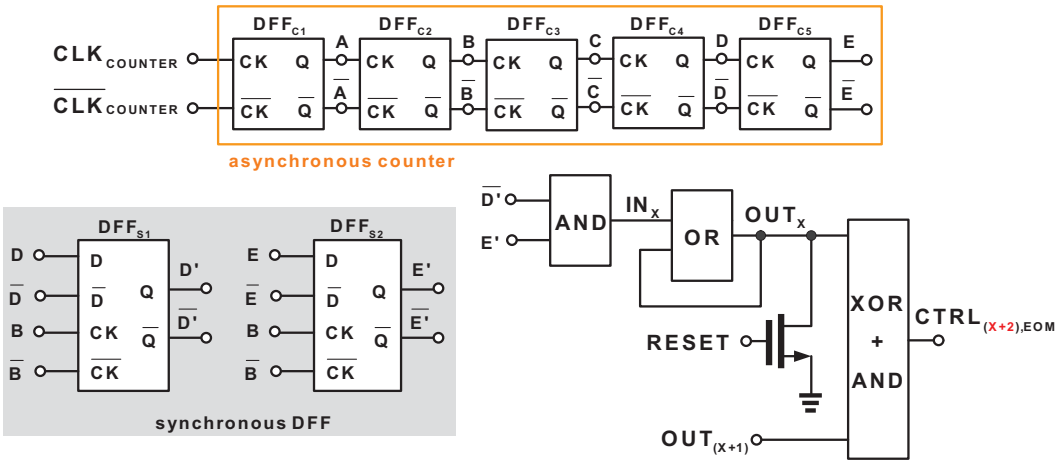


Figure 4.14: Block diagram of optimal decision circuit.

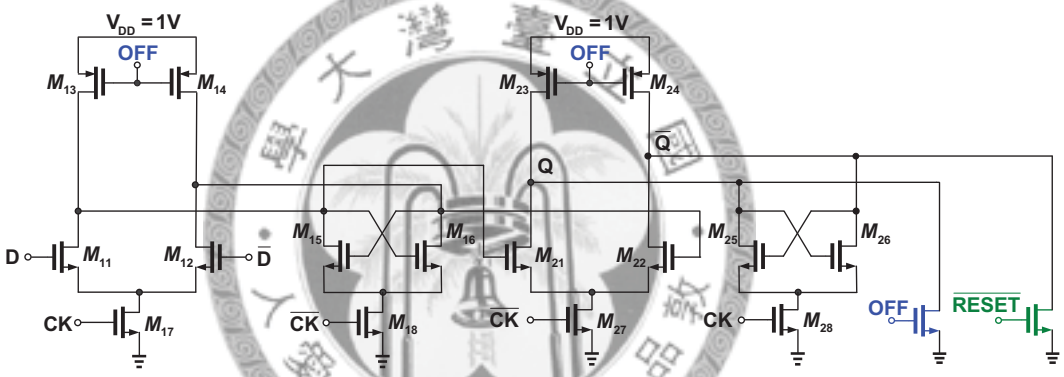


Figure 4.15: Schematic circuit of D flip-flop in counter.

come from ring oscillator. The other D flip-flops are driven by outputs of previous stage. Therefore, the loading of ring oscillator is decreased. In addition, this counter does not need extra gates like synchronous counter except D flip-flops.

The AND gate in Fig. 4.14 outputs signal ONE when the counter counts to sixteen. Due to the asynchronous architecture, a delay exists between every output of D flip-flop. In order to avoid undesirable glitch, DFF_{S1} and DFF_{S2} are required to synchronize $\overline{D}$ and E ,and get synchronous signals, $\overline{D'}$ and E′. These D flip-flops use B and $\overline{B}$ as clocks, and the schematic is identical with that in Fig. 4.15. Similarly, OFF and $\overline{RESET}$ are high at EOM turned off, and outputs of the D flip-flops are pulled to ground.

After EOM has decided which phase of clock is used to recovers data, the counter, DFF_{S1} and DFF_{S2} are all turned off. Nevertheless, the result of EOM system should be

stored and maintained. An OR gate placed as Fig. 4.14 achieves this requirement. In this circuit, OUT_X becomes ONE once IN_X changes from ZERO to ONE. OUT_X returns to ZERO until RESET goes high. As mentioned in Section 4.1.3, two ONE signals probably exist simultaneously at the node X_{KX} as shown in Fig. 4.9. It represents there are two phase clocks selected finally. In order to avoid this situation, a XOR gate and an AND gate are demanded in Fig. 4.14, and then this system correctly selects only one proper phase clock to recover data. If there are two phase clocks selected simultaneously, the first sampling phase clock is perferably chosen.

4.2 Multiphase Generator

This eye-opening monitor demands clocks with various phase to sample data. LC oscillators and ring oscillators also can meet this requirement. Although high Q LC oscillators might have lower phase noise, ring oscillators have the advantages of wider tuning range and smaller area. Hence, a ring oscillator is used here to generate multiphase. In practical application, there should be a phase-locked loop to lock the clock frequency. This work is the prototype to demonstrate the concept of the EOM CDR circuit. Therefore, only a ring oscillator is employed to generate clocks instead of a phase-locked loop. In order to decrease noise and lock the clock frequency, injection locking technique is included extra.

The gate delay and the number of stages decide the operating frequency in the ring oscillator. The fundamental circuit is depicted in Fig. 4.16(a). The phases' relation of different N stages is in Fig. 4.16(b), and the operating frequency can be represented by delay T_D as

$$\omega_{osc} = 2\pi \cdot f_{osc} = \frac{\pi}{N \cdot T_D}. \tag{4.9}$$

In addition, Fig. 4.17 shows the overall schematic circuits used in this CDR to generate multiphase clocks.

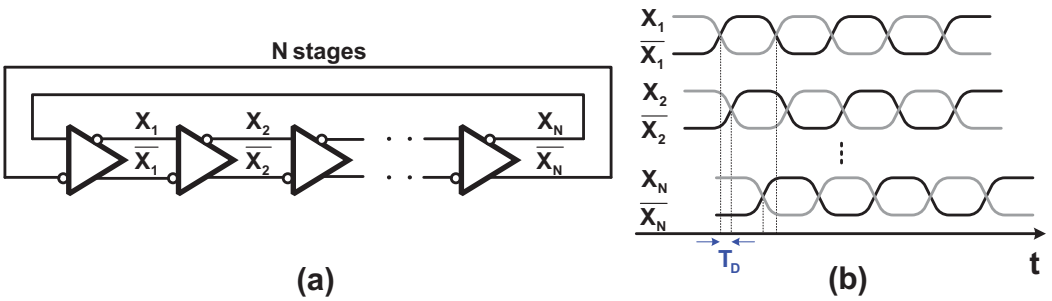


Figure 4.16: (a)Differential ring oscillator, (b)Relation of output phases.

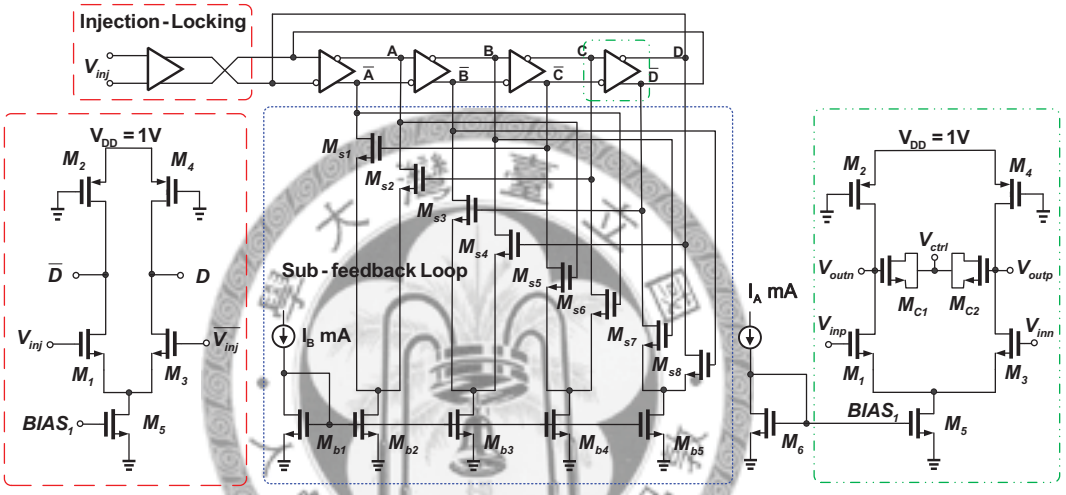


Figure 4.17: Block diagram of the differential ring oscillator

4.2.1 First-Harmonic Injection Locking Technique

The low quality factor of ring oscillators leads to high jitter and phase noise. In order to improve these characteristics, injection locking technique is included. Injection-locked ring oscillator can be distinguished into three categories : first-harmonic, super-harmonic and sub-harmonic. It is based on the relation between incident frequency and the oscillating frequency. A first-harmonic ring oscillator which has the same operating frequency with the incident frequency is used here.

According to [10], the operating frequency and phase noise of injection-locked ring oscillator are analysed. Fig. 4.18(a) shows the first-order model of the injection-locked oscillator where ω_i represents the injection-locked frequency of the N-stage ring oscillator. The operating frequency of ring oscillator has been formulated in Eq.(4.9). The

delay T_D is defined as the time when the output reaches 50% of the voltage of signal ONE, and assume the voltage of signal ONE is V_{DD}. Therefore, the delay T_D without

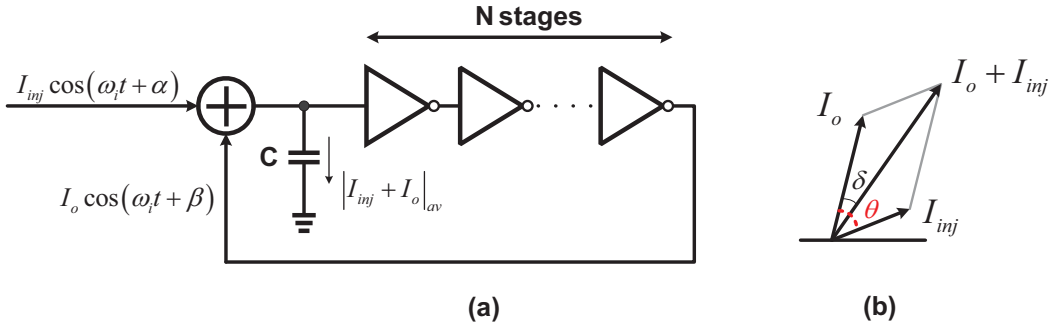


Figure 4.18: (a)First-order model of the injection-locked oscillator,(b)Phasor representation of the currents

injection locking stage can be written as

$$T_D = \frac{C \cdot V_{DD}}{2\,|I_o|_{av}}, \tag{4.10}$$

and with Eq.(4.9) the free-running frequency is

$$\omega_0 = \frac{\pi}{N \cdot T_D} = \frac{2\pi \cdot |I_o|_{av}}{N \cdot C \cdot V_{DD}}. \tag{4.11}$$

The delay $T_{D,inj}$ after including injection locking stage is

$$T_{D,inj} = \frac{C \cdot V_{DD}}{2\,|I_o + I_{inj}|_{av}}. \tag{4.12}$$

Using Eq.(4.9) and Eq.(4.12) yield the injection-locked frequency as

$$\omega_i = \frac{\pi}{N \cdot T_{D,inj}} = \frac{2\pi \cdot |I_o + I_{inj}|_{av}}{N \cdot C \cdot V_{DD}}. \tag{4.13}$$

It can also derive a frequency range, in which the output frequency is locked to the injected signal. This range is called locking range ω_L and can be written as

$$\omega_0 - \omega_L \le \omega_i \le \omega_0 + \omega_L, \tag{4.14}$$

and

$$|\Delta\omega| = |\omega_i - \omega_0| \le \frac{\omega_0}{2Q} \cdot S = \omega_L, \tag{4.15}$$

where Q is the quality factor of the oscillator and S is the injection strength.

$$Q = \frac{\omega_0}{2}\frac{\delta}{\Delta\omega}, \tag{4.16}$$

and

$$S = \frac{|I_{inj}|_{av}}{|I_o|_{av}}. \tag{4.17}$$

In [10], L_{ext} and L_{free} respectively represent the phase noise of the injected signal and the free-running oscillator. Combining the two sources mentioned above generating noise, it gives the overall phase noise L_{total} as

$$L_{total} = \frac{\omega_L^2 \cdot \cos\theta}{(\Delta\omega)^2 + \omega_L^2 \cdot \cos^2\theta} \cdot L_{ext} + \left(\frac{\Delta\omega}{\omega_L}\right)^2 \cdot L_{free}. \tag{4.18}$$

Eq.(4.18) shows that if injected frequency is close to the free-running frequency ($\Delta\omega \approx 0$), the phase noise of injected signal dominates the total noise. On the other hand, if the injected frequency is near the edges of locking range ($\omega_0 \pm \omega_L$), the phase noise of free-running oscillator impacts more significant.

4.2.2 Sub-Feedback Technique

In order to increase the speed of eight-phase ring oscillator, additional inverters in the sub-feedback loop are used to construct fast loop in long chain ring oscillator [11] [12]. Fig. 4.19(a) demonstrates the general block diagram of ring oscillator which has n stages with sub-feedback loops. Here define i as the *feedback index* and it represents the number of stages in each sub-feedback loop.

The fundamental theory of increasing operating frequency by sub-feedback loop can be illustrated from the transfer function $H(j\omega)$ of the single stage shown in Fig. 4.19(b). g_m represents the transconductance of the transistors in the main loop, and G_m is for the sub-feedback loop. In addition, define θ as the phase difference between two adjacent nodes, and ϕ as the phase difference between nodes X_n and X_{n+i-1} ($\phi = (i-1)\theta$). The transfer function can be written as

$$H(j\omega) = \frac{V_n}{V_{n-1}} = \frac{-g_m R}{(1 + G_m R\cos\phi) + j(\omega RC - G_m R\sin\phi)}. \tag{4.19}$$

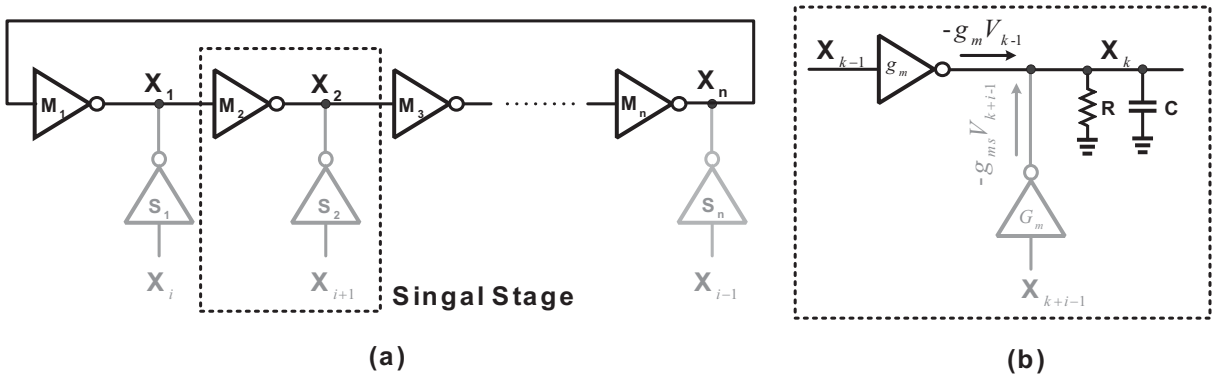


Figure 4.19: (a)General block diagram of sub-feedback ring oscillator, (b)Single stage equivalent circuit.

According to Barkhausen criterion, an oscillator can oscillate when it has at least unity gain and phase shift of 2π or $2n\pi$ where n is integer. When this oscillator achieves the minimum required gain, Eq. (4.19) can be written as

$$\begin{aligned} g_m R &= \sqrt{(1+G_m R\cos\phi)^2 + (\omega_0 RC - G_m R\sin\phi)^2} \\ &= \left|\frac{(1+G_m R\cos\phi)}{cos\theta}\right|, \end{aligned} \tag{4.20}$$

and the operating frequency can be indicated as

$$\begin{aligned} \omega_0 &= \left[G_m R\sin\phi + \tan\theta\,(1+G_m R\cos\phi)\right]/RC \\ &= \tan\theta/RC + k_0 G_m/C \end{aligned} \tag{4.21}$$

where

$$k_0 = \sin\left[(i-1)\theta\right] + \tan\theta\cdot\cos\left[(i-1)\theta\right]. \tag{4.22}$$

$\tan\theta/RC$ represents the original operating frequency of a ring oscillator without sub-feedback loops. Change the values of k_0 and G_m to decide the operating frequency finally. From the definition of k_0, when i is odd, k_0 is positive, and if i is even, k_0 is negative. Therefore, only as i is odd, the frequency can increase. In order to implement eight-phase generator, four differential stages ring oscillator with $i = 3$ are used. The circuit is depicted in Fig. 4.17 in detail.

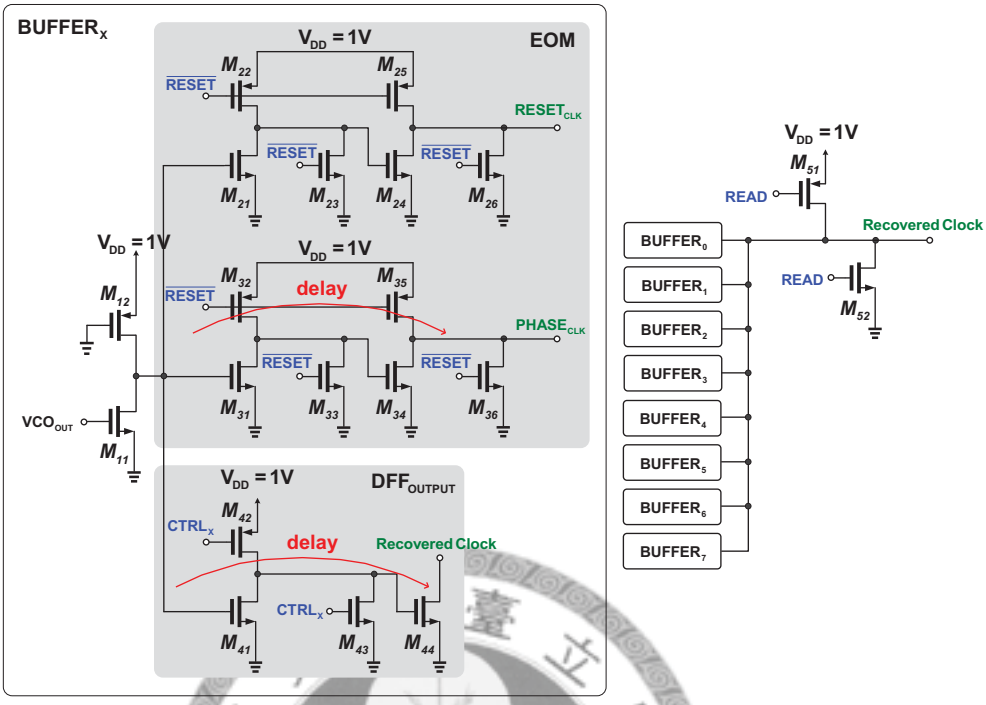


Figure 4.20: Buffer of the ring oscillator.

4.2.3 Buffer

Eight phase clocks supply to the EOM and output D flip-flop to recover data. For the reason to save power, turn off the buffers when the clocks do not be used. Therefore, there should be switches to control buffers. The buffer of every phase clock is demonstrated in Fig. 4.20. The clock buffer supplied to EOM can be turned off by $\overline{\text{RESET}} = 1$ after the EOM has selected a proper phase clock to sample data. Moreover, the clock buffer for output D flip-flop turns off as READ = 1 when the EOM is operating.

4.3 Decision Circuit

When the sampling phase clock has been selected by the EOM, a decision circuit is demanded here to recover data. It is composed of delay and a d flip-flop. The block diagram of decision circuit is depicted in Fig. 4.21. In this diagram, the recovered clock comes from Fig. 4.20, and has identical delay with those clocks, $\text{PHASE}_{\text{CLK}}$ and $\text{RESET}_{\text{CLK}}$, importing into the EOM.

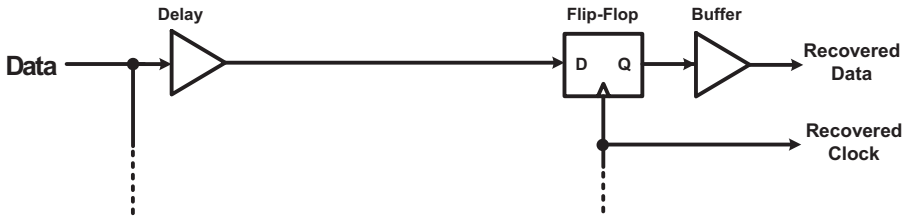


Figure 4.21: Block diagram of delay dummy and D flip-flop.

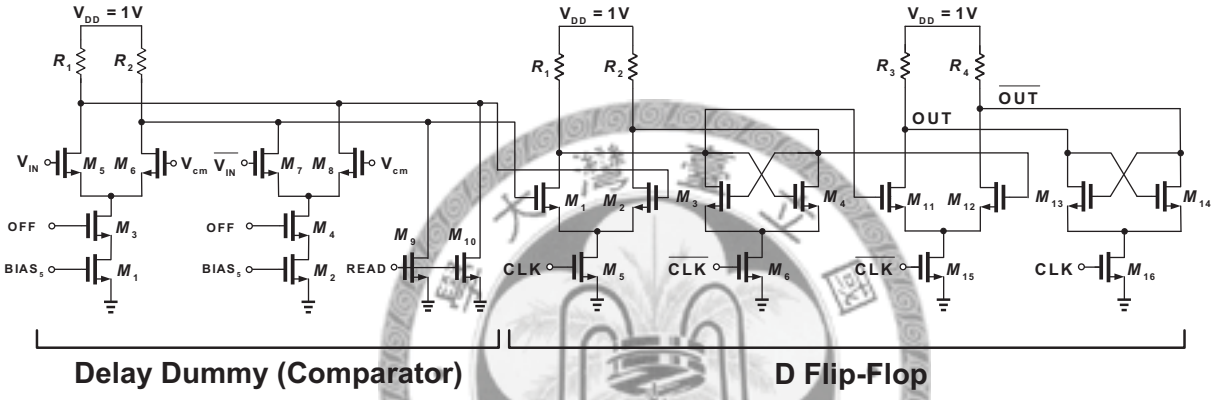


Figure 4.22: Schematics of the delay dummy and D flip-flop.

Additionally, it can be seen in Fig. 4.2 that before the data is sampled by clock, it goes through a comparator and has a time delay. Because the delay of the clocks importing the D flip-flop and the data samplers of EOM are equal, a delay dummy is needed before data reaching the output D flip-flop. This dummy generates an identical delay with the comparator of the data sampler in EOM.

The schematics of delay dummy and D flip-flop are shown in Fig. 4.22. The delay dummy is similar to the comparator of data sampler. The only difference is that the compared voltage is V_{cm} in spite of $V_{REF,H}$ and $V_{REF,L}$. When the EOM has selected the optimal sampling phase clock, READ is disable, and this delay dummy is switched on. At the same time, recovered clock from Fig. 4.20 is also generated because of READ = 0. Finally, the D flip-flop can recover data with selected sampling clock.

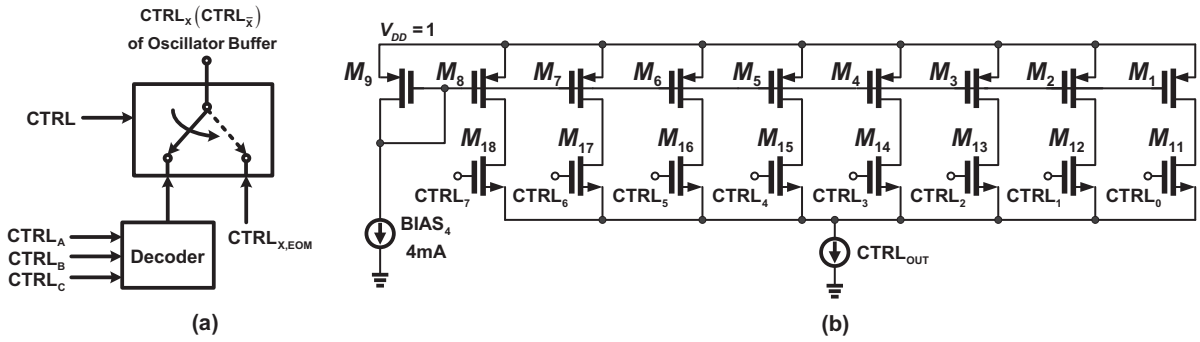


Figure 4.23: (a)External controller and (b)phase detector for testing.

4.4 Testing Circuit

For the purpose of checking the performance of recovering data with every phase clock, include an external controller with a three-to-eight decoder to control the clocks. This controller is only composed by logic gates and MOS switches. Therefore, the detailed circuit is not shown here and just the block diagram depicted in Fig. 4.23(a). It can decide which phase of clocks to sample data by external control signals, $\mathrm{CTRL_A}$, $\mathrm{CTRL_B}$ and $\mathrm{CTRL_C}$, or by the EOM, $\mathrm{CTRL_{X,EOM}}$. When CTRL = 1, the clock used to recover data is determined by external signals. On the other hand, the clock is selected by the control signals from the EOM at CTRL = 0.

Except the controller mentioned above, a circuit is designed to detect which phase of clocks is selected. The circuit is illustrated in Fig. 4.23(b). When various phase of clocks is selected, different $\mathrm{CTRL_X}$ is changed to high and the output current, $\mathrm{CTRL_{OUT}}$, alters, owing to the various size of the current mirror transistor. The width ratio of transistors in Fig. 4.23(b) can be depicted in Eq. (4.23).

$$M_9 : M_8 : M_7 : M_6 : M_5 : M_4 : M_3 : M_2 : M_1 = 8 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1. \quad (4.23)$$

4.5 Simulation Results

In this section, summarize the performance of each block in this eye-opening monitor CDR. Furthermore, the performance listed here are all post-simulation results.

4.5.1 Multiphase Generator

The performance of oscillator is listed in Table 4.1. The power consumption includes the buffers of oscillator in Fig. 4.20. When the EOM is turned off, the buffers generating $\text{RESET}_{\text{CLK}}$ and $\text{PHASE}_{\text{CLK}}$ are shut down, and the buffers producing DFF_{CLK} are switched on. Therefore, the power consumption is lower at EOM in OFF mode.

		SS Corner	TT Corner	FF Corner
Tuning Range (GHz)		7.9 -11.5	8.8 -13.4	12 -16.4
Power Consumption (mW)	ON	74	90	113
	OFF	40	50	63

Table 4.1: Performance summary of ring oscillator

Fig. 4.24 demonstrates the spectrum of ring oscillator. It respectively shows the spectrum of free-running oscillator and injection-locked oscillator. Here the oscillator is locked at 13GHz.

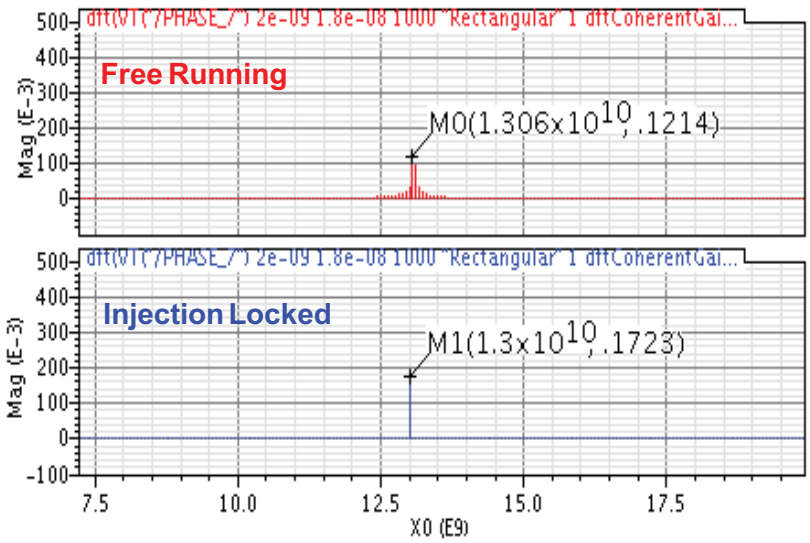


Figure 4.24: Spectrum of oscillator in free-running and injection-locked situation.

Additionally, the simulation result of eight phase clocks are in Fig. 4.25. From this

figure, the amplitude of various phase and the time interval between two neighbor clocks are not identical, but these do not impact the operation of this EOM CDR. The clock amplitude is only required large enough to sample data. Furthermore, in this circuit, the eye-opening monitor can select one of the eight phase clocks to recover data with demanded BER. Therefore, the various time interval between two neighbor clocks does not the matter.

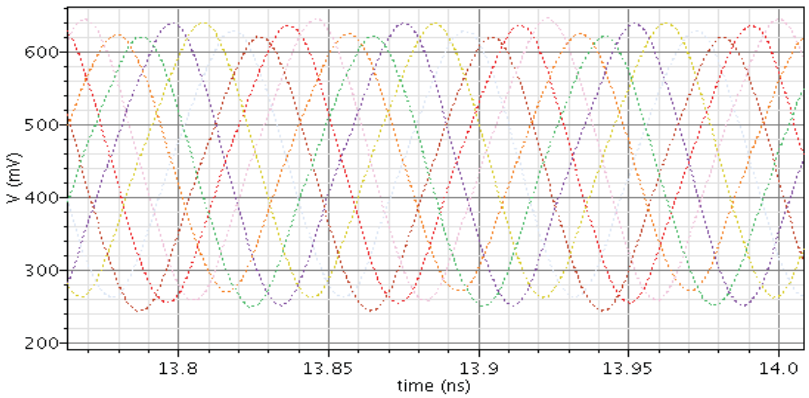


Figure 4.25: Eight phase clocks in time domain.

4.5.2 Eye-Opening Monitor CDR

In this simulation, the input data is 200mV (peak-to-peak) and the dc level is 0.6V. Additionally, various length models of FR-4 channel are added for simulating real situation. When the EOM has selected and stored one sampling phase clock to recover data, the EOM should be turned off to save power, and CDR outputs recovered data and clock. The power consumption of this EOM CDR is listed in Table 4.2.

The recovered clock and data are depicted in Fig. 4.26. From this figure, it can be seen that after EOM is reset and starts operating, it needs about 16 cycles to select appropriate sampling clock. When the sampling phase clock has been chosen and stored, recovered data and clock are outputted. In addition, one index of the performance of the CDR is the eye diagram of recovered data. When received data passes through 15cm FR-4 channel, the eye diagram of the recovered data in this CDR is shown in Fig. 4.27.

	Power Consumption (mW)					
	SS Corner		TT Corner		FF Corner	
	ON	OFF	ON	OFF	ON	OFF
Eye-Opening Monitor	198	10	239	11	273	12
Multiphase Generator & CDR	70	48	88	60	114	75
Buffer	33		40		50	
Total Power (w/o Buffer)	268	58	327	71	387	87

Table 4.2: Power consumption of this EOM CDR.

This figure also shows the eye diagrams of the CDR which is operating in various corner at 10GHz. The jitter can achieve about 2 ps (peak-to-peak) in TT corner.

In TT corner, the eye diagrams of received data and recovered data in various length channels are demonstrated in Fig. 4.28. This EOM CDR can recover input data up to 30cm FR-4 board.

4.6 Layout

The total area of this EOM CDR is 1*1.16mm^2. The layout and the paths of signals are demonstrated in Fig. 4.29.

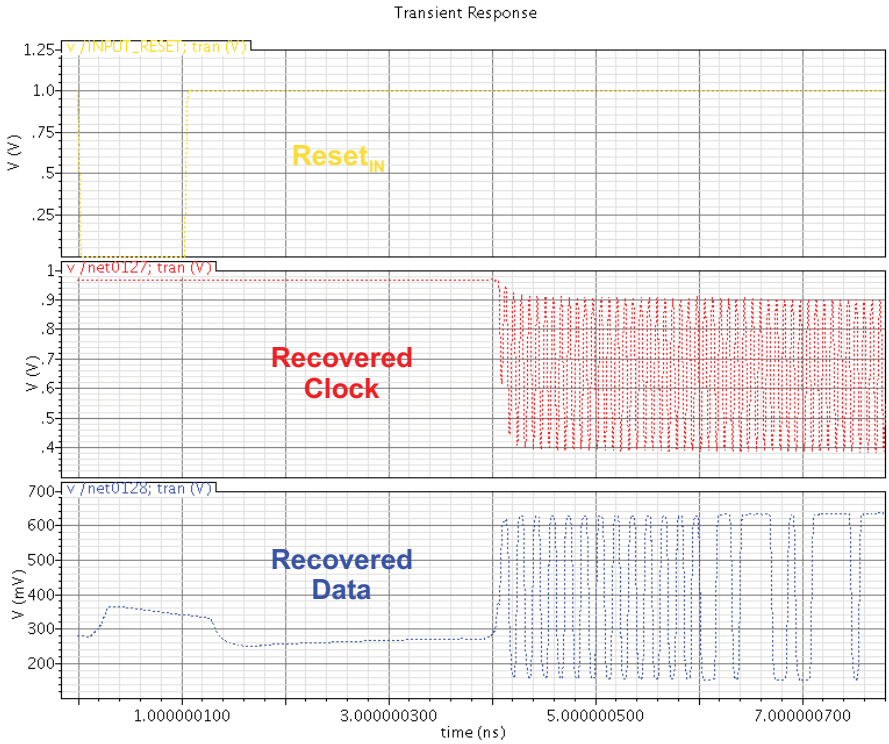


Figure 4.26: Recovered clock and data.

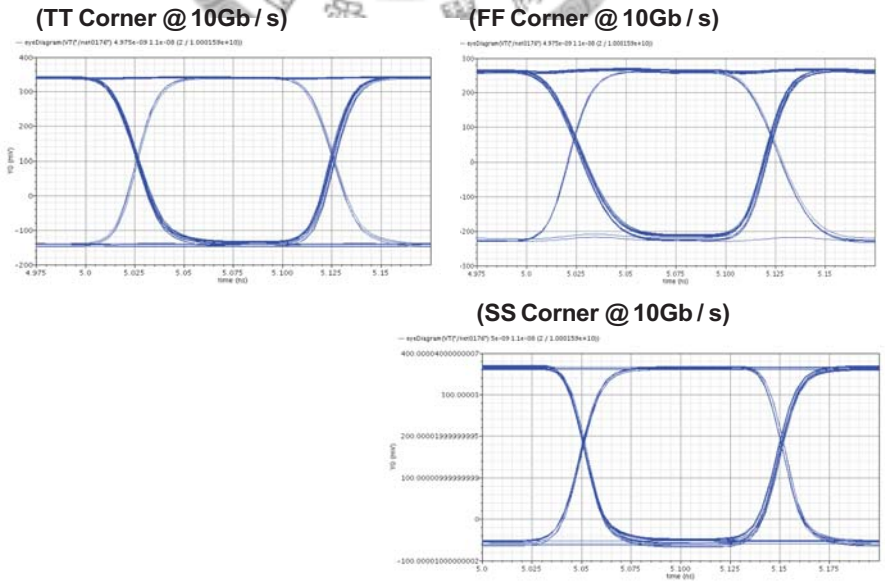


Figure 4.27: Eye diagram of the EOM CDR.

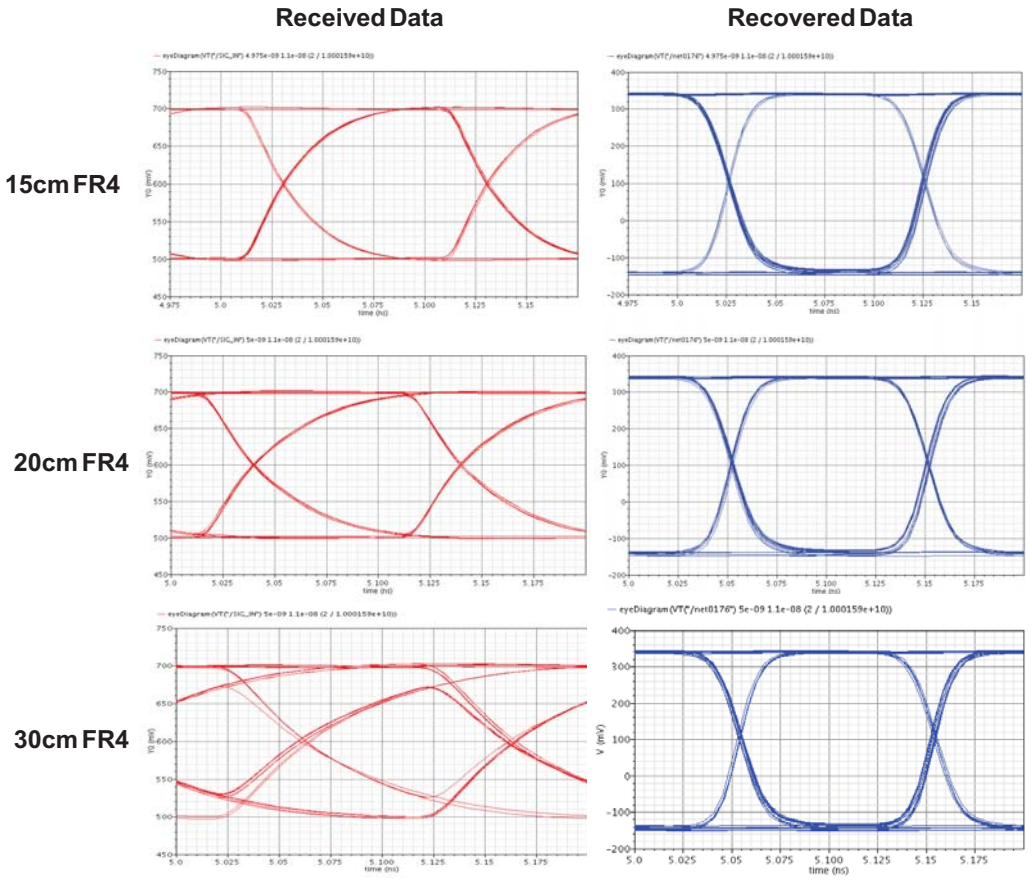


Figure 4.28: Eye diagram of the received data and recovered data.

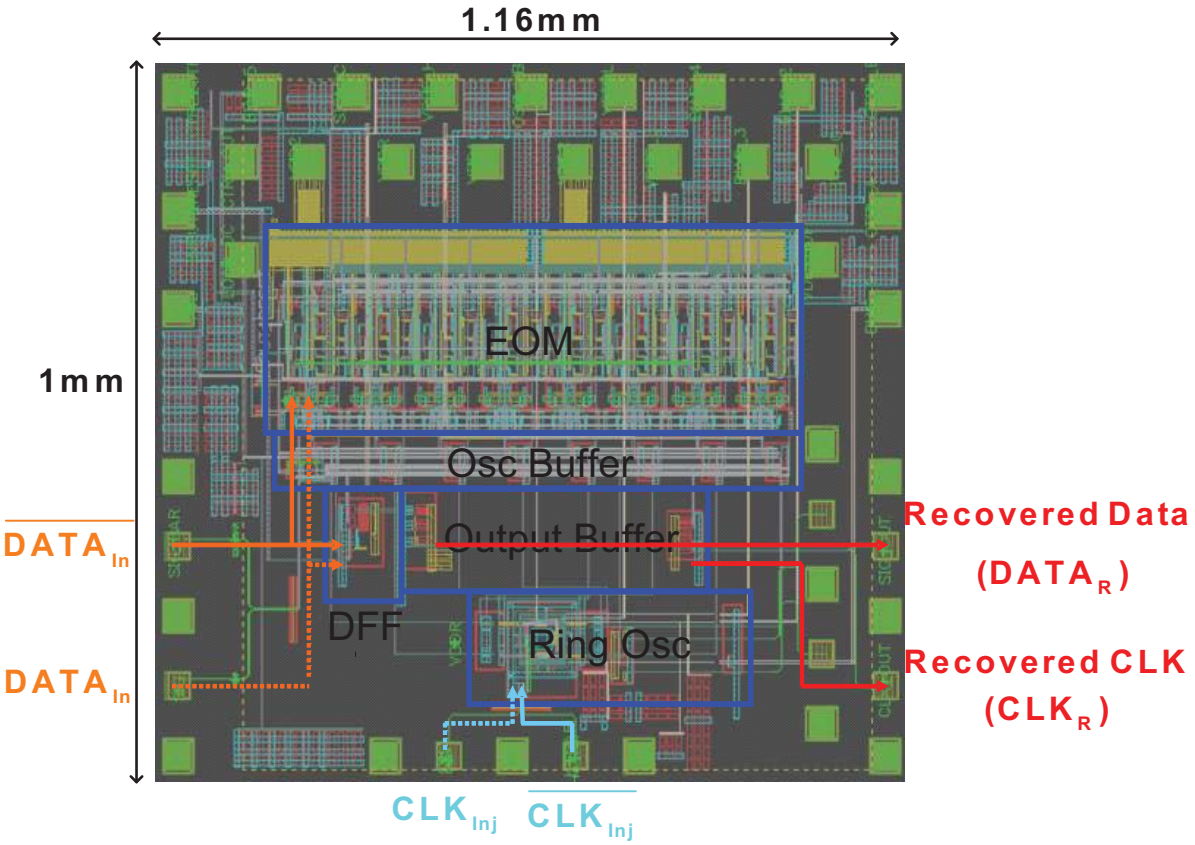


Figure 4.29: Layout of the EOM CDR.

Chapter 5

Experiment Results

5.1 Testing Environment

In this thesis, the eye-opening monitor CDR circuit has been designed and fabricated in 90nm CMOS technology. The settings of testing environment are described in this section. Fig. 5.1 shows the die photo of this circuit. The CDR core occupies $0.7^{*}0.8\text{mm}^2$. The signals including differential input data (DATA_{In} and $\overline{\text{DATA}_{\text{In}}}$), differential injecting clock (CLK_{Inj} and $\overline{\text{CLK}_{\text{Inj}}}$), recovered data ($\text{DATA}_{\text{R}}$) and recovered clock ($\text{CLK}_{\text{R}}$) are all probed on wafer to import and get signals. The DC supply, bias and control voltage are located on the top of this chip and fed through printed circuit board (PCB) and bonding wires.

Testing setup is illustrated in Fig. 5.2. Rohde & Schwarz FSUP signal source analyzer is used to measure the spectrum and phase noise of recovered clock. Agilent J-BERT N4903A is used to generate PRBS input data and injecting clock. Additionally, it receives recovered data and clock to compute the bit error rate of this CDR circuit. There are two oscilloscopes demanded here. Agilent 86100C measures the eye diagram of recovered data, and Tektronix TDS6604 is used to detect the time domain signal of received data.

In the next sections, the performance of multiphase generator is measured first, and then test the function of the EOM CDR circuit.

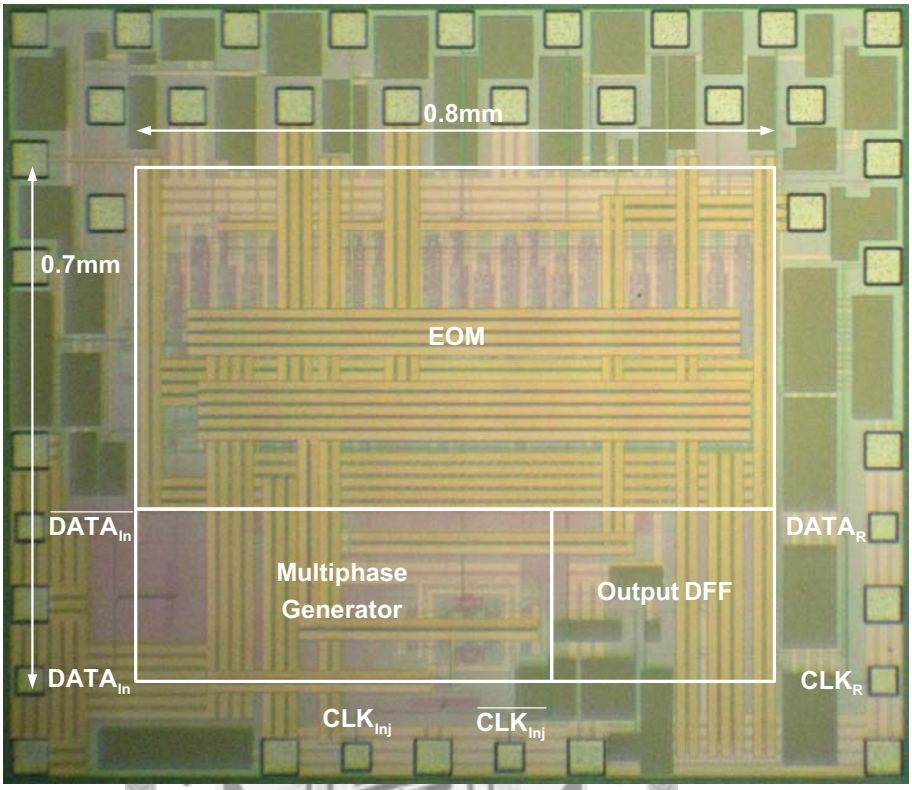


Figure 5.1: Die micrograph.

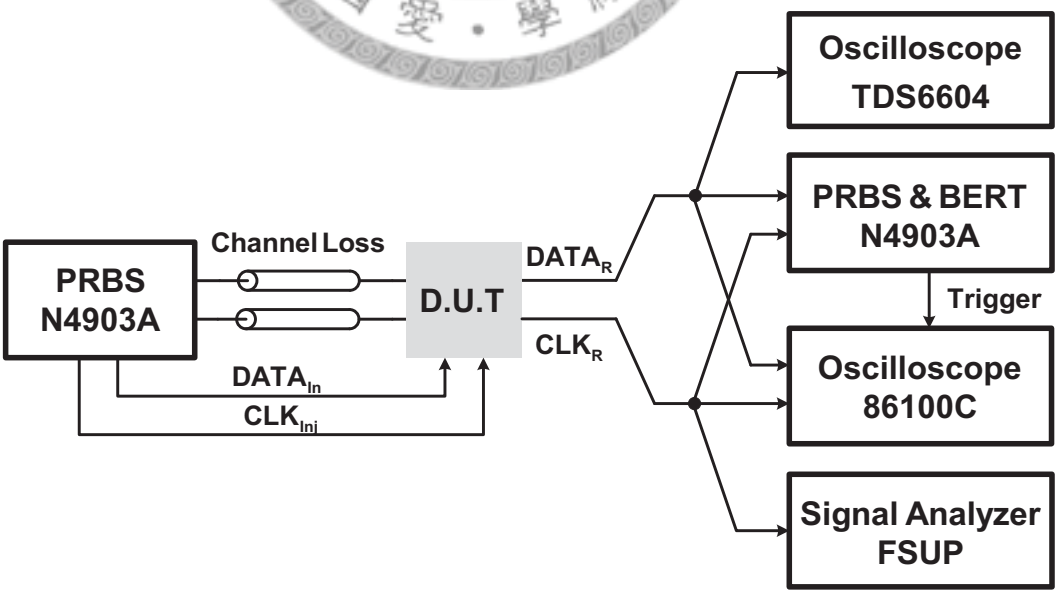


Figure 5.2: Testing setup.

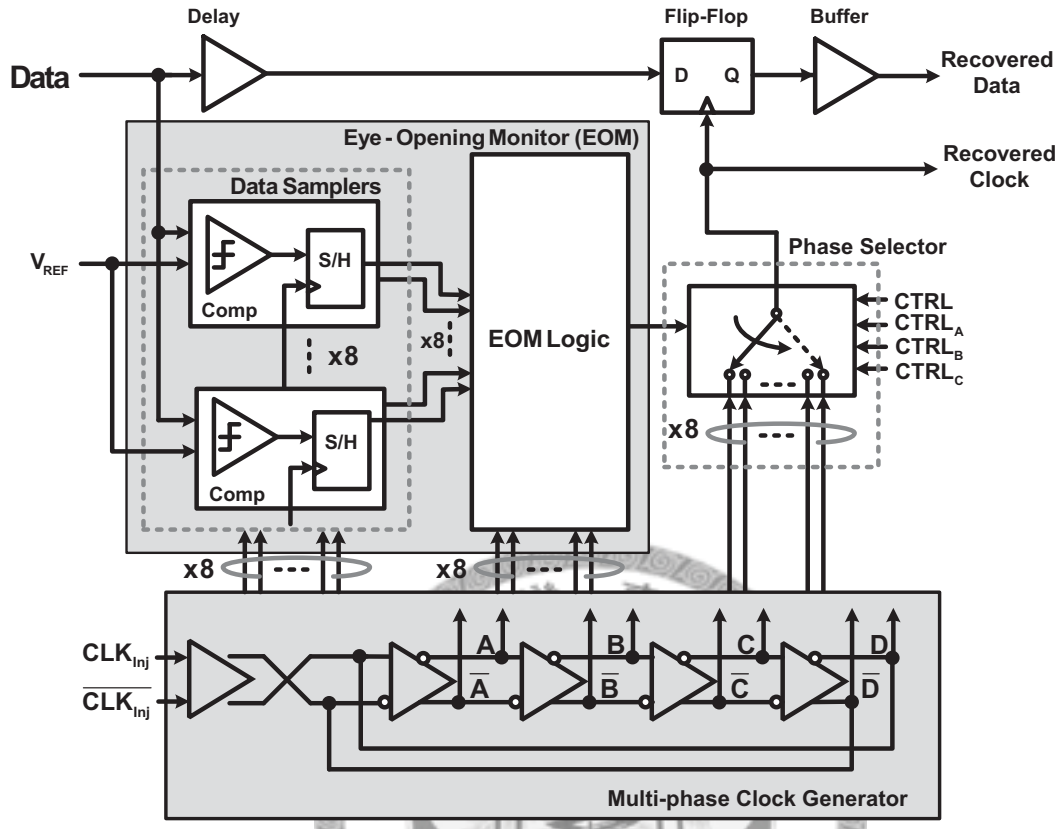


Figure 5.3: Block diagram of the EOM CDR.

5.2 Multiphase Generator

In this measurement, the EOM is turned off, and only the multiphase generator, phase selector and output D flip-flop are operating. Because it can be controlled by $CTRL_A$, $CTRL_B$ and $CTRL_C$ in Fig. 5.3 to decide which phase is used to recover data and as recovered clock, the performance of the multiphase generator can be measured from the recovered clock.

Although this multiphase generator can operate at about 12GHz, the EOM CDR can only achieve 9Gb/s. Therefore, the measured result here is mainly at 8GHz and 9GHz. The measured spectra of free running and injected situation are demonstrated in Fig. 5.4, and the phase noise is depicted in Fig. 5.5.

From the measurement of phase noise, it can be seen that phase noise is suppressed under -110dBc/Hz at 1MHz offset by injection locking technique. In addition, rms jitter

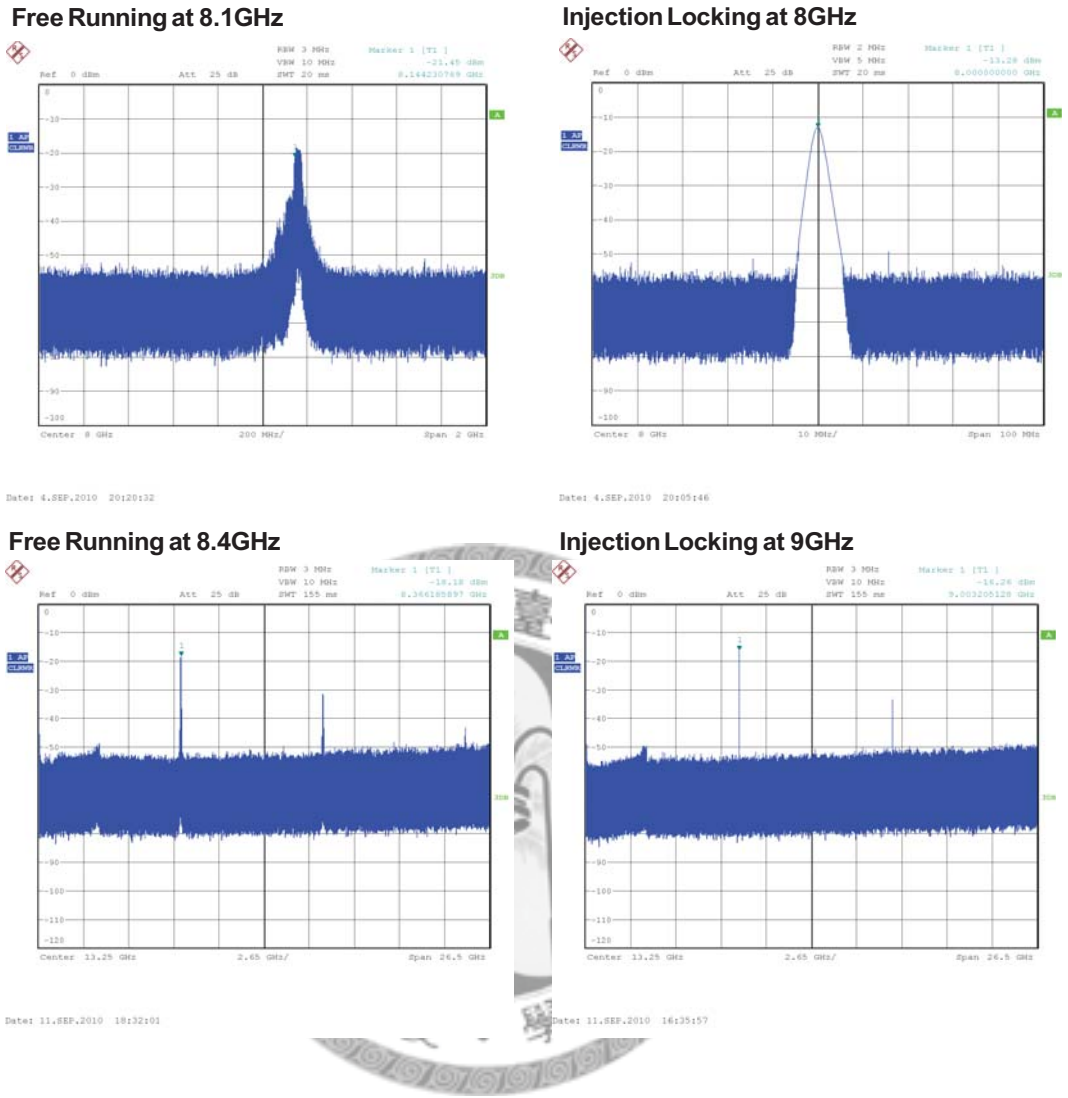


Figure 5.4: Spectra of free running and injection locking clock at 8GHz and 9GHz.

is also effectively decreased by injection locking technique from 2ns to 0.07ps at 8GHz, and from 23ps to 1.5ps at 9GHz. Finally, Table 5.1 shows the performance summary of this multiphase generator.

5.3 Eye-Opening Monitor CDR

This EOM CDR is designed to select appropriate sampling phase clock quickly and output recovered data. Fig. 5.6 demonstrates the timing diagram of the recovered data. The EOM is operated at 8Gb/s and turned on at t=0. From this figure, the EOM CDR spends about 2ns (16 cycles) to choose sampling clock, and this is identical with the

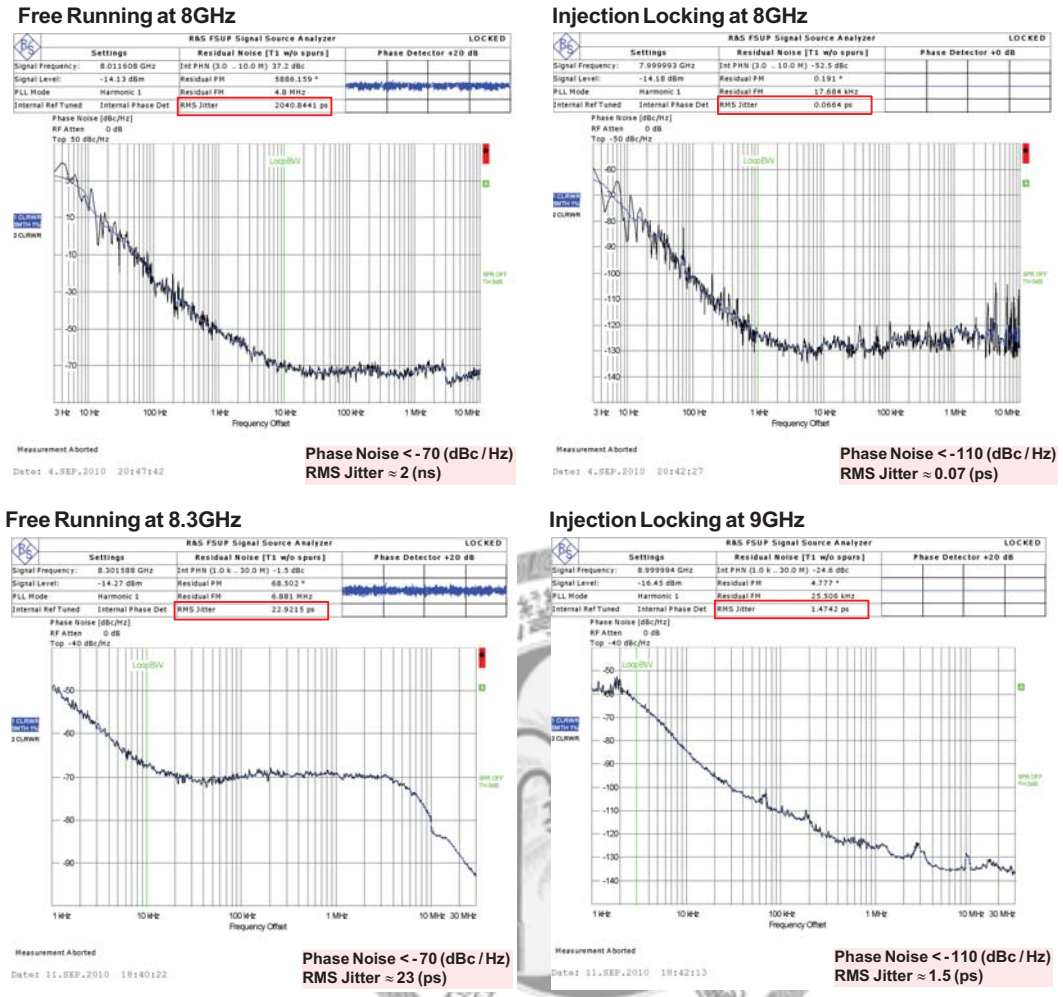


Figure 5.5: Phase noise of free running and injection locking clock at 8GHz and 9GHz.

simulation result.

As input data is 8Gb/s and ideal (without channel loss), the eye diagram and BER of the recovered data is in Fig. 5.7. In order to accomplish the BER measurement of received data, the close loops of the EOM is disabled and the sampling phase clock is selected by external control lines. The jitter(rms) of recovered data is only 1.4ps when the received data is 200mV (peak-to-peak) and PRBS $= 2^{31} - 1$.

For simulating undesirable factors, let the input data passing through various length channels on standard FR4 substrate. Because the channel has bandwidth limitation and loss, the input data seems to be disturbed by noise and ISI. The characteristics of these channels are measured and demonstrated in Fig. 5.8. In this figure, the gain at

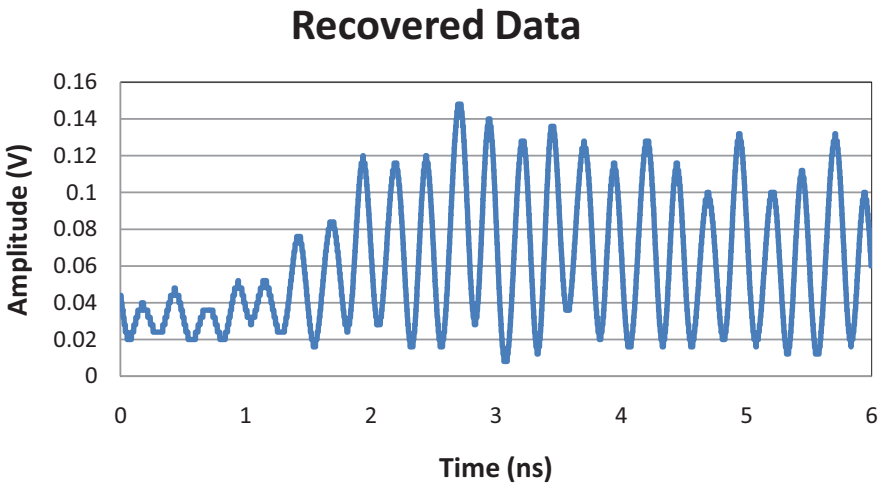


Figure 5.6: Timing diagram of the recovered data.

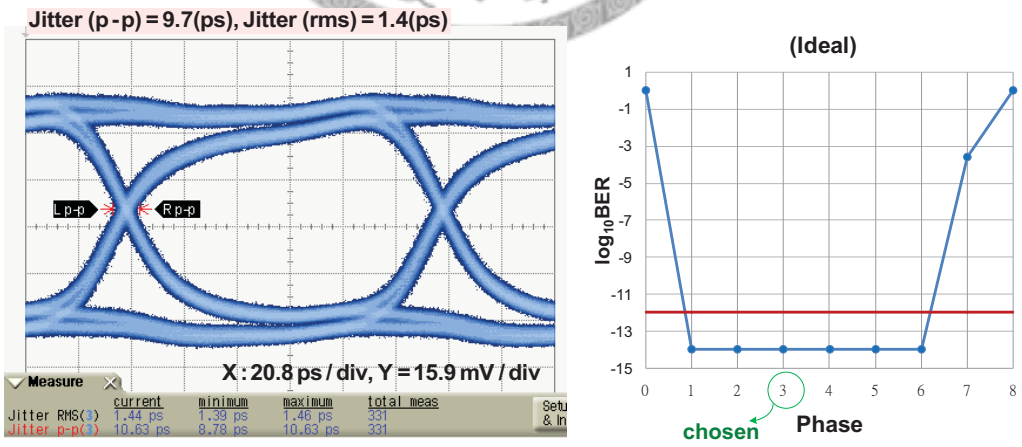


Figure 5.7: Eye diagram and BER of received data.

		SS Corner	TT Corner	FF Corner	This Work Measurement
Tuning Range (GHz)		7.9 -11.5	8.8 -13.4	12 -16.4	7.2-12.3
Power Consumption (mW)	ON	70	88	114	70
	OFF	48	60	75	49
Phase Noise (dBc/Hz)	FREE	-61	-67	-	-71
	INJ	-111.3	-118.1	-115.6	< -110

Table 5.1: Performance summary of this multiphase generator.

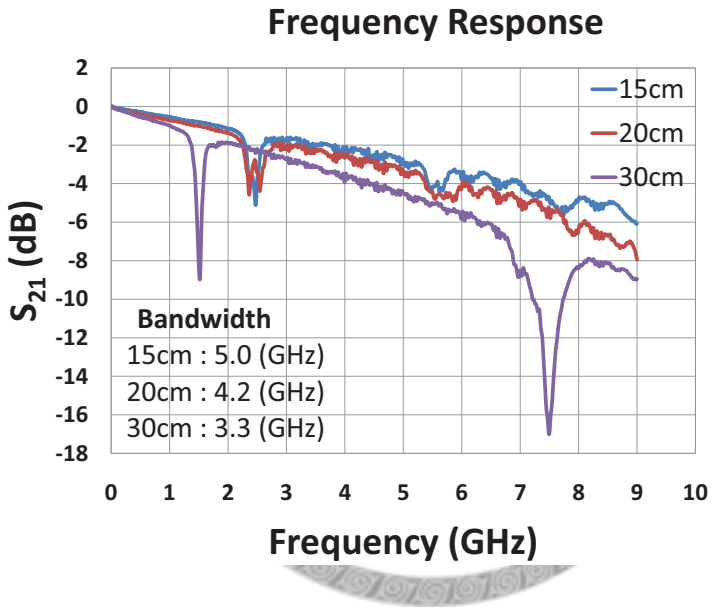


Figure 5.8: Characteristics of various length channels.

some frequency is particularly small. This is because the channel is not perfect 50Ohm matching there.

In order to evidence that this EOM CDR can select sampling phase clock at the position with low BER, the closed loops of this EOM CDR are first disabled and the BER of recovered data with each sampling phase clock can be obtained by manually selecting phase clock from external control lines. The bathtub BER measurements for different channels are depicted in Fig. 5.9.

When the EOM is turned on and with no external control, it performs automatic phase selection. Fig. 5.10 shows the measured eye diagrams of received data and recov-

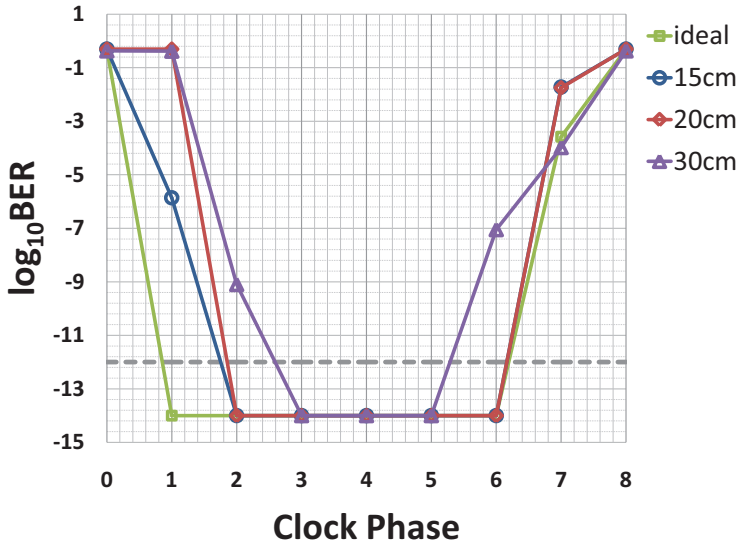


Figure 5.9: BER of the data recovered by various sampling clocks in different channels.

ered data for the 15cm, 20cm and 30cm differential FR-4 lines while the sampling phase clock is selected automatically by EOM. The input data here is 200mV(peak-to-peak) and PRBS $= 2^{31} - 1$.

For 30cm FR4 channel, the recovered data with phase 3 to phase 5 has low BER, and these phase clocks are all appropriate for phase selection. As the EOM is turned on and with no external control, the EOM automatically selects phase 4 clock to recover data. From the bathtub BER measurement in Fig. 5.9 and the result of automatic phase selection by the EOM CDR in Fig. 5.10, the performance of this EOM CDR circuit is evidenced.

Furthermore, the highest operating speed which this EOM CDR can achieve is 9Gb/s. The eye diagrams of received data and recovered data passing through 15cm channel at 9Gb/s are shown in Fig. 5.11.

Without any pre-equalizer or pre-emphasis circuit, this EOM CDR can recover 8Gb/s data up to 30cm FR4 channel with BER $< 10^{-12}$. That is, the architecture can determine the appropriate sampling position and recover the data properly. Therefore, it can relax the bandwidth and group delay requirements of the receiver front-end circuits in the high-speed serial links. The measured performance is summarized in Table 5.2, and Table 5.3 lists the comparison of this EOM CDR with other references.

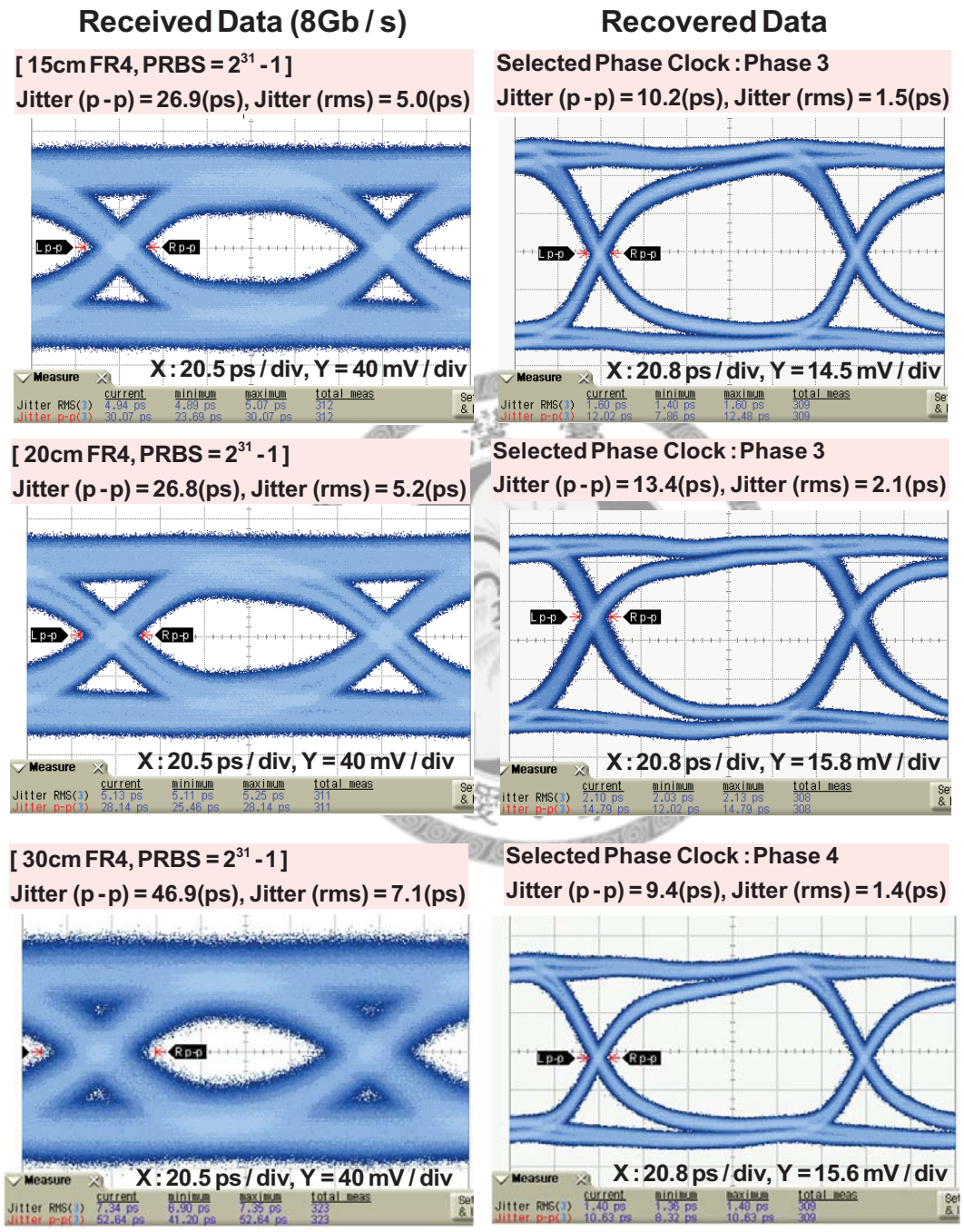


Figure 5.10: Eye diagram of received data and recovered data at 8Gb/s.

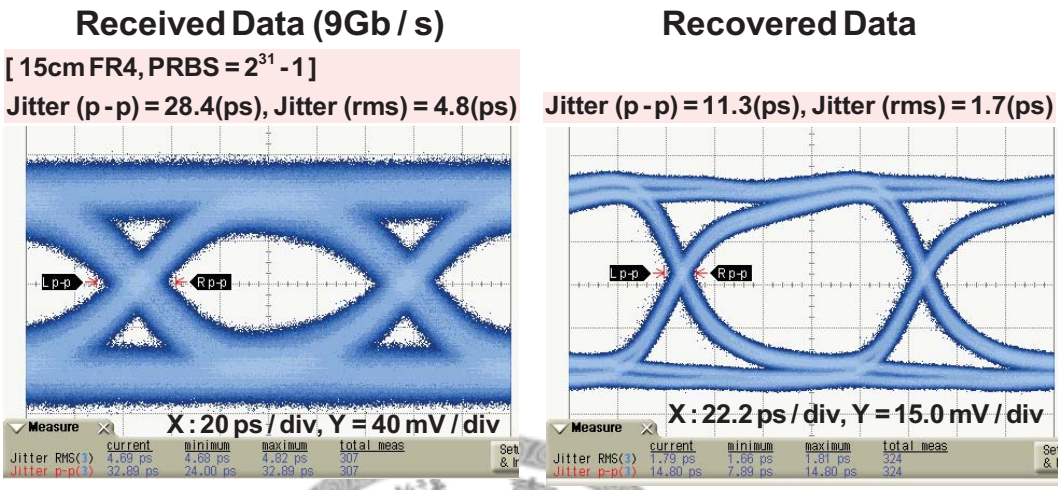


Figure 5.11: Eye diagram of received data and recovered data at 9Gb/s.

Data Rate	8Gb/s		
Input Power	200 mV_{pp}		
Locking Time	< 400 bits		
Jitter (rms)	< 2 ps		
BER (2^{31}-1 PRBS)	15cm FR4 , 20cm FR4 , 30cm FR4		
	< 10^{-12}		
Power (mW)		EOM ON	EOM OFF
	EOM	184	12
	Multiphase Generator	70	49
	Total Power (w/o buffer)	254	61
Supply Voltage	1V		
Area	0.7 × 0.8 mm^2		
Technology	90nm GP CMOS		

Table 5.2: Performance summary of measurement.

	Process	Data Rate (Gb/s)	Power Supply (V)	Power Consumption (mW)	Jitter (ps)	FR-4 Length (inch)	Area (mm^2)
2007, JSSC Razavi [13]	0.13 μm CMOS	10	1.6	133	--	☆24	0.94*0.65
2007, RFIC [14]	0.18 μm CMOS	10	1.5	290 (w/i buffers)	◇0.74 (rms)	★9	2.0*2.0
2007, CICC [15]	0.13 μm CMOS	10	1.2	164	--	☆12 30	0.39*0.39
*2008, JSSC NEC [16]	0.18 μm SiGe BiCMOS	40	3.3	1600	0.189(rms)	--	2.0*2.5
This Work	90nm CMOS	8	1	(ON) 254 (OFF) 61	▲9.7 (p-p) 1.4 (rms)	★12	0.7*0.8

* Use eye-opening monitor , but calculate with PC.

△ 2^7-1 PRBS, ◇ 2^{15}-1 PRBS, ▲ 2^{31}-1 PRBS

☆ with equalizer, ★ without equalizer

Table 5.3: Comparison of this EOM CDR circuit with others.

Chapter 6

Conclusion

Clock and data recovery (CDR) is a critical component in the receiver end of wired communication system. Because the clock is not transmitted directly, the timing information should be acquired from the received data to allow synchronous operations. Moreover, the data received in the receiver is noisy, so the data should be sampled again to eliminate the noise. Hence, CDR is demanded to recover data and clock, and the received data can be read precisely.

In traditional CDR, the optimal sampling position is always assumed at the middle of input signal and all CDR circuits attempt to recover data at this position. Nevertheless, when data is transmitted, it is impacted by some factors such as noise or ISI phenomenon. An equalizer is demanded to compensate the received data in the receiver. If utilize conventional CDR, the equalizer should extend the bandwidth to 0.7 data rate at least. This is because the sampling position is fixed at the middle of received data in typical CDR. This thesis proposes an eye-opening monitor CDR based on oversampling CDR to eliminate this drawback. No matter how much gain the equalizer can compensate, the EOM CDR can adjust sampling position according to various input data and recover data at the position with low bit error rate. Hence, the requirement of equalizer is reduced and not so strict as that in employing conventional CDR.

This proposed EOM CDR can adjust sampling position according to various input data, and is realized in 90nm CMOS. The core circuits occupy $0.7^{*}0.8mm^{2}$ of die area. The eight phase generator using ring oscillator and injection technology consumes 50mW from a 1V supply. In addition, the measured integrated rms jitter of clock for the

8GHz output is only 0.07ps. The EOM CDR circuit consumes 254mW when the EOM technique is operating, and only dissipates 61mW while the optimal phase clock is selected and the EOM logics are disabled. Furthermore, the CDR performance with non-ideal input data pattern of $2^{31} - 1$ PRBS all can be recovered with BER $< 10^{-12}$ at 8Gb/s in various lengths of FR-4 trace.

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