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master thesis

一個在切換頻率中利用電流平均控制來減低暫態漣波的控制方法之直流降壓式轉換器

A Current Average Control Method for Transient-Ripple Reduction in Frequency Hopping DC-DC Converters

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本論文係戴嘉南（r97943143）在國立臺灣大學電子所完成之碩士學位論文，於民國 100 年 1 月 26 日承下列考試委員審查通過及口試及格，特此證明

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A Current Average Control Method for Transient-Ripple Reduction in Frequency Hopping DC-DC Converters

By

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THESIS

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摘要

本論文闡述一個切換頻率中利用電流平均控制來減低暫態漣波控制方法的直流電壓轉換器，並以台積電0.35-μm 2P4M 3.3V/5V Mixed Signal CMOS製程製作。當使用切換頻率技術時，由於電感的電流連續性，使得切換頻率前和切換頻率後所產生的電感電流交流值不同，在輸出電容產生出一暫態漣波電壓，此論文提出一個如何控制電感電流才能使之無此暫態漣波電壓，其方式為利用延長或縮短充電(放電)電流的時間來達到平均電感電流，此時間為切換頻率前後充電(放電)電感電流時間的平均值，實現方式是利用額外電路準確計算此時間後，以脈衝的型式插入原本的脈衝調變訊號。

依據量測的結果，本晶片的切換頻率設定在880k-3.4MHz，暫態漣波在頻域上改進14.1dB，時域上改進88%。跳頻技巧最多可使EMI降低23.55dB，功率效率最高為90%。晶片總面積占2.126mm^2，而其它的量測結果也包含在本論文內。

Abstract

This thesis presents an inductor current average control method for transient-ripple reduction in frequency hopping DC-DC converters and is implemented in a standard 0.35-μm 2P4M 3.3V/5V Mixed Signal CMOS process. When using the frequency-hopping technique, there is transient ripple on the output voltage due to the difference of inductor current between two different frequencies. This thesis proposes a method which predicts the average inductor current and inserts a calculated-width pulse between two frequencies to reduce the transient ripple on the output voltage.

Measurement results are performed with the switching frequency of this chip operating between 0.88 MHz and 3.4 MHz. The transient ripple on the output voltage is reduced by 88% and the undesired spur is reduced by 14.1 dB. The frequency-hopping technique achieves 23.55 dB reduction of the EMI spur magnitude. The maximum power efficiency achieved 90%. The chip occupied 2.126 mm^2, and the other detailed measurements are included in this thesis.

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Chapter 1 Introduction

1.1 Motivation

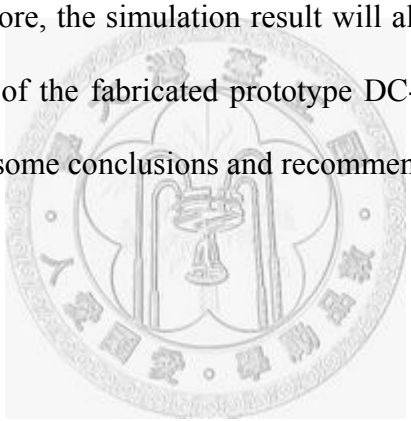
The electromagnetic interference (EMI) problem of switched-mode power supplies [1] has received more and more attention with the introduction of the international electromagnetic compatibility (EMC) directive. The control of the switched-mode power supplies is generally associated with the use of the pulse-width-modulation (PWM) technique. Several variable frequency (VF) methods have been proposed for EMI-reduction such as random switching frequencies [2]-[4], frequency hopping (FH) [5]-[6], sigma-delta modulation [7]. While using these VF methods, there is a latent problem that the inductor current ripple varies with different frequencies. This variation results in an undesired spur in the frequency spectrum and a transient ripple on the output voltage.

These variable frequency techniques are widely used in mobile systems where different spectrum-sensitive circuits such as communication ICs are major application. Further, reducing the size of the passive filter in power converter design becomes an important consideration because of these mobile systems and portable devices. Unfortunately, when the inductor of the passive filter in buck converters is decreased, the inductor current ripple increases. Therefore, the undesired spur must be taken into account. Even if it is utilized in baseband applications, the transient ripple on the output voltage is still undesired in a typical DC-DC converter. This thesis presents an inductor current average control (ICAC) method for transient-ripple reduction in frequency hopping DC-DC converters. By using this method, it reduces the undesired spur without

increasing the size of the passive filter.

1.2 Thesis Organization

This thesis is organized as six chapters. In Chapter 2, the fundamental specification and requirements of the DC-DC converters are investigated such that limitations and trades-offs for designing can be understood easily. In Chapter 3, the algorithm for the proposed technique in a PWM DC-DC buck converter using variable frequency technique will be demonstrated and the detailed operations will be introduced. For simplicity, use the frequency-hopping technique to represent the variable frequency technique. In Chapter 4, the design and analysis of the circuits in each building block will be described. Furthermore, the simulation result will also be presented. In Chapter 5, the measurement results of the fabricated prototype DC-DC buck converter will be presented. Chapter 6 offers some conclusions and recommendations for future work.



Chapter 2 Fundamental of DC-DC Buck Converter

2.1 Performance Metrics

2.1.1 Efficiency

The efficiency of DC-DC converters is an important topic in electronic system. In general, the DC-DC converter converts a dirty voltage and current into a clean voltage and current. Therefore, the regulator is equal to a medium in electronic system. Since it is only a medium, the power loss is as less as it can be. The less energy the DC-DC converter requires, the more energy can be obtained by the other main electronic circuits. If the DC-DC converter has low efficiency, not only power is wasted but also unnecessary heat is generated, which will increase unnecessary cost for cooling and decrease reliability.

The efficiency of a switched-mode DC-DC converter is defined as the ratio of the output power and input power as follows:

$$\eta = \frac{v_{OUT} \times i_{OUT}}{(V_{IN} \times i_{Quiescent}) + (R_{onp} \times i_P^2 + R_{onn} \times i_N^2) + P_{others} + (v_{OUT} \times i_{OUT})} \times 100\% \quad (2.1)$$

where the definition of V_{IN}, v_{OUT}, i_{OUT}, $i_{Quiescent}$, R_{onp}, R_{onn}, i_P and i_N are shown in Fig. 2.1. V_{IN} is the unregulated voltage and v_{OUT} is the regulated voltage. i_{IN} is the supply current and i_{OUT} is the load current. R_{onp}, i_P, R_{onn} and i_N are the on-resistance and current of power transistors M_P and M_N, respectively. $i_{Quiescent}$ is the current flowing into the feedback circuit. In the denominator, the first term $V_{IN} \times i_{Quiescent}$ means quiescent power consumption which is the power consumption in the chip when there is no output

current (open circuit). The second term $R_{onp} \times i_P^2 + R_{onn} \times i_N^2$ means power consumption in power transistors including conduction loss and switching loss, and the third term P_{others} means power consumption such as *I-V* overlap loss, current ripple loss and gate-driving loss. According to the above equation, the first term to the third term in denominator must be minimized to improve efficiency. Saving power consumption in feedback circuit decreases the value of the first term.

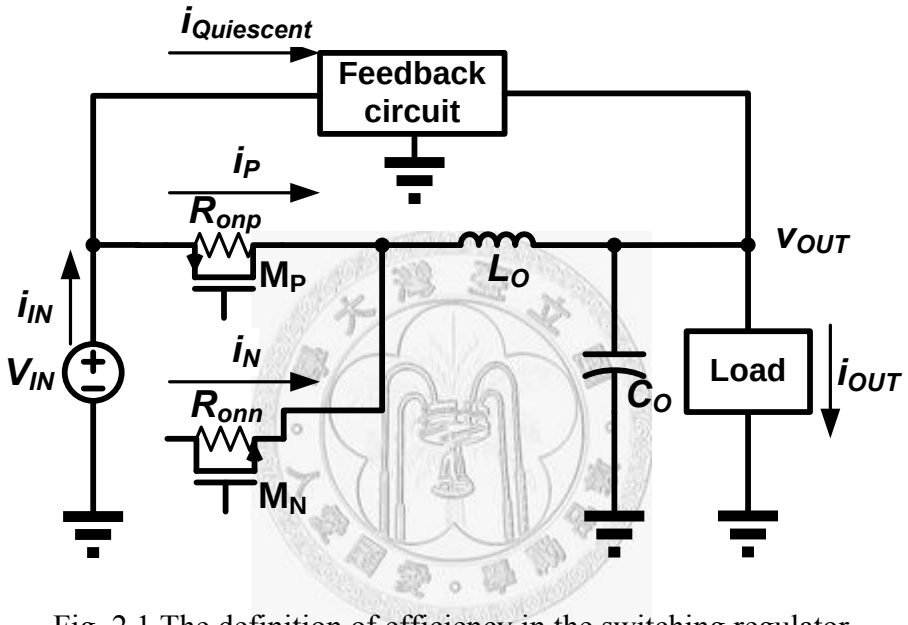


Fig. 2.1 The definition of efficiency in the switching regulator

2.1.2 Regulation

This is an index about influence of environment on the output voltage. It is the measurement of how close the output voltage stays to its nominal value over full range of operating conditions. In general, it is divided into three components: line, load, and temperature regulation [8].

2.1.2.1 Line Regulation

Line regulation is the effect the output voltage as varying the input voltage. There

are usually two methods to define line regulation. The first definition *line regulation* is percentage of changes in output voltage versus changes in input voltage. It is defined as

$$LNR = \left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)\Bigg|_{I_O=const} \left(\frac{\text{mV}}{\text{V}}\right) \tag{2.2}$$

The second definition *percentage line regulation* includes the parameter of output nominal voltage into the first definition. So its value is highly related to output dc voltage. It is defined as

$$PLNR = \left(\frac{\frac{\Delta V_{out}}{V_{out,nom}} \times 100\%}{\Delta V_{in}}\right)\Bigg|_{I_O=const} \left(\frac{\%}{\text{V}}\right) \tag{2.3}$$

2.1.2.2 Load Regulation

Load regulation is the percentage change in the steady state output voltage when the load current changes. There are usually two methods to define load regulation. The first definition *load regulation* is as

$$LOR = \left(\frac{\Delta V_{out}}{\Delta I_O}\right)\Bigg|_{V_{in}=const} \left(\frac{\text{mV}}{\text{A}}\right) \tag{2.4}$$

The second definition *percentage load regulation* includes the parameter of output nominal voltage into the first definition. So its value is highly related to output dc voltage. It is defined as

$$PLOR = \left(\frac{V_{out(\min L)} - V_{out(FL)}}{V_{O(FL)}}\right) \times 100\%\Bigg|_{V_{in}=const} (\%) \tag{2.5}$$

2.1.2.3 Temperature Regulation

Temperature Regulation is the effect of change in environmental temperature on the output voltage. The definition *thermal regulation* is as

$$THR \equiv \left. \frac{\frac{\Delta V_O}{V_{Onom}} \times 100\%}{\Delta P_D} \right|_{I_O=const \& V_{in}=const} \quad (\frac{\%}{\mathrm{W}}) \tag{2.6}$$

Although many factors influence regulation of output voltage, the DC-DC converter has feedback circuit to compensate for such changes and keep the output within specified limits.

2.1.3 Transient Response

Transient Response is defined as a variation of output voltage when load current suddenly changes from one level to another level. The output voltage drops when load current steps up or increases when load current steps down since the additional or insufficient current supplied from the output capacitor. The transient response is a function of the bandwidth of DC-DC converter, output inductor, output capacitor, equivalent series resistance (ESR) of output capacitor and the load current as shown in Fig. 2.2. In past, this parameter is often ignored in industry. But in present age of high speed electronic manufactures, this parameter is more and more important because most kinds of electronic manufacture need to supply a large number of current in few microseconds even in few nanoseconds. If the DC-DC converter does not keep its output voltage which is supplied to electronic manufactures not change drastically in a big variation of load current, it will highly affect performance of electronic manufactures.

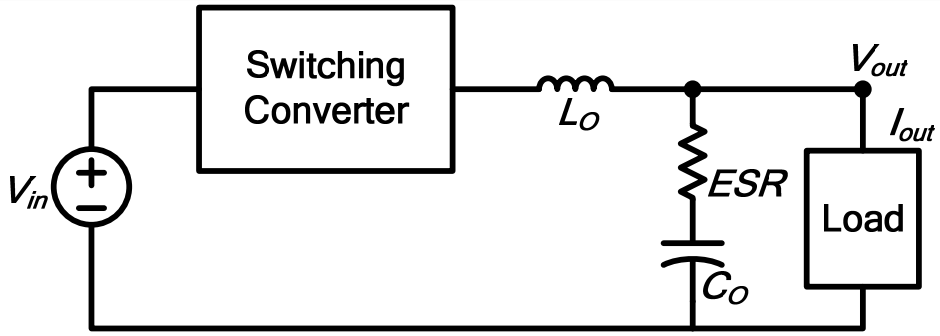


Fig. 2.2 Circuit diagram of the switching converter

Fig. 2.3 shows time characteristic of the transient response. During the time Δt_1, a large current is pulled from the load, the finite bandwidth of the switching converter is too slow to provide enough output current to the load. Therefore, the output capacitor must compensate the difference between switching converter current and load current. As a result, the voltage ΔV_1 can be calculated as

$$\Delta V_1 = \frac{\Delta I \times \Delta t_1}{C_O} + \Delta I \times ESR \tag{2.7}$$

The time period Δt_1 is mainly determined by the bandwidth of the switching converter. Besides, a large output capacitor will keep on providing charges to the load and holding output voltage without transient spur. The sum of Δt_1 and Δt_2 is the "Recovery Time" and it takes for the output to return within the specified regulation limits. ΔV_1 is "Deviation of Output Voltage" between two different load current ΔI. When the load steps down suddenly, the output voltage will jump. Before the inductor current is back to steady state, the excessive current charges the output capacitor. Therefore, ΔV_2 can be calculated as

$$\Delta V_2 = \frac{\Delta I \times \Delta t_3}{C_O} + \Delta I \times ESR \tag{2.8}$$

The length of the time period Δt_2 and Δt_4 is dependent on the time required for pass power transistors, M_P and M_N, in Fig. 2.1 to charge or discharge the output capacitor, and it is also dependent on the phase margin of the whole circuit loop.

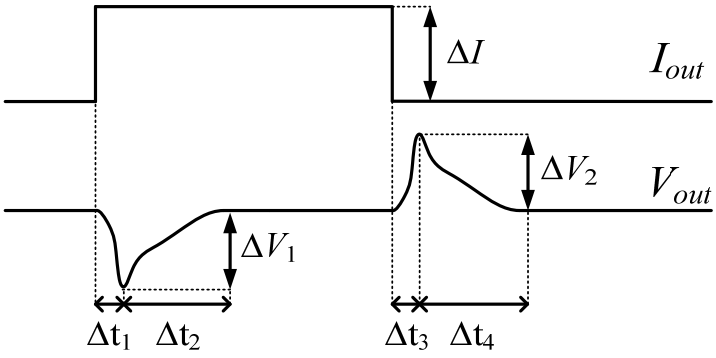


Fig. 2.3 The transient response of output voltage when a dynamic load is applied

2.2 Architecture of DC-DC Converters

A DC-DC converter is composed of a power stage and a feedback network. The power stage contains power transistors and an output filter. In the switched-mode DC-DC converter, the power stage contains power PMOS and NMOS transistors and the output filter which consists of an inductor *L* and a filtering capacitor *C*. Many feedback networks have been proposed and their goal in common is to provide a stable output voltage. These architectures will be discussed in detail as following.

2.2.1 DC-DC Buck Converter Operation

The buck converter, is a well-known converter that is capable of converting a higher voltage into a lower voltage. The switch produces a rectangular waveform $V_s(t)$ as illustrated in Fig. 2.4. The voltage of $V_s(t)$ is equal to the dc input voltage V_{IN} when the switch is in position 1, and is equal to zero when the switch is in position 2. In practical, the switch is realized using power semiconductor devices, such as transistors and diodes, which are controlled to turn on and turn off as required to perform the function of the ideal switch. The switching frequency f_{sw}, equals to the inverse of the

switching period T_s, generally lies in the range of 10 kHz to 10 MHz, depending on the switching speed of the semiconductor devices. The duty ratio D is the fraction of time that the switch spends in position 1, and is a number between zero and one. The complement of the duty ratio D' is defined as (1-D).

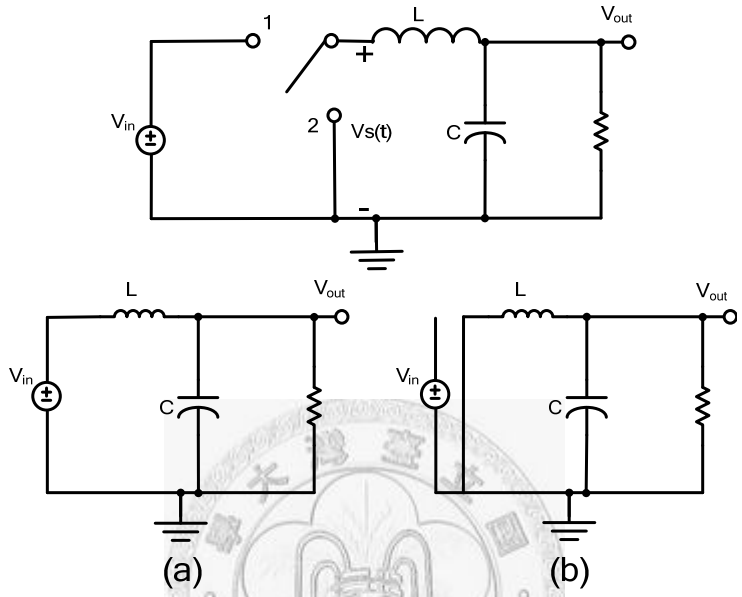


Fig. 2.4 Buck converter (a) the switch in 1 (b) the switch in 2

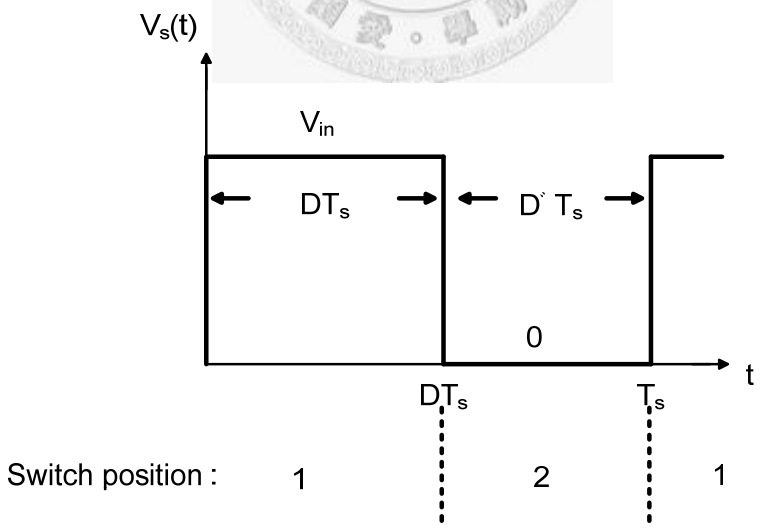


Fig. 2.5 Steady-state output waveform $V_s(t)$

The switch reduces the dc component of the voltage: the switch output voltage $V_s(t)$ has a dc component that is less than the converter dc input voltage V_{IN}. From Fourier analysis, we know that the dc component of $V_s(t)$, as shown in Fig. 2.5, is given by its

average value $\langle V_S \rangle$

$$\langle V_S \rangle = \frac{1}{T_S}\int_0^{T_S} V_S(t)dt = DV_{IN} \tag{2.9}$$

So the average value, or dc component, of $V_s(t)$ is equal to the duty cycle times the dc input voltage V_{IN}. The output voltage is reduced from the input voltage by a factor of D.

What remains is to insert a low-pass filter as shown in Fig. 2.4. The filter is designed to pass the average of $V_s(t)$ but reject the components of $V_s(t)$ at the switching frequency and its harmonics. The output voltage V_{out} is then essentially equal to the average of $V_s(t)$. Fig. 2.6 depicts the control characteristic of the converter and the buck converter has a linear control characteristic. Note that the output voltage is less than or equal to the input voltage, since $0 \leq D \leq 1$. Feedback systems are constructed to adjust the duty cycle D for regulating the converter output voltage. Inverters in digital controlled or error amplifiers in analog controlled could be built, in which the duty cycle varies slowly with time depending on feedback bandwidth.

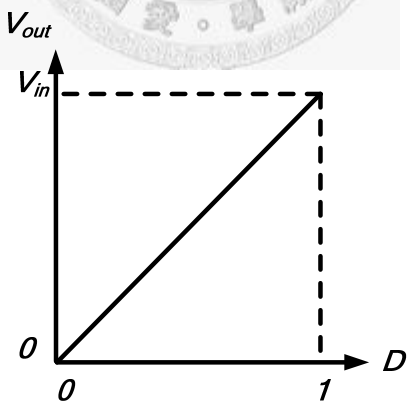


Fig. 2.6 Output characteristic of buck converters

The conventional buck converter with inductor current and voltage waveforms shows in the Fig. 2.7. The transistor M1 is usually switched at high frequency to produce a chopped output voltage V_s. This is then filtered by the LC filter to generate a smooth load voltage V_{out}. When transistor M1 turns on, $V_s = V_{in}$, the voltage across the inductor

is:

$$V_L = L \times \frac{di}{dt} = V_{in} - V_{out} \tag{2.10}$$

As a result, I_L increases linearly. When transistor M1 turns off, the current through the inductor cannot instantaneously fall to zero, so the diode provide a return path for the current to circulate through the load. During this period, V_s=0, so the voltage across the inductor is:

$$V_L = L \times \frac{di}{dt} = -V_{out} \tag{2.11}$$

So I_L decreases linearly. The peak-to-peak current ripple is:

$$\Delta I = t_{on} \times \frac{V_{in} - V_{out}}{L} = \frac{V_{in} \times T}{L} \times D \times (1 - D) \tag{2.12}$$

Therefore, the maximum current and the minimum current are defined separately as:

$$\begin{aligned} I_{\max} &= \frac{V_{out}}{R} + \frac{\Delta I}{2} \\ I_{\min} &= \frac{V_{out}}{R} - \frac{\Delta I}{2} \end{aligned} \tag{2.13}$$

In Fig. 2.7(a), the continuous conduction mode (CCM) means that the minimum inductor current never falls to zero. When the minimum current falls to zero, it is discontinuous conduction mode (DCM) as shown in Fig. 2.7(b). In the steady state condition, the average voltage across an inductor over a complete is zero.

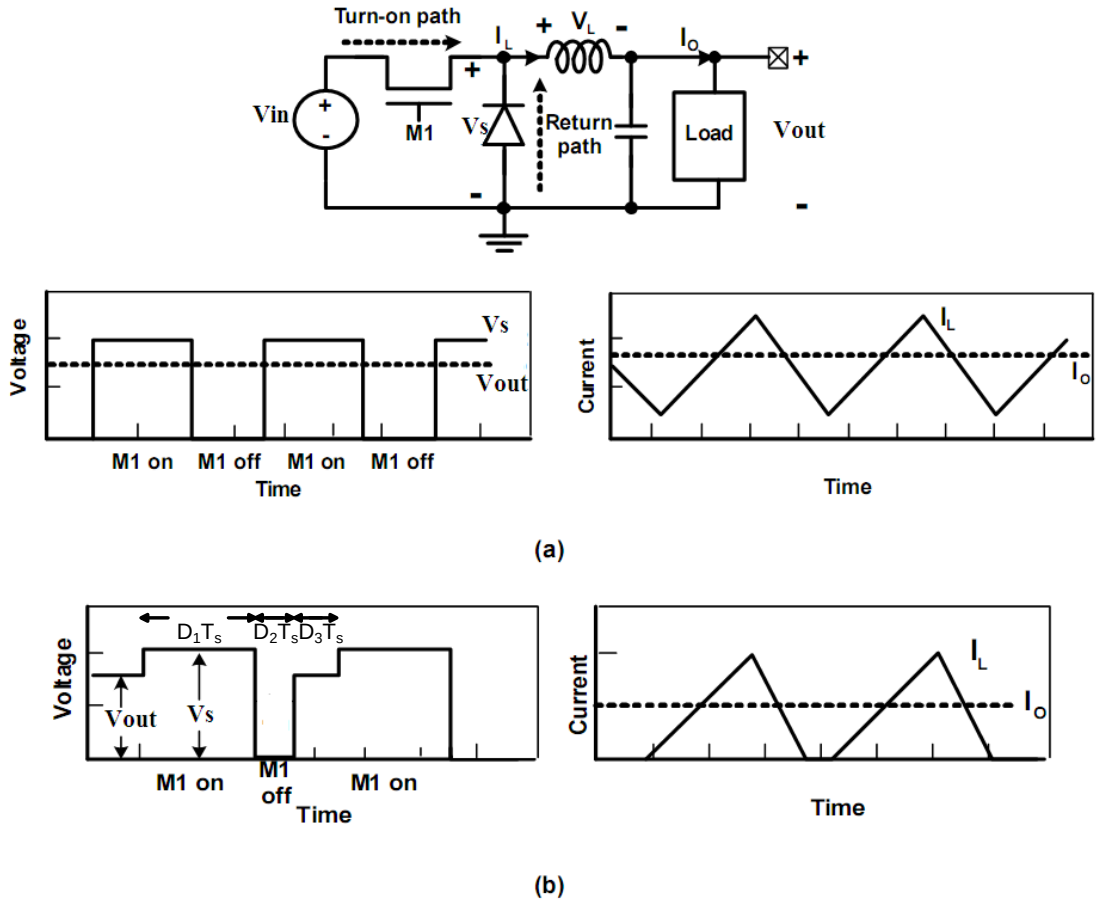


Fig. 2.7 (a) The diagram and waveforms of continuous mode (b) The waveforms of discontinuous mode

In DCM,

$$\langle V_L(t)\rangle = D_1(V_{in} - V_{out}) + D_2(-V_{out}) + D_3(0) = 0 \tag{2.14}$$

Solution for conversion ratio yields

$$Conversion\ ratio = \frac{V_{out}}{V_{in}} = \frac{D_1}{D_1 + D_2} \tag{2.15}$$

From Fig. 2.7(b), the average inductor current is calculated:

$$\begin{aligned} \frac{1}{T_S}\int_0^{T_S} i_L(t)dt &= \frac{1}{T_S}\left[\frac{1}{2} i_{peak}(D_1 + D_2)T_S\right] \\ Average\ inductor\ current &= \frac{V_{out}}{R} = (V_{in} - V_{out})\left(\frac{D_1 T_S}{2L}\right)(D_1 + D_2) \end{aligned} \tag{2.16}$$

Elimination of D_2 from conversion ratio equation and average inductor current equation, and solution for the conversion ratio V_{out}/V_{in}, yields

$$\frac{V_{out}}{V_{in}} = \frac{2}{1+\sqrt{1+\frac{4K}{D_1^2}}}, where\ K = 2L/RT_S \tag{2.17}$$

The result of conversion ratio *M(D)*:

$$\begin{cases} D & \text{for CCM} \\ \dfrac{2}{1+\sqrt{1+\dfrac{4K}{D_1^2}}} & \text{for DCM} \end{cases} \tag{2.18}$$

2.2.2 Estimation of Output Voltage Ripple

Considering the buck regulator of Fig. 2.8(a), the inductor current $i_L(t)$ with a dc component I_L and linear ripple of peak magnitude Δi_L are shown in Fig. 2.8(b). It is impossible to build a perfect low-pass filter that allows the dc component to pass but completely removes the components at the switching frequency and its harmonics. So the low-pass filter must allow at least some small amount of the high-frequency harmonics generated by the switch to reach the output.

The output voltage switching ripple should be small in any well-designed converter, since the object is to produce a dc output. For example, in a computer power supply having a 3.3 V output, the switching ripple is normally required to be less than a few tens of millivolts, or less than 1% of the dc output.

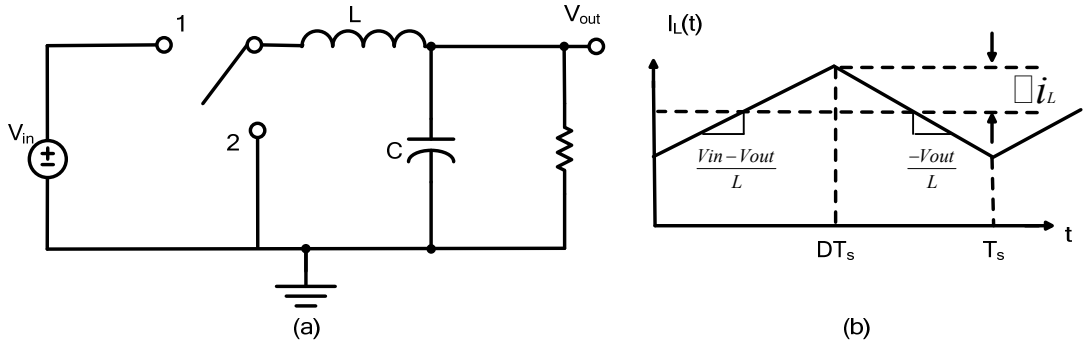


Fig. 2.8 Buck converter (a) circuit (b) steady-state inductor current waveform

In a well designed converter, in which the capacitor provides significant filtering of

switching ripple, the capacitance is chosen large enough that its impedance at the switching frequency is much smaller than the load impedance. Hence nearly all of the inductor current ripple flows through the capacitor, and very little flows through load. As shown in Fig. 2.9, the capacitor current waveform $I_C(t)$ is then equal to the inductor current waveform with the dc component removed. The current ripple is linear, with peak value Δi_L.

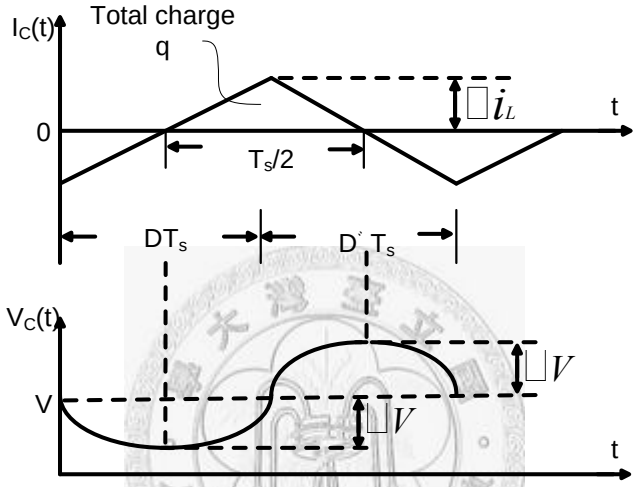


Fig. 2.9 Output capacitor voltage and current waveforms for the buck converter in Fig.2.6

From Fig. 2.9, by the capacitor relation $Q=CV$, the charge q is the integral of the current waveform between its zero crossings.

$$q = C(2\Delta V) \tag{2.19}$$

$$q = \frac{1}{2}\Delta i_L \frac{T_S}{2} \tag{2.20}$$

Substitution of equation (2.20) into equation (2.21), and solution for the voltage ripple peak magnitude ΔV yields

$$\Delta V = \frac{\Delta i_L T_S}{8C} \tag{2.21}$$

This expression can be used to select a value for the capacitance C such that a given

voltage ripple is obtained. In practical, the additional voltage ripple caused by the capacitor equivalent series resistance (ESR) must also be included. The voltage ripple with ESR is calculated as

$$\Delta V = i_C(t) \times ESR + \frac{\Delta i_L T_S}{8C} = \Delta i_L \times (ESR + \frac{T_S}{8C}) \tag{2.22}$$

In general, the ripple caused by first term "ESR" is much greater than caused by second term (T_s/8C). So consideration of ESR is essential for estimation of output voltage ripple in switching converter.

2.2.3 Feedback-Loop Stabilization

The simply feedback mechanism is illustrated in Fig. 2.10. The converter is composed of power stage and feedback network. The power stage contains a pair of switching elements, which consists of the power PMOS and NMOS transistors, and an output filter, which consists of an inductor and a capacitor. In feedback network, the difference of βV_{out} which the output voltage is scaled down by resistor series and the reference voltage V_{ref} is fed to the error amplifier. And then the output of the error amplifier and the ramp will pass through the comparator to define the duty cycle (PWM). The duty cycle controls the duration of the conducted time between the PMOS and the NMOS to achieve desired voltage such that the feedback is finished to regulate the output voltage The feedback system can be described as Fig. 2.11. The transfer function of the LC filter is defined as:

$$H_{LC}(s) = \frac{1}{s^2 LC + 1} \tag{2.23}$$

The transfer function of the feedback network is defined as:

$$H_{RR}(s) = \frac{R_2}{R_1 + R_2} \tag{2.24}$$

where $T3(s) = H_{LC}(s) \times H_{RR}(s)$.

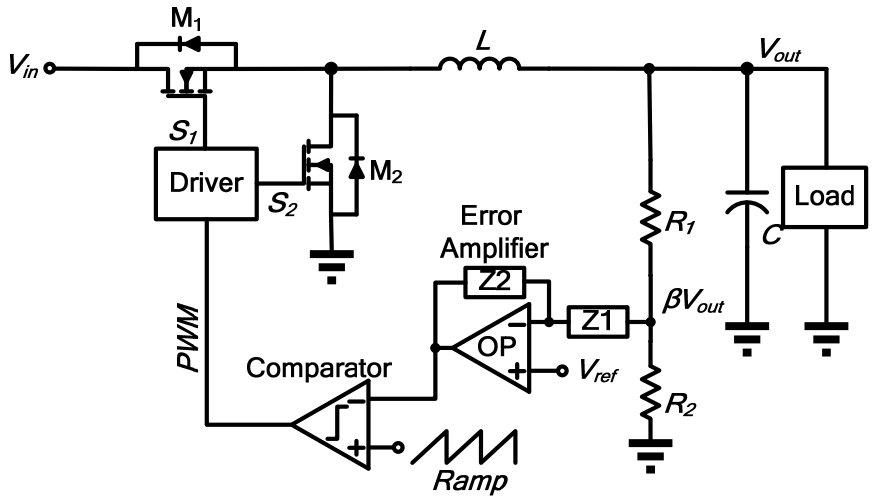


Fig. 2.10 The simply diagram of the PWM converter

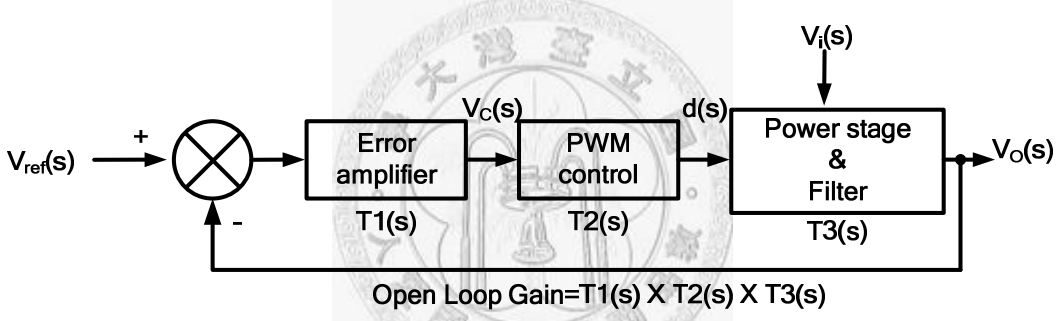


Fig. 2.11 The transfer function of feedback system

It is fixed-amplitude pulse of adjustable turn-on ratio of the PWM modulator. Therefore, the transfer function of the PWM modulator is defined as:

$$T2(s) = \frac{V_P}{V_T} \tag{2.25}$$

where V_T is amplitude of ramp waveform and V_P is the amplitude of PWM signal. The $H_{RR}(s)$ and T2(s) do not effect on phase shift but they can decay the DC gain. As a result, there is only error amplifier T1(s) that can provide gain boost to increase the total gain and influence phase for better phase margin.

Next, two types of the error amplifier will be introduced. The first is type II shown in Fig. 2.12 (a), and it has two poles and one zero. The transfer function is calculated as:

$$\frac{V_2}{V_1} = -\frac{1+sR_2C_1}{sR_1(C_1+C_2)(1+sR_2\frac{C_1C_2}{C_1+C_2})} \approx -\frac{1+sR_2C_1}{sR_1(C_1+C_2)(1+sR_2C_2)} \quad ,assume\ C_1 \gg C_2 \tag{2.26}$$

The poles locate at the origin and the frequency $f_p = \frac{1}{2\pi R_2 C_2}$, the zero locates at the frequency $f_z = \frac{1}{2\pi R_2 C_1}$. The frequency response is shown in Fig. 2.10(b) and (c). The gain in the middle frequency is $\frac{R_2}{R_1}$. As a result, appreciate resistors are chosen, and it can compensate the loss caused by the LC filter.

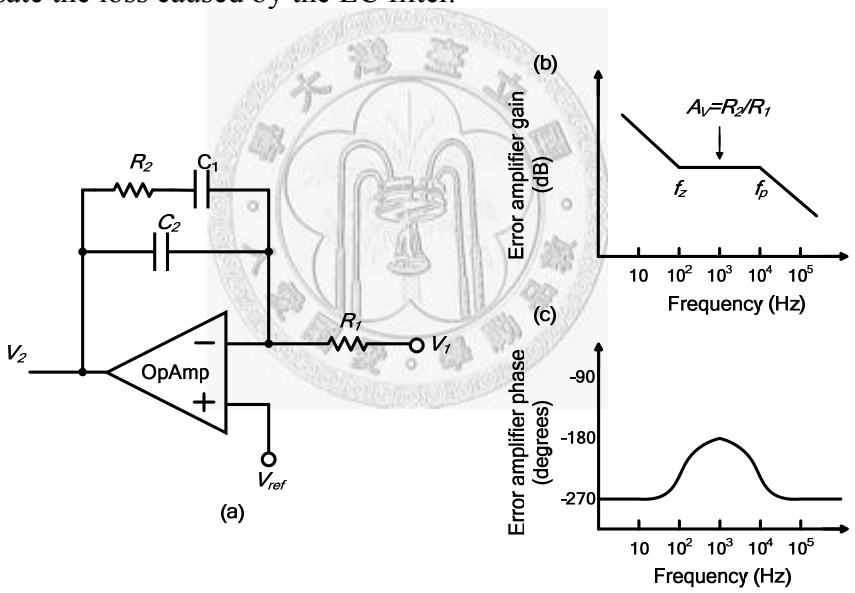


Fig. 2.12 Type II compensator with two poles and a zero

The second is type III, as shown in Fig. 2.13(a), and it has three poles and two zeros. The transfer function is calculated as:

$$\frac{V_1}{V_2} = -\frac{(1+sR_2C_1)(1+s(R_1+R_3)C_3)}{sR_1(C_1+C_2)(1+sR_3C_3)(1+sR_2\frac{C_1C_2}{C_1+C_2})} \approx -\frac{(1+sR_2C_1)(1+sR_1C_3)}{sR_1(C_1+C_2)(1+sR_3C_3)(1+sR_2C_2)} \quad ,assume\ C_1 \gg C_2, and\ R_1 \gg R_3 \tag{2.27}$$

The poles locate at the origin, the frequency $f_{p1} \approx \frac{1}{2\pi R_2 C_2}$ and the frequency $f_{p2} \approx \frac{1}{2\pi R_3 C_3}$. The zeros locate at the frequency $f_{z1} \approx \frac{1}{2\pi R_2 C_1}$ and the frequency $f_{z2} \approx \frac{1}{2\pi R_1 C_3}$. The gain and phase of this compensator is shown in Fig. 2.13 (b) and (c).

In summary, the maximum phase boost in type II compensator is 90 degrees, and in type III compensator is 180 degrees. According to stability and cost, the system will use the appropriate compensator to achieve desired performance.

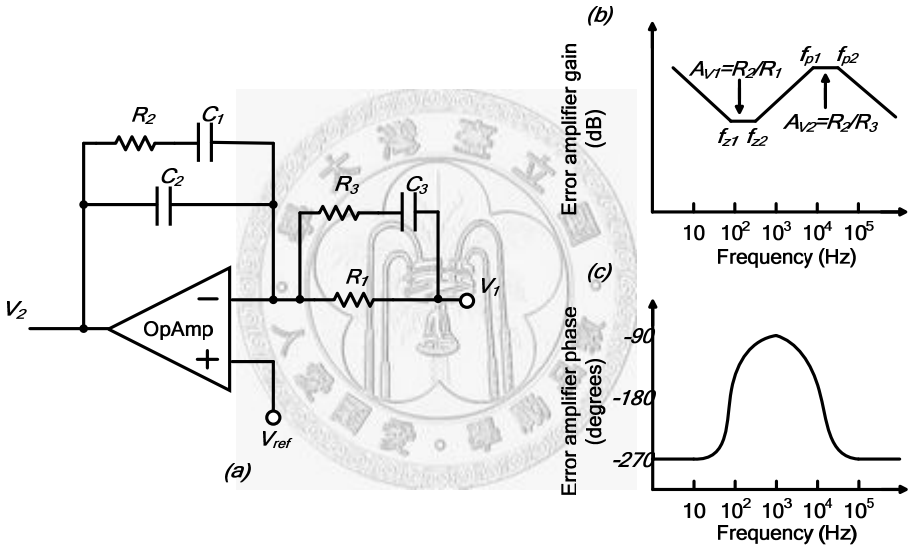


Fig. 2.13 Type III compensator with three poles and two zeroes

2.3 Variable Frequency

In variable frequency techniques, there are four typical random switching methods discussed firstly. Then we will introduce a simplest method which is frequency hopping (FH). Since the main issue in this thesis focuses on the moment between different frequencies, the FH technique is a good choice to represent the main issue. Therefore, here uses the FH technique in following analysis,

2.3.1 Random Switching

There are four general random switching schemes for switched-mode DC-DC converters, including random-pulse-position-modulation (RPPM), random-pulse-width-modulation (RPWM), and random-carrier-frequency-modulation with fixed-duty-cycle (RCFMFD) and with variable-duty-cycle (RCFMVD), respectively. They are categorized by the random modulation of pulse which drives power transistors. The parameters of pulse are shown in Fig. 2.14. T_k is the duration of the kth cycle. ε_k is the delay time of the pulse. α_k is the duration of the pulse in the kth cycle. d_k which equals to α_k/T_k is the duty cycle period of the switch turning on in the kth period. The amplitude of pulse is rail to rail of input voltage. Their operation will be addressed as following paragraphs.

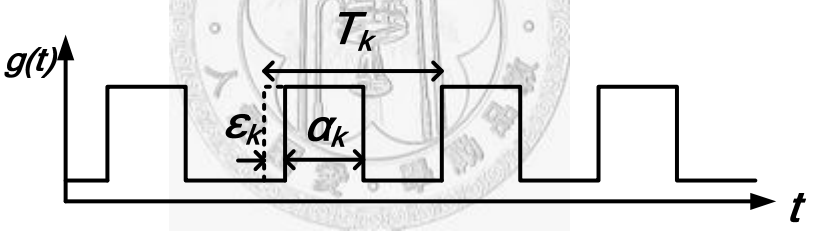


Fig. 2.14 Switching parameters

RPPM is similar to the classical PWM scheme with constant switching frequency. However, the position of the gate pulse or delay time ε_k is randomized within each switching period, instead of commencing at the start of each cycle. RPWM allows the pulse width α_k to vary, but the average pulse width is equal to the required duty cycle. RCFMFD exhibits randomized switching period T_k and constant duty cycle $d=\alpha_k/T_k$, while RCFMVD exhibits randomized switching period T_k and constant pulse width α. With the aid of Fig. 2.15, the characteristics of the pulse $g(t)$ in each scheme are summarized in Table 2.1.

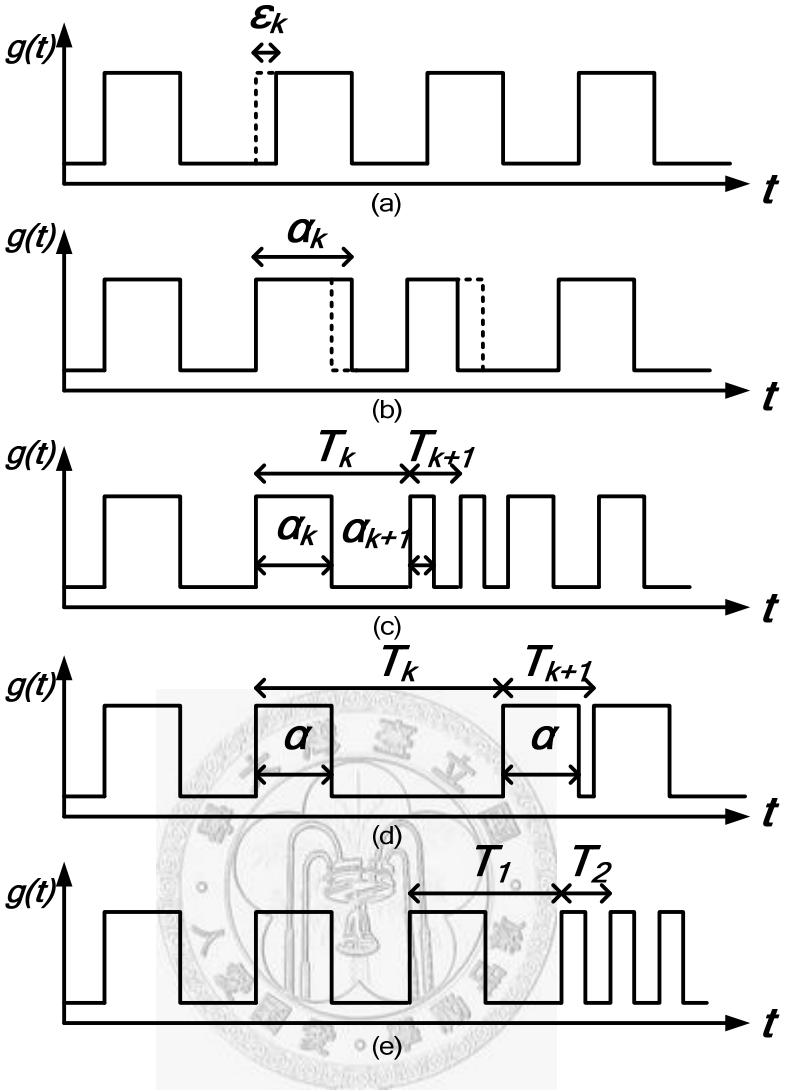


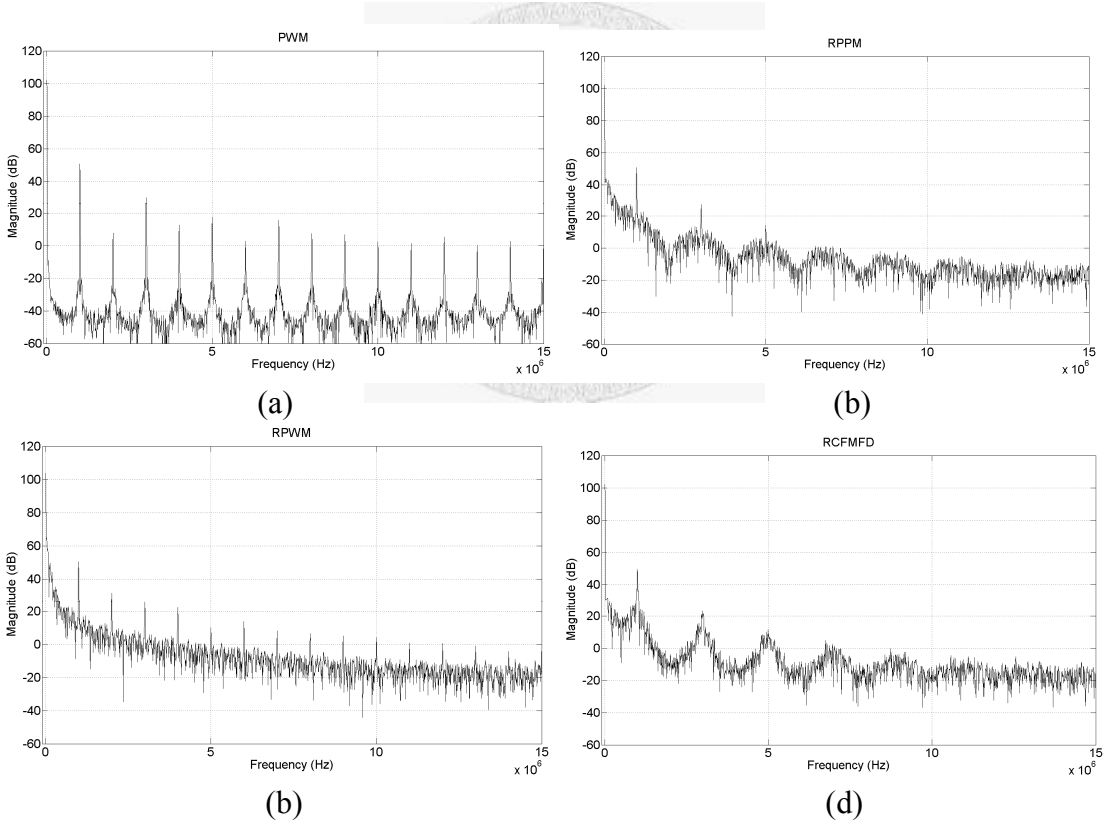
Fig. 2.15 Switching signal with randomized modulation (a)RPPM (b)RPWM (c)RCFMFD (d)RCFMVD (e)FH

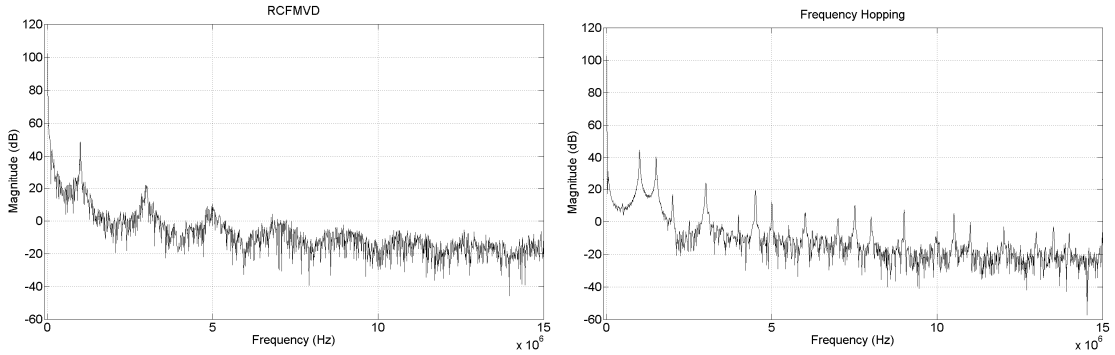
Table 2.1 Characteristics of different random switching schemes

Switching schemes	T_k	α_k	$d=\alpha_k/T_k$	ε_k
Standard PWM	Fixed	Fixed	Fixed	Fixed
RPPM	Fixed	Fixed	Fixed	Randomized
RPWM	Fixed	Randomized	Randomized	Fixed
RCFMFD	Randomized	Randomized	Fixed	Fixed
RCFMVD	Randomized	Fixed	Randomized	Fixed
FH	Integer sets	Integer sets	Fixed	Fixed

2.3.2 Frequency Hopping

Compared to random switching schemes, the frequency-hopping (FH) technique utilizes couples of fixed switching frequencies to achieve EMI-peak reduction. Using predictable frequencies relax the complexity of the filter. Its characteristic of the pulse is shown in Fig. 2.15(e). The spectrum results of these variable frequency techniques are shown in Fig. 2.16. Table 2.2 aids to understand each reduction for peak of EMI. Another issue is the output voltage in time domain. In Fig. 2.17, these techniques have different phenomena in steady state. The reason is that the duty cycle varies in RPWM and RCFMVD.





(e) (f)

Fig. 2.16 Output spectrum of different switching schemes

Table 2.2 Comparison of different switching schemes

Switching schemes	Peak of EMI (dB)
Standard PWM	50.77
RPPM	50.61
RPWM	50.4
RCFMFD	49.56
RCFMVD	48.56
FH	44.48

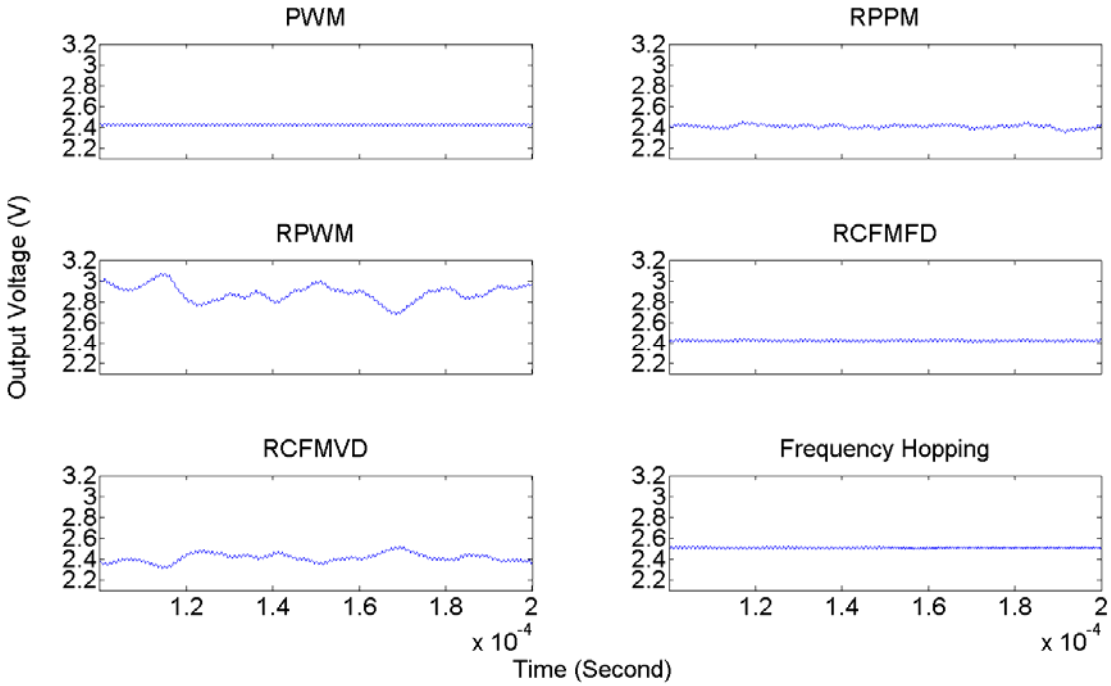


Fig. 2.17 Transient waveform of different switching schemes

Chapter 3 Proposed Architecture

3.1 Introduction

The inductor current average control (ICAC) is proposed in this paper. When using variable frequency techniques such as random switching or frequency hopping (FH), the inductor current ripple varies as the switching frequency changes. This variation of current ripple results in a transient ripple on the output voltage and undesired spur. In order to reduce this effect, this thesis discusses the best moment between different frequencies and how to implement. As aforementioned, the main issue focuses on the best moment between different frequencies and the FH technique adapts to this situation. Therefore, it discusses the hopping moment in following analysis

3.2 Specification of DC-DC Buck Converter

The preliminary specification of DC-DC buck converter of this design is shown in Table 3.1. This work is used in portable devices to drive power amplifiers of RF circuits such as power-level tracking [14]. Therefore, the off-chip components must be small (L_O>4.7μH and C_O>10μF in conventional circuits) and the output current is determined by the power amplifier. Output voltage range is utilized to the standby mode and active mode in portable devices for saving power. Input voltage range is determined by the battery type. Switching frequency is usually fixed in typical PWM converters, but in spread spectrum methods such as frequency hopping (FH), it needs a particular frequency range.

Table 3.1 Specification of designed DC-DC buck converter.

Specification	**Parameters**
Input voltage, V_{IN}	3.6-5 V
Output voltage, v_{OUT}	0.8-3.4 V
Max. output current, I_O	450 mA
Output inductor, L_O	1 μH
Output capacitor, C_O	1 μF
Switching frequency, f_{req}	2-3 MHz

3.3 System Architecture

In this chapter, the detailed operation of the chip will be discussed. The typical architecture is illustrated in Fig. 3.1. A PWM buck converter provides a regulated output voltage v_{OUT} from an unregulated input voltage V_{IN}. The PWM controller compares the ramp signal, v_{ramp}, with the output of the error amplifier to generate a square wave, v_{PWM}, for voltage regulation. The gate driver drives the power transistors, M_P and M_N, with dead-time control to avoid a shoot-through current. The power transistors induce current passing a low pass filter which is composed with an inductor, L_O, and a capacitor, C_O to the load, I_O. Note that the frequency of v_{ramp} determines the operation frequency and is able to change for hopping the frequency.

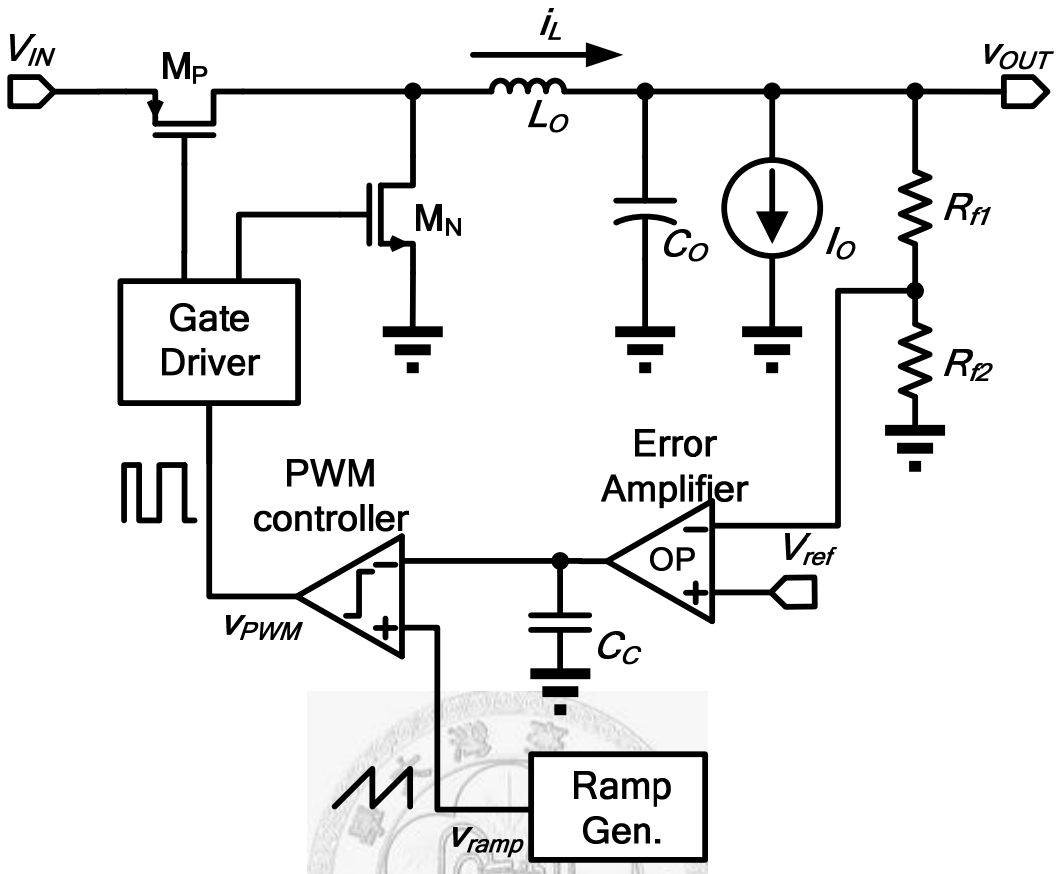


Fig. 3.1 Structure of a conventional PWM buck converter.

3.4 Inductor Current Average Control (ICAC)

As shown in Fig. 3.2, the FH technique with a lower frequency, f_1, and a higher frequency, f_2 [5] can avoid the energy concentrated on a single frequency at f_{nohop}. Their magnitudes are 6dB down as two frequencies hopping in comparison with the magnitude at only one frequency. However, the converter output suffers transient ripples for several periods after hopping and it would result in an undesired spur at f_{trans}.

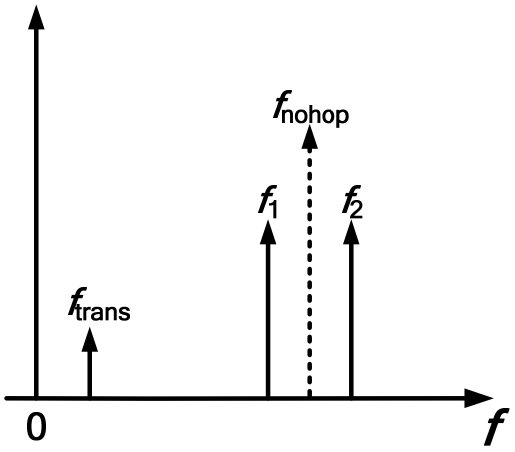


Fig. 3.2 Energy spread to multiple frequencies with the FH technique.

As shown in Fig. 3.3, in conventional PWM DC-DC converters [3], it assumes the frequency hopping at falling edge of v_{PWM} for simplicity and random in practically. The inductor current, i_L, increases during on duty cycle period, and decreases during off duty cycle period. In the example of Fig. 3.3, $T_{on,1}$ and $T_{on,2}$ represent the on duty cycle period of switching period at the low and high frequencies respectively. $T_{off,1}$ and $T_{off,2}$ represent the off duty cycle period of switching period at the low and high frequencies respectively. It reaches its peak/valley currents at the rising edge or the falling edge of v_{PWM}. After the hopping moment, the average of the transient inductor current would be different from that of the steady-state inductor current, I_L, due to the current continuity property of inductor. But, it would gradually approach I_L when the inductor current is back to steady state. Therefore, the difference, $\Delta I_{L,trans}$, charges (or discharges) C_O and generates transient ripple, Δv_{trans} on the output voltage. Its frequency response is the undesired spur at f_{trans} is dominated by L_O and C_O [15]. The undesired spur can be reduced by a larger capacitor but it pays a longer time to settle. Or, a larger inductor can be used but it occupies a larger area in the circuit.

An Inductor Current Average Control (ICAC) technique for FH structure is

proposed in this paper. As shown in Fig. 3.4, the best hopping moment could be chosen. The best time length, T_X, is calculated to correspond to the best hopping state, which maintains the same I_L between the two frequencies. It modulates the off/on duty cycle period to be T_X width. The calculated value of T_X will be discussed in detail later. In the proposed hopping state, the output ripple voltage is improved by making the amount of charging close to the amount of discharging in the capacitor. If transient ripple on the output voltage is reduced, the undesired spur at f_{trans} in Fig. 3.4 is also reduced.

The best hopping state can be derived either in the off duty cycle period or the on duty cycle period. The proposed technique for FH from low to high and from high to low in these two different duty cycle periods will be discussed separately. Note that hopping in the off duty cycle period using ICAC is implemented in this chip.

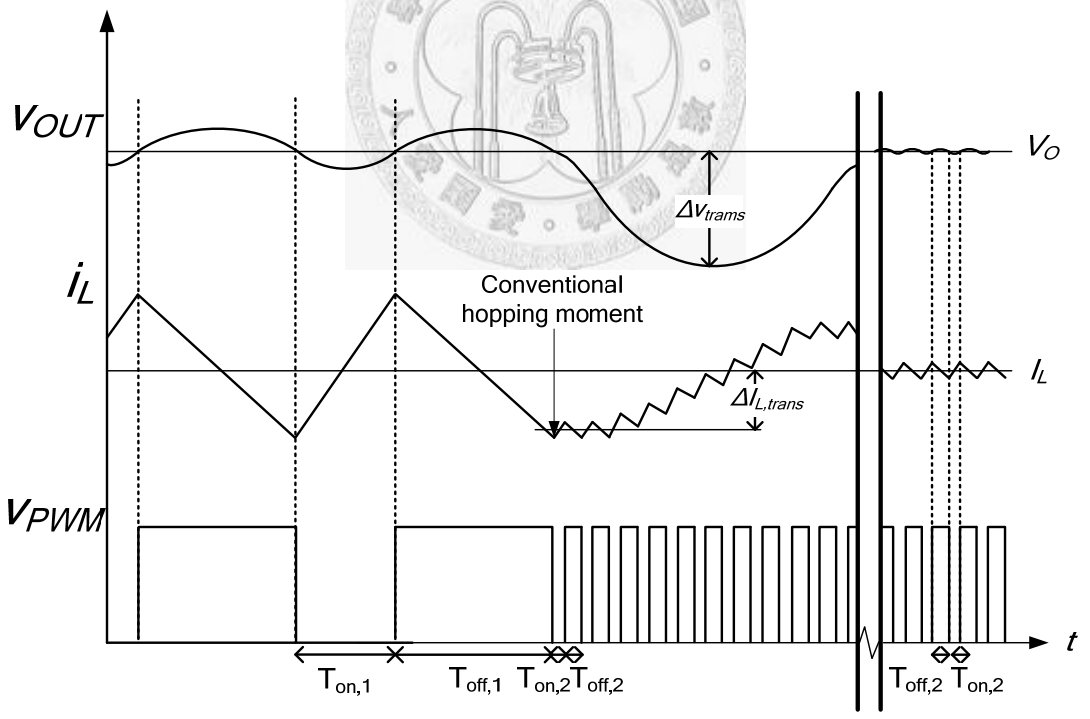


Fig. 3.3 Transient waveforms of output voltage, inductor current and PWM signal in a conventional converter.

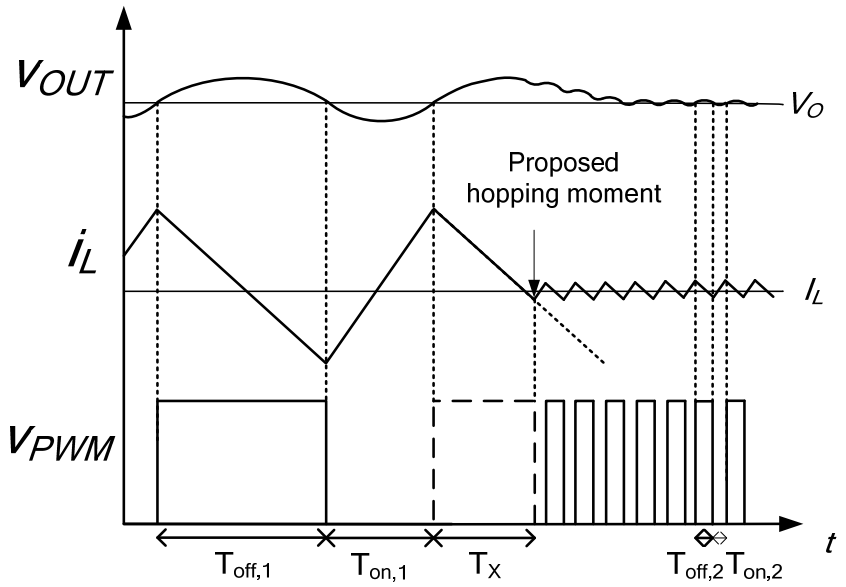


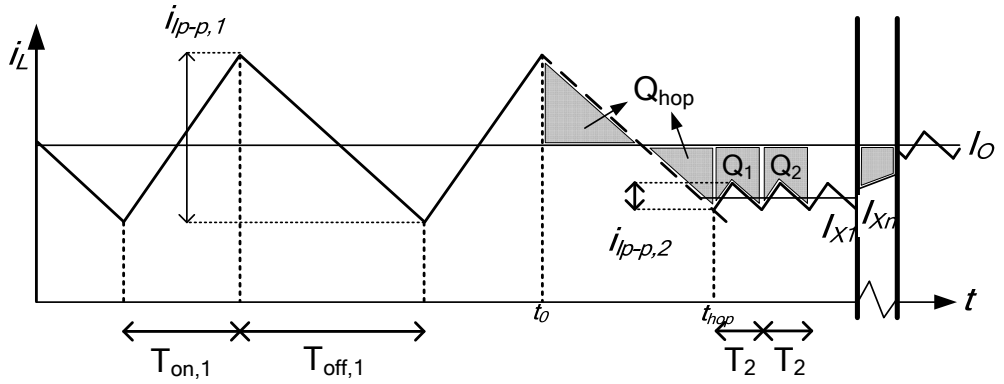
Fig. 3.4 Transient waveforms of output voltage, inductor current and PWM signal in the converter with the proposed ICAC technique.

3.4.1 Hopping in Off Duty Cycle Period

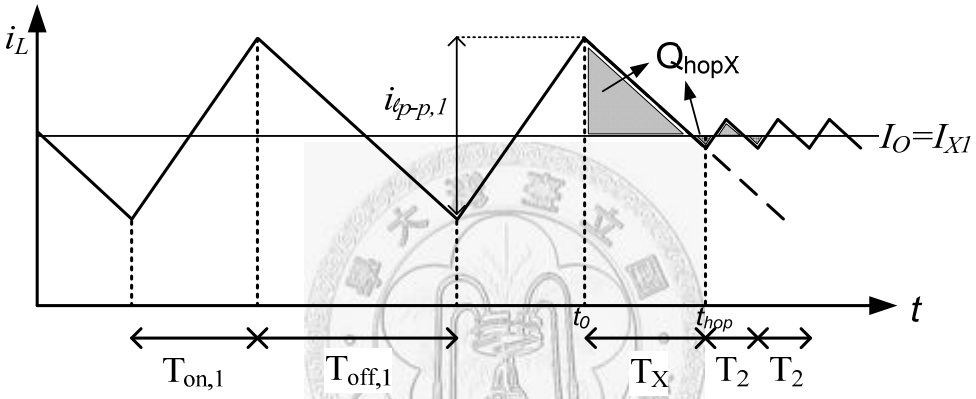
As mentioned before, there are two choices to hop, here discusses hopping in off duty cycle period with two parts. One is the frequency hopping from low to high, and another is the frequency hopping from high to low.

3.4.1.1 Hopping frequency from low to high

To reduce the complexity of transient response analysis, the loading is supposed to be a constant current source, I_O as indicated in Fig. 3.1. Therefore, the load current I_O is equal to the average or dc current I_L.



(a)



(b)

Fig. 3.5 (a) Conventional and (b) proposed transient inductor current that hops frequency from low to high in off duty cycle period.

As shown in Fig. 3.5(a), the net charge on the capacitor, ΔQ, after t_0 is

$$\Delta Q = Q_{hop} + Q_1 + Q_2 + \cdots \tag{3.1}$$

$$= \left(I_{Xhop} - I_O\right)\left(t_{hop} - t_0\right) + \left(I_{X1} - I_O\right)T_2 + \left(I_{X2} - I_O\right)T_2 + \cdots$$

where I_{Xhop} is the average of transient inductor current from t_0 to t_{hop} and I_{Xi}, i=1,2,… is the average of transient inductor current at the ith period of v_{PWM} after t_0. t_0 is the time at which the inductor current is at its peak or valley and the capacitor voltage is at its dc value, V_O. t_{hop} is the hopping moment. $T_2=T_{off,2}+T_{on,2}$ is the period of v_{PWM} after hopping.

The transient response can be separated into two parts, the charge in the hopping interval Q_{hop} and total charge after hopping $Q_T=Q_1+Q_2+\ldots$. Since settling time is longer than one period, Q_{hop} is much smaller than Q_T.

$$\Delta Q = Q_{hop} + Q_T \cong Q_T \tag{3.2}$$

As illustrated in Fig. 3.5(a), Q_T is approximated with a triangular area. Its height is the difference between I_O and I_{X1}. Its width, T_T, is the time from t_{hop} to the steady state.

$$\begin{aligned} Q_T &= \frac{1}{2}\left(I_{X1} - I_O\right)T_T \\ &= \frac{1}{2}(-\frac{1}{2}i_{lp\text{-}p,1} + \frac{1}{2}i_{lp\text{-}p,2})T_T \end{aligned} \tag{3.3}$$

$$m_{off} = \frac{-i_{\ell p\text{-}p,1}}{T_{off,2}} = \frac{-i_{\ell p\text{-}p,2}}{T_{off,2}} = \frac{-DV_{IN}}{L_O} \tag{3.4}$$

where $i_{lp\text{-}p,1}$ and $i_{lp\text{-}p,2}$ are the peak-to-peak values of the inductor current at low frequency and high frequency respectively. m_{off} is the slope of the decreasing inductor current. D is the duty cycle.

Then, the conventional transient ripple on the output voltage can be obtained as

$$\Delta v_{trans} \cong \frac{Q_T}{C_O} \cong \frac{1}{4}\frac{V_{IN}D(1-D)}{L_O C_O}(T_1 - T_2)T_T \tag{3.5}$$

where T_1, T_2 are the periods of the low and high frequencies respectively.

In order to minimize Q_T in (3.3), the best time T_X of t_{hop} is proposed as follows. In Fig. 3.5(a), I_{X1} can be calculated as

$$I_{X1}\left(t_{hop}\right) = I_O + \frac{1}{2}i_{lp\text{-}p,1} + m_{off} \times \left(t_{hop} - t_0\right) + \frac{1}{2}i_{lp\text{-}p,2} \tag{3.6}$$

According to (3.3), if I_{X1} equals I_O, Q_T=0, most charge during transient settling time can be eliminated.

$$I_O + \frac{1}{2}i_{\ell p\text{-}p,1} + m_{off} \times \left(t_{hop} - t_0\right) + \frac{1}{2}i_{\ell p\text{-}p,2} = I_O \tag{3.7}$$

the proposed best time T_X can be calculated as

$$T_X = t_{hop} - t_0 = -\frac{\frac{1}{2}i_{lp-p,1}}{m_{off}} - \frac{\frac{1}{2}i_{lp-p,2}}{m_{off}} = \frac{1}{2}T_{off,1} + \frac{1}{2}T_{off,2} \tag{3.8}$$

The proposed best time T_X is $\frac{1}{2}(T_{off,1}+T_{off,2})$, which is the average of off duty cycle period at low and high frequencies. Its corresponding transient waveform is illustrated in Fig. 3.5(b). Since I_X equals I_O, according to (3.3), only the rest of charge, Q_1, would affect transient ripple of the output voltage.

$$Q_{hopX} = \frac{1}{2}(\frac{1}{2}i_{lp-p,1})(\frac{1}{2}T_{off,1}) - \frac{1}{2}(\frac{1}{2}i_{lp-p,2})(\frac{1}{2}T_{off,2})$$

$$= \frac{1}{2}(\frac{1}{2}i_{lp-p,1} - \frac{1}{2}i_{lp-p,2})T_X \tag{3.9}$$

$$\Delta v_{trans,ICAC} = \frac{Q_{hopX}}{C_O} = \frac{1}{4}\frac{V_{IN}D(1-D)}{L_O C_O}(T_1 - T_2)T_X \tag{3.10}$$

According to (3.5) and (3.10), the conventional and proposed transient ripples on the output voltage are proportional to $(T_1-T_2)T_T$.and $(T_1-T_2)T_X$ respectively.

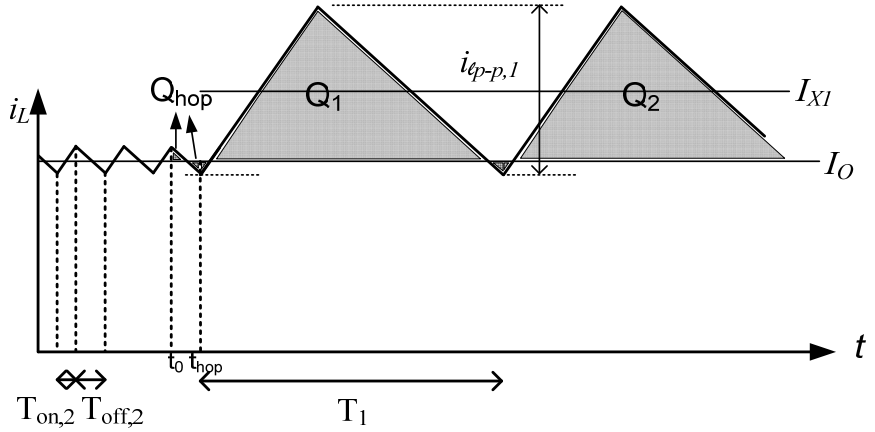
3.4.1.2 Hopping frequency from high to low

As shown in Fig. 3.6(a), when the frequency hops from high to low, the average of transient inductor current I_{X1} is over the average inductor current I_O. Similarly, I_{X1} can be approximated as

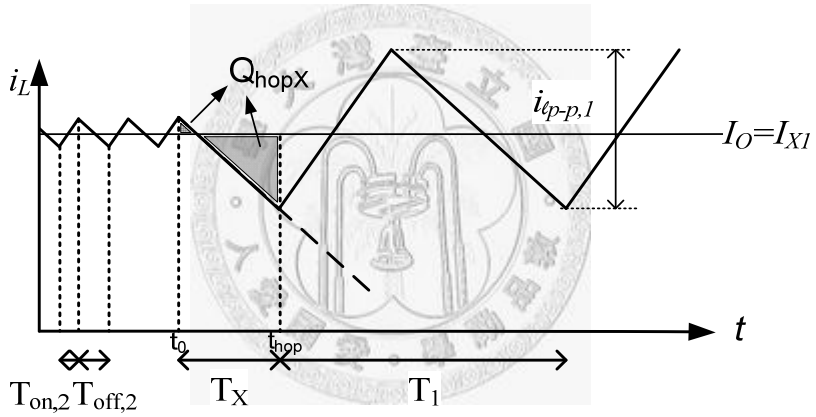
$$I_{X1}(t_{hop}) = I_O + \frac{1}{2}i_{lp-p,2} + m_{off} \times (t_{hop} - t_0) + \frac{1}{2}i_{lp-p,1} \tag{3.11}$$

Likewise, if let I_{X1} in (3.11) equal to I_O, we obtain $T_X=t-t_0=\frac{1}{2}(T_{off,1}+T_{off,2})$. T_X is the same when it hops from high to low. It is the average of off duty cycle period at low and high

frequencies.



(a)



(b)

Fig. 3.6 (a) Conventional and (b) proposed transient inductor current that hops frequency from high to low in off duty cycle period

3.4.2 Hopping in On Duty Cycle Period

3.4.2.1 Hopping frequency from low to high & from high to low

Similar to the analysis in 3.4.1, the only different part is the average of transient inductor current I_{X1}

$$I_{X1}\left(t_{hop}\right)=I_O+\frac{1}{2}i_{lp\text{-}p,1}+m_{on}\times\left(t_{hop}-t_0\right)+\frac{1}{2}i_{lp\text{-}p,2} \tag{3.12}$$

$$I_{X1}\left(t_{hop}\right)=I_O+\frac{1}{2}i_{lp\text{-}p,2}+m_{on}\times\left(t_{hop}-t_0\right)+\frac{1}{2}i_{lp\text{-}p,1} \tag{3.13}$$

I_{X1} in (3.12) is hopping from low to high and I_{X1} in (3.13) is hopping from high to low. Let I_{X1} in (3.12) and (3.13) equals to I_O as shown in Fig. 3.7 and Fig. 3.8 respectively, we obtain the similar $T_X=t-t_0=\frac{1}{2}(T_{on,1}+T_{on,2})$. It is the average of on duty cycle period at low and high frequencies

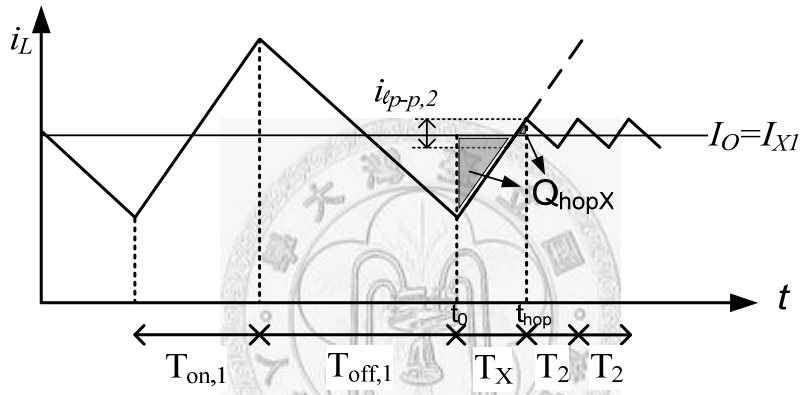


Fig. 3.7 Proposed transient inductor current that hops frequency from low to high in on duty cycle period.

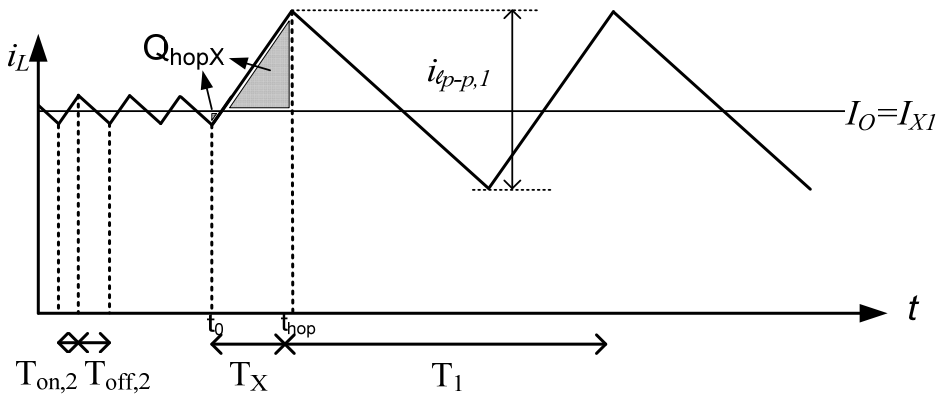


Fig. 3.8 Proposed transient inductor current that hops frequency from high to low in on duty cycle period.

Chapter 4 Circuit Implementation and Simulation Results

Based on above analysis, the proposed system circuit is shown as Fig. 4.1. Except for the conventional buck converter architecture, there are two DACs and an ICAC block. Two DACs change the output voltage and the switching frequency respectively. An ICAC block before the gate driver block is utilized to insert a calculated-width pulse for modulating the best time in frequency hopping.

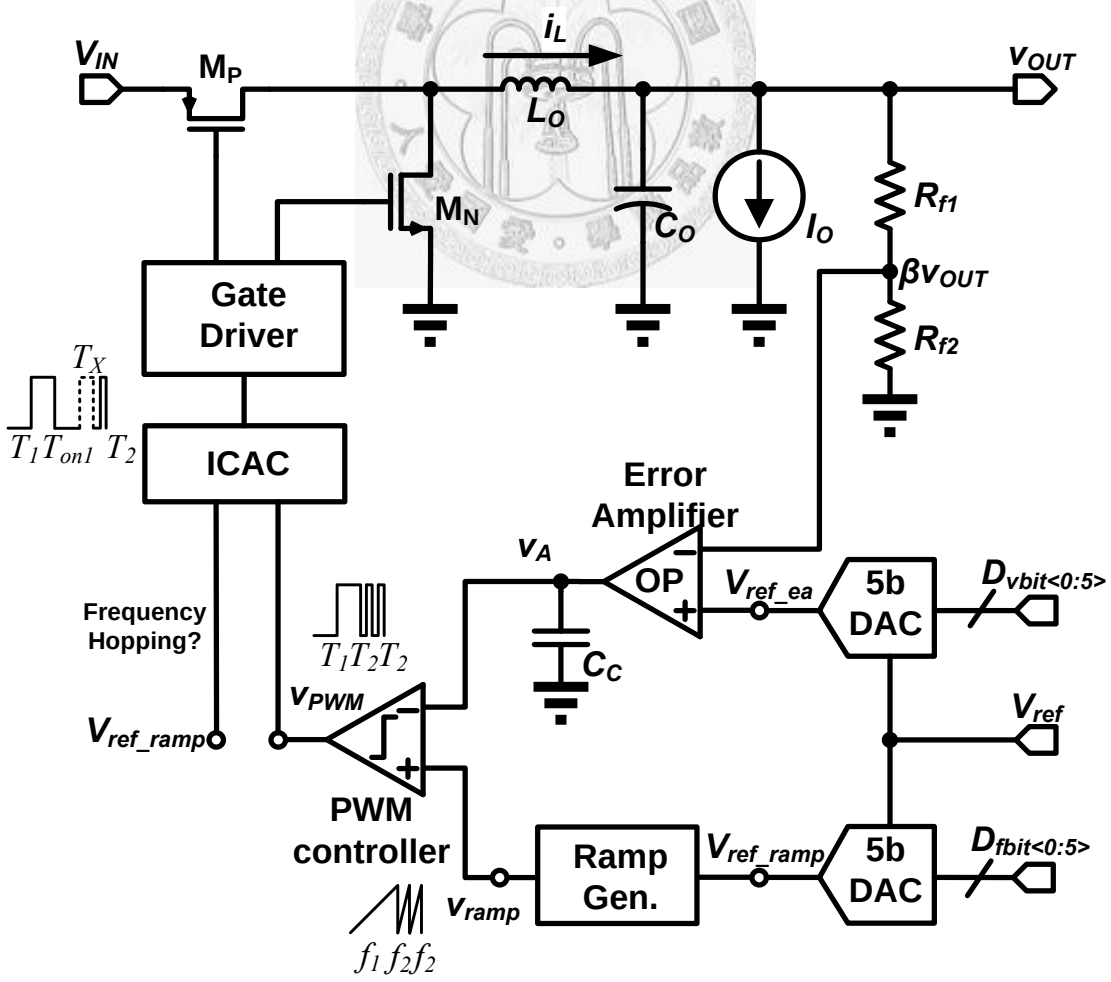


Fig. 4.1 Block diagram of the FH buck converter with ICAC controller

4.1 Amplifier Circuit

There are two type amplifiers in this work. One is slower and only used in the error amplifier circuit. Another one is faster and provides higher DC gain in this work which needs operational amplifiers (OP).

4.1.1 Error Amplifier

There are many compensation methods such as type II and type III. But as the operation frequency changes in the FH technique, the feedback-loop stabilization is much more difficult since these methods compensate the particular frequency range. Based on the simplicity and independence from the switching frequency, a dominant-pole compensation is used in this error amplifier to compensate the stability of the system.

To avoid any second pole involving in this dominant pole, it uses a one-stage simple operational amplifier as shown in Fig. 4.2. The unit-gain frequency ω_t is given by

$$\omega_t = \frac{g_{m1,2}}{C_C} \tag{4.1}$$

There are two components which define the unit-gain frequency. Firstly, to make lower unit-gain frequency for dominant-pole compensation, the compensation capacitor C_C is chosen as large as possible and is limited by the area on chip. Secondly, another component is the transconductance of input transistors, $g_{m1,2}$.

$$g_m = \sqrt{2C_{OX}\frac{W}{L}I_D} \tag{4.2}$$

To make smaller g_m, it is chose p-input, small W/L ratio and small bias current $I_{tail}=2I_D$.

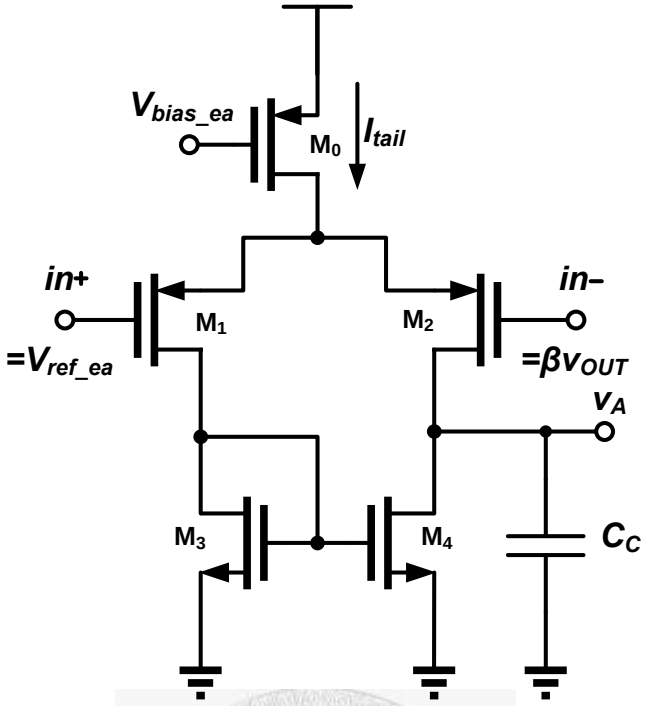


Fig. 4.2 Schematic of the error amplifier

Fig. 4.3 shows the AC analysis of the error amplifier. Open loop DC gain is 44 dB. Phase margin is 90 degree and the unity gain bandwidth is 113 kHz as C_C=42 pF.

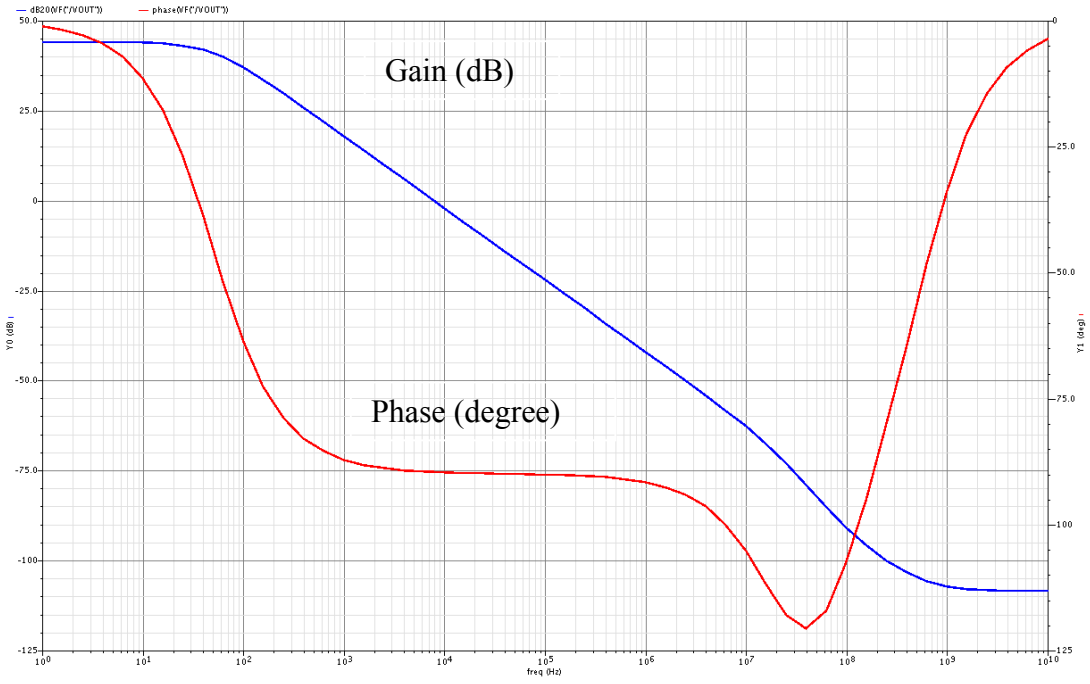


Fig. 4.3 Frequency response of the error amplifier

4.1.2 Operational Amplifier

In order to provide high DC gain, it chooses the folded-cascode structure as shown in Fig. 4.4 [11]. Its DC gain A_V and 3dB frequency ω_{3dB} are given by

$$A_V = g_m r_O \tag{4.3}$$

$$\omega_{3dB} = \frac{g_m}{C_L} \tag{4.4}$$

It is necessary to add an output stage when it drives resistance load. Therefore, some of these OPs have a NMOS common-drain stage as output buffer as listed in Table 4.1. Table 4.1 also shows two different tail currents. Several operational amplifiers do not need high frequency response, so they could use smaller tail current to save power. As shown in Fig. 4.5 and Fig. 4.6, their DC gain and 3dB frequencies are 69 dB, 43 MHz and 61.5 dB, 16 MHz respectively. The DC gain of OP with output buffer is lower due to the body effect. From Fig. 4.7, we have

$$A_V = \frac{\frac{1}{g_{mb}} // r_{Ob1} // r_{Ob2}}{(\frac{1}{g_{mb}} // r_{Ob1} // r_{Ob2}) + \frac{1}{g_m}} \tag{4.5}$$

Equation (4.5) represents that body effect decreases the DC gain. Although it can by reduced by using PMOS common-drain stage, it needs a shift-down circuit rather than shift-up circuit in this work.

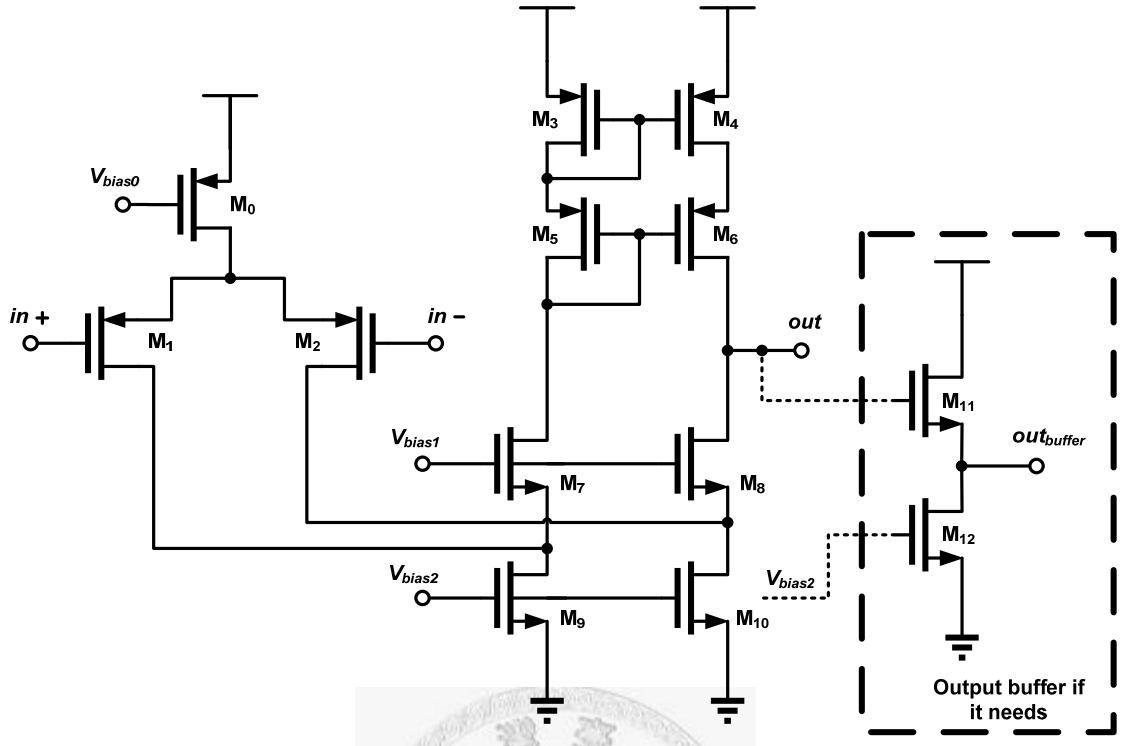


Fig. 4.4 Schematic of folded-cascade operational amplifier

Table 4.1 OP types used in this work

	I_{tail}=2 μA	I_{tail}=5 μA	With Buffer
Subtractor		O	O
Input of RampGen.		O	
Input of S&H		O	O
Buffer of V_{ref}	O		
Buffer of v_A	O		O
Buffer of v_{ramp}		O	O

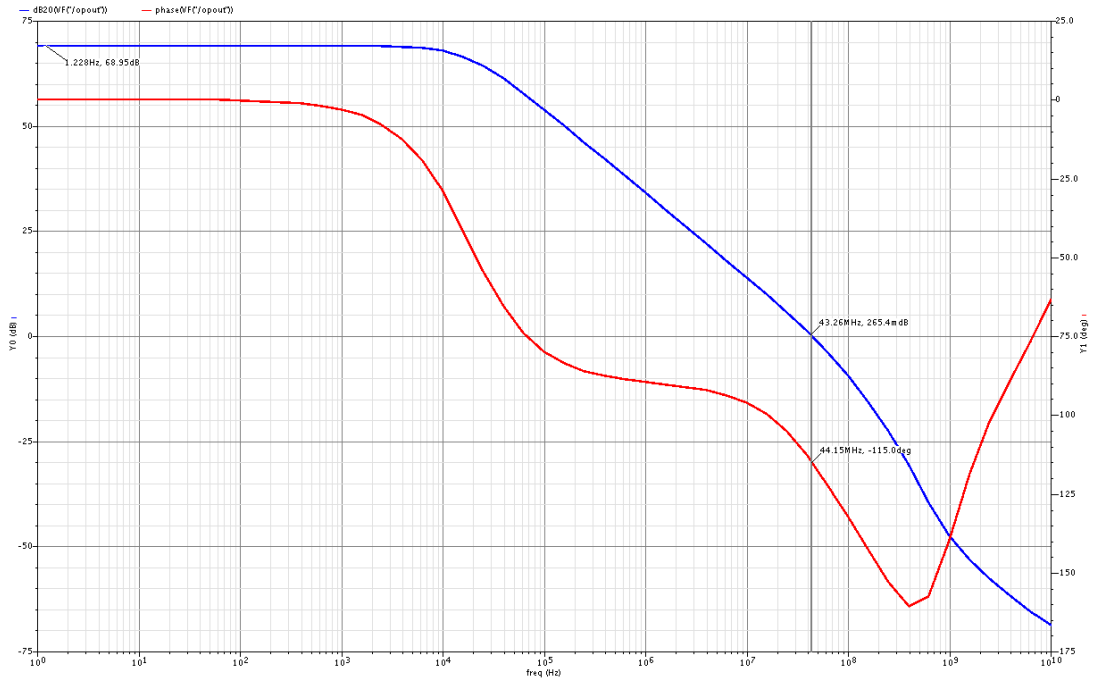


Fig. 4.5 Frequency response of the OP-Amp without output buffer

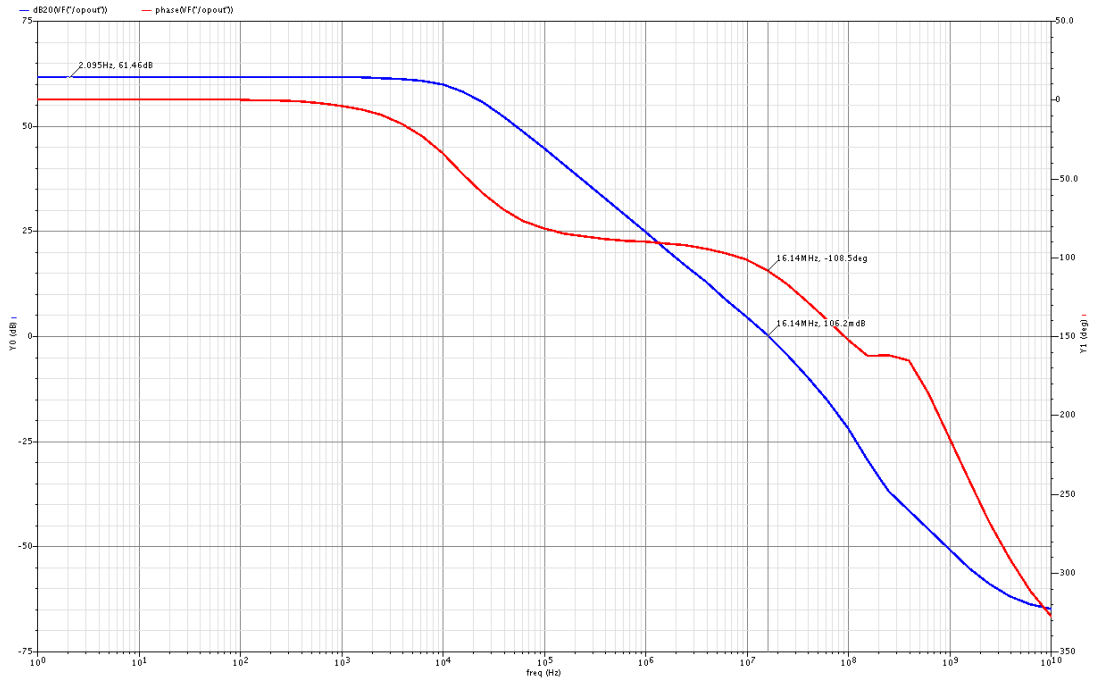
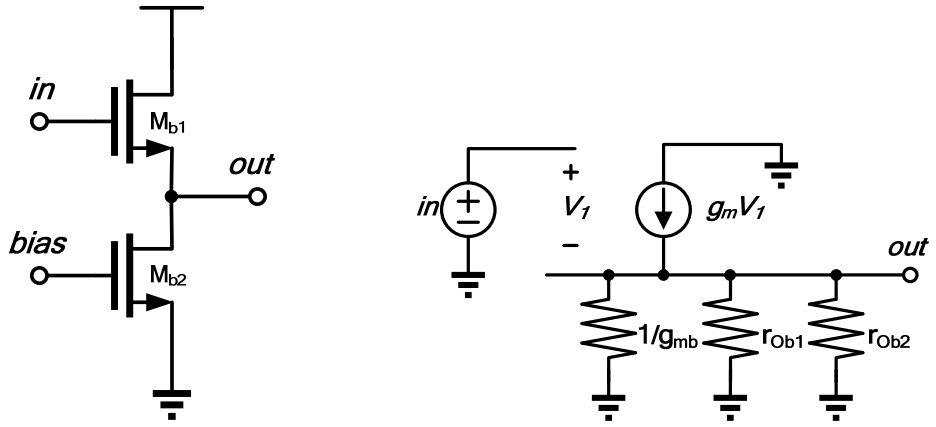


Fig. 4.6 Frequency response of the OP-Amp with output buffer



(a) (b)

Fig. 4.7 Common-drain output buffer (a) circuit. (b) small-signal equivalent circuit

4.2 Comparator Circuit

A comparator is a circuit that compares the instantaneous value of an analog input voltage with a reference voltage, and then generates a logic output level depending on whether the input is larger or smaller than the reference level.

As shown in Fig. 4.8, it is implemented by a source-coupled differential pair with positive feedback to provide a high gain. The gain of the positive feedback gain stage is given by

$$A_V = \sqrt{\frac{\mu_p(\frac{W}{L})_1}{\mu_n(\frac{W}{L})_3}} \times \frac{1}{1-\alpha} \tag{4.6}$$

where $\alpha=(W/L)_5/(W/L)_3$ is the positive feedback factor.

The inverter chains are used to increase the response of the output signal and pull the output to digital level. The inverter stage acts as a driver stage such that the size of M_7 and M_8 can be made smaller. With the smaller size of M_7 and M_8, the effect of the parasitic capacitance at the gates of M_7 and M_8 is decreased for a faster response.

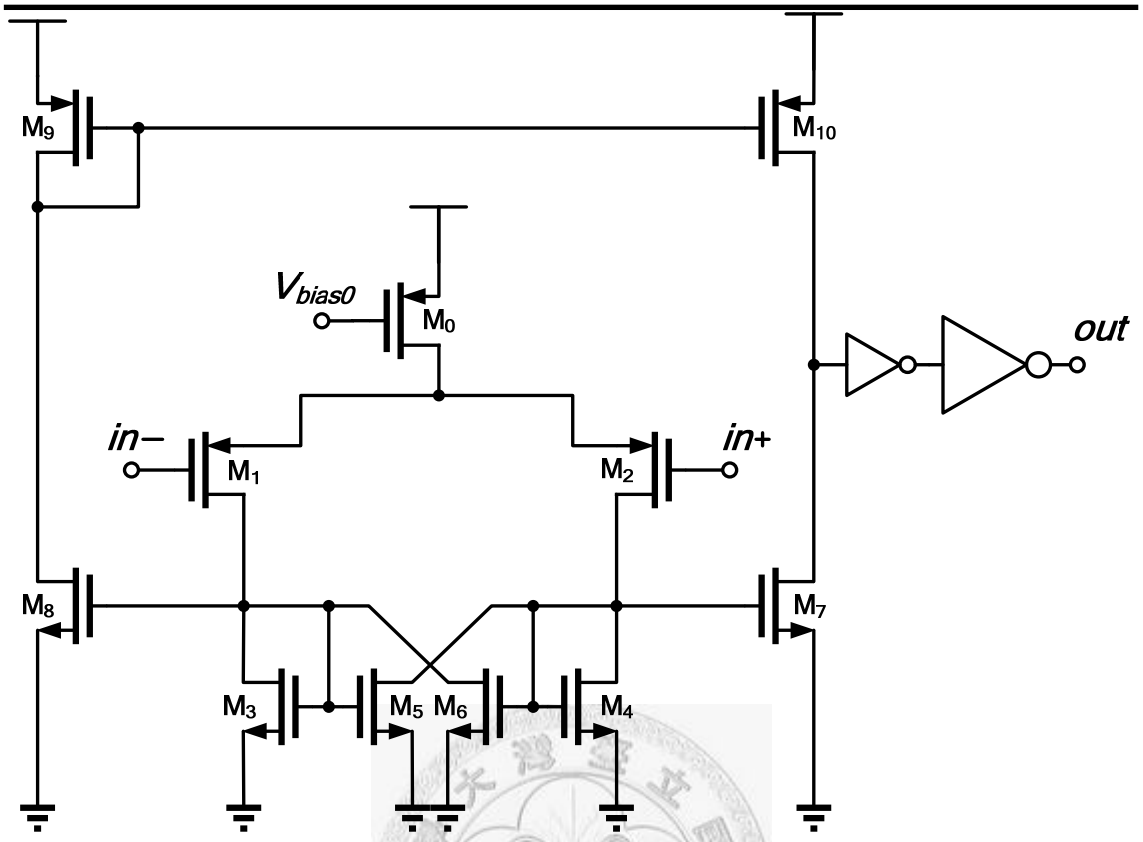


Fig. 4.8 Schematic of the comparator

The comparators are needed one for the PWM controller, two for the ramp generator circuit (*RampGen.0*), two for the detector and two for the calculated pulse circuit (*RampGen.1* and *RampGen.2*) in the ICAC block.

4.3 Ramp Generator Circuit

The ramp generator is the circuit which generates a ramp signal for PWM controller as shown in Fig. 4.9. To clamp the upper band V_{High} and lower band V_{Low}, there are two comparators and one SR latch in the right side of Fig. 4.9. The reference voltage V_{ref_ramp} provides a current i_t through a resistor R_t and i_t is given by

$$i_t = \frac{V_{ref\_ramp}}{R_t} \tag{4.7}$$

Then the current mirror copies i_t to charge the capacitor C_t to generate the ramp signal v_{ramp}. The comparators compare the amplitude of the ramp signal with V_{High} and V_{Low} to

turn on or turn off the transistor M_{disc} which is paralleled with C_t. When M_{disc} cuts off, current i_t charges the voltage of v_{ramp} up linearly to V_{High}, and then M_{disc} will turn on to discharge the voltage of v_{ramp} sharply back to V_{Low}. The charge stored in C_t is given by

$$Q = \frac{i_t}{f_{req}} = C_t \times (V_{High} - V_{Low}) \tag{4.8}$$

where f_{req} is the switching frequency of the buck converter, and hence

$$\frac{V_{ref\_ramp}}{(f_{req} \times R_t)} = C_t \times (V_{High} - V_{Low}) \tag{4.9}$$

to give the relationship of switching frequency of

$$f_{req} = \frac{1}{R_t C_t} \frac{V_{ref\_ramp}}{V_{High} - V_{Low}} \tag{4.10}$$

According to above equation (4.10), there are five choices to change the switching frequency in the buck converter. The passive components, R_t and C_t, are on-chip to shrink the area on PCB in this work so that they should be small. Here chooses changing the V_{ref_ramp} to vary the slope of ramp since there is a feedback OP at V_{ref_ramp} node for stability rather than V_{High} and V_{Low}.

The circuit and the truth table of SR latch used in this circuit are shown in Fig. 4.10 and Table 4.2.

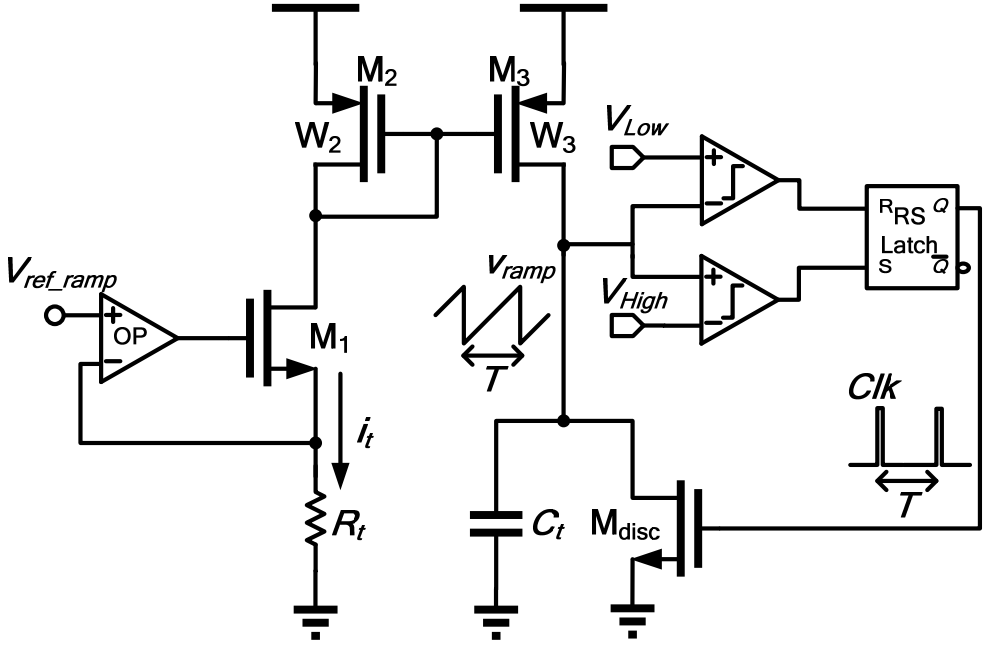


Fig. 4.9 Schematic of ramp generator

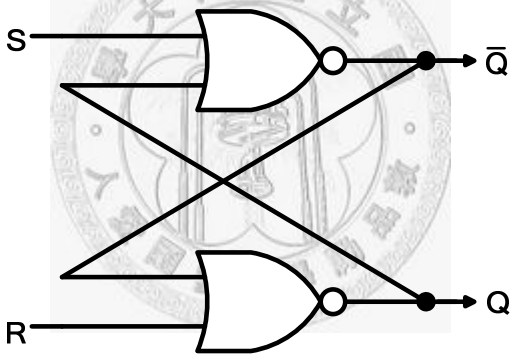


Fig. 4.10 The circuit of SR latch

Table 4.2 The truth table of SR latch

S	R	Q(n+1)	Qbar(n+1)
0	0	Q(n)	Qbar(n)
0	1	0	1
1	0	1	0
1	1	Forbidden	

Fig. 4.11 shows the ramp signal v_{ramp} and the control signal of $M_{disc,}$ Clk. V_{Low} is 0.1 V and V_{High} is 1 V. According to equation (4.10), the switching frequency is determined by the passive component values which are dependent on the process variation. Therefore, Fig. 4.12 shows the switching frequency considering FF, SS, and TT corners and 10% variation on the resistor R_t and capacitor C_t. The frequencies in these corners fit the specification of frequency (2-3 MHz)

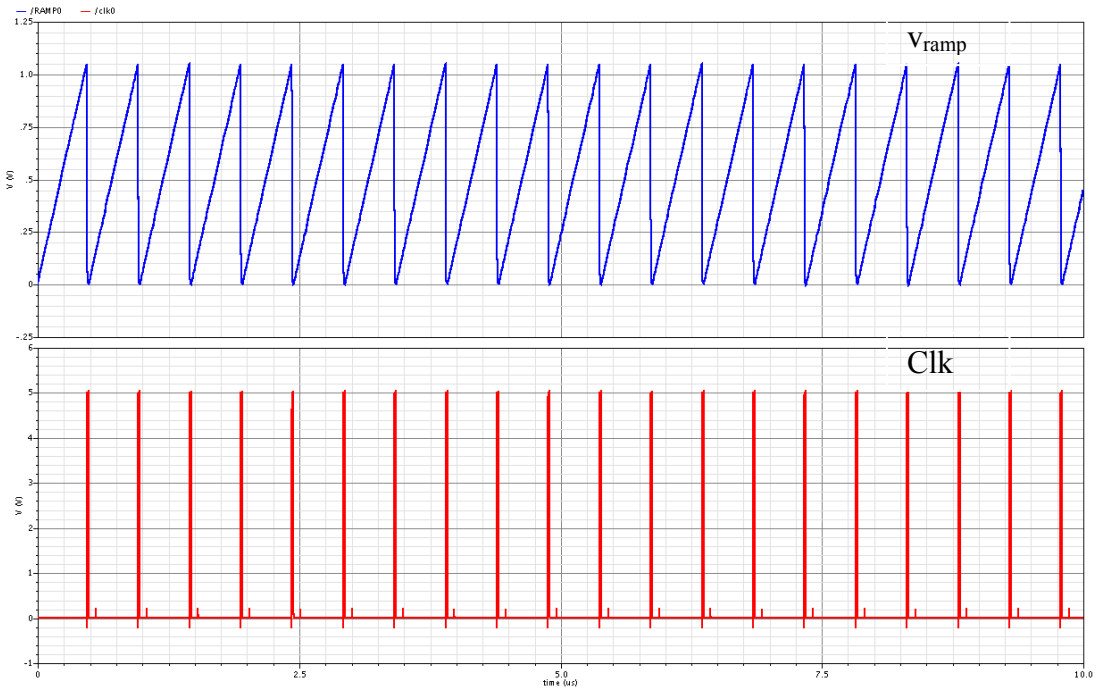


Fig. 4.11 The simulation result of ramp generator

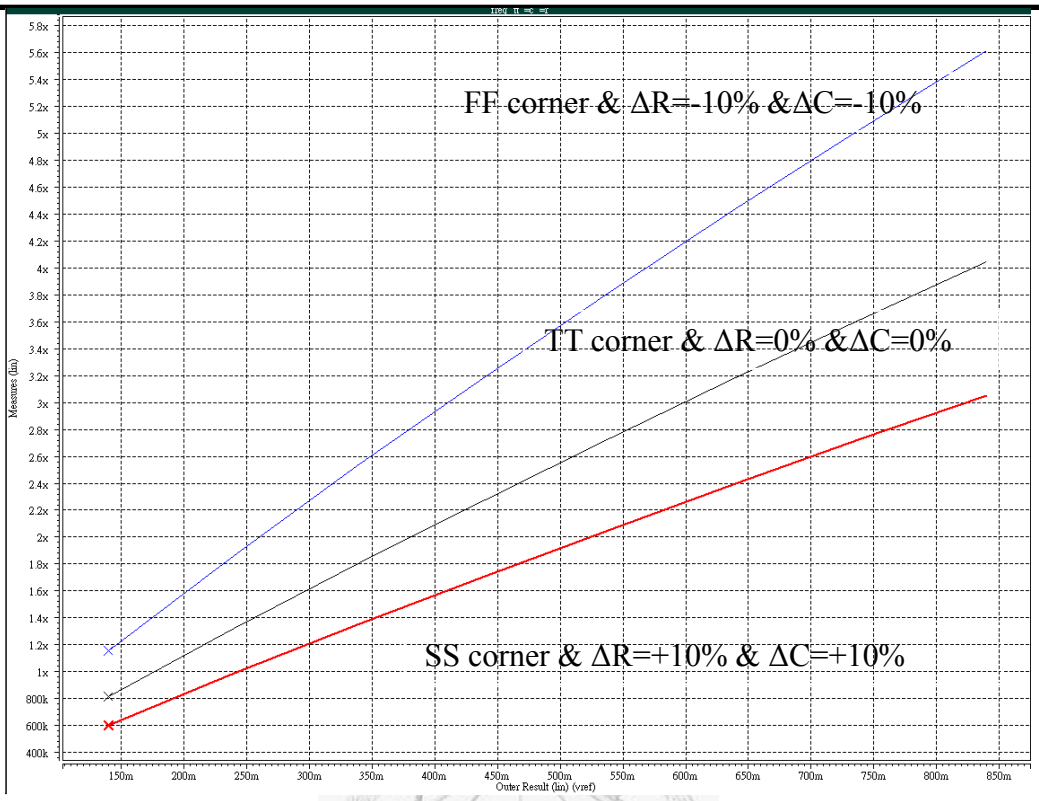


Fig. 4.12 The simulation of frequency considering process variation

4.4 Digital-to-Analog Converter (DAC)

There are two group 5-bit digital inputs in this work to control the output voltage and switching frequency respectively. To convert the digital inputs into an analog voltage used in Ramp generator and error amplifier, it uses DACs. As shown in Fig. 4.13, a current-steering array is utilized. The left side transfer the sum of current from branches through a current mirror circuit to the right side. Finally, the current transfers into an analog voltage by a resistor R_{fix2}. There are two identical DAC in this design, one is V_{ref_ea} for error amplifier (*EA*) and another is V_{ref_ramp} for Ramp generator (*RampGen.0*). Its output voltage is given by

$$V_{ref\_ea}(or V_{ref\_ramp}) = V_{ref}\left(\frac{D_{bit4}}{R_{d4}} + \cdots + \frac{D_{bit0}}{R_{d0}} + \frac{1}{R_{fix1}}\right)R_{fix2} \qquad (4.11)$$

The INL and DNL are shown in Fig. 4.14. It could be observed that ±0.17 LSB for DNL and ±0.14 LSB for INL.

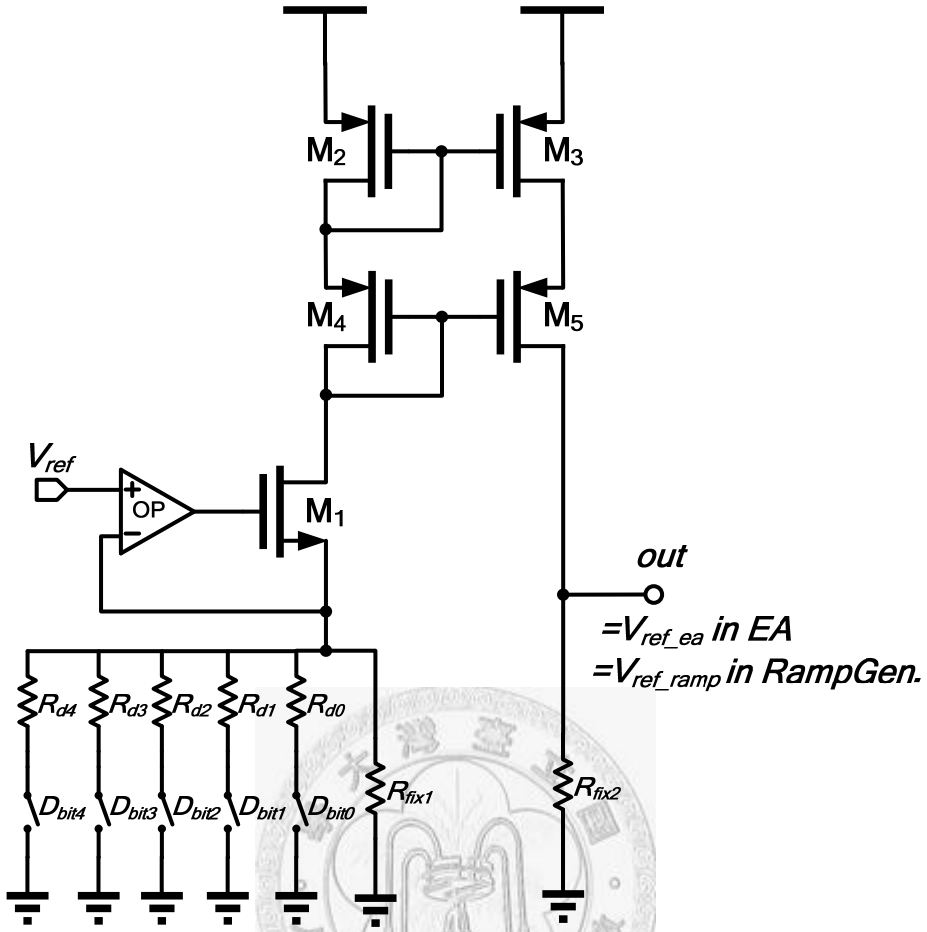


Fig. 4.13 Schematic of DAC

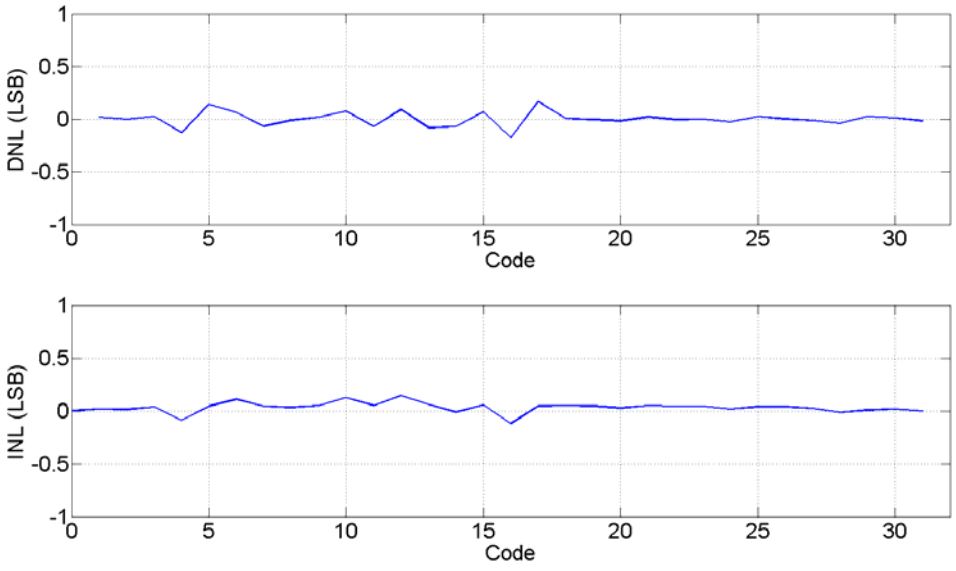


Fig. 4.14 INL and DNL of DAC

4.5 Inductor Current Average Control (ICAC)

This circuit is the key to complete the inductor current average control method. According to the analysis in Chapter 3, it needs an additional pulse which pulse width equals T_X. To implement this pulse, there are two parts, sample and hold (S&H) circuit and calculated pulse circuit. If there is no S&H, the signal of hopping triggers the v_{ramp} changing slope synchronously as shown in Fig. 4.15. It causes a random shape ramp with two different slopes and an unpredicted period when hopping signal arrives. The unpredicted period of off cycle $T_{off,unknown}$ perhaps equals $T_{off,2}$ when the "Hopping Signal" arrives before v_{ramp} over v_A, but the unpredicted period of on cycle $T_{on,unknown}$ becomes a random interval depending on the ratio between two different slope of v_{ramp} as depicted in Fig. 4.15. On the other hand, the $T_{on,unknown}$ perhaps equals $T_{on,1}$ when the "Hopping Signal" arrives after v_{ramp} over v_A, but $T_{off,unknown}$ becomes a random interval depending on the ratio between two different slope of v_{ramp}. As it uses a S&H circuit in frond end of V_{ref_ramp}, we can choose the time we want to hop the frequency of v_{ramp} without two slope in one period of v_{ramp}. All we have to do is turn off the v_{ramp} during the arrival of "Hopping Signal" and insert a calculated-width pulse D_{Tx} to be a pseudo period in v_{PWM} as shown in Fig. 4.16. It also relaxes the settling time of V_{ref_ramp}. V_{ref_ramp} needs a few nanoseconds without S&H, but D_{Tx} around hundred nanoseconds with S&H giving V_{ref_ramp} more time to settle.

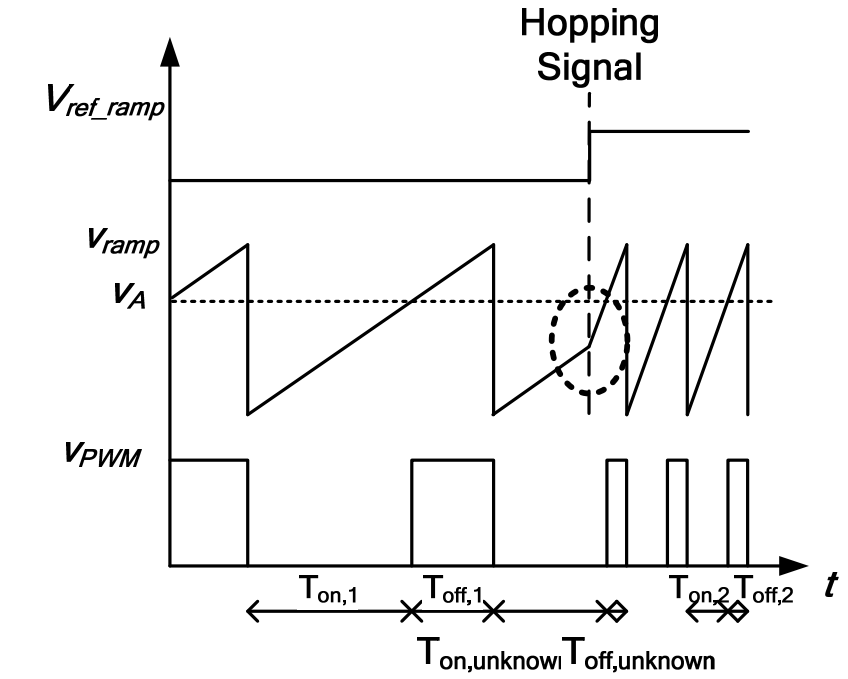


Fig. 4.15 Ramp generator without S&H in front end

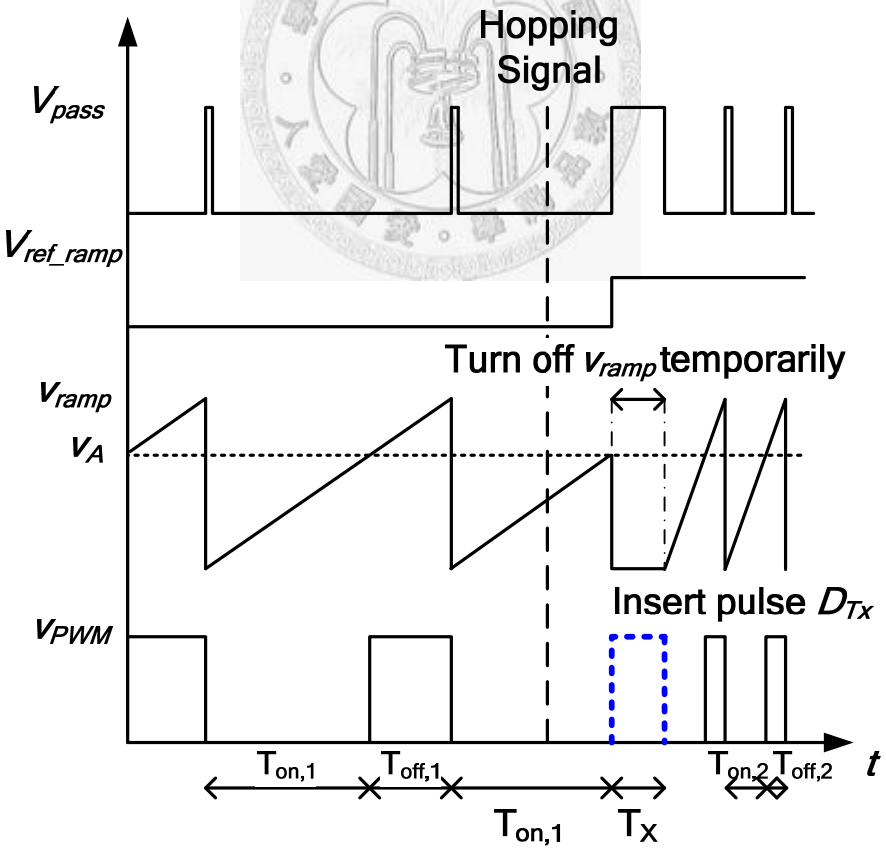


Fig. 4.16 Ramp generator with S&H in front end and calculated pulse circuit in parallel

4.5.1 Sample and Hold Circuit (S&H)

It utilizes a simple RC circuit to complete sample and hold (S&H) circuit where V_{ref_ramp} is the input of S&H, V_{ref_rampQ} is the output of S&H and V_{pass} is the control signal of sample phase as shown in Fig. 4.17. In Fig. 4.18, a detector circuit which detects if the V_{ref_ramp} changes is implemented with dual comparators and one XOR logic gate. Its output signal *Change* represents that a "Hopping Signal" arrives to trigger DAC of V_{ref_ramp} to change V_{ref_ramp} larger or smaller synchronously. Note that larger V_{ref_ramp} means higher frequency of v_{ramp}. We give attention to the V_{pass} of S&H in this paragraph.

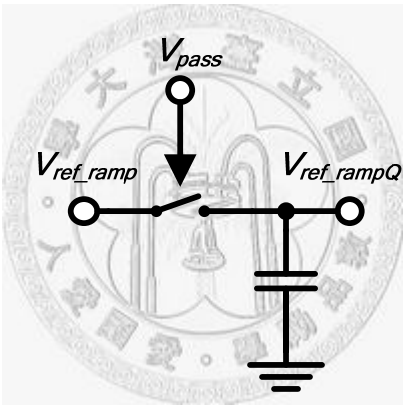


Fig. 4.17 Circuit of the sample and hold

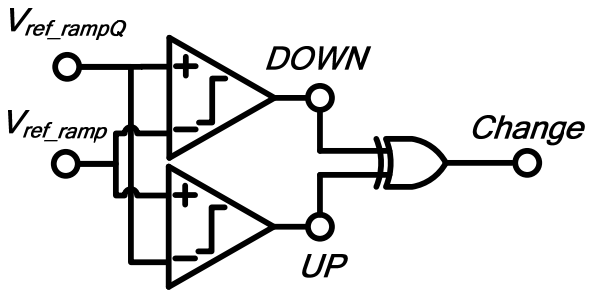


Fig. 4.18 Diagram of the detector of hopping

As illustrate in Fig. 4.19, there are three paths, Best Case Path, Worst Case Path and Normal Case Path. (1) In Normal Case Path, it turns on V_{pass} fully by SW_{Best}=0 and SW_{Worst}=0. It causes that V_{ref_rampQ} changes whenever V_{ref_ramp} changes like shown in Fig. 4.15. (2) In Worst Case Path, V_{pass} turns on at the rising edge of v_{PWM}. It represents the

frequency hops at the moment where the inductor current reaches peak value. By this way, the transient ripple gets the worst and largest voltage. (3) In Best Case Path, V_{pass} turns on as the same as *Clk* when *Change*=0($\overline{Change}$=1). *Clk* is the gate of M_{disc} in the Ramp generator circuit in Fig. 4.9 and is the discharging phase of v_{ramp}. While the *Change* detects the difference between V_{ref_ramp} and V_{ref_rampQ}, it masks *Clk* by AND logic gate. During *Change*=1, V_{pass} is triggered by $D_{Rampcomp1}$. $D_{Rampcomp1}$ is the rising edge of D_{Tx} and the width of D_{Tx} will be discussed later.

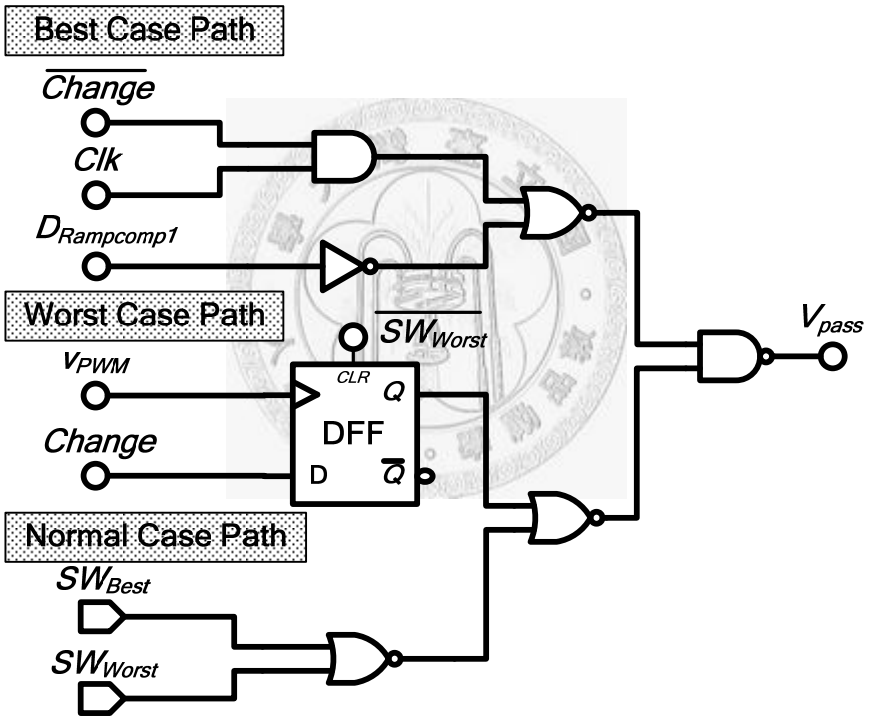


Fig. 4.19 Diagram of the control signal of sample time

Table 4.3 Conclusion of control signal of sample time

Case	SW_{Best}	SW_{Worst}	V_{pass}
Normal	0	0	Always high
Best	1	0	=*Clk* as not hopping =$D_{Rampcomp1}$ as hopping
Worst	0	1	=*Clk* as not hopping =v_{PWM} as hopping
X	1	1	X

4.5.2 Calculated Pulse Circuit

A calculate-width pulse D_{Tx} is analyzed in this paragraph. The width (or time length) of this pulse must equal to T_X =0.5($T_{off,1}$+$T_{off,2}$) in Equation (3.8). It is composed by two parts, half of off duty cycle period of the previous frequency 0.5$T_{off,1}$ and half of off duty cycle period of the following frequency 0.5$T_{off,2}$. From Fig. 4.20, we have

$$\frac{dv_{ramp}}{dt} = \frac{i_t}{C_t} = \frac{V_{ref\_ramp}}{R_t C_t} \tag{4.12}$$

$$T_{off} = \frac{R_t C_t}{V_{ref\_ramp}} \times (V_{High} - v_A) \tag{4.13}$$

$$\frac{1}{2} T_{off} = \frac{R_t C_t}{V_{ref\_ramp}} \times \frac{1}{2} (V_{High} - v_A) \tag{4.14}$$

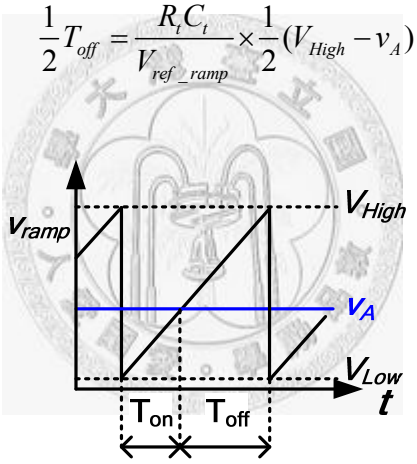
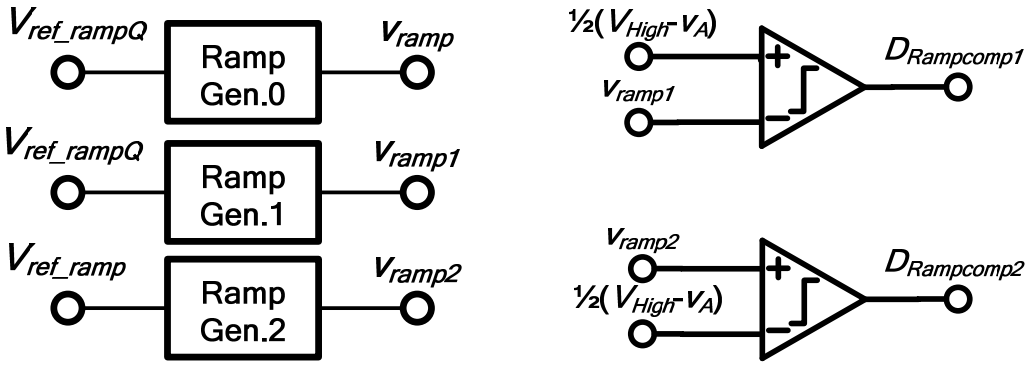


Fig. 4.20 Relationship between voltage and time length in a ramp signal

According to Equation (4.14), as long as we have the half of difference between V_{High} and v_A, we obtain 0.5$T_{off,1}$ and 0.5$T_{off,2}$ by given V_{ref_rampQ} and V_{ref_ramp}. Therefore it needs two additional ramp generators to implement as shown in Fig. 4.21(a). In these three ramp generators, it utilizes the same value of resistors R_t, R_{t2} and capacitors C_t, C_{t1}, C_{t2} to keep the only vary factor V_{ref_ramp} of v_{ramp}. By careful layout such as common centroid, we expect it should have good matching between these passive components. v_{ramp1} is the output of the first additional ramp generator (*RampGen.1*), and it has the same slope as original v_{ramp} due to the held input V_{ref_rampQ}. v_{ramp2} is the output of the second additional

ramp generator (*RampGen.2*), and it has the slope of following ramp signal due to the unheld input V_{ref_ramp}. In Fig. 4.21(b), $D_{Rampcomp1}$ is triggered at the time $0.5T_{off,1}$ and $D_{Rampcomp2}$ is triggered at the time $0.5T_{off,2}$.



(a) (b)

Fig. 4.21 (a) Diagram of the additional ramp generators (b) Output of additional ramp generators

The complete circuit of ICAC is separated into analog part and digital part. The analog part is shown in Fig. 4.22 and the digital part is shown in Fig. 4.23. It shows more detail of Fig. 4.21 such as reset signal and the used passive components. The transient waveform is shown in Fig. 4.24. The discharging transistor M_{disc} in *RampGen.0* is triggered by *Clk* in steady state or D_{Tx} in frequency hopping state. When M_{disc} is triggered by D_{Tx}, it means that v_{ramp} resets when the calculated pulse is inserted in the circuit. By this operation, v_{PWM} is only determined by the calculated pulse in frequency hopping state. The discharging transistor M_{disc1} in *RampGen.1* is triggered by $\overline{D_{Tx}}$ and then v_{ramp1} starts. $D_{Rampcomp1}$ calculates $0.5T_{off,1}$ by comparing v_{ramp1} with $0.5(V_{High}\text{-}v_A)$ and then it triggers the discharging transistor M_{disc2} in *RampGen.2*. $D_{Rampcomp2}$ calculates $0.5T_{off,2}$ by comparing V_{ramp2} with $0.5(V_{High}\text{-}v_A)$. Finally, $D_{Rampcomp2}$ ends the D_{Tx} and completes the ICAC as shown in Fig. 4.23.

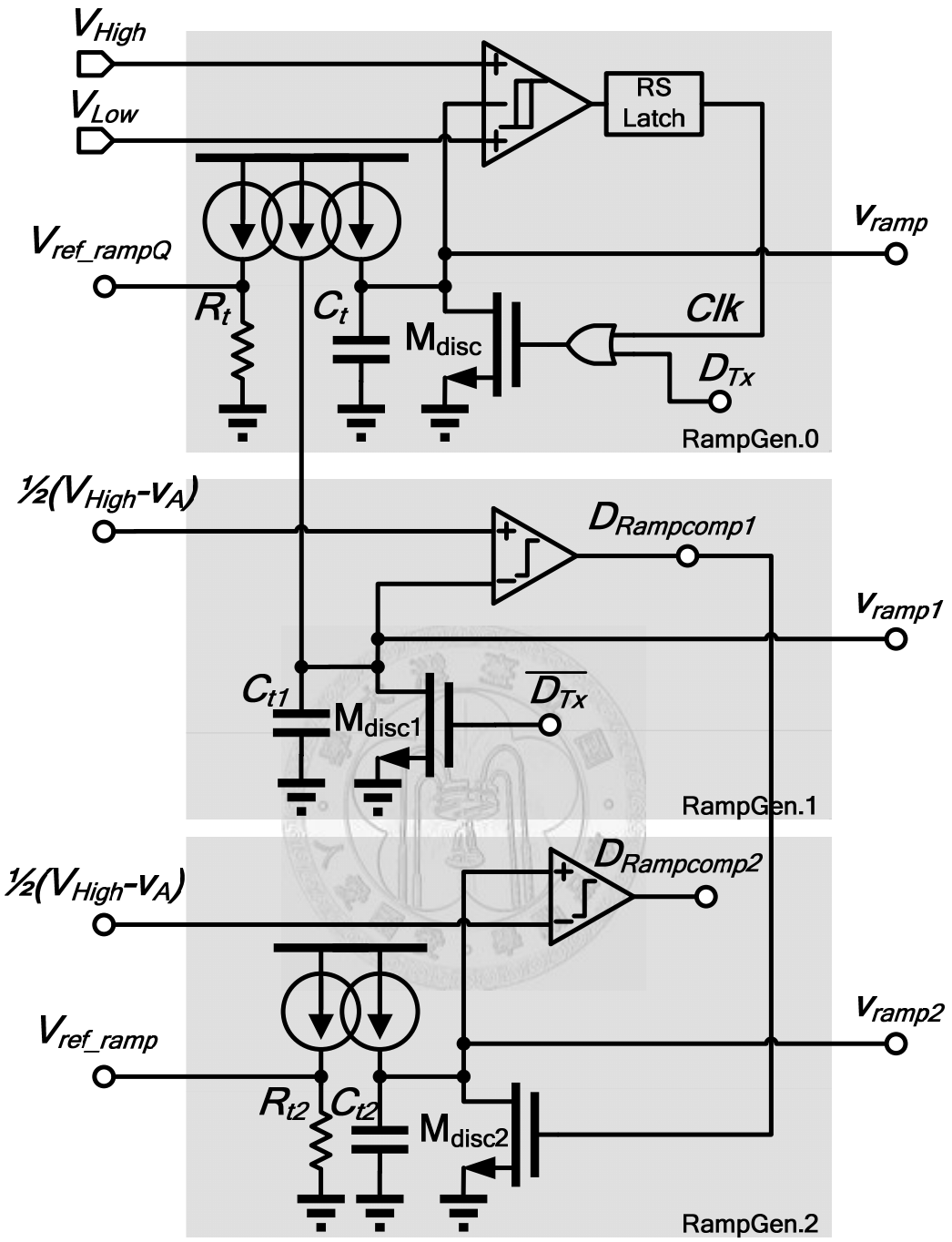


Fig. 4.22 Diagram of full Ramp generators

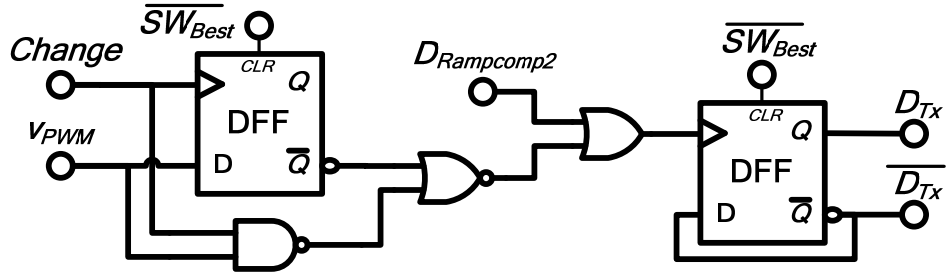


Fig. 4.23 Diagram of the calculated-width pulse circuit

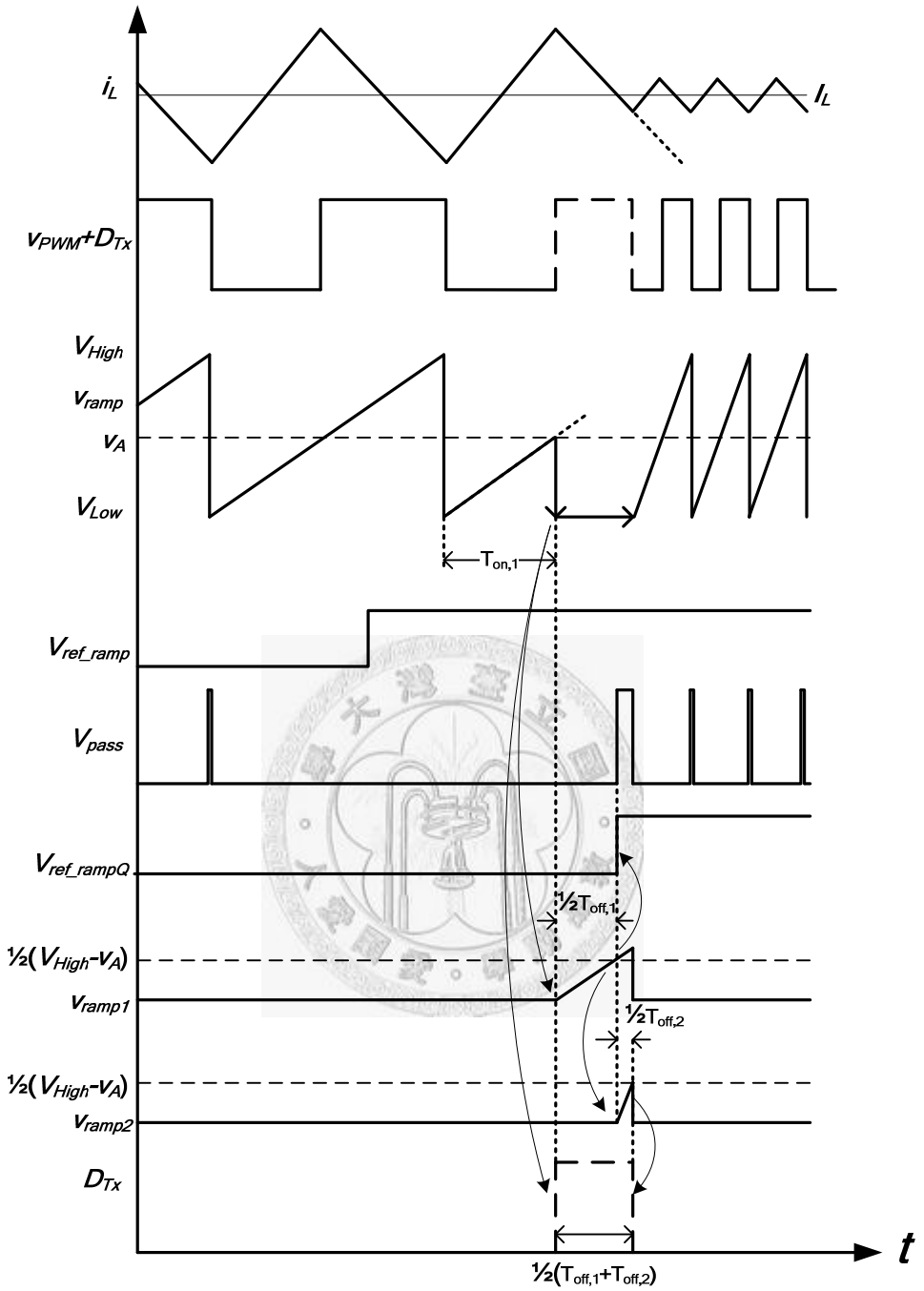


Fig. 4.24 Transient waveform of ICAC

4.5.3 Consideration of Delay Time

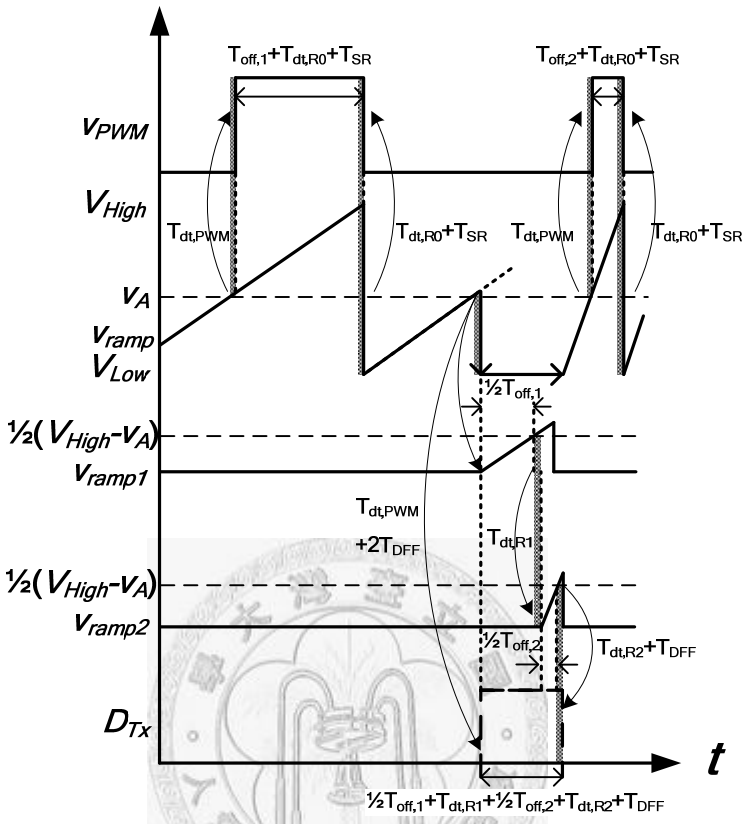


Fig. 4.25 Waveform of calculated pulse including delay of components

Since the technique is used in time domain, the delay time must design carefully. The comparators are the main delay time of the calculated pulse. Fig. 4.25 depicts the more detailed information for calculated pulse from Fig. 4.24. According to aforementioned analysis in Fig. 4.24, the rising edge of D_{Tx} passes through one PWM controller and two DFF. During the D_{Tx}=1, there is one comparator between *RampGen.1* and *RampGen.2*. The falling edge of D_{Tx} passes through one comparator of *RampGen.2* and one DFF. The total width of D_{Tx} including delay time is

$$\frac{1}{2}T_{off,1}+T_{dt,R1}+\frac{1}{2}T_{off,2}+T_{dt,R2}+T_{DFF} \tag{4.15}$$

where $T_{dt,R1}$ is the delay time of comparator in *RampGen.1*, $T_{dt,R2}$ is the delay time of comparator in *RampGen.2*, and T_{DFF} is the delay time of DFF. The concept of D_{Tx} is in

order to complete the average of the off duty cycle period before hopping and after hopping. The off duty cycle period before hopping including delay time is $T_{off,1}+T_{dt,R0}+T_{SR}$. The off duty cycle period after hopping including delay time is $T_{off,2}+T_{dt,R0}+T_{SR}$. $T_{dt,R0}$ is the delay time of the upper band comparator in front of the SR-Latch and T_{SR} is the delay time of the SR-Latch both in *RampGen.0*. The average of the off duty cycle period before hopping and after hopping is

$$\frac{1}{2}[(T_{off,1}+T_{dt,R0}+T_{SR})+(T_{off,2}+T_{dt,R0}+T_{SR})]=\frac{1}{2}T_{off,1}+\frac{1}{2}T_{off,2}+T_{dt,R0}+T_{SR} \tag{4.16}$$

Compare (4.15) with (4.16) and ignore the delay time of SR-Latch T_{SR} which is about a few picoseconds.

$$T_{dt,R1}+T_{dt,R2}+T_{DFF}=T_{dt,R0} \tag{4.17}$$

Use the same comparators in *RampGen.1* and *RampGen.2*.

$$T_{dt,R1}=T_{dt,R2}=T_{dt,R1,2} \tag{4.18}$$

$$2T_{dt,R1,2}+T_{DFF}=T_{dt,R0} \tag{4.19}$$

These comparators all compare a ramp signal with a dc voltage except for the detector. Due to the linearity of ramp signal, we can design the offset voltage of the comparators V_{offset} to determine the delay time easily. We have the offset voltage from [13]

$$V_{offset}=(V_{TH,1}-V_{TH,2})+(\sqrt{\frac{2I_{D1}}{k'(\frac{W}{L})_1}}-\sqrt{\frac{2I_{D2}}{k'(\frac{W}{L})_2}}) \tag{4.20}$$

$$\begin{cases} I_{D1}=I_D+\Delta I_D \\ I_{D2}=I_D-\Delta I_D \end{cases} \tag{4.21}$$

Substituting (4.21) into (4.20) gives

$$=\Delta V_{TH}+\sqrt{I_D}(\sqrt{\frac{2(1+\Delta I_D/I_D)}{k'(W/L)_1}}-\sqrt{\frac{2(1-\Delta I_D/I_D)}{k'(W/L)_2}}) \tag{4.22}$$

The offset voltage is proportional to the square root of I_D. Thus, we only have to change the tail current to set the delay time.

The delay time and offset voltage of comparators are listed in Table 4.4 and shown in Fig. 4.26. In this work, $T_{dt,R1,2}$ is the delay time of $Comp_{fast}$ which is used in *RampGen.1* and *RampGen.2* and $T_{dt,R0}$ is the delay time of $Comp_{slow}$ which is used in the upper band comparator in *RampGen.0*. $Comp_{mid}$ is used in PWM controller and $Comp_{withoffset}$ is used in detector circuit to avoid noise. The delay time of logic gates are listed in Table 4.5.

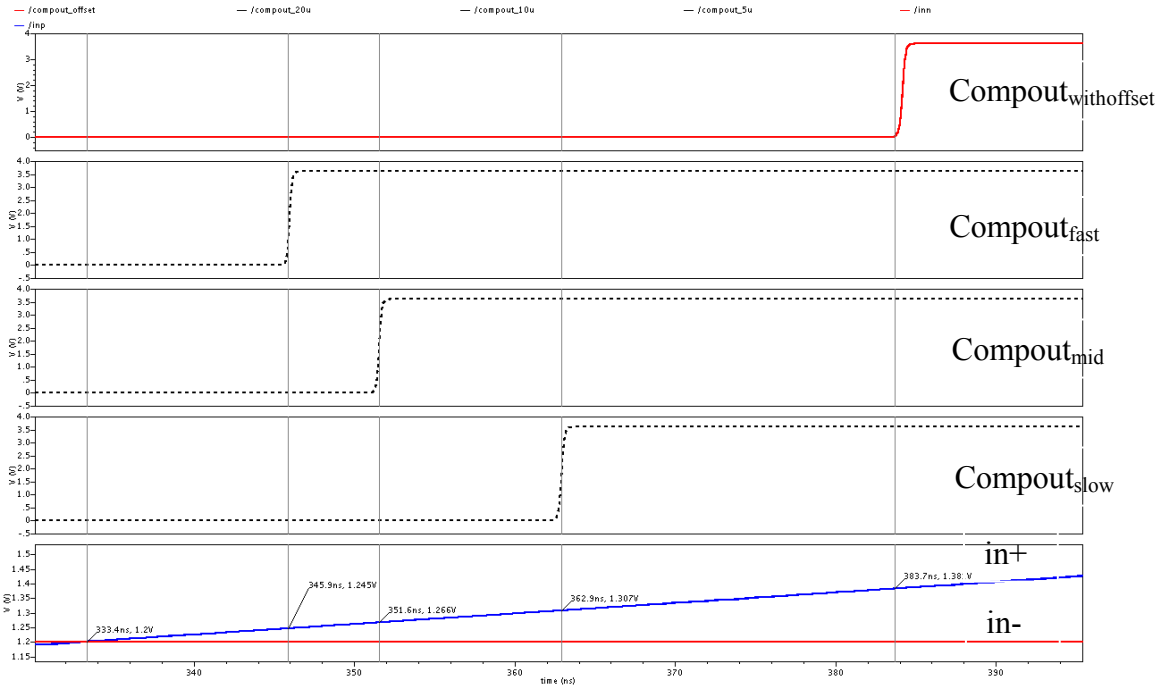


Fig. 4.26 Transient waveform of offset of the comparator

Table 4.4 Delay time of comparators

	Delay Time	Offset
$Comp_{withoffset}$	50.3ns	180mV
$Comp_{fast}$	12.5ns	45mV
$Comp_{mid}$	18.2ns	66mV
$Comp_{slow}$	29.5ns	107mV

Table 4.5 Delay time of logic gate circuits

	Delay Time
Inverter	~ps
NAND	~ps
NOR	~ps
SR-Latch	~ps
DFF	4.5ns

4.6 Gate Driver with Dead Time Control

The width over length of the two power transistors of DC-DC buck converters must be large in order to reduce conduction loss. Due to the large size of these two transistors, the capacitive load of PWM controller has become very large. Therefore, a driver with the enough driving capability is required between PWM controller and power transistors. Conventional tapered CMOS buffer consumes the short-circuit power due to simultaneous turn on of the two power transistors. Short-circuit power consumption can be eliminated by a driver with dead time control as shown in Fig. 4.27.

The basic operation principle of this buffer is to confirm that one power transistor turns on after the other power transistor turns off by using the feedback signal at V_{pin}, V_{nin} and the delay line of inverter chain. The delay line increases width by stage since M_1-M_6 is still large. Therefore, the power transistors do not turn on simultaneously, and then the short circuit is not caused in any condition.

When the input signal v_{PWM} falls from V_{DD} to G_{ND}, the internal node N_1 rises from G_{ND} to V_{DD} and turning on M_6 causing node V_{nin} falls from V_{DD} to G_{ND} firstly. V_{nin} is the gate voltage of power transistor M_N and M_N is turned off. Then the node N_2 triggered by V_{nin} after some delay. V_{pin} falls to G_{ND} at last. This flow guarantees the power transistor M_P turns on after the power transistor M_N turns off.

When the input signal v_{PWM} rises from G_{ND} to V_{DD}, the internal node N_1 falls from

V_{DD} to G_{ND} and turning on M_1 causing node V_{pin} rises from G_{ND} to V_{DD}. V_{pin} is the gate voltage of power transistor M_P and M_P is turned off firstly. By similar above analysis, the power transistor M_N turns on after the power transistor M_P turns off.

Fig. 4.28 shows the simulation result of the gate driver with dead time control. I_P and I_N are the current of M_P and M_N respectively. The dead-time control works since there is no short current in M_P or M_N.

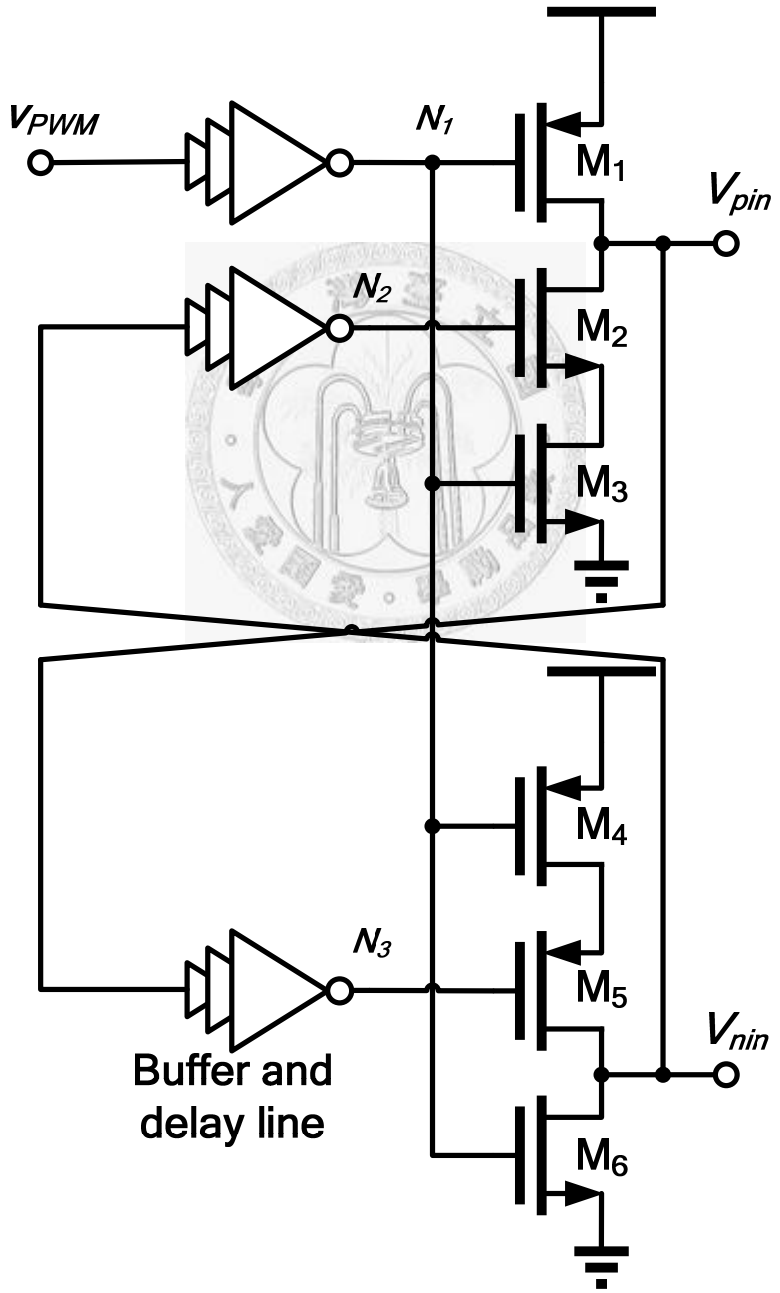


Fig. 4.27 Schematic of the gate driver with dead time control

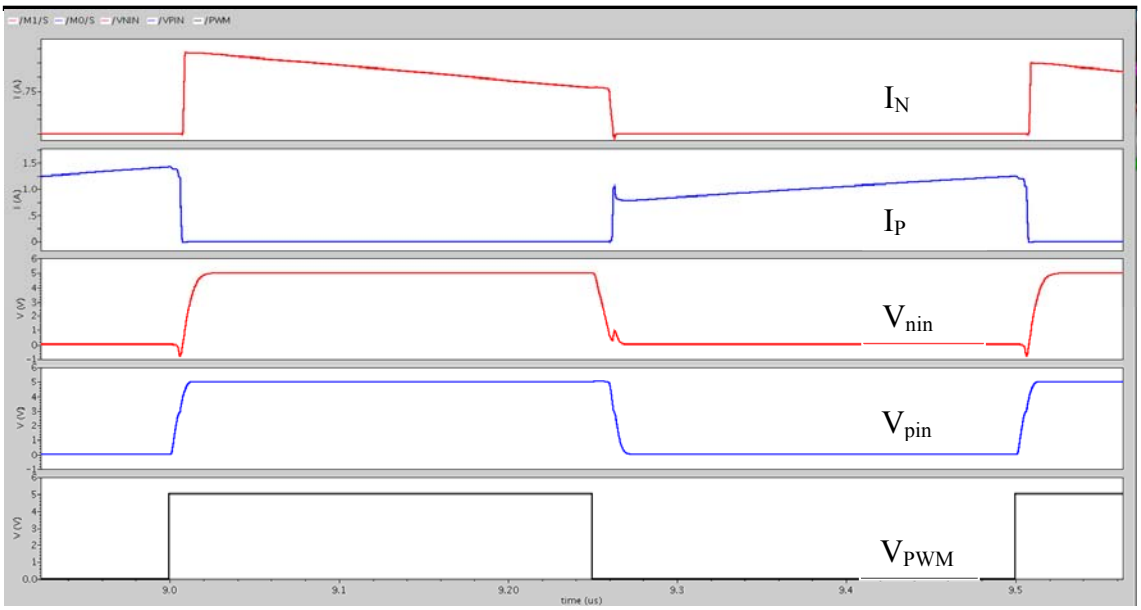


Fig. 4.28 The simulation result of the gate driver with dead time control

4.7 Power Stage Circuit

The power stage is formed by two power transistors (M_P and M_N), an inductor L_O and a filtering capacitor C_O as shown in Fig. 4.29. These components are flowed with large current by the loading such as power amplifiers. The inductor and the capacitor are off-chip. Therefore, the power transistors are the only circuit flowed a large current in the chip. It passes current from V_{in} and G_{ND} to L_X which is determined by V_{pin} and V_{nin}. The control signal V_{pin} and V_{nin} are non-overlapped from the gate driver with dead time control as above mention. We must design and layout it carefully to avoid burning the chip for reliability.

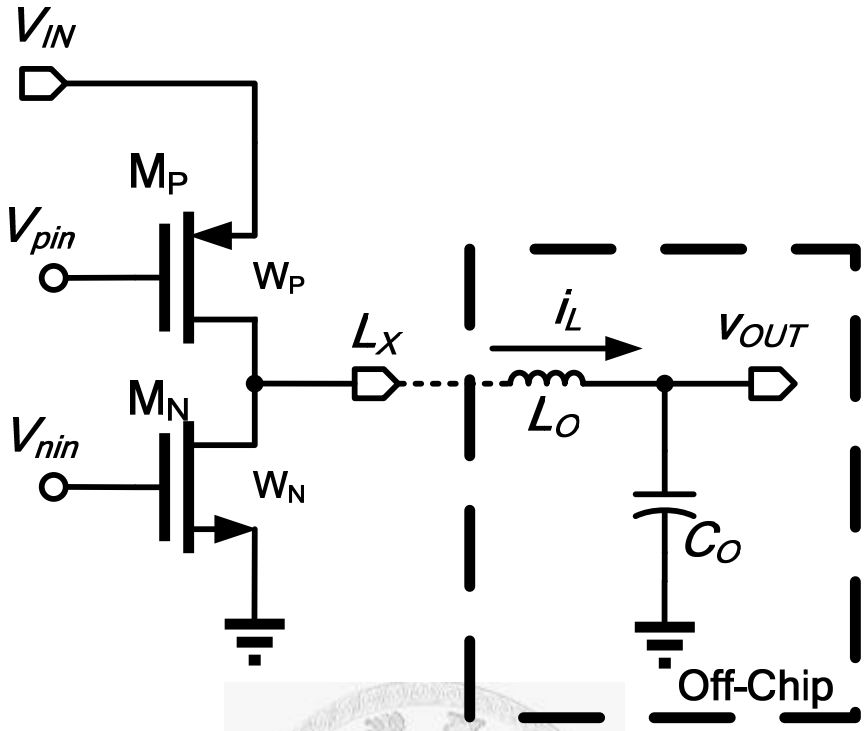


Fig. 4.29 Schematic of the power stage

Firstly, the transistors operate in triode region for switched-mode DC-DC converter. The width W over length L of the transistors determines the on-resistance (4.23) and the current capability (4.24).

$$R_{on} = \frac{1}{\mu C_{OX} \frac{W}{L}(V_{GS} - V_{TH})} \tag{4.23}$$

$$I_D = \mu C_{OX} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{\ 2}] \tag{4.24}$$

The width and length mean the gate capacitance of the transistor. To reduce the switching loss, the length is chosen the minimum length of the process and the width is tuned the minimum enough to provide the load current. There is an intelligent method to tune the width. Turn on the PMOS or NMOS fully, and then sweep the width to measure the on-resistance of the PMOS or NMOS. Fig. 4.30 shows the simulation result. In this simulation, it fixes the width and sweeps the number of finger due to the convenience of layout. The chosen width and length of power transistors in this work are shown in Table 4.6.

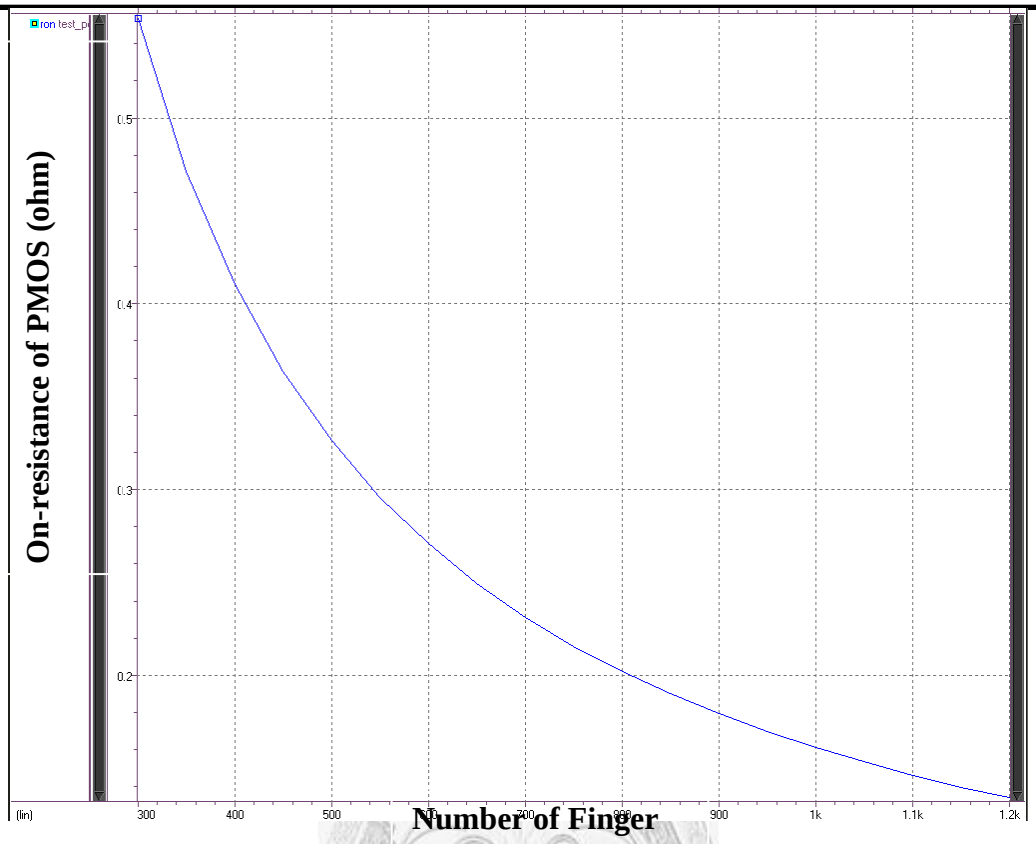


Fig. 4.30 Simulation of on-resistance of PMOS

Secondly, the layout of the power transistors must consider the current path and maximum current density of metal. The floor plan of power transistor in this work is shown in Fig. 4.31. Since the power stage is a 3-port circuit, the T-shape layout is the best solution. The PMOS passes the current from V_{IN} to L_X and the NMOS passes the same current from G_{ND} to L_X. The resistance on the current path must be calculated totally including the resistance of metal to obtain the voltage of L_X (4.25) and (4.26). They are listed in Table 4.7.

$$V_{Lx} = V_{IN} - R_{P,total} \times I_{D,P} \quad \text{as PMOS on} \tag{4.25}$$

$$V_{Lx} = R_{N,total} \times I_{D,N} \quad \text{as NMOS on} \tag{4.26}$$

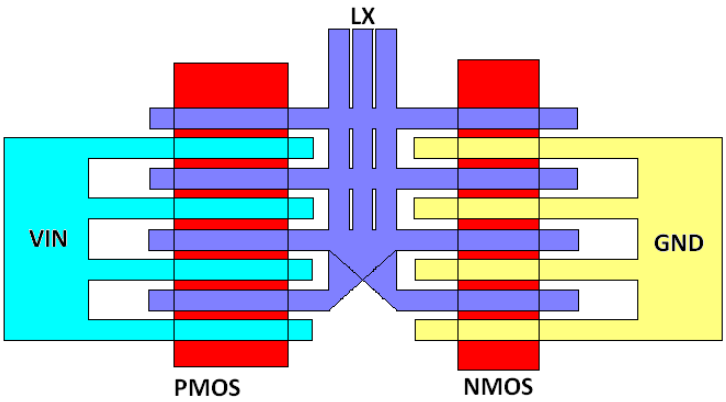


Fig. 4.31 Floor plan of the power stage on chip

Table 4.6 Size of power transistors

	Width (μm)	Length (μm)
Power PMOS	56,000	0.5
Power NMOS	24,000	0.5

Table 4.7 Resistance of power stage

Resistance	Value (mΩ)
node(V_{in})-node(Source of M_P) of Metal	18.5
Ron of M_P	160
Metal on M_P	43
node(Drain of M_P)-node(L_X) of Metal	29
node(L_X)-node(Drain of M_N) of Metal	29
Ron of M_N	100
Metal on M_N	14
node(L_X)-node(Source of M_N) of Metal	7
Total resistance node(V_{in}) -node(L_X)	250
Total resistance node(L_X)-node(G_{ND})	150

4.8 Simulation Results

This section describes simulation results of the designed DC-DC buck converter. The parasitic components are also included to make the simulation more believable. The design parameters and the pin connections of the simulation are given in Table 4.8, and the voltages such as threshold voltages, reference voltages are input by outside control.

Table 4.8 Design parameters and pin connections of the simulation

Supply and Bias	Value
V_{IN}	5 V
GND	0 V
V_{DD_A}	5 V
V_{SS_A}	0 V
V_{DD_D}	5 V
V_{SS_D}	0 V
V_{High}	1 V
V_{Low}	0.1 V
V_{ref}	0.4 V
I_{ea}	0.4 μA
$I_{OP(slow)}$/ $I_{OP(fast)}$	2 μA/5 μA
Passive Components	Value
R_{f1}	80 kΩ
R_{f2}	20 kΩ
R_t& R_{t1}& R_{t2}	35 kΩ
C_t& C_{t1}& C_{t2}	6 pF
R_{d0_f}& R_{d0_v}	80 kΩ
R_{d1_f}& R_{d1_v}	40 kΩ
R_{d2_f}& R_{d2_v}	20 kΩ
R_{d3_f}& R_{d3_v}	10 kΩ
R_{d4_f}& R_{d4_v}	5 kΩ
R_{fix1}	5 kΩ
R_{fix2}	4 kΩ
R_{s1}	20 kΩ
R_{s2}	40 kΩ
C_C	42 pF
Off-Chip Components	Value
Output Inductor, L_O	1 μH
Output Capacitor, C_O	1 μF
Max. output current, I_O	450 mA
Other Spec.	Value
Switching frequency, f_s	0.8-3.4 MHz

4.8.1 Frequency Hopping

There are two parts to represent the simulation results of frequency hopping. Firstly, using fast Fourier transform (FFT) with Hamming window prove the reduced spur on spectrum. Secondly, the transient ripple on the output voltage could be observed from the transient waveform.

4.8.1.1 Spectrum

As aforementioned operation, the ICAC controller is triggered when the frequency of the ramp generator hops. Then, it modulates the time length of the on/off cycle period between two hopping frequencies, f_1 and f_2, to be T_X. All the following simulation results are based on the case of hopping in the off duty cycle period.

A comparison of output spectrums between conventional and proposed FH converters is shown in Fig. 4.32. The undesired spur at f_{trans} =159 kHz of the conventional converter is almost higher than the magnitudes at the hopping tones, f_1=2.1 MHz and f_2=2.9 MHz. The proposed ICAC controller can effectively reduce the spur and the maximum reduction is 18.9 dB. Fig. 4.33 depicts that the magnitude of undesired spur at f_{trans} increase as Δf, the difference between f_1 and f_2, increases. The spur is suppressed 15-19 dB with ICAC within the range of 400 kHz to 3.2MHz.

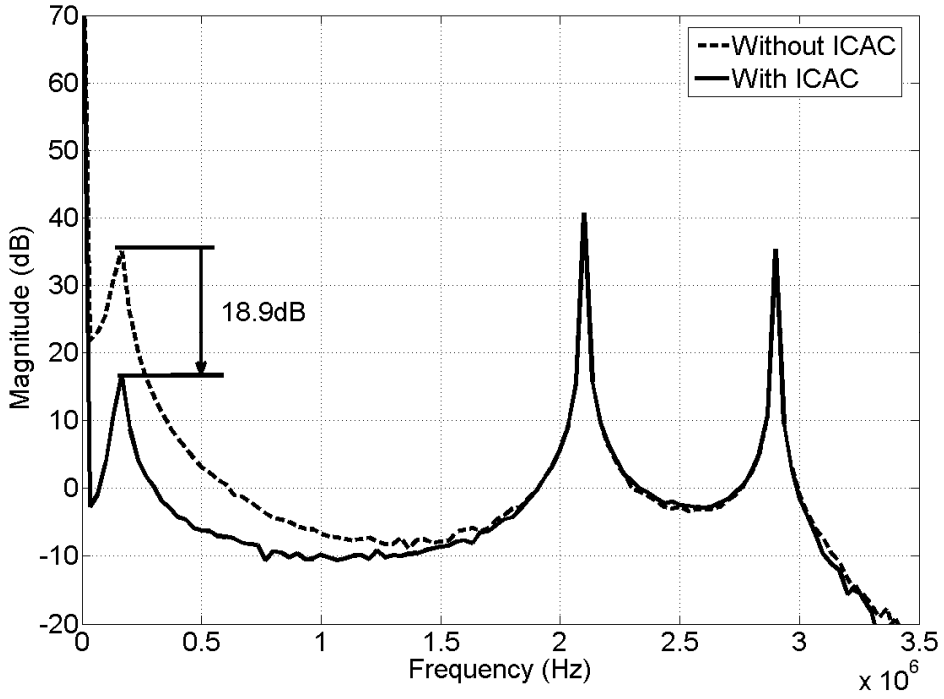


Fig. 4.32 Output spectrums of the buck converter

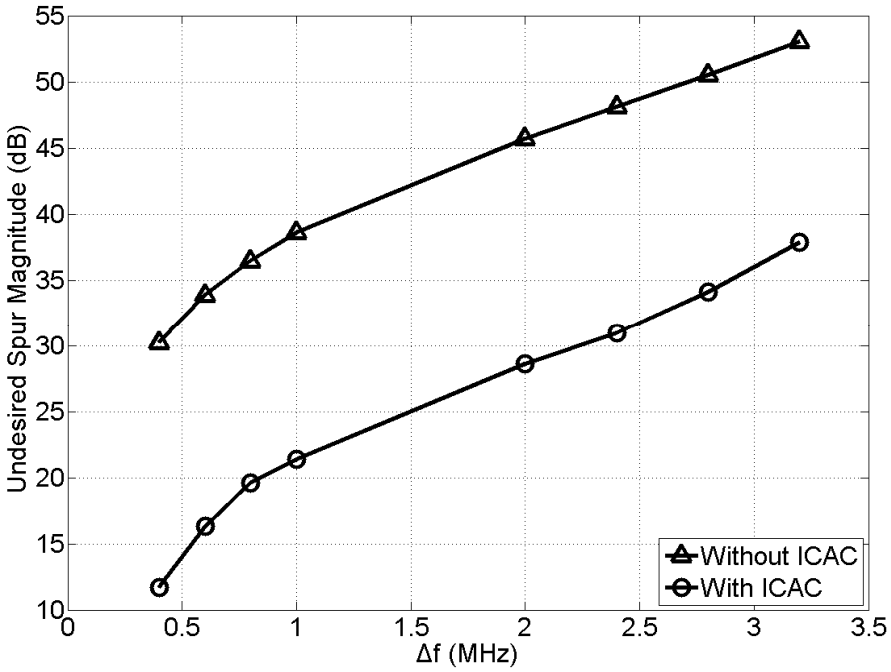


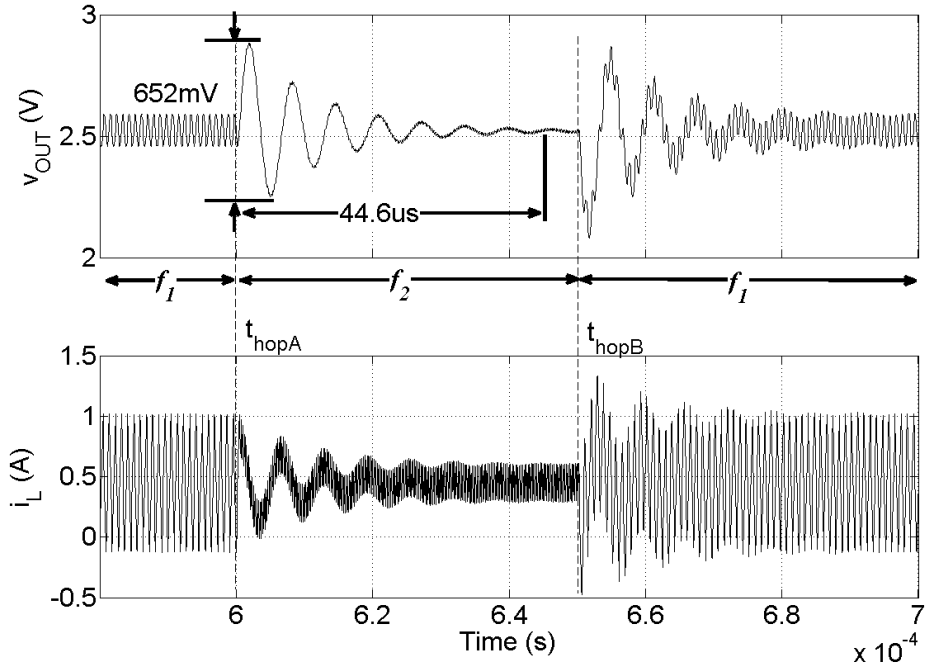
Fig. 4.33 The undesired spur magnitude versus Δf.

4.8.1.2 Transient Ripple on the Output Voltage

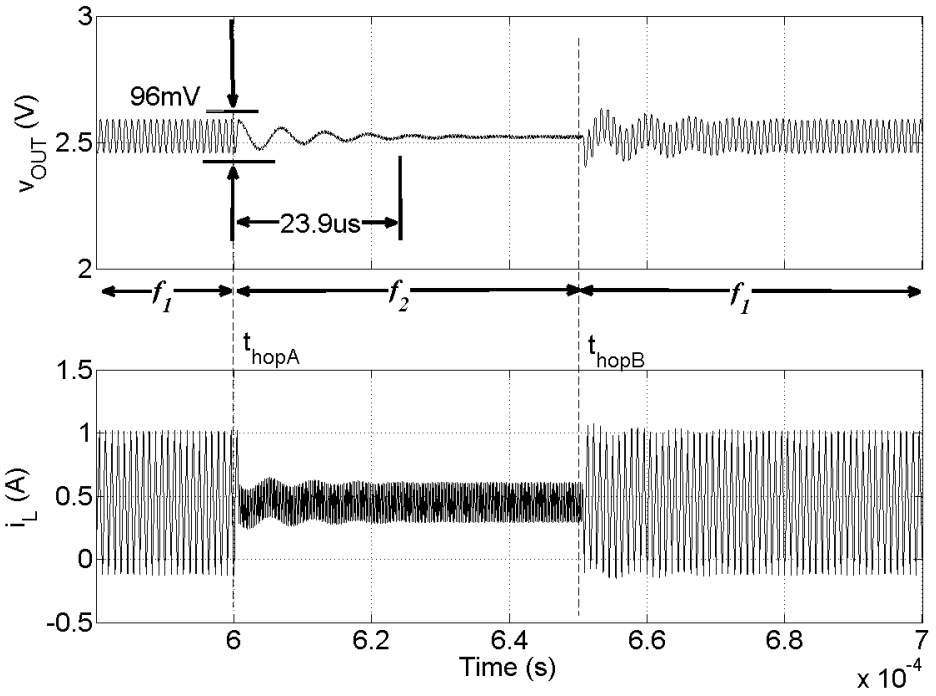
Fig. 4.34 shows the transient ripple reduction with the proposed ICAC technique. In Fig. 4.34(a), the conventional inductor current, i_L, returns to steady state from the peak current. t_{hopA} and t_{hopB} are the hopping moments from f_1=1.1 MHz to f_2=3.9 MHz and from f_2 to f_1 respectively. It causes huge transient-ripple voltage, Δv_{trans}, that is 652 mV at t_{hopA}, on the output voltage, v_{OUT}. The proposed ICAC keeps i_L to have the same dc component I_L as shown in Fig. 4.34(b). The transient-ripple voltage is reduced from 652 mV to 96 mV. The settling time, which limits the number of the switching frequencies, is also decreased from 44.6 μs to 23.9 μs for 1% settling.

$\Delta v_{trans,ICAC}$ is much smaller than Δv_{trans} and both of them increases as the difference between T_1 and T_2, ΔT, increases as illustrated in Fig. 4.35. The simulation results match with the analysis results in the equations (3.5) and (3.10). Furthermore, the simulated T_T is generally 8 times longer than T_X. This result verifies the assumption in the above

analysis that Q_{hopX} in (3.9) is much smaller than Q_T in (3.3).



(a)



(b)

Fig. 4.34 FH transient responses (a) Without ICAC. (b) With ICAC.

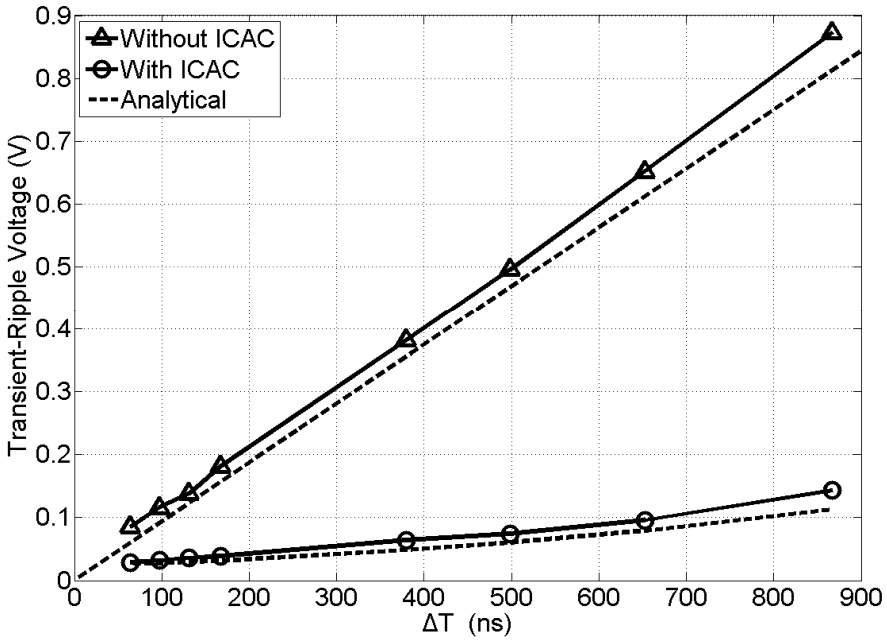


Fig. 4.35 Simulated and analytical results of the transient-ripple output voltage versus ΔT.

Fig. 4.36 shows the improvement of Δv_{trans} versus ΔT. It is defined by

$$\eta_V = \frac{\Delta v_{trans} - \Delta v_{trans,ICAC}}{\Delta v_{trans}} \tag{4.27}$$

η_V can achieve up to 85.3%. It proves the effectiveness of the proposed ICAC technique to reduce transient ripple on the output voltage.

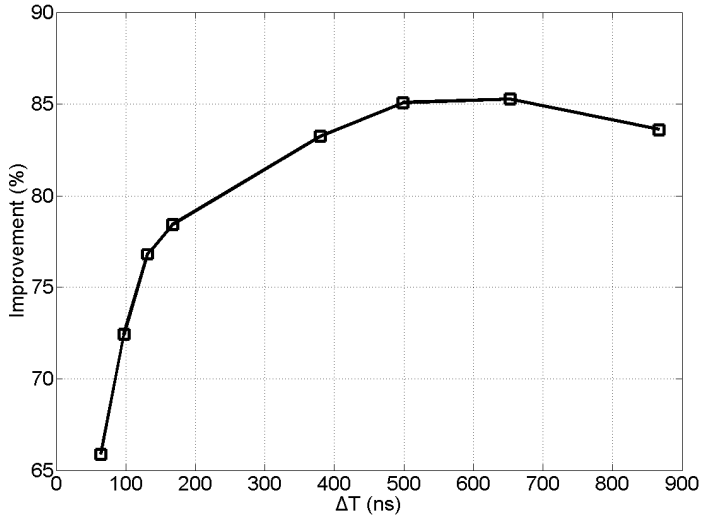
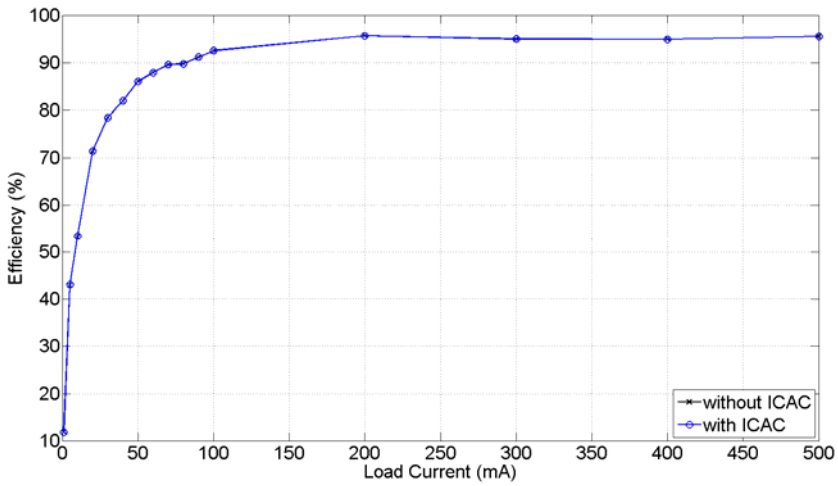


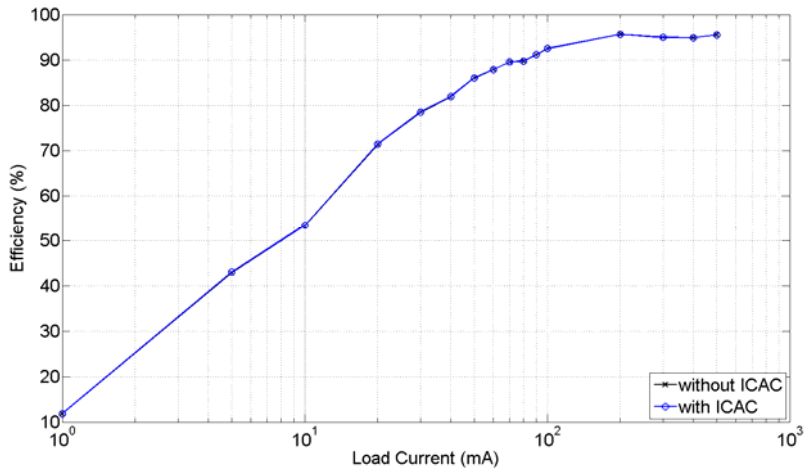
Fig. 4.36 Improvement of transient ripple on the output voltage versus ΔT.

4.8.2 Efficiency

Fig. 4.37 shows the simulated efficiency of the PWM DC-DC converter using ICAC. The maximum is 95% when load current is 200 mA. The efficiency decreases as smaller load current due to switching loss. Comparing to conventional architectures, the ICAC method needs two ramp generators, one subtractor and some logic gates. However, these additional circuits turn off at steady state besides except for three operational amplifiers. And these operational amplifiers use little current (~56 μA) since they do not need fast response.



(a)



(b)

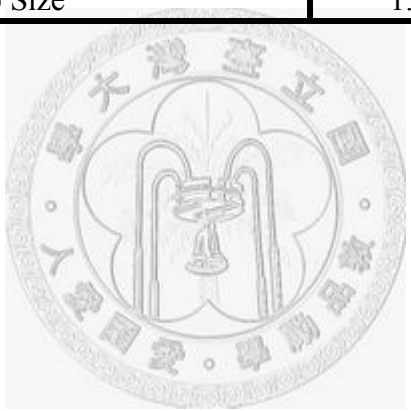
Fig. 4.37 Simulated efficiency of using ICAC and without ICAC (a) with linear scale. (b) with log scale

4.9 Performance Summary in simulation

The performance summary of this work is shown in Table 4.9.

Table 4.9 Performance summary in simulation

Specification	Simulation
Input Voltage, V_{IN}	3.6-5 V
Output Voltage, v_{OUT}	0.8-3.4 V
Max. Output Current, I_O	450 mA
Switching Frequency, f_{req}	0.8-3.4 MHz
Transient Ripple on the Output Voltage	96 mV
Settling time	23.9 μs
Max. Improvement	85.3%
Max Spur Reduction	18.9 dB
Max. Efficiency	95%
Chip Size	1.397 × 1.522 mm^2



Chapter 5 Experiment Results

5.1 Measurement Setup

Fig. 5.1 shows the floor plan of the DC-DC buck converter in this thesis. The power transistors are located at the upper side to close the pads so that reduces the resistance on the current path and the voltage drop. The power transistors and the driver are high noise components because a large amount of current flows through them and it could generate high temperature and serious noise disturbance. In order to alleviate the effect upon the feedback circuits, the power transistors must be surrounded by a wide guard ring. The metal which flows through a large amount of current must be wide enough to endure the current density. Every node of power transistors has three pads to reduce the inductance and the resistance of bonding wires. The analog parts are located at the lower side away from the noisy power transistors and separated from the power transistors by digital parts such as the logic gates and the driver.

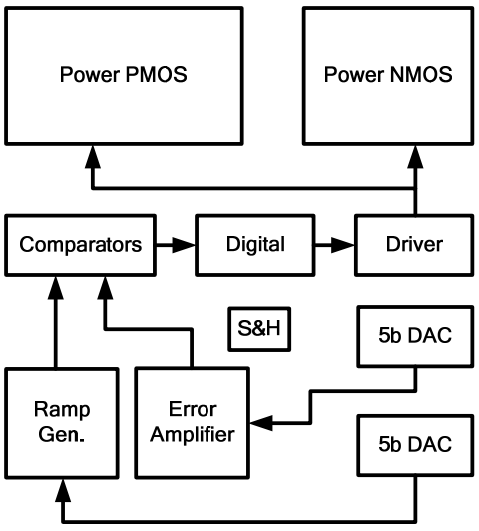


Fig. 5.1 The floor plan of the DC-DC buck converter

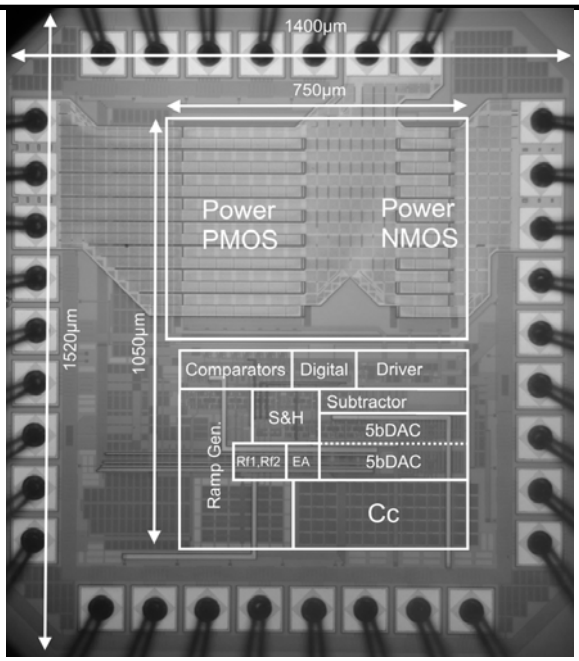


Fig. 5.2 Chip microphotograph

Fig. 5.2 shows the microphotograph of the core chip. The chip is fabricated in 0.35μm 2P4M CMOS technology. The active area is about $1.050 \times 0.75\text{mm}^2$ and the total chip area including pads is $1.397 \times 1.522\text{mm}^2$. The layout of the DC-DC buck converter is illustrated in Fig. 5.3. Table 5.1 shows the pin function of the prototype converter.

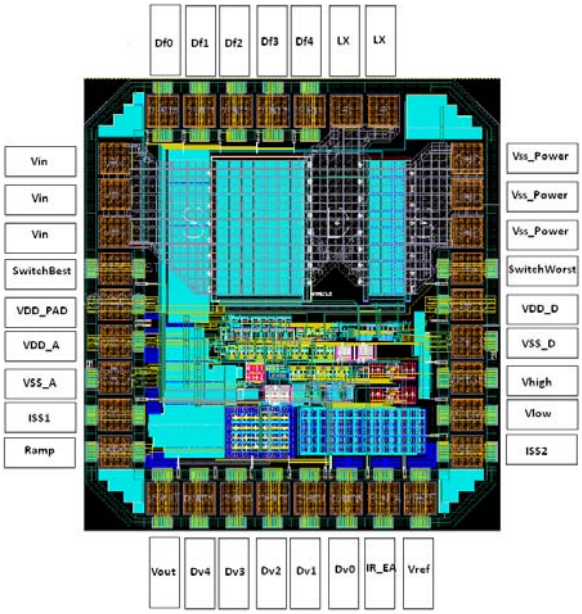


Fig. 5.3 Layout for DC-DC buck converter with pin labels

Table 5.1 The function of the pin in the DC-DC buck converter

Pin	description
V_{SS_POWER}	The ground of power transistors
V_{IN}	Input voltage
V_{DD_A}	Analog supply
V_{SS_A}	Analog ground
V_{DD_D}	Digital supply
V_{SS_D}	Digital ground
V_{DD_PAD}	supply for PAD
L_X	Output point of power transistors
V_{Ramp}	Ramp voltage
V_{out}	Output voltage
V_{High}	The maximum voltage of Ramp voltage
V_{Low}	The minimum voltage of Ramp voltage
V_{ref}	Reference voltage for DAC
SwitchBest	Selection of proposed circuit
SwitchWorst	Selection of conventional circuit
Dv4	The MSB of the input of DAC which controls the output voltage
Dv3	The 4^{th}bit of the input of DAC which controls the output voltage
Dv2	The 3^{rd}bit of the input of DAC which controls the output voltage
Dv1	The 2^{nd}bit of the input of DAC which controls the output voltage
Dv0	The LSB of the input of DAC which controls the output voltage
Df4	The MSB of the input of DAC which controls frequency
Df3	The 4^{th} bit of the input of DAC which controls frequency
Df2	The 3^{rd} bit of the input of DAC which controls frequency
Df1	The 2^{nd} bit of the input of DAC which controls frequency
Df0	The LSB of the input of DAC which controls frequency
I_{SS1}	Bias point of bias circuit which is fast
I_{SS2}	Bias point of bias circuit which is slow
I_{R_EA}	Bias point of bias circuit which controls the error amplifier

As shown in Fig. 5.4, the measurement environment setup is introduced as following. The LM317 is used to stabilize the power supply and reference voltage of the chip and the Chroma 6300 electronic load is the loading of the DC-DC buck converter. Chroma 6300 is used at constant current (CC) mode as a stable loading in this work. The main function focuses on the hopping frequency moment. Firstly, adjust the output voltage by turning on or off the switches of Dv<0:4>. Secondly, choose the expected frequency by turning on or off the corresponding switches of Df<0:4> or feeding in the

digital code by FPGA. Finally, the Oscilloscope Tektronix MSO 4034 is used to measure the voltages and the currents. It is also obtained the transient data and fast Fourier transform (FFT). Some extra passive components are configured according to the requirement shown in Fig. 5.4.

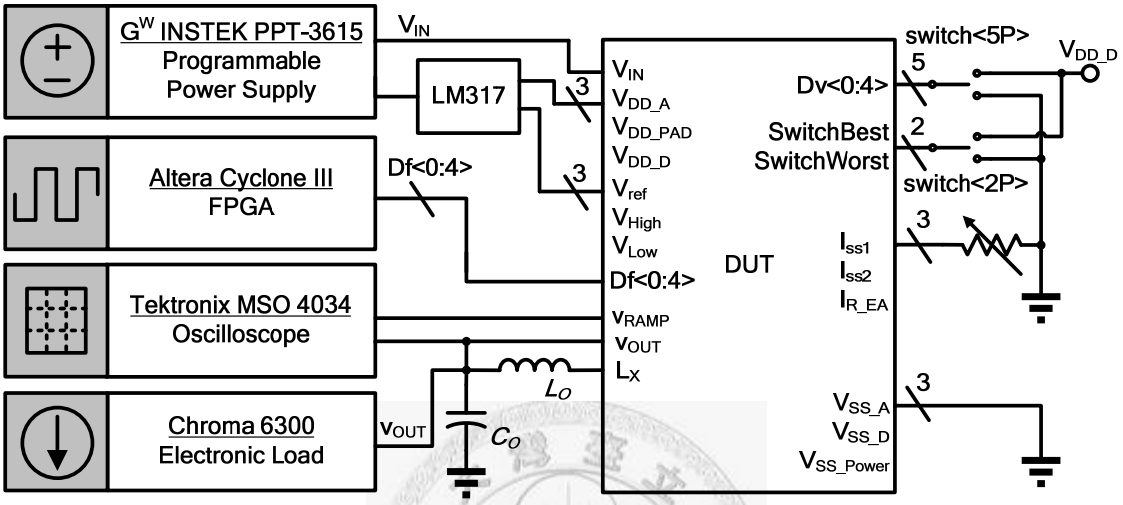
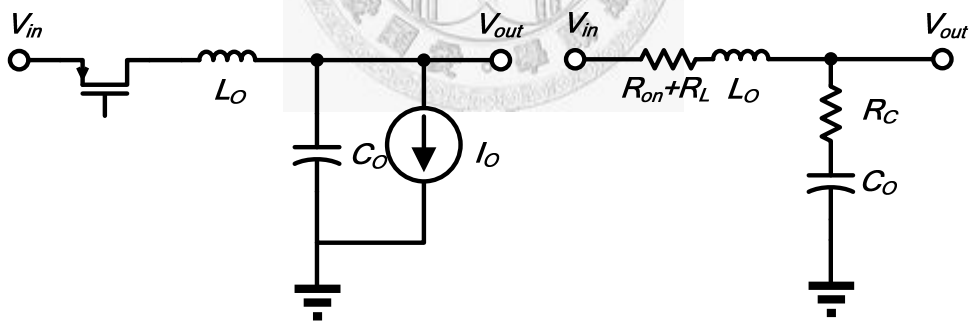


Fig. 5.4 The measurement environment setup



(a) (b)

Fig. 5.5 (a) output stage (b) equivalent circuit of output stage

Due to the second-order response of the output stage affecting the improvement directly, it needs to discuss the component of time constant and damping period [18]. The output stage is organized by an inductor L_O, a capacitor C_O, and a loading such as a current source I_O or a resistor R. Fig. 5.5 shows the equivalent circuit of output stage including the equivalent series resistance (ESR), R_L and R_C, of the inductor and

capacitor respectively. The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{(R_C + \frac{1}{sC_O})}{(R_{on} + R_L + sL_O) + (R_C + \frac{1}{sC_O})} \tag{5.1}$$

$$\begin{cases} \alpha = \dfrac{R_{on} + R_L}{2L_O} \\ \omega_0 = \dfrac{1}{\sqrt{L_O C_O}}, \omega_d = \sqrt{\omega_0 - \alpha^2} \end{cases} \tag{5.2}$$

$$\begin{cases} \text{damping period } T_d = \dfrac{2\pi}{\omega_d} \\ \text{time constant } \dfrac{1}{\alpha} = \dfrac{2L_O}{R_{on} + R_L} \end{cases} \tag{5.3}$$

The pole frequency ω_0 and time constant are obtained from equation (5.1). In this measurement, the ESR of capacitor R_C and inductor R_L are 20mΩ and 450mΩ respecitively. The ESR of inductor is main different between simulation and measurement. In simulation, it estimates 45 mΩ for ESR of inductor from data sheet and the corresponding time constant is longer. However, the practical ESR of inductor at 2MHz is 450mΩ and the corresponding time constant is shorter in measurement. Since the ESR of inductor R_L is too large to neglect, the improvement of measurement is shrinked than simulation. Fig. 5.6 and Fig. 5.7 are the schematic of the test board. The following Table 5.2 lists the components used in PCB and Fig. 5.8 is the picture of the real test board.

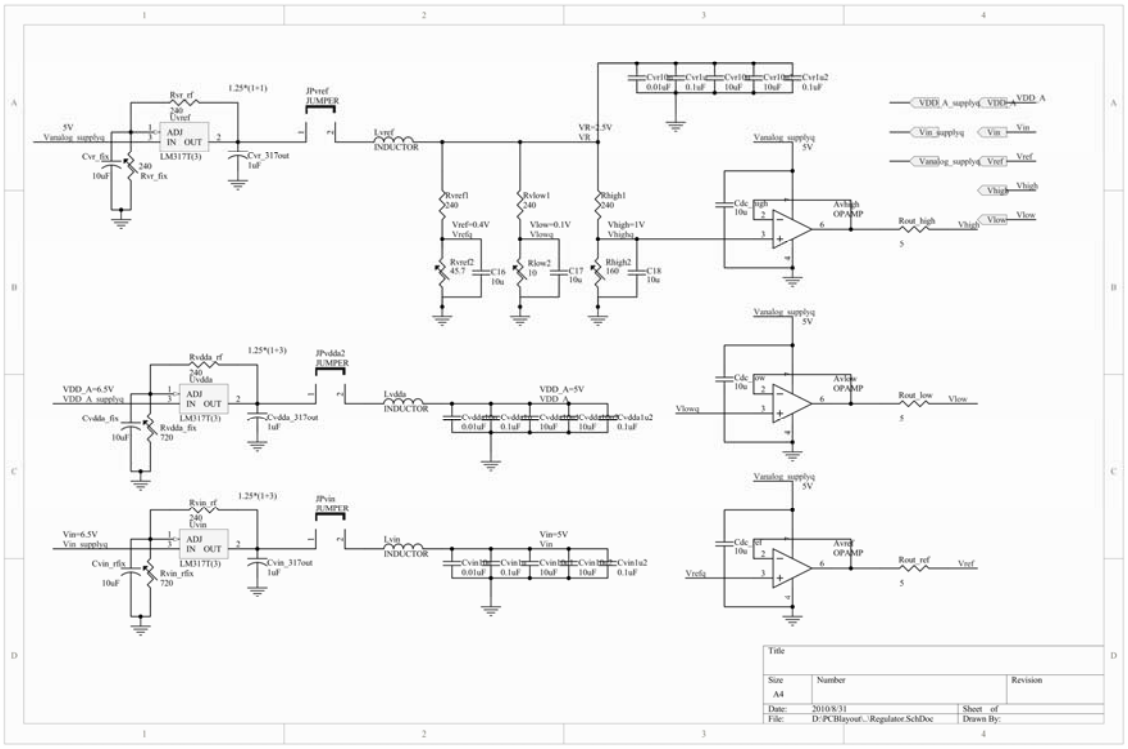


Fig. 5.6 The schematic of power supplies and reference voltages on PCB

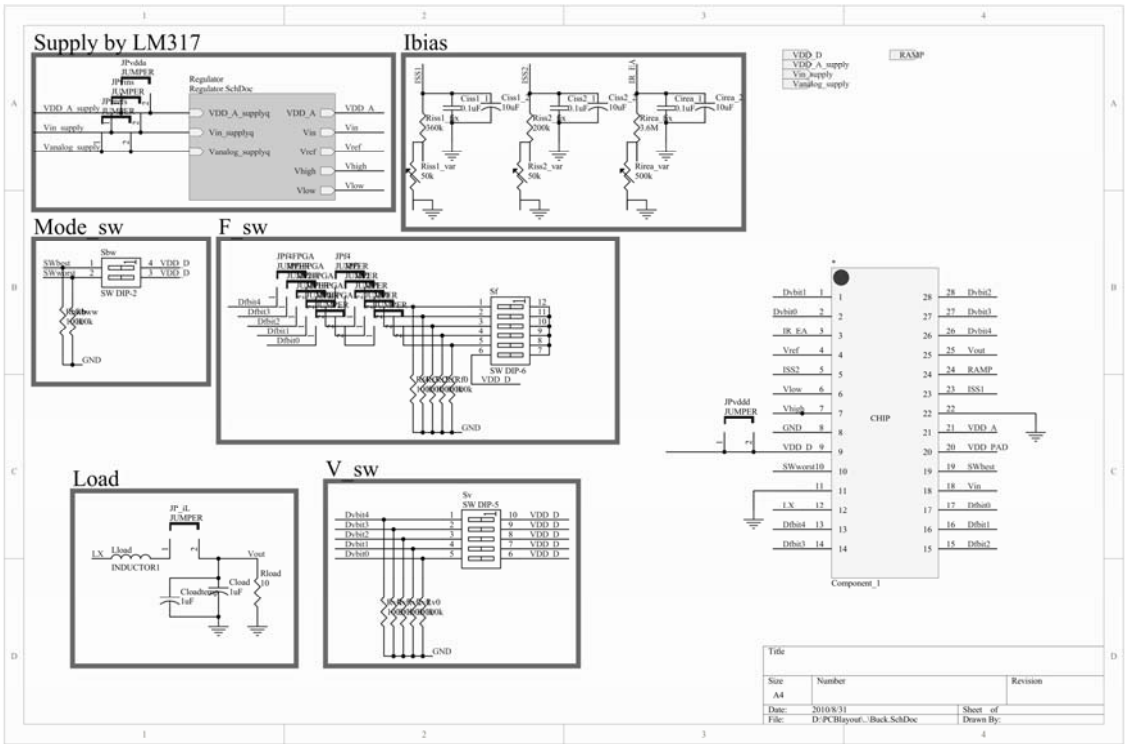


Fig. 5.7 The schematic of DC-DC converter side

Table 5.2 The components on PCB for testing the DC-DC converter

Component Designator	QTY	Description
Uvref, Uvdda, Uvin	3	LM317
Avref, Avhigh, Avlow	3	OP 8031
Lload	1	1 μH inductor
Cload	1	1 μF, 0805 Ceramic Capacitor
Lvref,Lvdda,Lvin	3	Ferrite Bead
JPvref,JPvdda,JPvin	3	Jumper
Sv, Sf	2	Switch(5dip)
sbw	1	Switch(2dip)
Rout	3	5 Ω, 0402 Chip
R_rf	6	240 Ω, 0805 Chip
R_sw	5	100 kΩ, 0805 Chip
R_v	7	390 kΩ, 0805 Chip
Riss1	1	680 kΩ, 0805 Chip
Riss2	1	1.8 MΩ, 0805 Chip
Rirea	1	3.6 MΩ, 0805 Chip
VRvref, VRvlow	2	50 Ω, Top Adjust
VRvref, VRvhigh	2	500 Ω, Top Adjust
VRvdda, VRvin	2	1 kΩ, Top Adjust
VRiss1	1	100 kΩ, Top Adjust
VRiss2	1	200 kΩ, Top Adjust
VRirea	1	500 kΩ, Top Adjust
C10n1-3	3	10 nF, 0805 Chip Cap
C100n1-9	9	100 nF, 0805 Chip Cap
C1u1-3	3	1 μF, 0805 Chip Cap
C10u1-18	18	10 μF, 0805 Chip Cap

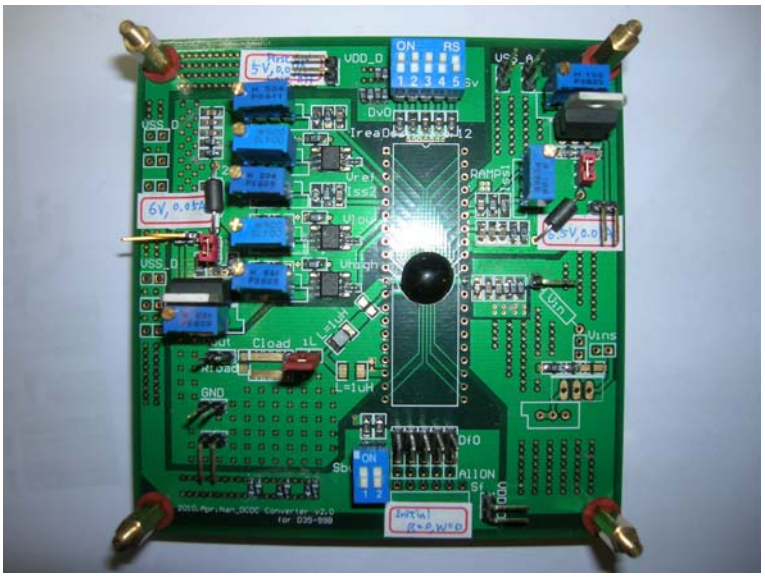


Fig. 5.8 The test board

5.2 Measurement Results

5.2.1 Static Measurement before using the Frequency-Hopping Technique

Before using the frequency-hopping technique, it needs to confirm the control signal of switching frequency *DFbit* works appropriately. The control signal *DFbit* relates to the corresponding switching frequency as shown in Fig. 5.9. The switching frequency has the capability of varying from 0.88 MHz to 3.415 MHz. This environment is under input voltage V_{IN}=5V, output voltage v_{OUT}=2.5V and load current I_O=450mA. The switching frequency is given by

$$f_{req} = \frac{V_{REF} DFbit}{R_t C_t (V_{High} - V_{Low})} \tag{5.4}$$

Another static measurement is the output voltage v_{OUT}. In this work, the output voltage has the capability of varying from 0.8V to 3.4V as shown in Fig. 5.10. It is controlled by the *DVbit*. This is environment is under V_{IN}=5V, switching frequency f_{req}=2MHz and load current I_O=450mA.

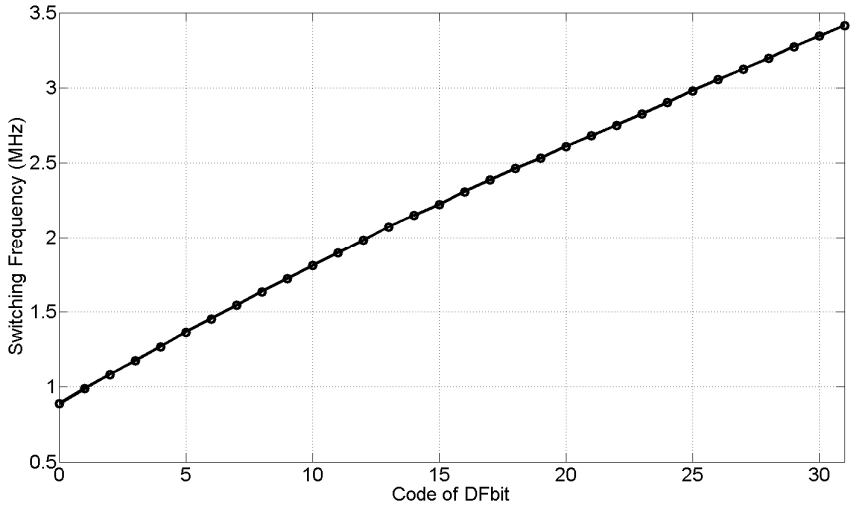


Fig. 5.9 Switching frequency relates to *DFbit.*

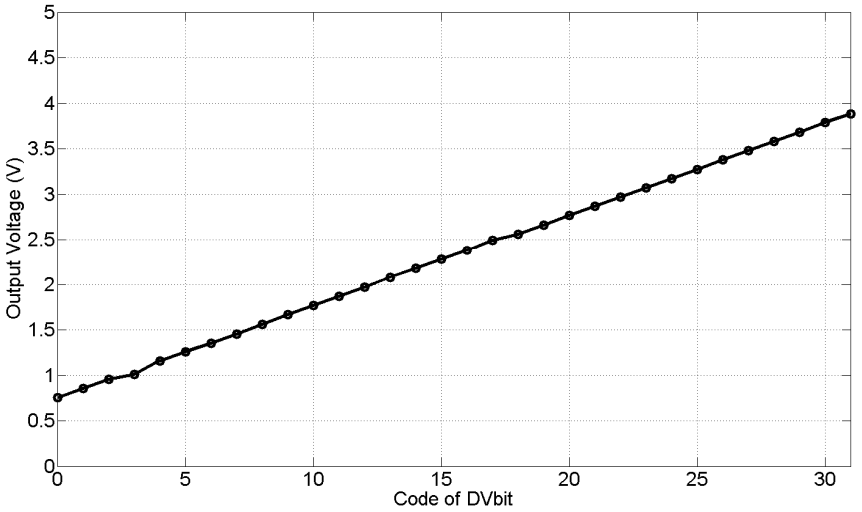


Fig. 5.10 Output voltage relates to *DVbit.*

5.2.2 Frequency Hopping

There are three parts to show the measurement results. Firstly, using fast Fourier transform (FFT) with Hamming window proves the reduced spur on spectrum. Secondly, the transient ripple on the output voltage could be observed from the transient waveform. Thirdly, the EMI reduction by using frequency-hopping technique is also provided.

5.2.2.1 Spectrum

The spectrum plots are shown as Fig. 5.11 and Fig. 5.12. In Fig. 5.11 there are two tones of switching frequencies at 0.88 MHz and 3.415 MHz which are the lowest and highest frequencies in this work, two harmonic tones of f_1 between 0.88 MHz and 3.415 MHz, and a spur at around 130 kHz. The spur is dominated by the output inductor 1 μH and the output capacitor 1 μF. The magnitude of this spur is reduced 12.4 dB by proposed method. It suggests that the proposed method is needed when the application have to hop larger difference of frequency. Fig. 5.12 shows the condition without harmonic tones when choosing there is no integer multiple between the hopping frequencies. There are two tones of switching frequencies at 1.7 MHz and 2.4 MHz, and a spur at around 130 kHz. The magnitude of this spur is reduced 12.2 dB.

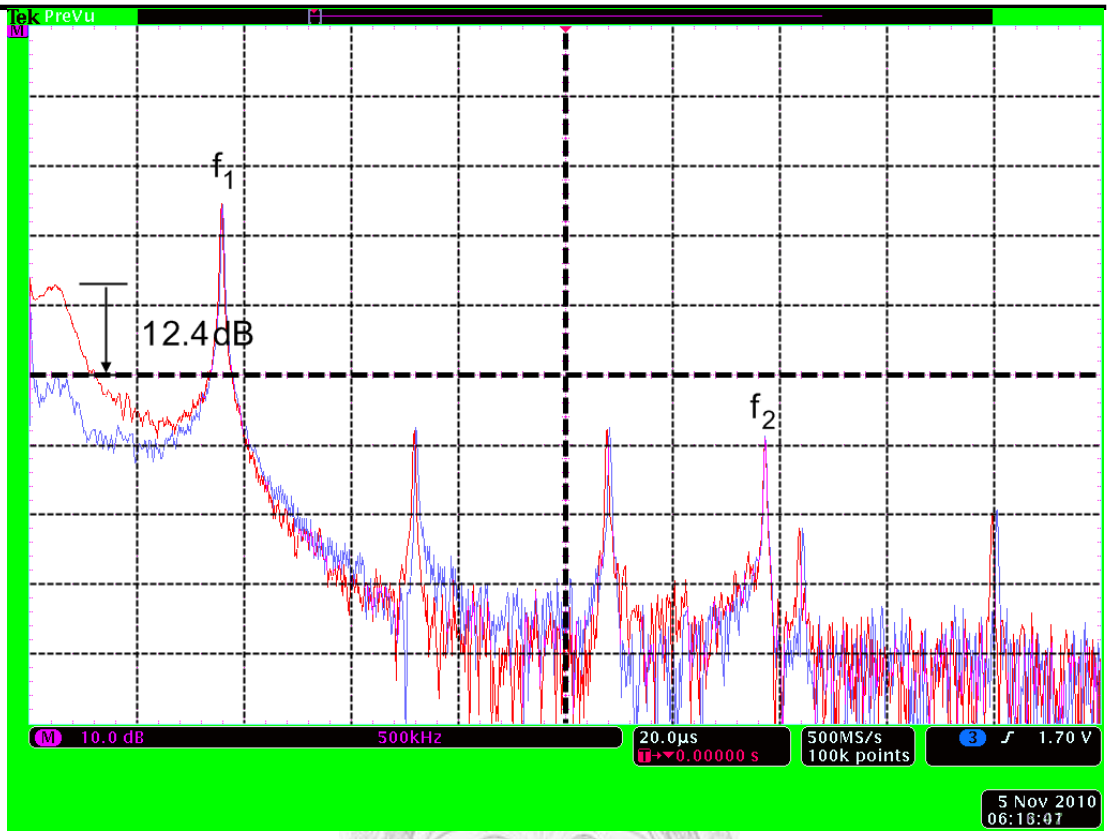


Fig. 5.11 Frequency hopping between 0.88 MHz and 3.415 MHz

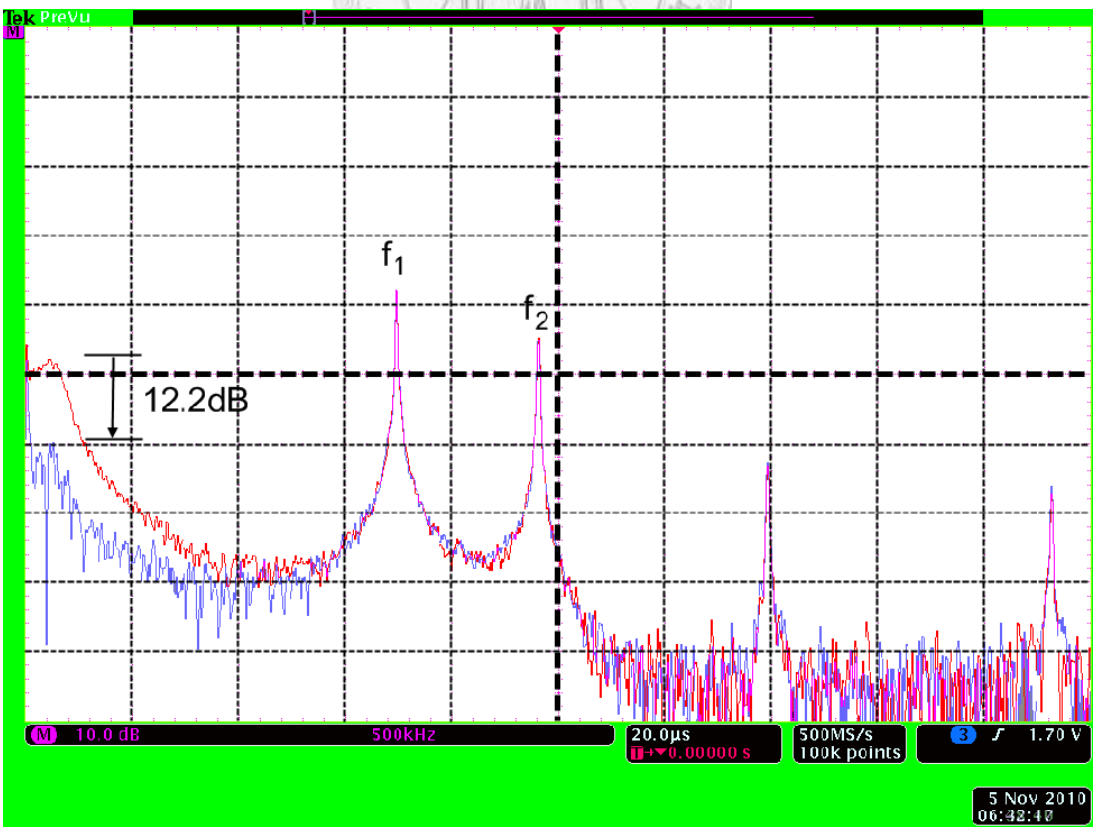


Fig. 5.12 Frequency hopping between 1.7 MHz and 2.4 MHz

Spur magnitude at f_{trans} as sweeping different Δf_{req} is shown in Fig. 5.13. Comparison of spur magnitude from Fig. 5.13 is shown in following Fig. 5.14. The maximum reduction is 14.1 dB at Δf_{req}=1.652 MHz which hopping frequencies are 1.173 MHz and 2.825 MHz.

The maximum of Δv_{trans} and spur reduction are perhaps not at the same Δf_{req} since the spur has the others effect issue such as settling time and damping times.

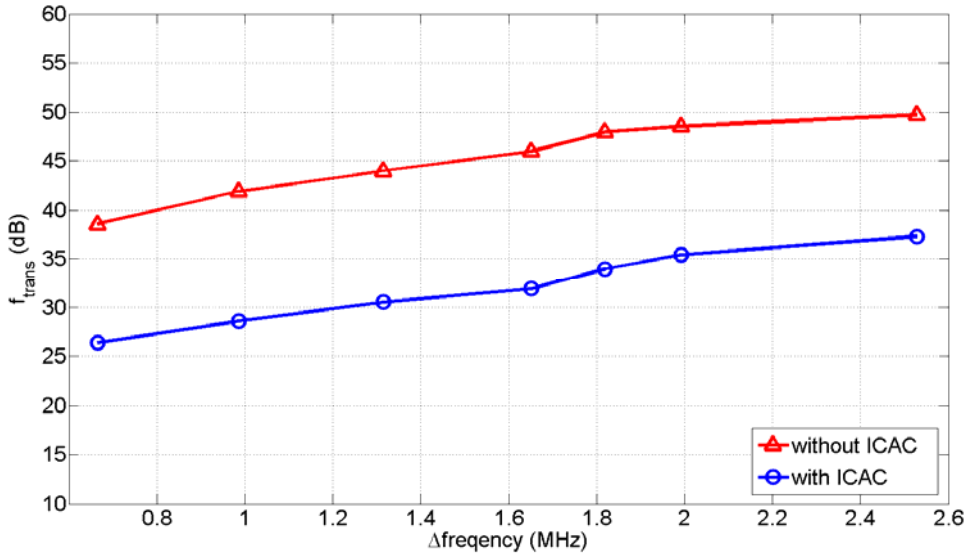


Fig. 5.13 Spur magnitude sweeps different frequencies with f_{center}=2 MHz

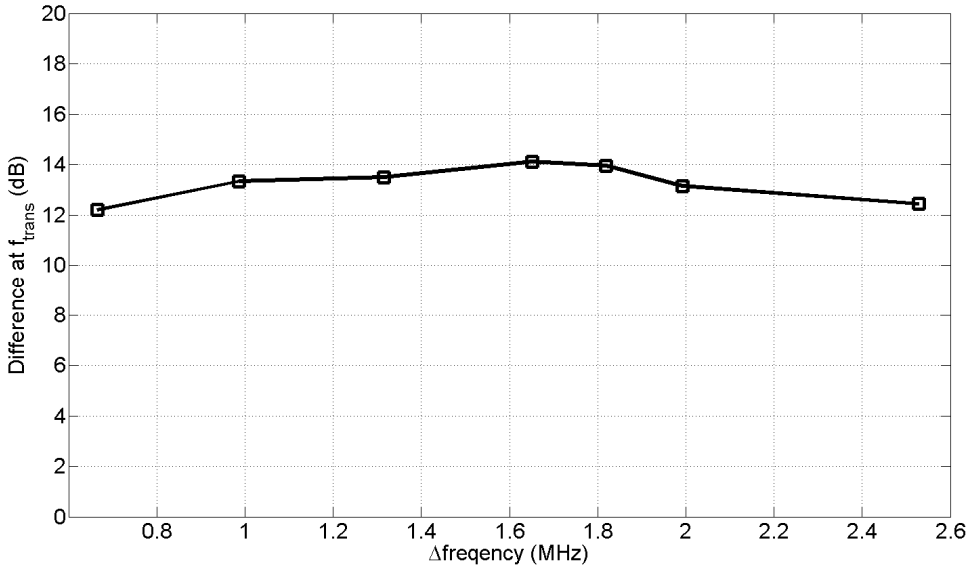
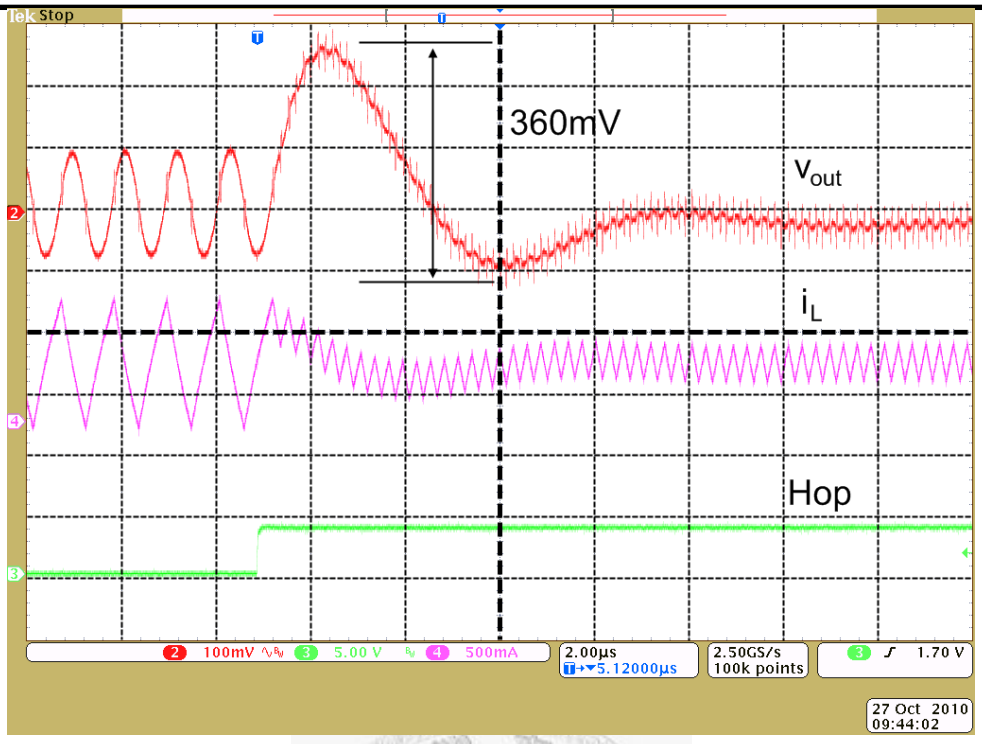


Fig. 5.14 Spur reduction sweeps different frequencies with f_{center}=2 MHz

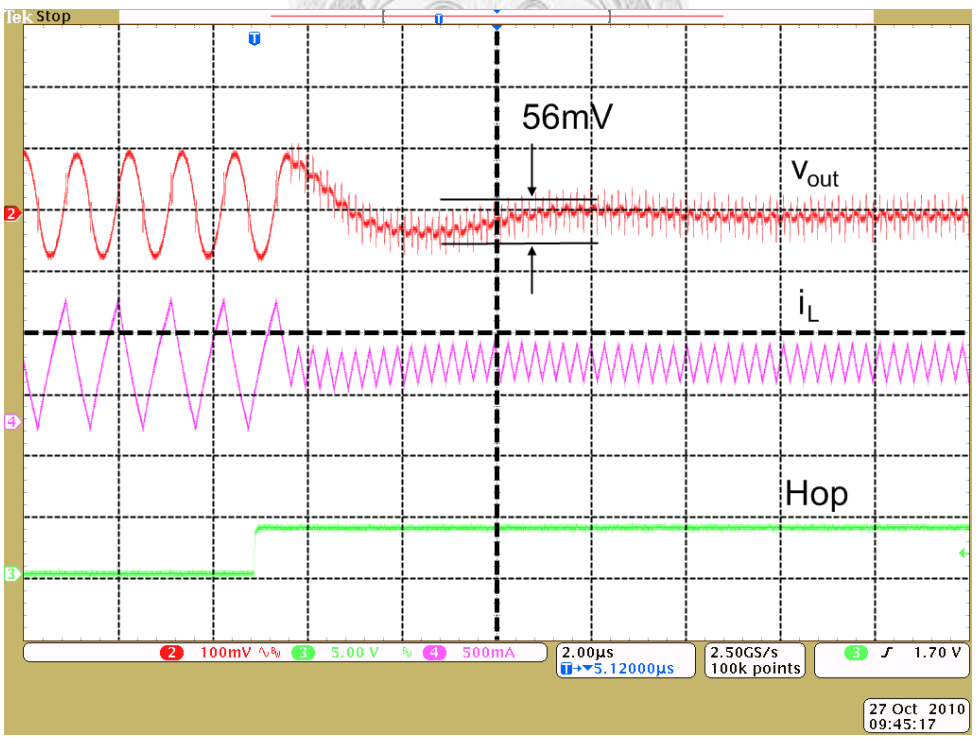
5.2.2.2 Transient Ripple on the Output Voltage

Fig. 5.15 shows the transient waveform of frequency hopping from 0.88 MHz to 3.415 MHz which are the lowest and highest frequencies in this work. When the Hop signal equals to logic 1, the switching frequency of the DC-DC converter changes to higher frequency. In Fig. 5.15(a), the inductor current i_L comes steady state from the peak current and it leads a difference of current. This difference of current flows into the output capacitor and induces a transient ripple on the output voltage Δv_{trans}. In Fig. 5.15(b), the inductor current is modulated by the ICAC technique. It changes the switching frequency at the average of the inductor current moment and reduces the difference of current. Therefore, there is almost no transient ripple on the output voltage. The transient ripple on the output voltage reduced from 360 mV to 56 mV and the settling time reduced from 15 μs to 9 μs.

In Fig. 5.16, it is the transient waveform of frequency hopping from 3.415 MHz to 0.88 MHz and the ICAC also works. Since the difference of the inductor current at high frequency is smaller and centralizes around the average of inductor current, the transient ripple voltage improves unapparent. For the transient ripple on the output voltage, there is more efficient improvement when frequency hops from low to high compares to frequency hops from low to high.

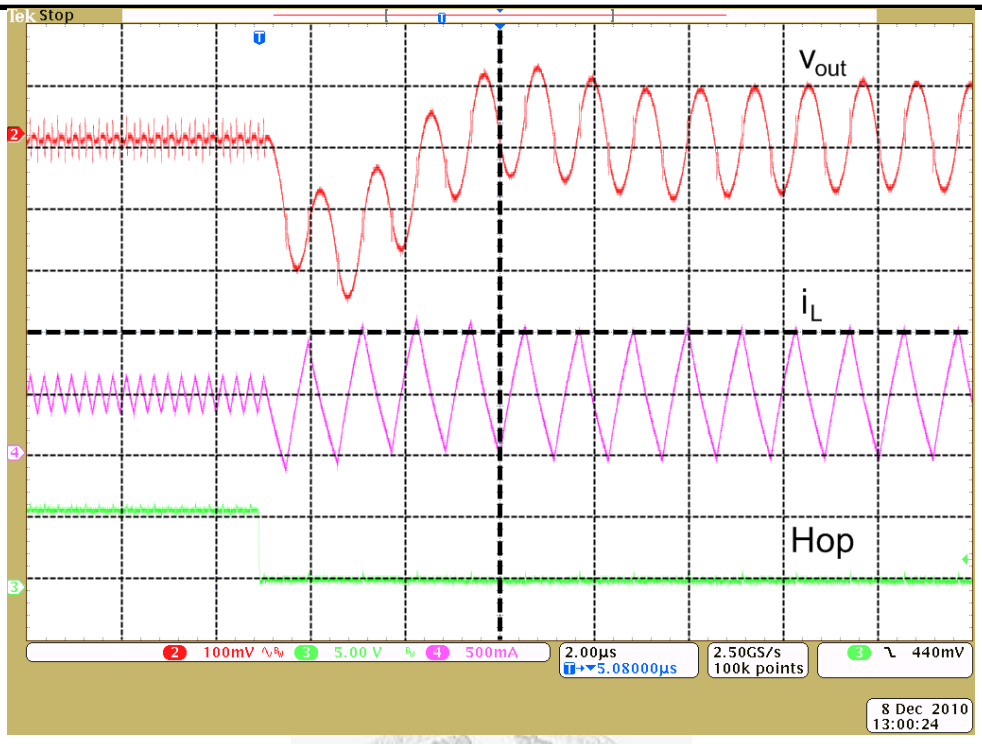


(a)

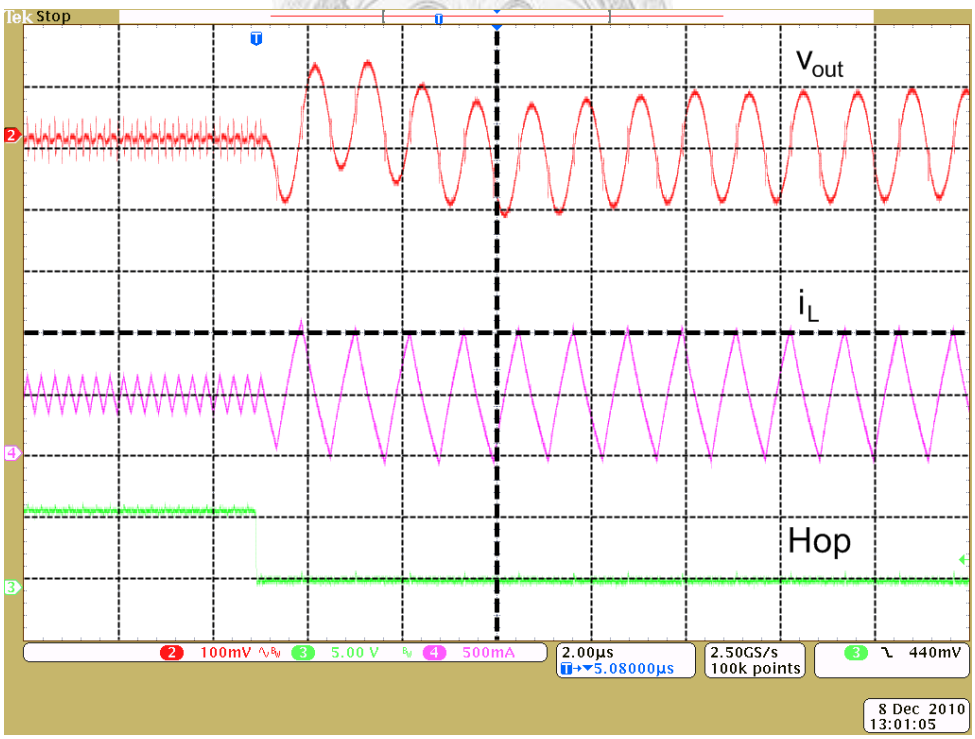


(b)

Fig. 5.15 Transient waveform of frequency hopping from 0.88 MHz to 3.415 MHz (a) without using ICAC and (b)with ICAC



(a)



(b)

Fig. 5.16 Transient waveform of frequency hopping from 3.415MHz to 0.88MHz (a) without using ICAC and (b) with ICAC

Fig. 5.17 depicts that the frequency-hopping technique without ICAC induces the larger transient ripple on the output voltage as the larger difference between two hopping frequencies. The transient ripples on the output voltage without ICAC method are reduced from 0.114 V to 0.36 V as difference of frequency from 0.325 MHz to 2.528 MHz. Comparatively; the transient ripples on the output voltage with ICAC method are reduced from 0.03 V to 0.056 V as difference of frequency from 0.325 MHz to 2.528 MHz. The transient ripple on the output voltage Δv_{trans} is positive related to the period of the switching frequency due to the charging and discharging interval on the output capacitor. To show Δv_{trans} corresponding the period of switching frequency, it uses the difference between two periods of switching frequency ΔT as a variable in Fig. 5.18.

Finally, define the improvement η_v to quantify the measurement results

$$\eta_V = \frac{\Delta v_{trans} - \Delta v_{trans,ICAC}}{\Delta v_{trans}} \tag{5.5}$$

It obtains the improvement shown in Fig. 5.19. From Fig. 5.19, the maximum improvement is 88% at ΔT=676 ns and the hopping frequencies are 0.988 MHz and 2.98 MHz (Δf_{req}=1.992 MHz).

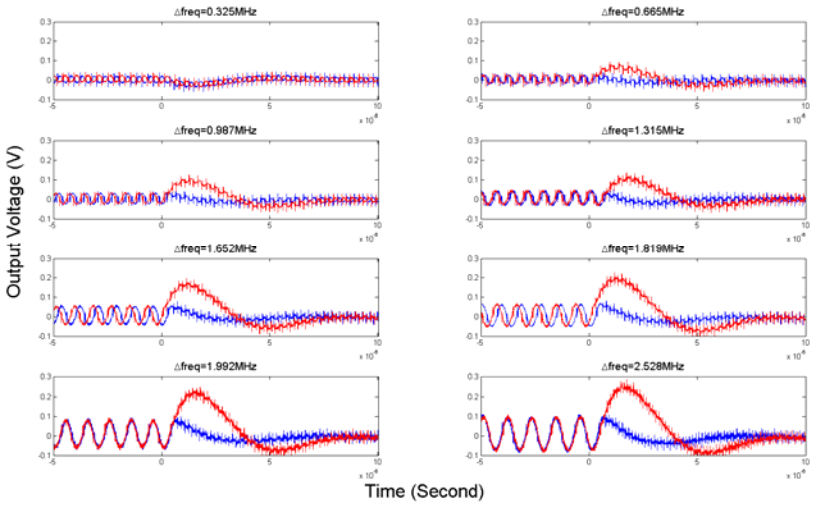


Fig. 5.17 Comparison between conventional and proposed methods as sweeping different frequencies with f_{center}=2 MHz

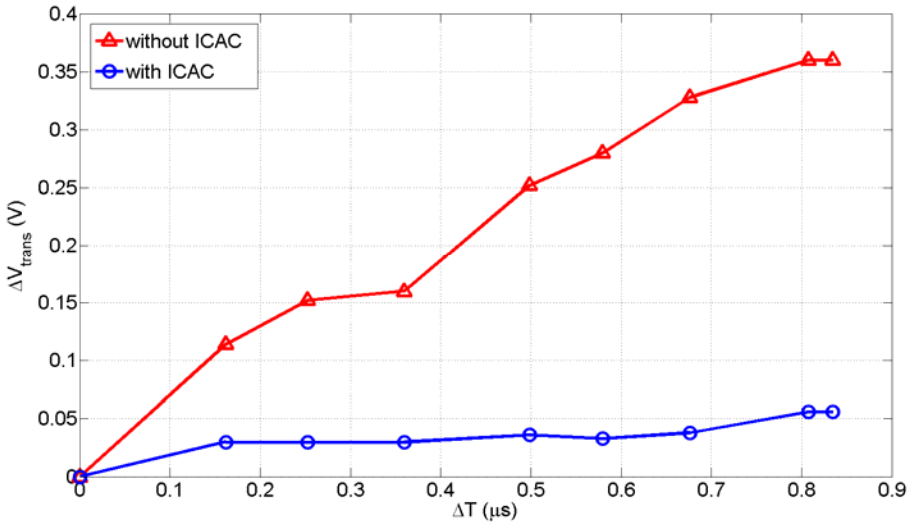


Fig. 5.18 Transient ripple on the output voltage sweeps different frequencies with f_{center}=2 MHz

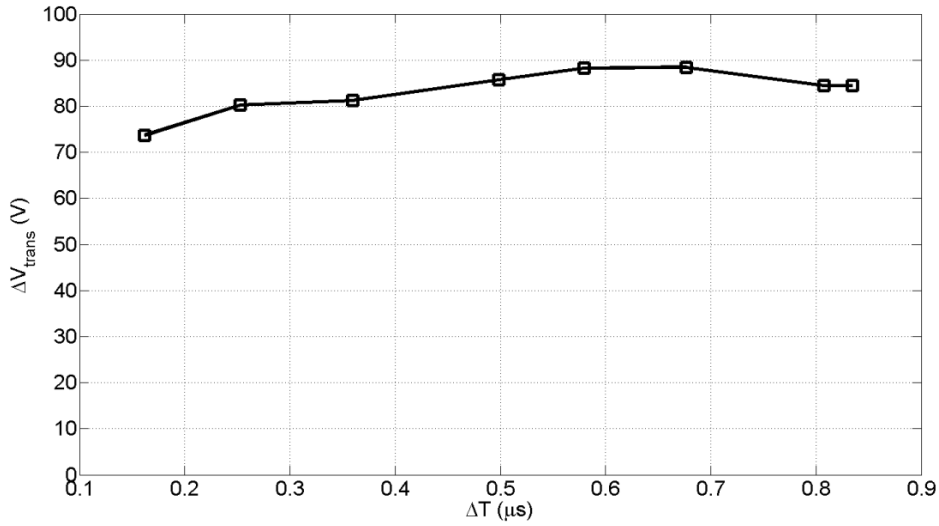


Fig. 5.19 Improvement sweeps different frequencies with f_{center}=2 MHz

Fig. 5.20 and Fig. 5.21 are the measurements of changing the supply voltage V_{IN}. This is environment is under switching frequency hopping from 0.88MHz to 3.415MHz and load current I_O=450 mA. In Fig. 5.20, it shows the transient waveform of the supply voltage from V_{IN}=5.0 V to V_{IN}=3.6 V. In Fig. 5.21, the comparison of the transient ripple on the output voltage between conventional and proposed methods is shown. There are

two different output voltages, v_{OUT}=1.2 V and v_{OUT}=1.8 V. Due to the transient ripple without ICAC is proportional to the difference of the inductor current Δi_L, we should know the component of Δi_L is

$$\Delta i_L = \frac{V_{IN} D(1-D)T}{L_O} \tag{5.6}$$

$$= (v_{OUT} - \frac{v_{OUT}^2}{V_{IN}}) \frac{T}{L_O} \tag{5.7}$$

where T is the period of switching frequency. By the equation (5.7), we obtain that Δi_L increases as v_{OUT} increases or V_{IN} increases. Therefore, Δv_{trans} without ICAC increases as shown in Fig. 5.21.

Fig. 5.22 is the measurement of changing the load current I_O. This is environment is under the switching frequency hopping from 0.88 MHz to 3.415 MHz, V_{IN}=5 V and v_{OUT}=2.5 V. Due to the improvement is independent to the dc current of inductor if the converter works in CCM, the load current does not affect the improvement. Fig. 5.22 depicts the improvement is almost the identical.

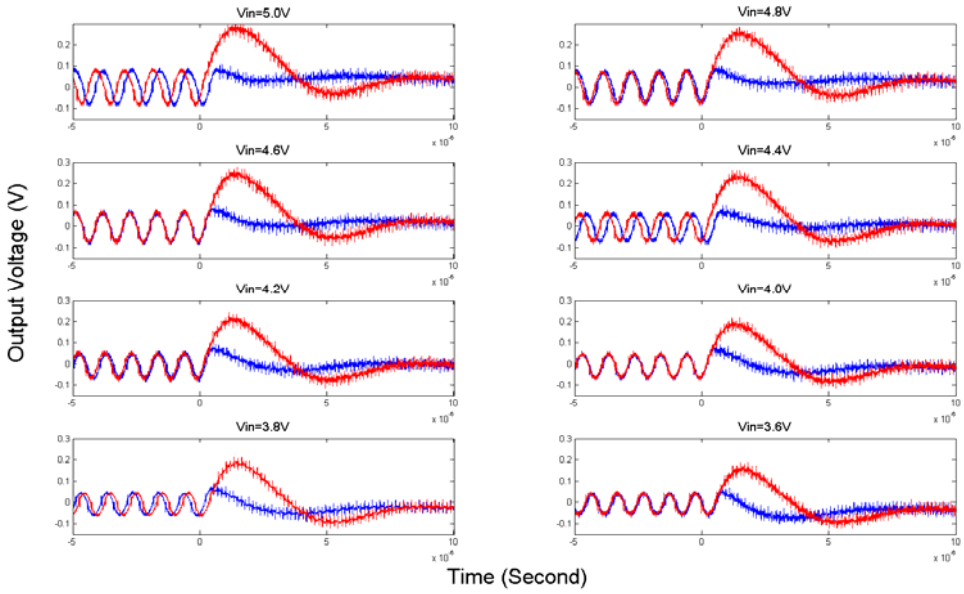


Fig. 5.20 Comparison between conventional and proposed methods as sweeping different supply voltage V_{IN} at v_{OUT}=1.8V

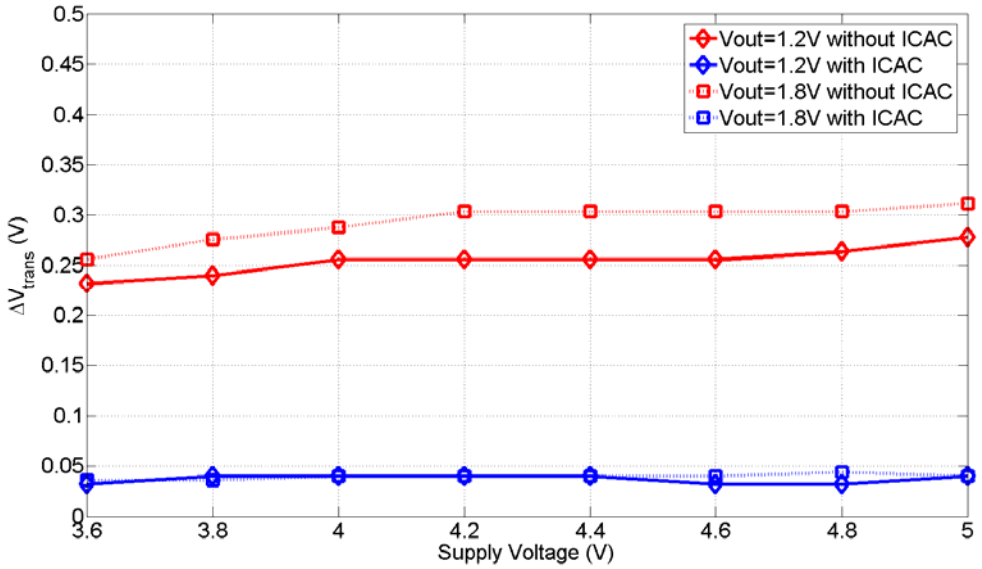


Fig. 5.21 Transient ripple on the output voltage sweeps different supply voltage V_{IN}

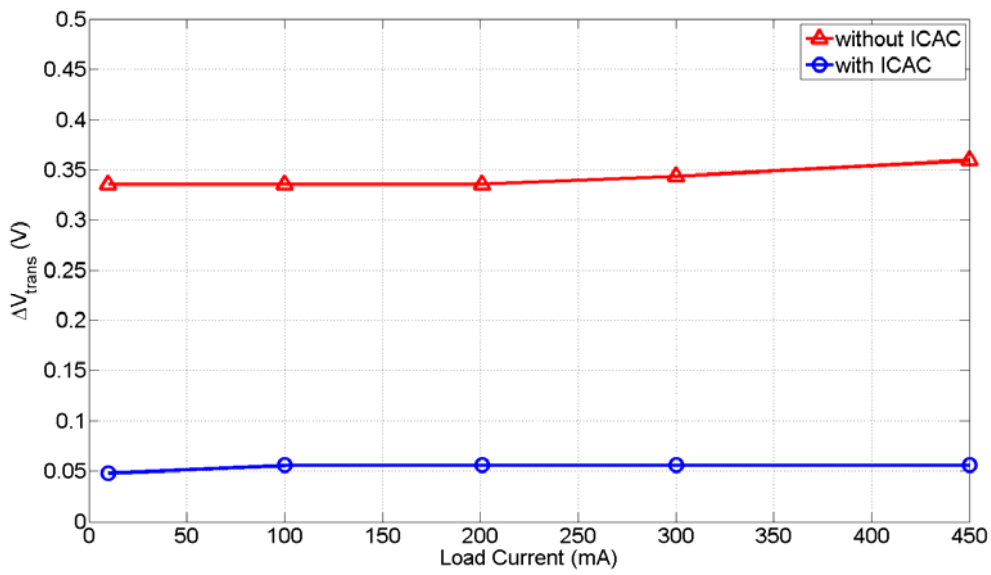


Fig. 5.22 Transient ripple on the output voltage sweeps different load current I_O

5.2.3 EMI Reduction

This thesis also provides the advantage of using the frequency-hopping technique. Fig. 5.23 shows the transient waveform of the output voltage and the inductor current with varying control signal of switching frequency *DFbit*. In this figure, *DFbit* changes seventeen levels at a rate of every 40 μs (*clk*) to generate seventeen switching

frequencies. Note that this *clk* is the period of the FPGA. The comparison of output spectrum between the one with only one switching frequency and the one hopping seventeen frequencies is shown in Fig. 5.24. It reduced the EMI by 23.55 dB. In Fig. 5.25, these spur magnitude are normalized by the one with only single switching frequency. The maximum reduction is 23.55 dB at seventeen different switching frequencies from 2 MHz to 3 MHz. These frequencies start from 2 MHz and hop increasing monotonically and then decreasing monotonically.

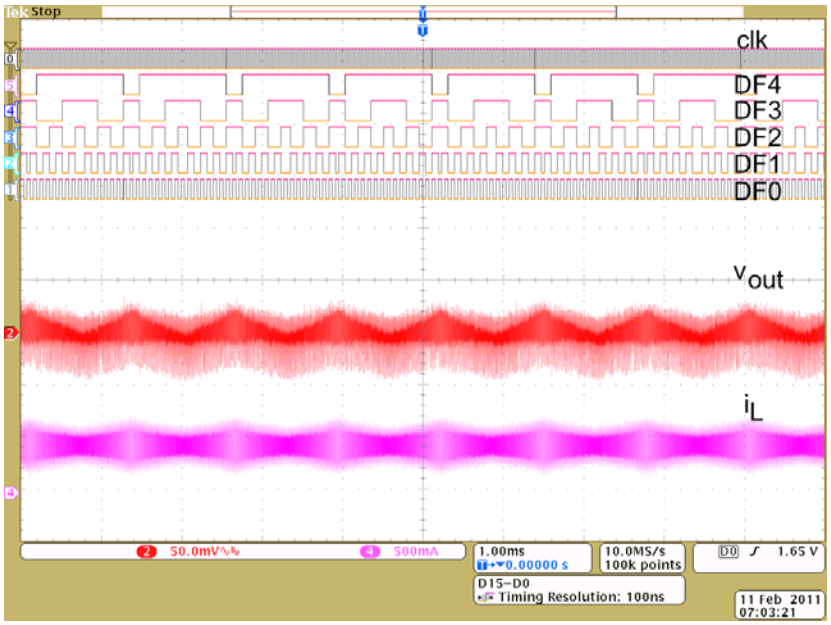


Fig. 5.23 Transient waveform of seventeen different switching frequencies

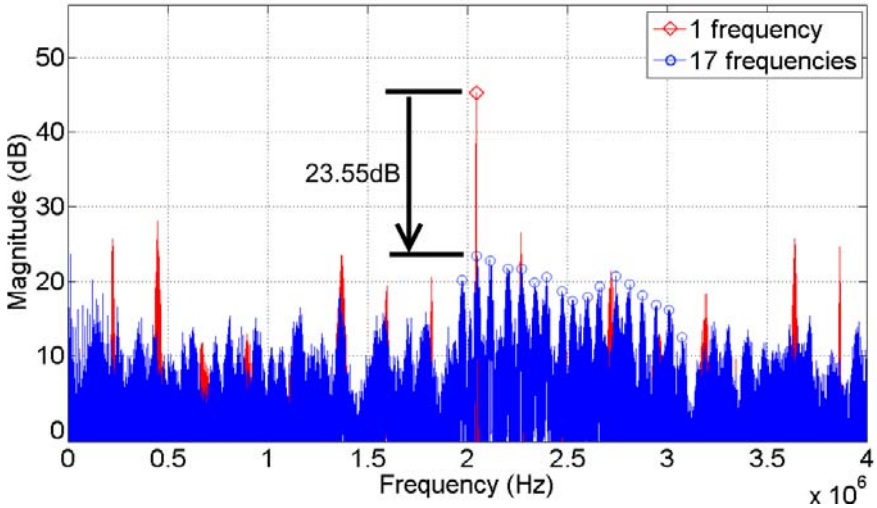


Fig. 5.24 Output spectrum using the frequency-hopping technique with seventeen switching frequencies

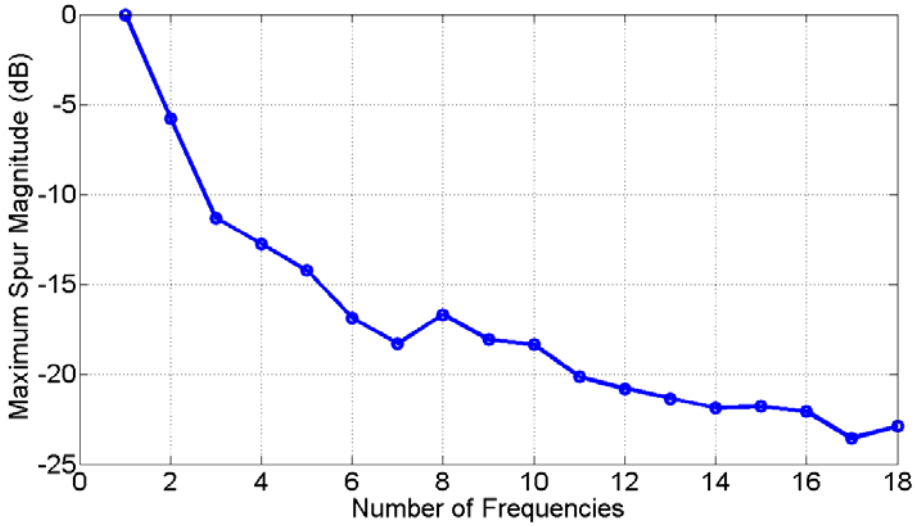
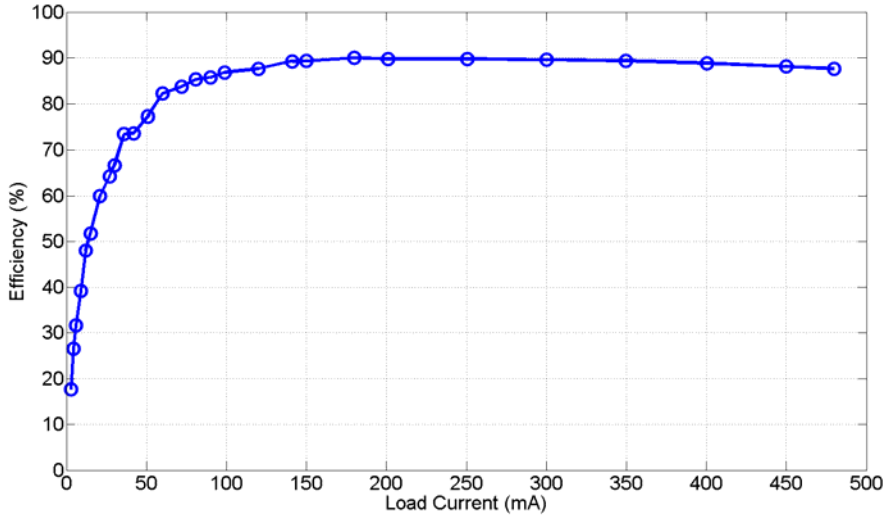


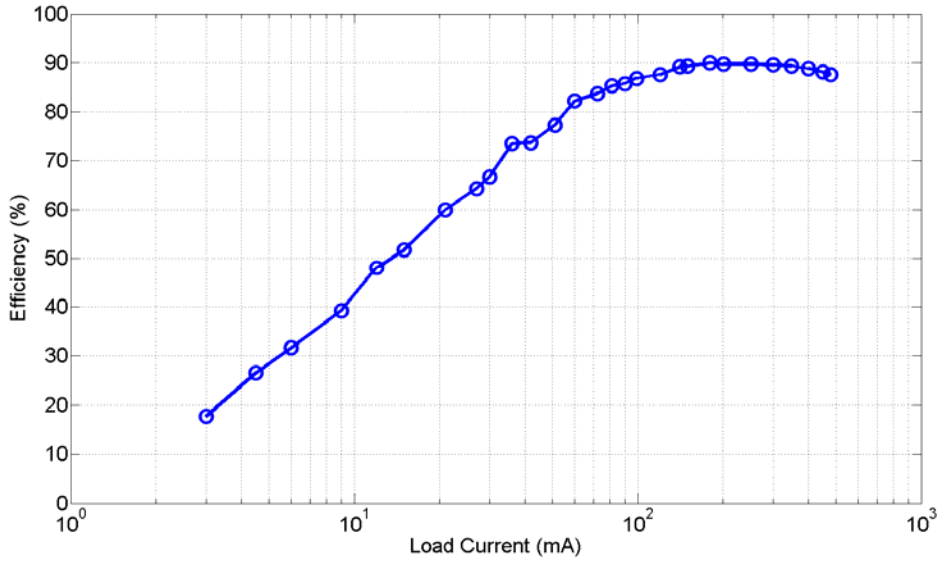
Fig. 5.25 The spur magnitude of EMI with various of number of switching frequencies using the frequency-hopping technique

5.2.4 Efficiency

Fig. 5.23 shows the measured efficiency of the DC-DC buck converter with respect to load current. This environment is under V_{IN}=5 V, v_{OUT}=2.5 V and switching frequency f_{req}=2 MHz. It can be represented by linear scale in Fig. 5.23(a) and by log scale in Fig. 5.23(b) respectively. The peak efficiency is 90% at load current=180 mA. The efficiency decreases as smaller load current due to switching loss.



(a)



(b)

Fig. 5.26 Efficiency at v_{OUT}=2.5V and V_{IN}=5V (a) with linear scale (b) with log scale

5.3 Performance Summary

The performance summary of this work is shown in Table 5.3 and the performance comparison is shown in Table 5.4.

Table 5.3 Performance summary in measurement

	Conventional	**Measurement**
Input Voltage, V_{IN}	3.6-5 V	3.6-5 V
Output Voltage, v_{OUT}	0.75-3.88 V	0.75-3.88 V
Max. Output Current, I_O	450 mA	450 mA
Switching Frequency, f_{req}	0.88-3.4 MHz	0.88-3.4 MHz
Transient Ripple on the Output Voltage	360 mV	56m V
Settling Time	15 μs	9 μs
Max. Improvement	88%	
Spur Reduction	14.1 dB	
Max. Efficiency	90 %	90 %
Chip Size	1.397 × 1.522 mm^2	1.397 × 1.522 mm^2

Table 5.4 Performance comparison

	PESC06[19]	ASSCC09[20]	CICC10[21]	This work
Technology	FPGA	FPGA	CMOS 0.35 μm	CMOS 0.35 μm
Input Voltage Range	2.7-3.6	1.8 V	2-3.3 V	3.6-5 V
Output Voltage Range	1.8 V	0.6-1.2 V	0.5-3 V	0.8-3.4 V
Inductor	2 μH	4.7 μH	2.2 μH	1 μH
Capacitor	4.7 μF	22 μF	2.2 μF	1 μF
Output Current Maximum	500 mA	400 mA	500mA	450 mA
Switching Frequency	1.74-2.84 MHz	1 MHz	0.8-1.2 MHz	0.8-3.4 MHz
Variable Frequency Method	DPWM+ RCFMFD	DPWM+ RPPM	PWM+ RCFMFD	PWM+ FH
Improvement of Transient Ripple Voltage	Not improved	Not improved	88.5%	88%
Spur Reduction	Not improved	Not improved	N/A	14.1 dB @159 kHz
Reduction in Conducted EMI Peak	23.4 dB	18 dB	15.6 dB	23.55 dB @2-3 MHz

Chapter 6 Conclusion and Future Work

6.1 Conclusion

The proposed ICAC technique used in a DC-DC converter for frequency hopping is introduced in this thesis. It effectively reduces the undesired spur while hopping frequency, transient settling time, which limits the hopping times, and the transient ripple on the output voltage. The measurement results show that the undesired spur and the transient-ripple voltage could be decreased around 14.1 dB and 88% between two hopping frequencies. The frequency-hopping technique reduces the EMI spur magnitude by 23.55 dB. By combining the above two techniques, the spectrum from the natural frequency of the filter to the switching frequency of the buck converter can be suppressed. It is important in a mobile wireless device.

6.2 Future Work

The loading of this DC-DC converter is supposed as a constant current and the best hopping time is based on this assumption. In the future work, it can include the situation that the load current varies. Although there are many methods to improve the transient response as the load current varies. Both the load current and switching frequency vary at the same time is a brand-new topic.

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