國立臺灣大學電機資訊學院電子工程學研究所

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以 0.18-μm CMOS 製程製作之 30GHz 鎖相迴路設計與實現

Design and Implementation of 30 GHz Phase-Locked Loop in a 0.18-μm CMOS Technology

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Design and Implementation of 30 GHz Phase-Locked Loop in a 0.18-μm CMOS Technology

By

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THESIS

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摘要

隨著製程的進步，使得射頻積體電路得以趨向高頻發展。由於無線通訊技術在工業、科學以及醫學等三大領域的快速發展與廣泛應用，市場對低成本、低功耗積體電路的需求有日以劇增的趨勢。為了確保毫米波電路能夠正常地運作，常見的方式即是使用較先進的製程來設計電路，但此一方法卻會導致成本的增加進而降低產品競爭力。因此，成本考量與電路性能之間取得平衡是設計者主要的課題。儘管如此，它仍然是一項具有挑戰性的任務。

在本篇論文中，我們藉由改善電路的架構，使得高頻電路如 30.4 GHz 鎖相迴路，能夠在 0.18-μm 標準互補式金氧半導體製程中實現，以達到節省成本的目的。由於電路架構的特性，傳統相位頻率偵測器的操作頻率受到明顯地限制，因此首要之務即是使用獨立的相位偵測器及頻率偵測器。除此之外，在壓控振盪器的設計中，我們引用了近橫向電磁傳輸線的技術來實現小面積及高頻的操作。不僅如此，近橫向電磁傳輸線同時還具備了良好的屏蔽能力，讓壓控振盪器本身更加穩定。除了鎖相迴路的架構介紹外，詳細的量測結果將呈現於本論文之後。藉以驗證上述方法之可行性，此鎖相迴路操作於 1.8 伏之供應電壓，消耗功率為 64.8 mW。


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Abstract

With the advances of the silicon integrated circuit technologies, radio-frequency IC designs are motivated toward higher frequency. Due to the rapid evolution of the wireless communication in industrial, scientific and medical band, the demands for the low-cost and low-power integrated circuit have been increased. To ensure millimeter-wave circuits and systems work properly, the fabrication technology must be scaled down for high-frequency operations. Unfortunately, there exists a tradeoff between cost and circuit performance. However, it is still a challenging task for the designer to implement millimeter-wave circuits while sustaining lower cost efficiently.

In this thesis, to reduce the cost of the fabricated circuit, a technique of the circuit topology is adopted such that a 30.4 GHz PLL can be realized in standard CMOS technologies. First, independent PD and FD are employed while the conventional PFD structure limits the operating frequency apparently. In addition, the synthetic quasi-TEM transmission line is introduced to the VCO for the small area and higher operating frequency, facilitating circuit implementation in standard 0.18-μm CMOS technologies. Meanwhile, by using the well-designed transmission line, the VCO can be more stable due to good shielding capability. With a standard design procedure of PLL, the experimental results are presented completely for demonstrations. Operated at a 1.8-V supply voltage, the fabricated circuit consumes a dc power of 64.8mW.


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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Recently, the advances in the fabrication technology have enabled chip to implement at the millimeter-wave band using the CMOS technology [1]-[4]. Due to the strong requirements for wireless communication in the industrial, scientific, and medical (ISM) applications, the evolution of lower cost, lower power, and highly integrated circuits has received great attention. Therefore, integrated circuits and systems are constantly motivated toward higher operating frequencies.

The phase-locked loop (PLL) is an essential circuit for providing a reference frequency signal. In the telecommunication, radio and other electronic applications, PLL has been extensively utilized. Several circuits based on the concept of the PLL, such as clock and data recovery (CDR) circuits and frequency synthesizers, are applied for communication and mobile systems. The frequency synthesizers are developed to play critical building components of the radio-frequency integrated circuit (RFIC) in the wireless transceivers, which produces the carrier signal to convert transmission data up to the desired frequency band.

Since the Federal Communication Commission (FCC) defines the frequency band from 22 GHz to 29 GHz as the applications of the vehicle short range radar (SRR) in 2003, the wireless communication technologies in this band catch everyone's eyes due to the significance of the driver safety and comfort in life. Nevertheless, the high cost of Ⅲ-Ⅴ technology in presently available radar modules limits its the wide utilization. The improvement of CMOS technology for high-frequency performance has enabled millimeter-wave circuits and systems with low cost and high volume.

Obviously, PLLs implemented in CMOS process operating beyond 20 GHz have also attracted great attention in integrated circuit design. It is especially a severe challenge for PLLs even though the building block such as VCO can be operated at relatively high frequency. Unfortunately, the operating frequency of PLL is severely suppressed due to restriction of the process. Meanwhile, significant frequency shift in VCO or dividers may occur due to the unexpected parasitic, thus inducing the loop to unlock.

To target the high-frequency PLL, more advanced process has been adopted [1]-[4]. However, the cost must be increased by using highly-advanced process such as 0.13-μm CMOS, 90-nm CMOS and 65-nm CMOS. In consideration of the cost and functionality for the PLL, the tendency toward low-area circuit based on the standard 0.18-μm CMOS technology will be the target.

As author's best knowledge, the published references show that the highest operating frequency is at 24 GHz in a standard 0.18-μm CMOS technology [5]. To further explore the limit of the CMOS technology, the 30-GHz PLL using a standard 0.18-μm CMOS technology is demonstrated in this thesis.

1.2 ORGANIZATION OF THIS THESIS

In the thesis, the high-frequency PLL is presented for the analysis, simulation and experimental verification. The circuit is implemented in a standard 0.18-μm CMOS technology, and the experimental results are demonstrated as well. There are five chapters in this thesis, which are organized as follows.

Chapter 2 provides the basic theories of the phase-locked loop. First, the overview of the PLL is given. Then the building blocks of the PLL are illustrated, including the phase-frequency detector, voltage-controlled oscillator, loop filter and frequency divider.

Chapter 3 presents a 30 GHz PLL for high-frequency operation using the TSMC 0.18-μm CMOS process. In this design, the synthetic quasi-TEM transmission line is adopted for the resonator of the VCO to reduce the chip area. In addition, the decomposed phase and frequency detection is utilized to alleviate the in-band phase noise.

Chapter 4 gives the measurement results for the PLL.

Based on the demonstration in the previous chapters, a conclusion is given in Chapter 5.


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CHAPTER 2

BACKGROUND

Being an essential building block in electronic applications, the phase-locked loop (PLL) is an important integral part of many analog and mix-signal systems. For a designer, the fundamental knowledge of PLL is necessary for the advanced points of view.

The remainder of this chapter is organized as follows. In Section 2.1, the basic concepts of a PLL are mentioned as a starting point of this thesis while the individual building block of a PLL is described in detail in Section 2.2. Then, the linear model of a PLL is introduced in Section 2.3. Finally, a general design procedure of a PLL in provided in Section 2.4.

2.1 BASIC CONCEPTS OF PLL

As shown in Fig. 2.1, a phase-locked loop (PLL) makes the local oscillator trace the input reference signal accurately and then maintains fixed output frequency and phase. In general, a PLL architecture contains a phase/frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage-controlled oscillator (VCO), and several frequency dividers. The function of a PFD is to generate UP/DOWN pulse signals according to the differences between the input reference frequency/phase and

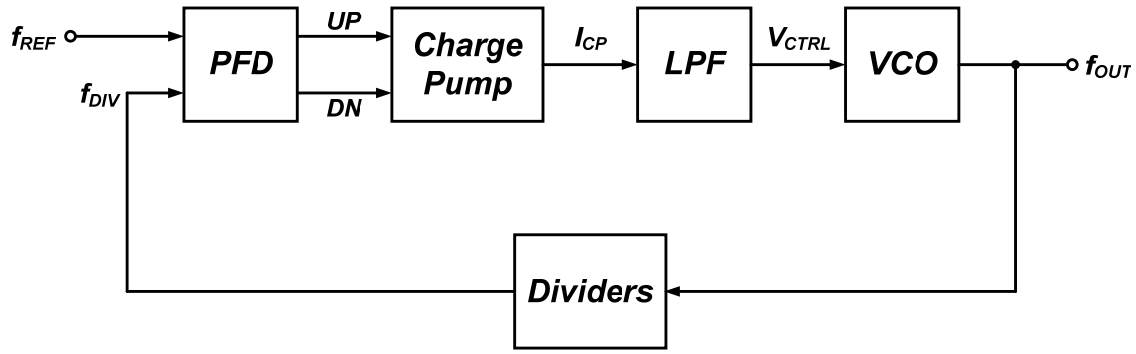


Fig. 2.1 Building block of the conventional PLL

the VCO output frequency/phase, and drives the charge pump circuitry to charge/discharge the low-pass filter. Thus the control voltage varies the output frequency of the VCO. With a division ratio N provided by a series of dividers, a negative feedback loop is formed and the phase locking can be achieved. According to the above description, the output frequency of the VCO is represented as

$$f_{OUT} = N \cdot f_{REF} \tag{2.1}$$

where f_{REF} and f_{OUT} represent the reference frequency and output frequency of VCO.

2.2 BUILDING BLOCKS OF PLL

In this section, each of the basic building blocks of a PLL is described in detail. Also, the operation principle of each block is mentioned by functions and illustrations.

2.2.1 Phase-Frequency Detector & Charge Pump

Since a PLL is a feedback system that compares the output phase with the input phase, the phase detector (PD) serves as a "phase comparator" and converts the phase

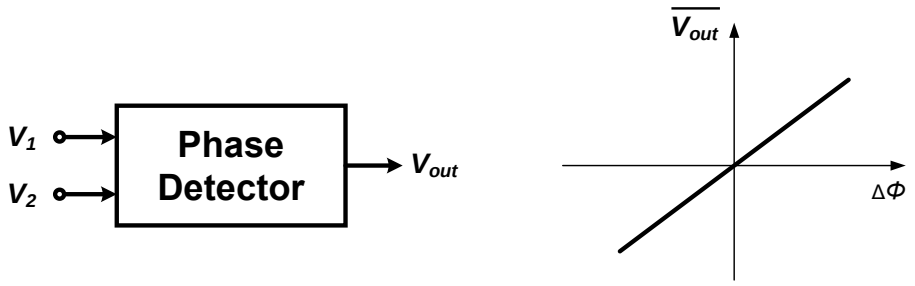


Fig. 2.2 The definition and the transfer curve of an ideal phase detector.

error into average output voltage $\overline{V_{out}}$. As illustrated in Fig. 2.2, $\overline{V_{out}}$ is linearly proportional to the phase difference $\Delta\phi$ and can be expressed as:

$$\overline{V_{out}} = K_{PD} \cdot \Delta\phi, \tag{2.2}$$

where K_{PD} represents the gain of the ideal PD.

In general, the transition from unlocked to locked situation is a complex procedure with nonlinear phenomenon because the PD senses different frequencies from input and output. In addition, the acquisition range is inadequate. Thus, the concept of frequency detection is introduced to overcome these problems. In practice, the phase frequency detector (PFD) is usually utilized in PLL implementations.

Called phase frequency detector (PFD), it merges the phase difference and frequency difference detection. The typical PFD consists of two D-type flip-flops (D-FFs) and an AND gate, as shown in Fig. 2.3. Driven by the signals from PFD, the CP induces charge current to charge/discharge the LPF so as to raise/lower the controlled voltage of the VCO. The timing diagrams of the PFD and CP illustrated in Fig. 2.4

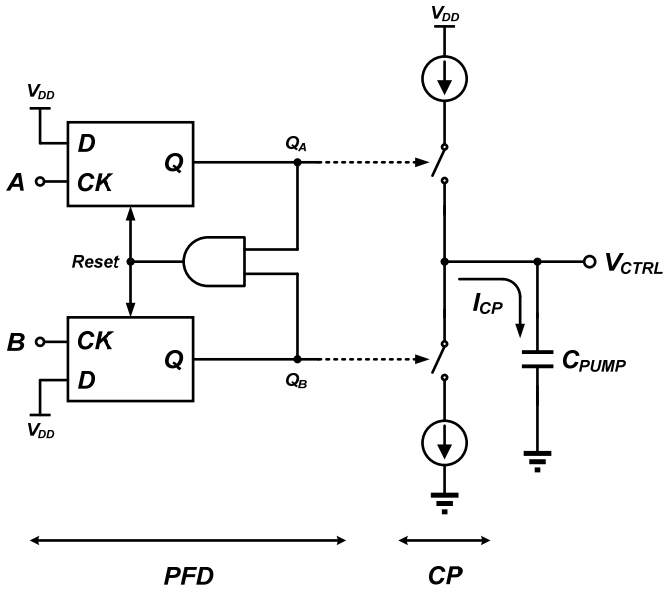


Fig. 2.3 The typical architecture of phase frequency detector (PFD) and charge pump (CP).

shows how they work functionally in two different conditions. For example, while the two inputs of the PFD have equal frequencies but there exists a phase difference between them, as shown in Fig. 2.4(a)(b), a periodic pulse will be generated and the pulse width is proportional to the phase difference, thus drives the VCO to oscillate faster or slower in order to trace the input reference signal. Apart from this situation, while the two inputs of the PFD have different frequencies, as shown in Fig. 2.4(c)(d), an irregular pulse strain appears at the output but the width of the pulse strain grows up continuously to urge effectively the VCO to oscillate as fast/slow as the input reference signal.

In summary, when PFD suffers from two unequal-frequency inputs, the controlled voltage of VCO will rise up or fall down sharply to keep the frequencies of these two

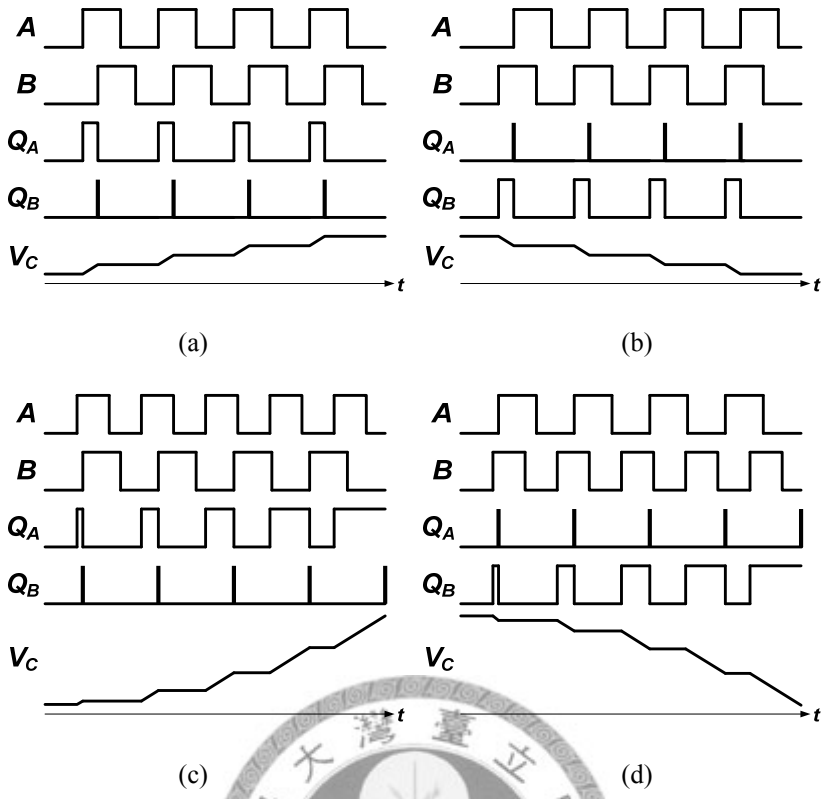


Fig. 2.4 The timing diagrams of the PFD.

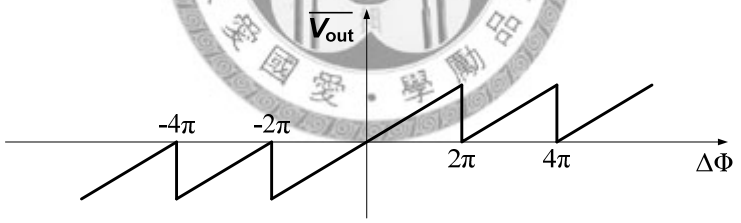
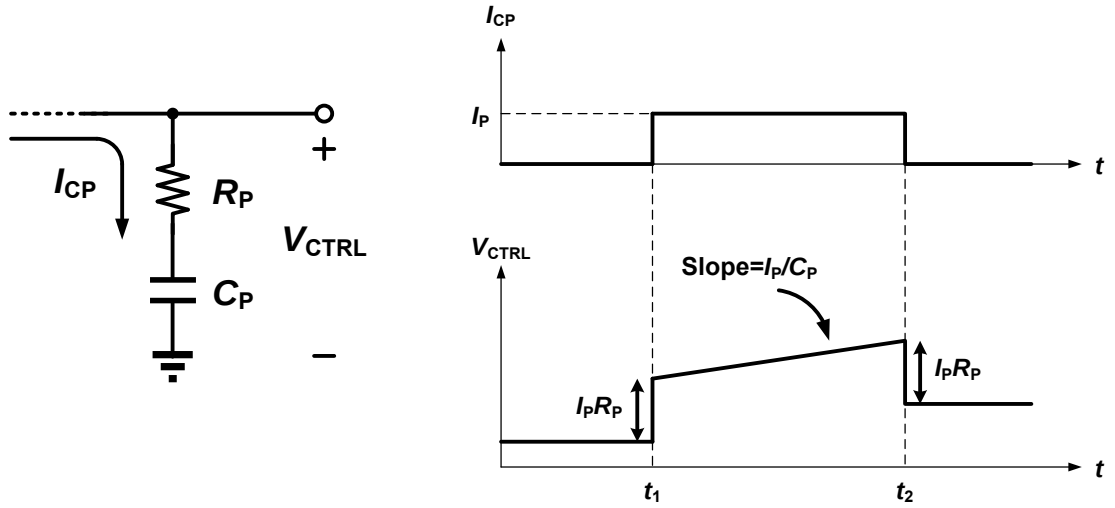


Fig. 2.5 The acquisition range of the PFD.

input signal being identical. Then the minimization of phase difference can be achieved easily by the periodic pulse strain. That's why the PFD has a larger acquisition range compared with simple PD. In fact, the PFD has infinite acquisition range, as illustrated in Fig. 2.5.



(a) (b)

Fig. 2.6 The first-order low-pass filter and its input/output signals.

2.2.2 Loop Filter

For the area and cost consideration, a low-pass filter constructed by passive elements, such as resistors and capacitors, is always used. The main reason is that the active filters have noise issues led from the active components such as OPAMPs. For the better filter performance, discrete passive elements are always applied.

As a LPF, the capacitor C_P illustrated in Fig. 2.6 transfers the pumping current into the voltage signal. In fact, the LPF formed by an individual capacitor may cause stability issues of the close-loop system because of its infinite dc gain. To avoid these issues, a resistor is usually added in series with the capacitor. However, the other non-ideal effects will crash the performance of the whole phase-locked loop.

Fig. 2.6(a) shows the so-called first-order filter and Fig. 2.6(b) illustrates the timing chart while charge pump circuit is activated. Obviously, the voltage jump occurs

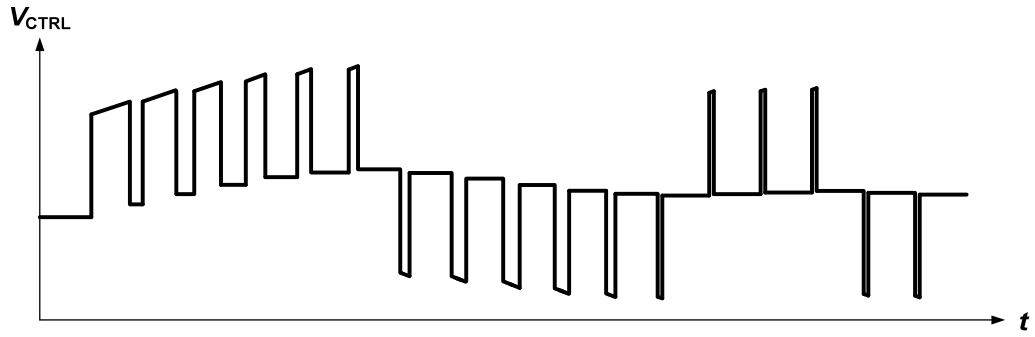


Fig. 2.7 The transient response of PLL while the first-order LPF is used.

at the transition moment of the charge pump current. Since the step signals can be seen as the high-frequency ac signal on the basis of the spectrum, the series capacitor C_P is deemed to be short-circuiting while the current is stepped up and down. Thus the voltage jump/drop reflected on the control node is

$$\Delta V = I_P \cdot R_P . \tag{2.3}$$

This may cause ripples in the phase-locked loop. As shown in Fig 2.7, the control voltage has large glitches while the PLL tries to lock the loop. This is called Granular effect [6]. To eliminate these unwanted glitches, a parallel capacitor can be added to avoid the voltage vibrations. The LPF will be upgraded to second-order one. For the PLL design, the order of the LPF is at least the second-order. Of course, the third-order one or higher may be used for the special requirements or better stability by cases.

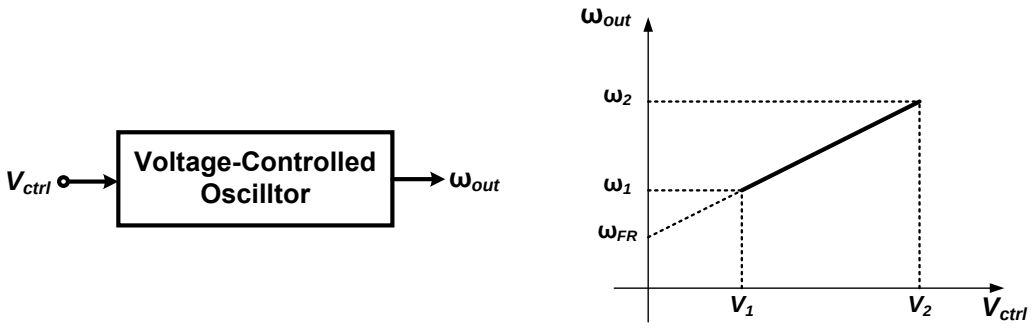


Fig. 2.8 The block diagram of a VCO and its characteristic.

2.2.3 Voltage-Controlled Oscillator

According to the definition, a voltage-controlled oscillator (VCO) is a signal source whose output frequency is the function a voltage signal. As shown in Fig. 2.8, a linear relationship between the output frequencies and the controlled voltage of a VCO is presented. Thus the output frequency is described as

$$\omega_{out} = \omega_{FR} + K_{VCO} \cdot V_{ctrl} \tag{2.4}$$

where ω_{FR} represents the free-running frequency, and K_{VCO} denotes the gain of VCO (expressed in rad/s/V) since it represents the slope of the characteristic. The achievable range, $\omega_2 - \omega_1$, is the tuning range of VCO.

Also called the sensitivity of this circuit, K_{VCO} is an important parameter in the design of a VCO. With the requirement of wide operating frequency, the value of K_{VCO} must be larger, thus leads to an increase of the fluctuation caused from the controlled voltage. Therefore, there is a tradeoff between the tuning range and the noise performance.

By integrating the frequency, the phase can be shown as

$$\phi(t) = \phi_0 + \int_{-\infty}^{t} \omega(t)dt \tag{2.5}$$

where ϕ_0 is the initial phase. Thus the output of an ideal VCO can be represented as

$$V_{out}(t) = A \cdot \cos[\omega_{FR} \cdot t + K_{VCO} \int_{-\infty}^{t} V_{ctrl}(t)dt]. \tag{2.6}$$

That is,

$$\phi_{out}(t) = K_{VCO} \int_{-\infty}^{t} V_{ctrl}(t)dt, \tag{2.7}$$

where ϕ_{out} is the output phase signal. Accordingly, the transfer function of the VCO in Laplace domain is

$$\frac{\theta_{out}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s}. \tag{2.8}$$

In other words, the VCO functions as an integrator.

2.2.4 Frequency Divider

Also called scaler or prescaler, a frequency divider is a circuit that takes an input signal of a frequency f_{in} and generates an output signal of a frequency f_{out}

$$f_{out} = \frac{f_{in}}{N}. \tag{2.9}$$

where N is the division ratio. For a stage of simple frequency divider, the one-stage division ratio is 2. For other special applications, the topologies of dual-modulus divider

will be utilized. Thus the division ratio of the dual-modulus may be N or N+1 depending on the logical state of modulus control.

Frequency divider is an important component for a PLL because it divides the frequency of the output signal and feed it back to the PFD. The PLL will generate a stable clock signal if the frequency difference between the reference signal and the divider output signal approaches to zero.

2.3 The Linear Model for PLL

After understanding the feature of each block, the linear model of PLL can be set up by formulas according to its functionality. Each block will be analyzed in frequency domain as the following descriptions.

2.3.1 Linear Model of PFD & Charge Pump

The phase-frequency detector works as a function of sensing the phase difference between the reference and divided signals and is seen as a phase subtractor. Also called phase error, the phase difference can be expressed as

$$\theta_e = 2\pi \frac{\Delta T}{T}, \tag{2.10}$$

where ΔT indicates the timing difference of these two signals and T means the period of the signal.

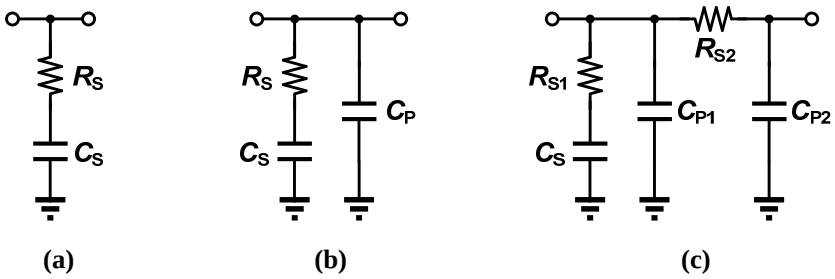


Fig. 2.9 Low-pass filter, (a)first order, (b)second order, (c)third order.

Charge pump circuit transfers the phase difference in the current signal, which denotes as

$$I_{PUMP} = I_{average} = \frac{\Delta T}{T} I_{CP}, \tag{2.11}$$

$$\Rightarrow I_{PUMP} = \frac{\theta_e}{2\pi} I_{CP}. \tag{2.12}$$

where I_{PUMP} is the equivalent current of charge pump. Thus the transfer function of PFD &CP can be expressed as

$$\Rightarrow \frac{I_{PUMP}}{\theta_e} = \frac{I_{CP}}{2\pi}. \tag{2.13}$$

2.3.2 Linear Model of LPF

Owing to the passive elements, the transfer function of the LPF can be derived easily by simple calculations. Fig. 2.9 shows three types of LPF. The glitch problem exists in the first-order LPF while the second-order one is more stable. To further suppress the spur of the PLL, an additional RC stage can be added to form a three-order one, as illustrated on Fig. 2.9(c).

For the proposed PLL in this thesis, a second-order filter is utilized. The loop filter

transfer function is described as

$$F(s) = (R_S + \frac{1}{sC_S}) \| \frac{1}{sC_P} = \frac{sR_SC_S + 1}{s2(C_SC_PR_S) + s(C_S + C_P)}. \tag{2.14}$$

Thus two time constants are defined

$$\omega_P = \cdot \frac{1}{R_S} \frac{C_S + C_P}{C_SC_P}. \tag{2.15}$$

$$\omega_Z = \frac{1}{R_S \cdot C_S}. \tag{2.16}$$

Hence, the transfer function can be expressed as

$$F(s) = K_F \cdot \frac{s + \omega_Z}{\frac{1}{\omega_P} s^2 + s}. \tag{2.17}$$

Where

$$K_F = \frac{R_S \cdot C_S}{C_S + C_P}. \tag{2.18}$$

2.3.3 Linear Model of VCO & Frequency Divider

The transfer function of the voltage-controlled oscillator is presented in (2.8). And from the formula (2.9), the linear model of the frequency divider can be simply derived as

$$\frac{f_{out}}{f_{in}} = \frac{1}{N}. \tag{2.19}$$

2.3.4 Stability Analysis of Phase-Locked Loop

To avoid the Granular effect while a first-order filter, the second-order one is used. With the linear model of the phase-locked loop, the frequency response can be

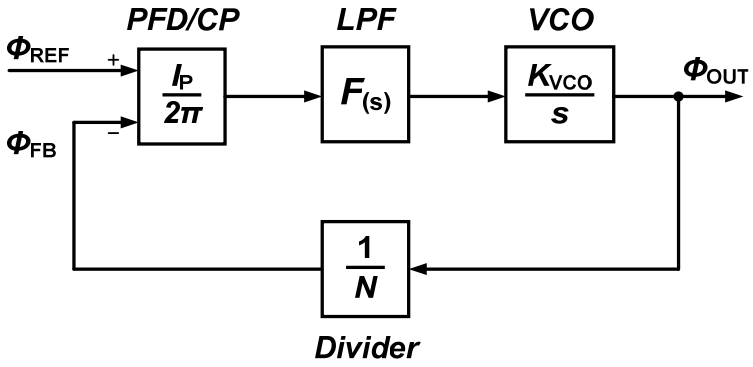


Fig. 2.10 Linear model of phase-locked loop.

characterized well. Fig. 2.10 shows the linear model of the whole circuit. Thus the loop gain can be presented as

$$G(s) = \frac{I_P K_F K_{VCO}}{2\pi N} \cdot \frac{s + \omega_Z}{s^2 (\frac{1}{\omega_P} s + 1)}. \tag{2.20}$$

In order to analyze the stability issue and find the cross-over frequency, s is directly replace by $j\omega$

$$G(j\omega) = -\frac{I_P K_F K_{VCO}}{2\pi N \omega^2} \cdot \frac{j\omega + \omega_Z}{(\frac{j\omega}{\omega_P} + 1)}. \tag{2.21}$$

Then, the phase equation of the loop gain is

$$\theta(j\omega) = \tan^{-1}(\frac{\omega}{\omega_Z}) - \tan^{-1}(\frac{\omega}{\omega_P}) + 180°. \tag{2.22}$$

For the maximum phase margin, the above equation is differentiated with ω and make the result to equal to zero

$$\frac{\theta(j\omega)}{d\omega} = \frac{\omega_Z}{\omega^2 + {\omega_Z}^2} - \frac{\omega_P}{\omega^2 + {\omega_P}^2} = 0. \tag{2.23}$$

$$\Rightarrow \omega_C = \sqrt{\omega_Z \omega_P}. \tag{2.24}$$

By definition, phase margin (measured in degrees) is the difference between phases of

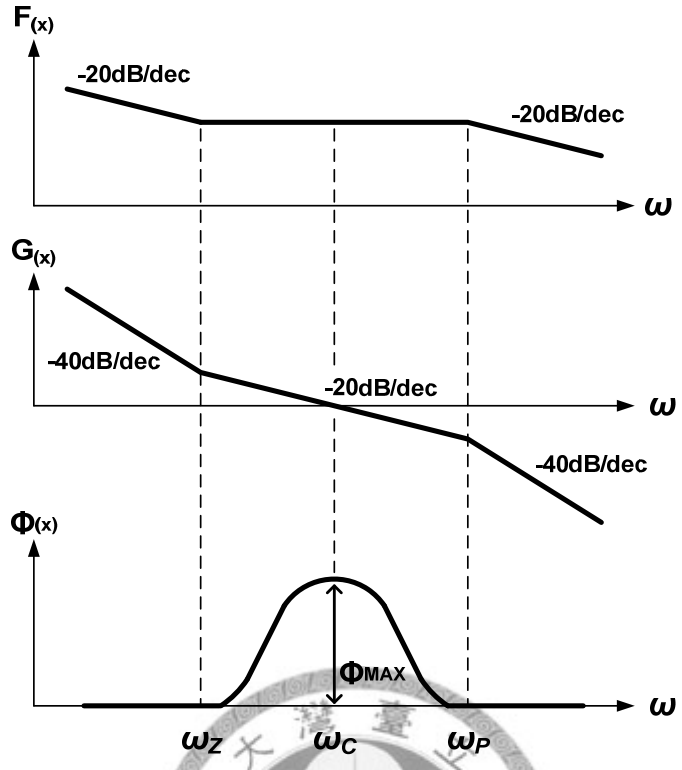


Fig. 2.11 The frequency response of third-order PLL.

the loop and 180° at unity-gain frequency. That is

$$\omega_{0dB} = \omega_C . \tag{2.25}$$

$$\Rightarrow | G(j\omega_{0dB}) | = | G(j\omega_C) | = 1 . \tag{2.26}$$

$$| G(j\omega_C) | = \left| -\frac{I_P K_F K_{VCO}}{2\pi N \omega_C^{\,2}} \right| \cdot \left| \frac{\sqrt{\omega_C^{\,2} + \omega_Z^{\,2}}}{\sqrt{(\frac{\omega_C}{\omega_P})^2 + 1}} \right| = 1 . \tag{2.27}$$

Suppose $\omega_Z << \omega_C << \omega_P$,

$$\Rightarrow \omega_C^{\,2} + \omega_Z^{\,2} \approx \omega_C^{\,2} \quad , \quad \frac{\omega_C}{\omega_P} \approx 0 . \tag{2.28}$$

$$\Rightarrow \omega_C = \frac{I_P K_F K_{VCO}}{2\pi N} . \tag{2.29}$$

Fig. 2.11 illustrates the frequency response of third-order PLL loop-gain transfer function. To design the phase-locked loop properly, a parameter γ can be defined to

Table. 2.1 The parameter γ and the corresponding phase margin.

γ	Phase Margin
1	0°
2	36.9°
3	53.1°
4	61.9°
5	67.4°
6	71°

indicate the maximum phase margin. According to the equation (2.24)

$$\gamma = \frac{\omega_C}{\omega_Z} = \frac{\omega_P}{\omega_C} \tag{2.30}$$

where the parameter γ is a non-zero integer. By choosing γ properly, the phase margin can be designed adequately for the stability of the third-order phase-locked loop. Table 2.1 shows the different γ value and its corresponding maximum phase margin.

In addition, the relationship between two capacitors C_S and C_P can be presented by

$$\frac{C_S}{C_P} = \gamma^2 - 1. \tag{2.31}$$

Thus, the loop-gain bandwidth can be further presented by

$$\omega_C = I_P \cdot R_S (1 - \frac{1}{\gamma^2}) \frac{K_{VCO}}{2\pi N}. \tag{2.32}$$

2.4 General Design Procedure of Phase-Locked Loop

After analyzing the PLL theoretically, a standard design procedure is necessary for designer to optimize the performances of PLL.

At first, some specifications and parameters must be determined to simplify the numerous difficulties. For the voltage-controlled oscillator, the oscillator gain K_{VCO} can be defined by either simulation result or the datasheets of VCO. The loop-gain bandwidth ω_C also can be decided according to the expected transient response. By the system applications, the division ratio N can be chosen directly. At last, the charge pump current I_P must be determined carefully by design. It can be set in the range from 0.1 to 1 mA if the loop filter is off-chip. Otherwise, the current can be reduced reasonably in order to save the chip area and power consumption.

Another important step is to decide the value of passive elements in the low-pass filter. According to the Table 2.1, the ratio of the two capacitors is known by choosing the maximum phase margin. For the general analog circuit design, PM is always be designed larger than 60 degrees. In fact, the popular value of parameter γ is 4 or 5. Utilizing the equation (2.32), the resistor R_S can be calculated after fixing the K_{VCO}, ω_C, N and I_P. Finally, the capacitors C_S and C_P can be found out by calculations.

Usually, this design procedure is provided as a design reference to find a rough solution. The proposed PLL in this thesis is also designed according to this method and is optimized by further simulations. The further discussions are presented in the next chapter in detail.

CHAPTER 3

DESIGN OF SYNTHETIC QUASI-TEM TRANSMISSION LINE FOR 30 GHZ PLL

A 30 GHz phase-locked loop (PLL) is presented for high-frequency operation. By using the synthetic quasi-TEM transmission line for the resonator of VCO, the chip area can be further reduced. Moreover, the in-band phase noise can be alleviated efficiently without affecting operating frequency range owing to the use of the decomposed phase and frequency detection in the circuit implementation. Using a standard 0.18-μm CMOS process, the proposed circuit is realized for demonstration.

The remainder of this chapter is organized as follows. In Section 3.1, a short introduction is illustrated. Section 3.2 describes the proposed architecture and operating principles of the PLL. The design and implementation of the building blocks are demonstrated in Section 3.3. The simulation results of the proposed PLL are presented in section 3.4, respectively. Finally, a summary is given in Section 3.5.

3.1 INTRODUCTION

Due to the advances in silicon integrated circuits technology, the implementation of millimeter-wave systems using CMOS and SiGe BiCMOS technologies is

developed, instead of Ⅲ-Ⅴ technologies which are more expensive in volume production and limited in manufacturing capacity. In recent years, millimeter-wave wireless applications have been rapidly developed applying to the unlicensed band, automotive radars, and advanced imaging systems. Furthermore, integrated circuits and systems are constantly pushed toward higher operating frequencies and higher level of integration due to the desired demand for lower cost, lower power, wider bandwidth and higher data rates in both wireless and wired communication systems.

Being the crucial building block in wireless communication systems, the phase-locked loop is typically employed to generate a stable frequency signal in a high-speed data link. In the recent development, many high-speed PLL designs operated at an output frequency from tens of gigahertz up to 50GHz have been successfully realized [1], [5], [7]-[10]. However, the highest-frequency operation of the published paper is 24 GHz in a standard 0.18-μm CMOS process. In fact, the PLL suffer from not only the phase noise of the VCO but also the severe substrate noise which can not be diminished even with large power consumption. Since the noise contributed by the other circuits can be coupled through the conductive substrate to the VCO, the performance of the phase noise will be degraded.

In the conventional PLL design, the resonator of VCO can be implemented by lumped LC elements. However, the lumped LC elements occupy larger chip area in

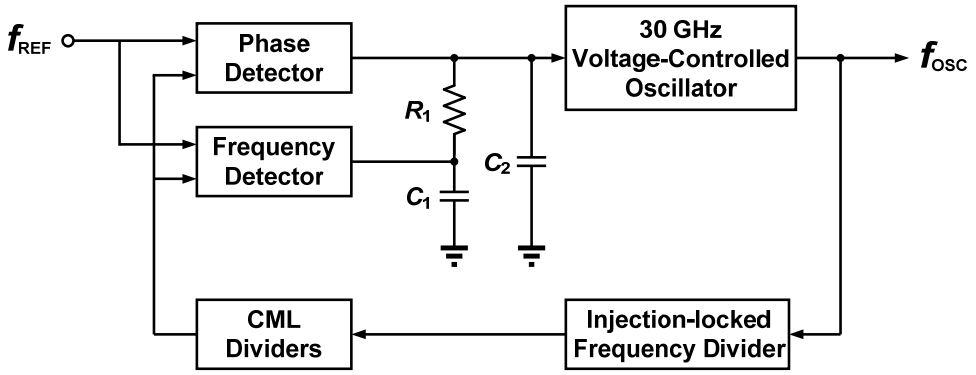


Fig. 3.1 The architecture of the proposed phase-locked loop.

general IC design. Therefore, to reduce the chip area, the synthetic quasi-TEM transmission line is utilized to realize the resonator of VCO at millimeter-wave band. Using a standard 0.18-μm CMOS process, a prototype circuit is demonstrated at the 30-GHz frequency band.

3.2 ARCHITECTURE

The schematic of the 30-GHz PLL architecture is shown in Fig. 3.1. The PLL is composed of a phase detector (PD), a frequency detector (FD), charge pumps, a second-order loop filter, a voltage-controlled oscillator (VCO), an injection-locked frequency divider (ILFD), and current-mode logic (CML) dividers.

In the proposed PLL discussed in this chapter, the reference signal is injected into the PD and FD, which are decomposed from the conventional PFD in order to

minimize noise while keeping a wide acquisition range [8]. In the conventional PLL design, the tri-state PFD is commonly applied to execute phase and frequency detection, as shown in Fig. 2.3. However, the operation frequency of the PFD is considerably limited due to the inherently slow feedback loop that is presented to reset the PFD to its neutral state, where both the Q_A and the Q_B signal are not active [11]. It is noted that the reset time including the propagation delay of the AND gate and the flip-flops will influence the maximum operation frequency of the PFD. Nevertheless, as the reference signal is provided at low frequency, the high dividing ratio will be adopted to generate the matched frequency for phase locking. At the same time, the high dividing ratio will raise the in-band phase noise at the PLL output, and eventually degrades the performance [12].

Therefore, the circuit composed of the PD and the FD is adopted [13], [14] in order to resolve the limitations mentioned above. With the FD enabled, the VCO frequency can be drove toward the desirable frequency. As the output frequency of the last divider is higher than the reference frequency, the loop filter will be charged continuously by the FD. In contrast, the loop filter will be discharged by the FD as the divided signal is lower than the reference frequency. If the divided signal is close to the reference frequency, the FD will be switched off automatically. The PD manages the phase lock of the entire closed-loop afterward. The PD compares the phase of the

reference frequency and the divided frequency and generates an error signal which is proportional to their phase difference. It is noted that the FD will be disabled as soon as the phase lock has been accomplished. Therefore, the influence on the output jitter can be ignored.

By way of charging/discharging the low-pass filter, the control voltage dominates the output frequency of the proposed VCO, which contains the synthetic quasi-TEM transmission line as the main part of resonator. Due to the high-frequency operation of the proposed VCO, the injection-locked frequency divider (ILFD) is employed to be the first divider, and CML-based frequency divider is used for the low-frequency operation. Finally, the quadrature output of the CML dividers is connected to PD and FD as a closed loop for the purpose of providing fixed frequency and the phase in comparison with the input reference signal.

3.3 CIRCUIT IMPLEMENTATION

Using a 1P6M 0.18-μm CMOS process, a 30-GHz PLL is implemented based on the proposed architecture. With a device layout optimized for the RF performance, the n-channel MOSFET in a deep n-well exhibits a cutoff frequency f_T up to 50 GHz. As for the on-chip passive components, a top AlCu metallization with a thickness of 2 μm and the metal-insulator-metal (MIM) structure with oxide intermetal dielectric are

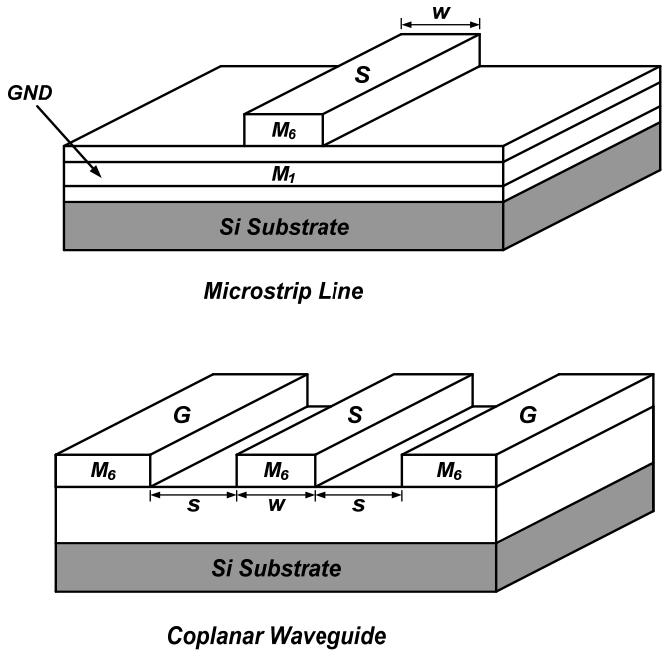


Fig. 3.2 The structures of the microstrip line and the coplanar waveguide.

provided in this technology.

3.3.1 The Proposed Topology of VCO

As we know, the area of the integrated circuits has been one of the essential issues in consideration of the cost. In a standard 1P6M 0.18-μm CMOS process, the spiral inductor is stable and widely used in general. However, it can be problematic while we design IC circuits work in millimeter-wave frequencies due to the large area of the spiral inductor. Therefore, many designs have been presented to provide a compact inductor instead of the large-area inductor in CMOS technologies in consideration of the reasonable circuit performance. Fortunately, the way of the transmission line developing a small inductance at higher frequencies is the most acceptable to the

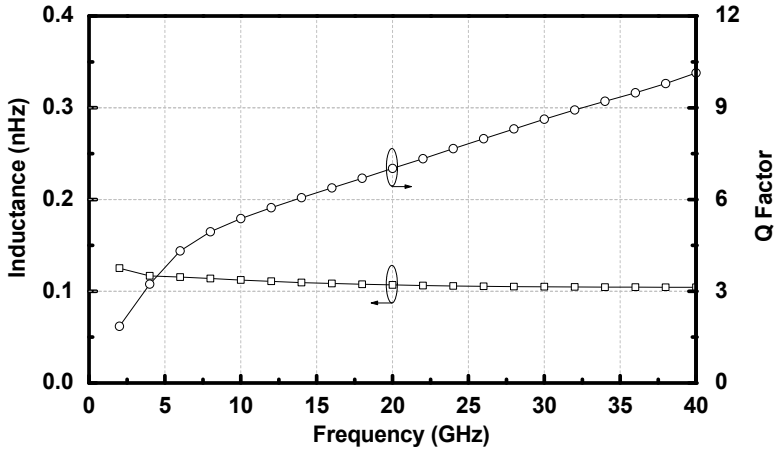


Fig. 3.3 The simulated inductance and Q factor of the microstrip line with the sweep of the frequency.

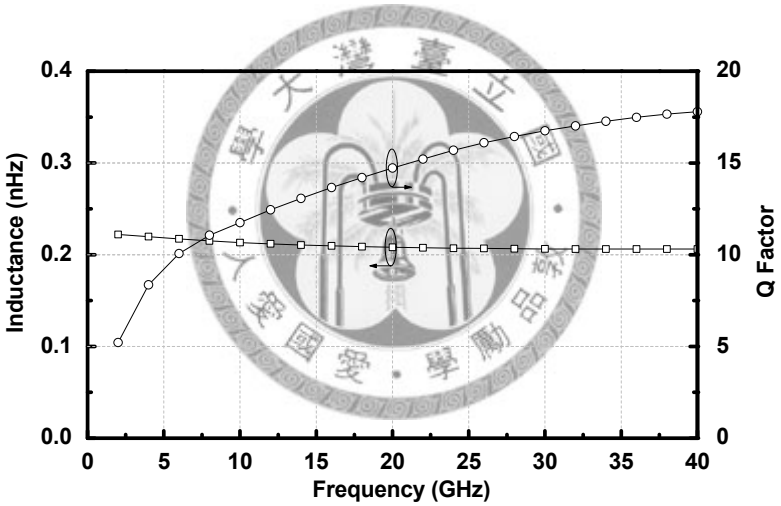


Fig. 3.4 The simulated inductance and Q factor of the coplanar waveguide with the sweep of the frequency.

designers.

3.3.1.1 Microstrip Line & Coplanar Waveguide (CPW)

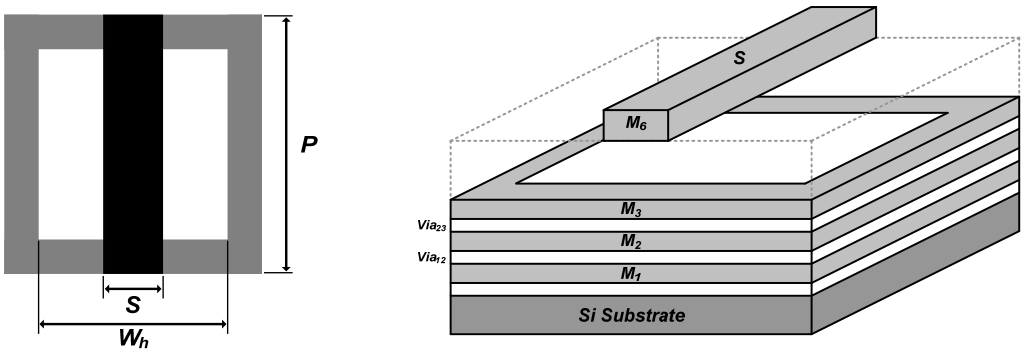
Adopted in CMOS technologies, the transmission line realizes an available

inductance without much performance degradation. Fig. 3.2 shows two transmission structures which are commonly used; the microstrip line and coplanar waveguide. The microstrip line (MSL) is typically implemented by using the top-layer metal as the signal line, and the bottom-layer metal for the ground plane [15]. The drawback of the microstrip line is the close proximity of the ground plane to the signal line, and the quality factor of the transmission line is further degraded. Another common on-chip transmission line is the coplanar waveguide (CPW) which is implemented with one signal line surrounded by two adjacent grounds [16]-[18]. The width of the signal line *w* is used to reduce the conductor loss while the signal to ground spacing *s* controls the characteristic impedance.

Fig. 3.3 and Fig. 3.4 demonstrate the inductance and Q factor for the microstrip line and coplanar waveguide, respectively. Apparently, the smaller inductance can be realized by using transmission line segments at high-frequency bands with a high quality factor. However, due to the large size of the two transmission lines, the synthetic quasi-TEM transmission line is adopted here to lower the area consumption.

3.3.1.2 Adopted Synthetic Quasi-TEM Transmission Line

Also called the complementary-conducting-strip (CCS) transmission line [19]-[22], the synthetic quasi-TEM transmission line forms the LC-tank of the VCO.



(a) (b)

Fig. 3.5 The structures of the synthetic quasi-TEM transmission line (a) 2-D top view of the CCS unit cell. (b) the structure of the CCS.

Fig. 3.5 shows the unit cell of the proposed CCS TL. The structural parameters of the unit cell are P, W_h, S. The periodicity (P) of the unit cell is 30 μm, and the mesh area (W_h) is 28 μm. The line-width (S) of the signal trace is 10 μm.

The unit cell of the CCS TL is composed of the signal trace and the mesh ground plane. The signal trace is realized by metal 6, and the mesh ground plane is made of metal layers from metal 1 to metal 3. The guiding characteristics, including the characteristic impedance, slow-wave factor (SWF) and Q factor, can be extracted by changing the structural parameters of the unit cell for the CCS TL. The slow-wave factor is defined as the normalized phase constant, and the Q factor is the ratio of the phase constant to twice of the attenuation constant. The SWF and Q factor can be expressed to be

$$SWF = \frac{\beta}{k_0} \tag{5.91}$$

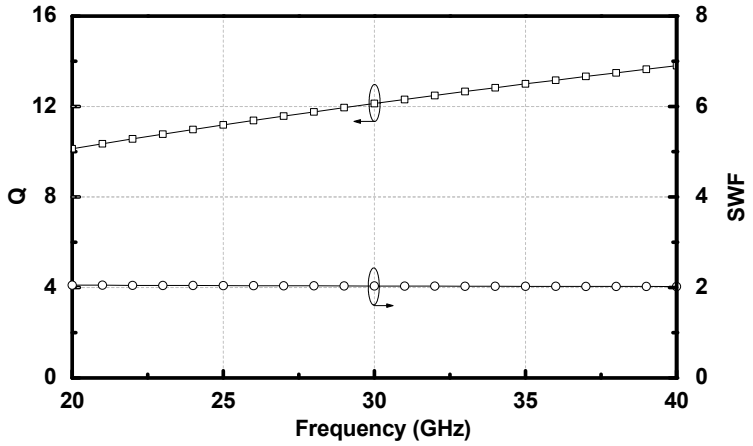


Fig. 3.6 The slow-wave factor and the Q factor of the CCS transmission line.

$$Q = \frac{\beta}{2\alpha} \tag{5.91}$$

where α is the attenuation constant and β is the phase constant.

The complex propagation constant γ and characteristic impedance can be calculated by the S-parameters simulation result extracted by Ansoft's commercial software package High Frequency Structure Simulator (HFSS). And the complex propagation constant γ is expressed to be

$$\gamma = \alpha + j\beta \tag{5.91}$$

Fig. 3.6 shows the slow-wave factor and the Q factor of the CCS transmission line. The real part of the characteristic impedance for CCS transmission line is 59 Ω, and the value of the Q factor at 30 GHz is 12.1. At the same time, the value of the slow-wave factor maintains 2 at frequencies from 20 GHz to 40 GHz.

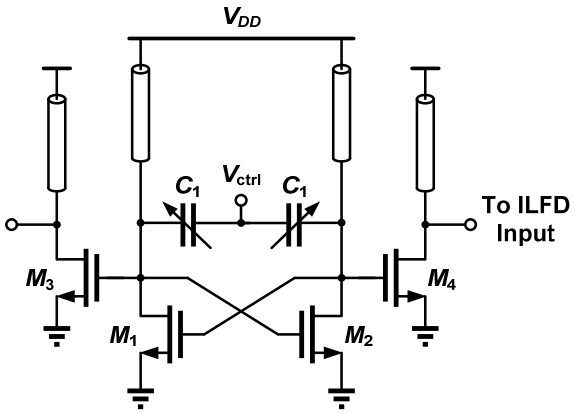


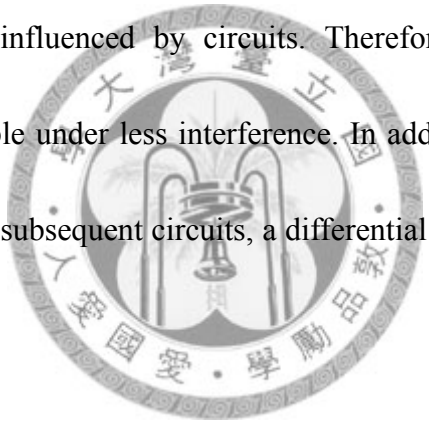
Fig. 3.7 The topology of the proposed voltage-controlled oscillator.

Moreover, to minimize the coupling between the components from the lossy silicon substrate, a well-defined CCS mesh ground plane which can shield most electromagnetic coupling and keep good isolation between circuits is employed [23]. Therefore, the LC tank of the proposed VCO is implemented by two-dimensional (2-D) CCS TL.

Fig. 3.7 illustrates the schematic of the 30-GHz voltage-controlled oscillator circuit which is composed of transmission line segments, a cross-coupled pair and varactors. The cross-coupled pair acting as a negative resistor is employed to compensate for the losses from the passive component. The varactors with the inversion-mode topology are employed for enhanced Q-factors at the high-frequency bands [24], while the maximum to minimum capacitance ratio of the varactor is 1.52. It is noted that the body terminal of the PMOS is connected to V_{DD} and the drain and the source are connected together to control voltage. In addition to the strong,

moderate and weak inversion region, the PMOS varactor can be operated in the accumulation region by connecting the body terminal to V_{DD}. Therefore, it tends to improve the tuning range of the VCO effectively as the capacitance ratio can be increased.

By properly choosing the dimensions of the CCS for the signal trace and the mesh ground plane, the required inductance with sufficient accuracy can be obtained. Due to the shielding effect of electromagnetic of the CCS, the characteristic of the transmission line is less influenced by circuits. Therefore, the voltage-controlled oscillator can be more stable under less interference. In addition, in order to alleviate the loading effect from the subsequent circuits, a differential output buffer is employed at the VCO output.



3.3.2 Injection-Locked Frequency Divider/CML Dividers

As an essential component in the phase-locked loop, the frequency divider is employed to provide a low-frequency replica of the input signal, facilitating the required phase locking. The frequency dividers have been generally realized at high-speed operation by current-mode logic (CML) dividers, miller dividers, dynamic logic dividers, and injection-locked frequency dividers (ILFD). Among the presented dividers, CML dividers [25], [26] based on flip-flop logic circuit are widely used for

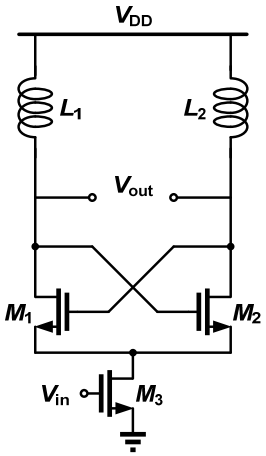


Fig. 3.8 The structures of the conventional injection-locked frequency divider.

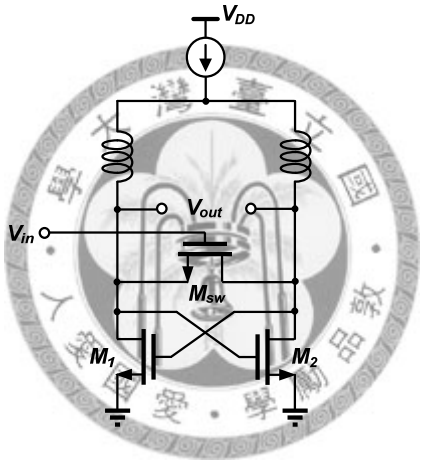


Fig. 3.9 The structures of the direct injection-locked frequency divider.

the advantage of wide locking range. However, the maximum operation frequency of this architecture is limited by the parasitic capacitance of the transistors. On the contrary, the Miller frequency dividers [27] can be implemented up to higher frequency, but suffer from narrow locking range. Dynamic logic frequency divider [28] is characterized for its lower power consumption, unfortunately with a limited range of operating frequency (about few gigahertz). ILFD [29]-[33] based on *LC*-tank has

generally lower power dissipation than CML and Miller dividers, and operate at relatively high frequency. Besides, ILFD is normally used in mm-wave PLL as the first divider stage.

The topology of the conventional ILFD shown in Fig. 3.8 is widely employed in high-frequency band. In general, the input stage is used to provide a signal path and a dc bias path. The tail current transistor M_3 with the requirement of the larger width for the tail current while the input transconductance leads to the huge input parasitic capacitance. Especially working at high frequencies, the injection current of M_3 will be passed to ground severely, thus results in inferior injection efficiency. In addition, inefficient injection will limit the locking range extremely [30]. Obviously it is not suitable to operate at millimeter-wave frequencies with the demand of the wider locking range.

In order to ensure high-frequency operations at 30 GHz, the direct-ILFD for the first divide-by-two circuit is adopted. Also called differential-ILFD shown in Fig. 3.9, this circuit consists of a *LC*-tank, a cross-couple pair, and a switching transistor M_{sw} for input signal. The signal from VCO output is injected directly into the resonator through the switching transistor M_{sw}. Meanwhile, the switching transistor acts as a drain-pumped mixer [33], which mixes the input signal and the free-running oscillator, result in the dominant injection current I_{inj}. The cross-coupled pair with LC-tank forms

the feedback loop [34]. With the absence of the input signal, the circuit is regarded as a free-running oscillator working at the half of the input signal. The locking range can be obtained [35]

$$\Delta\omega = \frac{\omega_o}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{5.91}$$

where Q is the quality factor of the resonant tank, ω_o is the self-oscillation frequency of the resonant tank, I_{inj} is the injection current of M_{sw}, and I_{osc} is the bias current. Apparently, the locking range is proportional to the injection ratio of the injection current to the bias current. That means that the wider locking range can be attained while the injection ratio is enhanced. Moreover, the quality factor of the *LC*-tank also affects the locking range directly. As the Q-factor of the tank is decreased, the locking range can be relatively raised. However, the phase noise will be significantly deteriorated due to lower Q-factor. While the power consumption can be reduced by increasing the Q-factor, the locking range will be relatively reduced. Therefore, the selection for the appropriate Q-factor is extremely important due to the trade-off between phase noise, locking range and power consumption.

Compared with the conventional ILFD, the injection efficiency can be enhanced by using the switching transistor so as to work functionally at high frequencies. Therefore, the size of the switching transistor can be designed smaller than the tail current transistor.

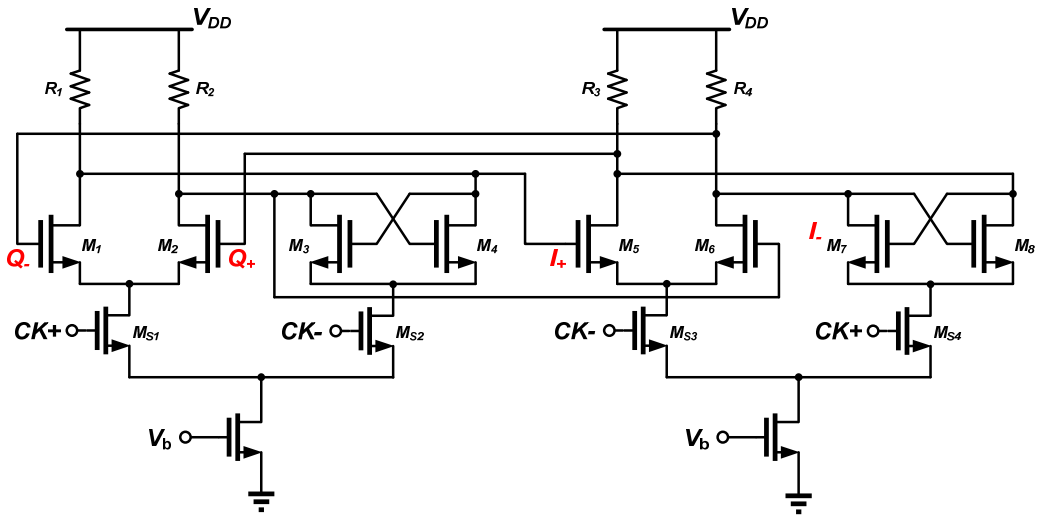


Fig. 3.10 The topology of the current-mode logic frequency divider.

Due to the operation at lower band for latter stages, the CML frequency divider is implemented for the divide-by-two circuits in consideration of chip areas and power consumption. Fig. 3.10 shows the topology of the CML divider that is formed with two CML latches. In addition to the function of frequency division, the CML dividers also generate quadrature output phases according to the differential output of ILFD. To attain the required frequency division, five CML dividers stages will be cascaded. Also called source-coupled logic (SCL), the CML frequency divider can achieve wider locking range while occupying lower chip area. As the operation frequency decreases, the bias current can be scaled down to reduce the power consumption. That means the load resistance can be increased for the smaller bias current.

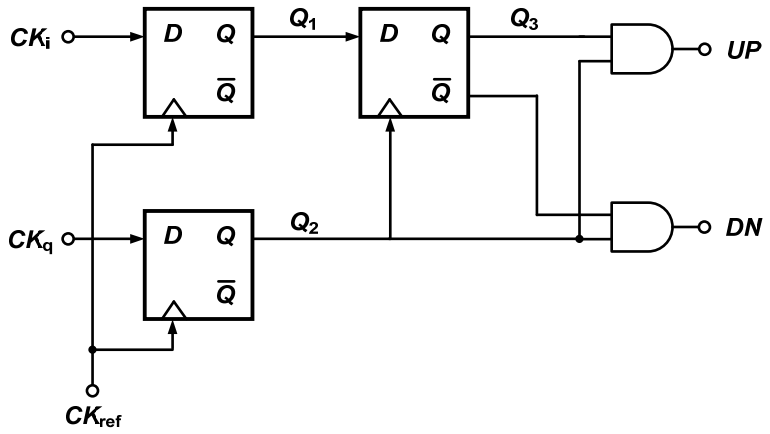


Fig. 3.11 The architecture of the FD adopted in this design.

Fig. 3.12 The architecture of the PD adopted in this design.

3.3.3 Phase Detector/Frequency Detector

The implementation of the PD are shown in Fig. 3.13 [13], based on the architecture provided in Fig. 3.12. In order to alleviate the noise contribution and the power dissipation, the PD and FD are merged with the charge pump circuit. The in-phase signal CK_i and quadrature-phase signal CK_q produced by the last stage of the CML divider generate the quarter-period pulses UP, while the CK_q and the reference signal CK_{ref} create the pulse DN. It is noted that the width of the pulse DN is proportional to the phase error. As the phase locking is achieved at desired output

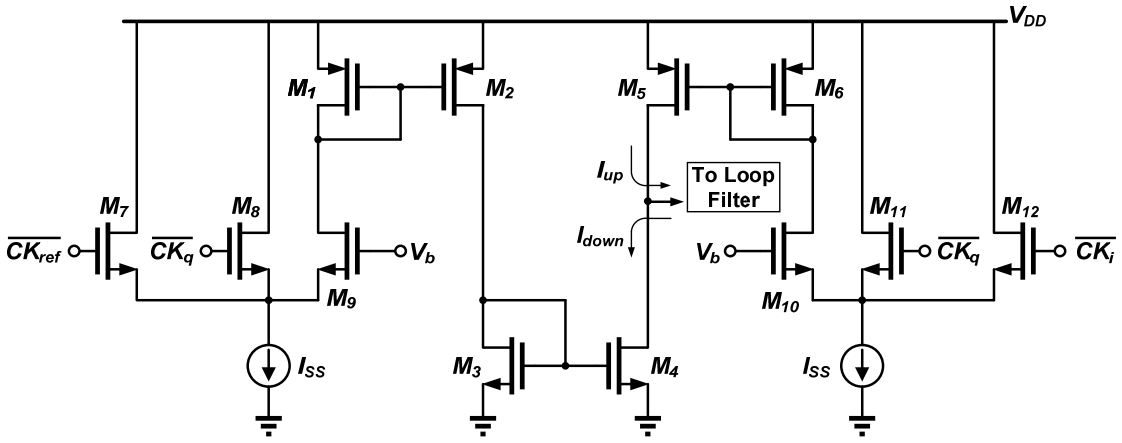


Fig. 3.13 The applied phase detector with the charge pump[13].

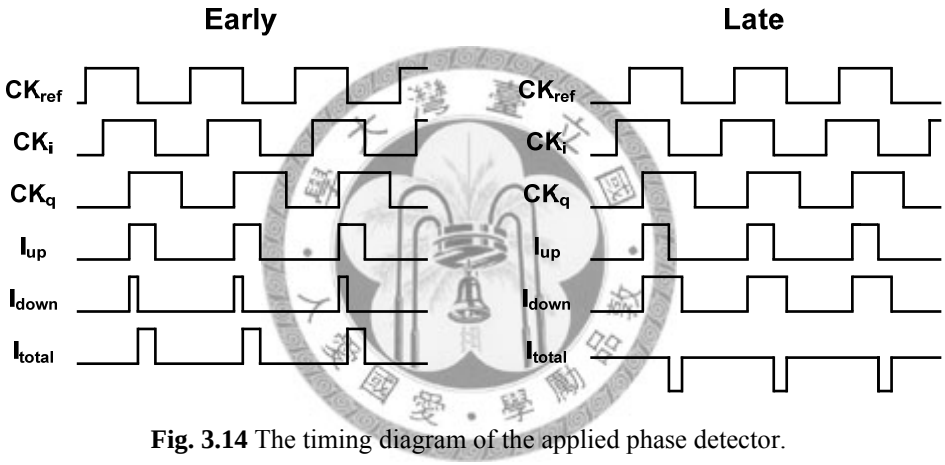


Fig. 3.14 The timing diagram of the applied phase detector.

frequency, the CK_i will be same with CK_{ref}. As a result, the width of the UP pulse is same with the DN pulse eventually.

Since the current mismatch in charge pump will affect the PLL jitter seriously, the channel length of the current mirror has to be chosen carefully according to channel-length modulation.

Fig. 3.11 illustrates the architecture of the FD for this design, which is a binary-type frequency comparator. As the divided signal CK_i is not equal to the

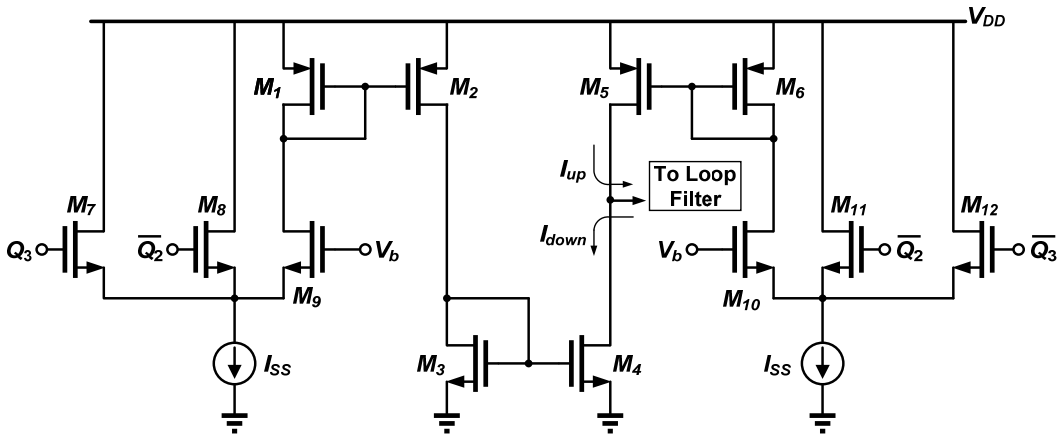


Fig. 3.15 The applied frequency detector with the charge pump [13].

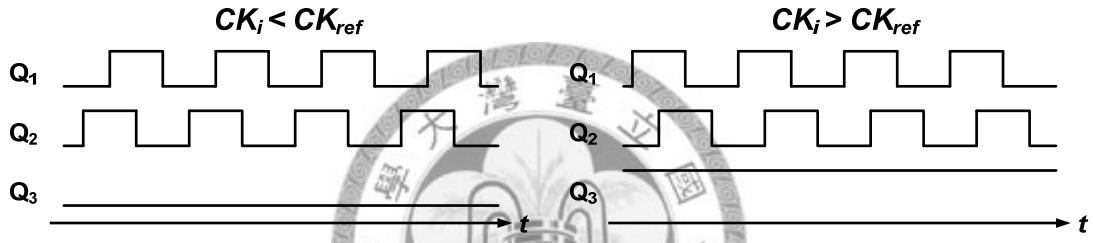


Fig. 3.16 The timing diagram of the applied frequency detector.

reference clock CK_{ref}, CK_i and CK_q are sampled separately by CK_{ref} while providing two periodic signals Q_1 and Q_2. By sampling Q_1 through Q_2, the signal Q_3 can be obtained.

The implementation of the FD based on Fig. 3.11 is illustrated in Fig. 3.15 [13]. It is observed the Q_3 would stay high and enable the charge pump to charge as the frequency of the divided signal CK_i is larger than CK_{ref}. As the frequency of the divided signal CK_i is small than CK_{ref}, Q_3 will stay low and enable the charge pump to discharge.

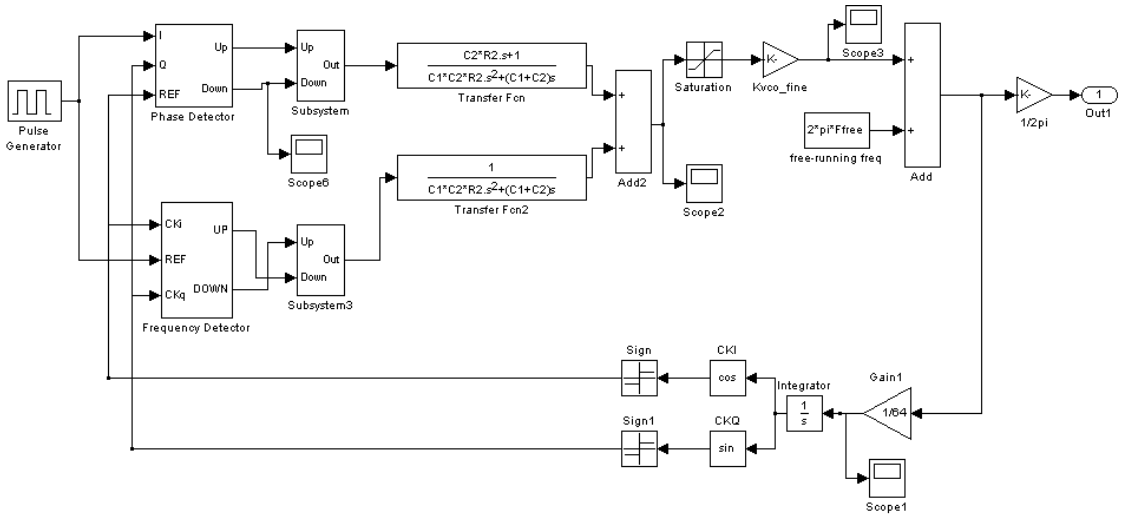


Fig. 3.17 The linear behavior simulation model for the 30GHz PLL.

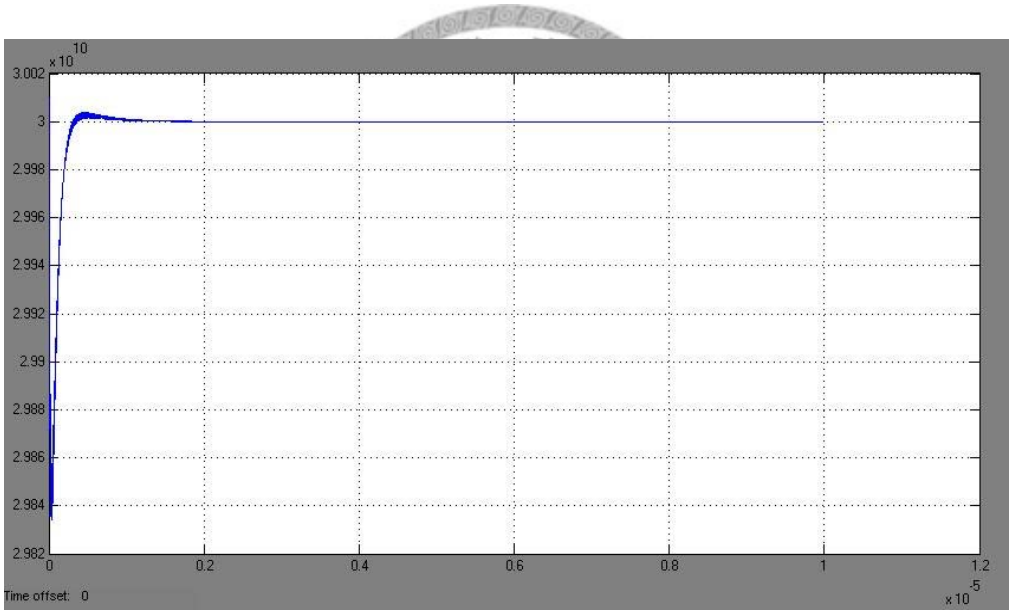


Fig. 3.18 The locking process of the behavior model for the 30GHz PLL.

As the loop is locked, the FD will not produce output signals to disrupt the normal behavior of the PLL. Moreover, Q2 would keep low upon lock. Note that Q2 is applied to the FD and have it disabled as the loop locked is achieved. In other words, the FD activates for 50% of the time during tracking, and automatically switches off when the

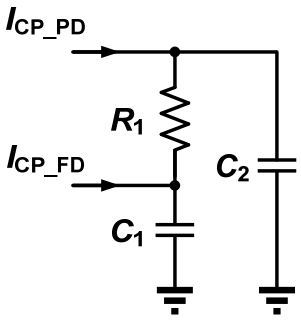


Fig. 3.19 The topology of the second-order loop filter.

Table. 3.1 The design value of the loop filter..

C1	1.9954 pF
C2	50.817 pF
R2	8.0562 kohm
Phase Margin	68°
Loop Bandwidth	2 MHz

frequency acquisition is accomplished [14].

3.4 SIMULATION RESULTS

3.4.1 The Behavior Simulation by Simulink

To know the lock behavior of the PLL, high-level simulations using simulink is performed. The linear behavior simulation model has been illustrated in Fig. 3.17. The PLL with the wider loop bandwidth would be locked to the desired frequency in several μs under the behavior simulation results, as shown in Fig. 3.18. In the linear behavior simulation model, the PD and FD are implemented by ideal digital D-flipflops. At the same time, the VCO is modeled as an ideal linear frequency integrator. The frequency

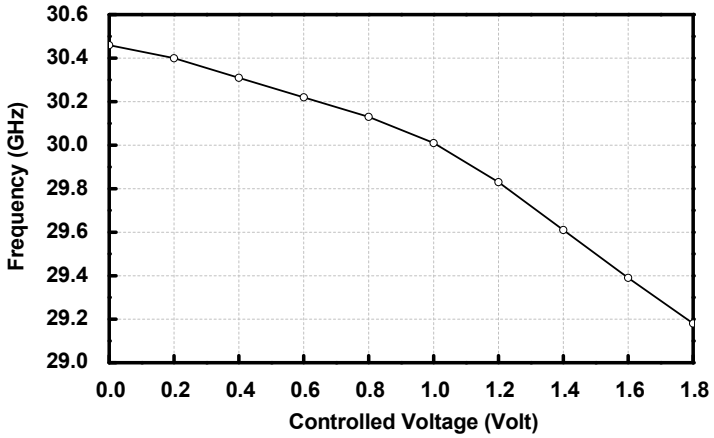


Fig. 3.20 The simulated tuning range of the VCO.

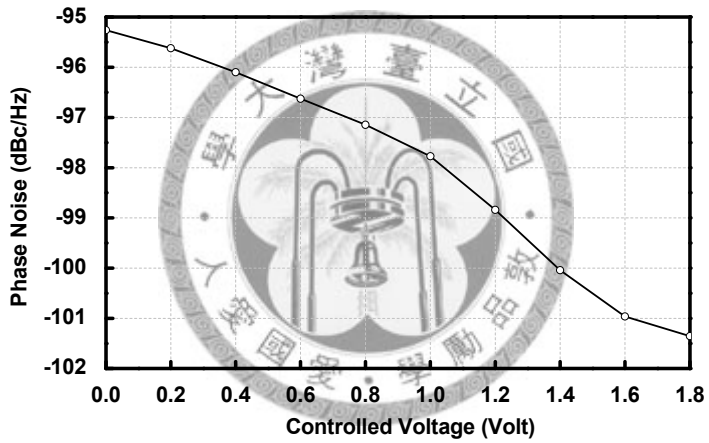


Fig. 3.21 The simulated phase noise of the VCO.

divider has a dividing ratio for 64. The loop filter shown in Fig. 3.19 is designed as a second-order filter, and the parameters of the low-pass filter are illustrated in Table. 3.1. According to the design value in Table. 3.1, the loop bandwidth of the loop filter is designed as 2 MHz, while the phase margin is 68°.

Table. 3.2 The locking range of the direct injection-locked frequency divider.

Temp.	*Corner*	*Freq. Range (GHz)*
25℃	TT	26.1~33.9
	SS	27.2~33.4
	FF	25.1~34.3
0℃	TT	25.8~34.5
	SS	27~33.9
	FF	24.8~34.8
75℃	TT	26.7~33.5
	SS	27.6~33
	FF	25.8~33.8

3.4.2 The Proposed VCO

The simulation result of the tuning range for the VCO in this design is shown in Fig. 3.20, while the output frequency of the VCO can be tuned from 29.19 GHz to 30.47 GHz. Meanwhile, the simulation result of the phase noise for the VCO is shown in Fig. 3.21. In this simulation result, the corner and the temperature are separately set at TT corner and 25℃ in 1.8V supply voltage. According to above simulation results, the tuning range is above 1280MHz, and the phase noise at an offset frequency of 1 MHz is below -95 dBc/Hz.

3.4.3 The Direct-ILFD

Table. 3.2 shows the simulation results for the locking range of the direct-ILFD with different corner and temperature variation. It is noted that the locking range of the

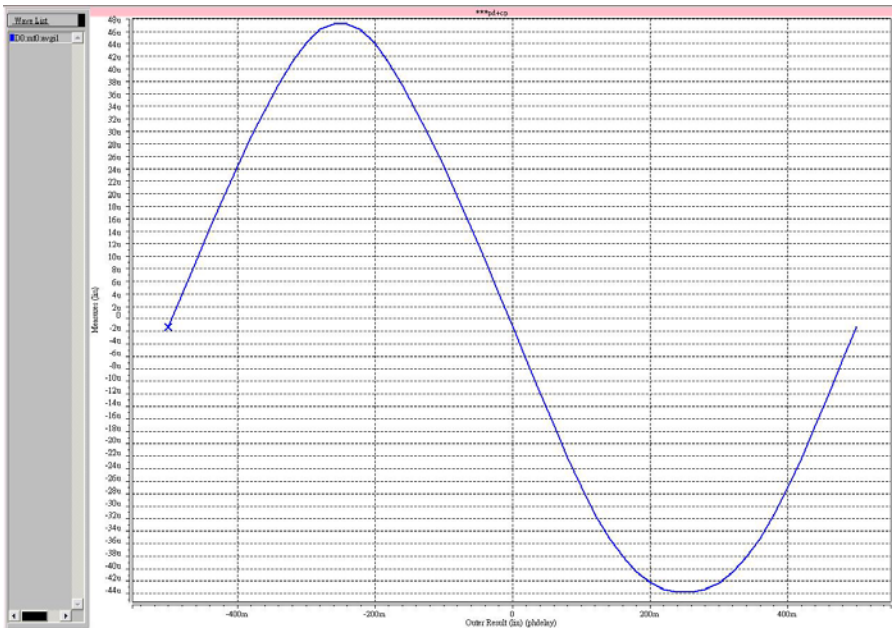


Fig. 3.22 The phase-to-current transfer of the phase detector.

direct-ILFD is wider than 5.4 GHz under the various conditions, which is much larger than the tuning range of the VCO. This implies that a safe locking is achieved under any circumstance.

3.4.4 The Phase Detector

Fig. 3.22 shows the PD characteristics of the simulated result. The figure illustrates the simulated mean charge pump output current as a function of the phase difference between the reference signal and divided signal. It can be observed that there is no gain degradation around zero degrees phase error. Therefore, the PD does not have a dead-zone problem.

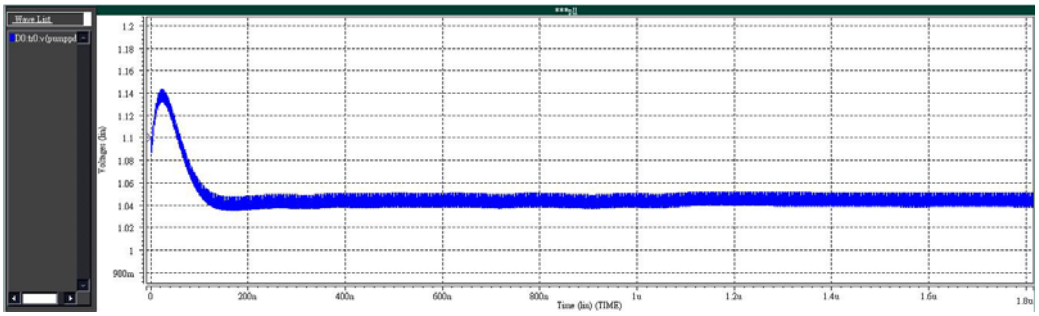


Fig. 3.23 The locking process of the 30-GHz PLL.

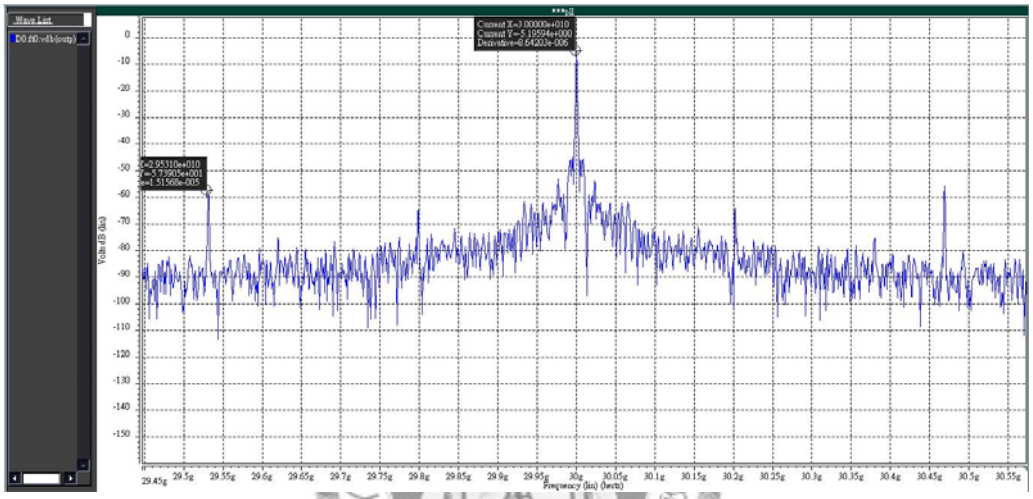


Fig. 3.24 The frequency spectrum for the PLL output.

3.4.5 The Locking Process of the PLL

The locking process of the 30 GHz PLL operating at TT-corner and 25℃ is shown in Fig. 3.23. At the same time, the FFT of the clock signal under the locked condition is shown in Fig. 3.24, which indicates the reference spur is about -52.2 dBc.

Table. 3.3 The 30GHz PLL performance summary.

Technology	TSMC 0.18-μm CMOS
Supply Voltage	1.8 V
Output Frequency	30 GHz
Reference Frequency	468.75 MHz
Multiply Ratio	64
Loop Bandwidth	2 MHz
VCO tuning range	1280 MHz
VCO phase noise	-95.2 dBc/Hz @ 1MHz offset
Total Power	71 mW

CHAPTER 4

EXPERIMENTAL RESULTS

According to the design procedure mentioned before, the performance of a 30-GHz PLL utilizing synthetic quasi-TEM transmission line is demonstrated in this chapter. Fabricated in the TSMC 0.18-μm CMOS process, the chip area of the whole circuit is about 0.737×0.647 mm^2, including the bonding pads and the on-wafer probing pads.

The microphotograph of the 30-GHz PLL is shown in Fig. 4.1 while the 2nd-order loop filter is realized by discrete components. Owing to the stability consideration of this circuit, the values of R_1, $C_1$and C_2 are 8.0562 kΩ, 1.9954 pF and 50.817 pF, respectively. Also, a FR4 printed circuit board (PCB) and SMA connectors are used to prevent the performance degradation from the unpredictable issues. By using the bonding-wires, DC pads and signal pads are connected to the PCB. The overall set-up is shown in Fig. 4.2.

With an Agilent E4448A PSA spectrum analyzer, the output characteristics of the PLL were evaluated properly. In order to get better performance of the phase noise, both an Agilent E5052B signal source analyzer (SSA) and an Agilent E5053A microwave downconverter are employed. Since the output frequency of the PLL is beyond the measurement frequency band of the signal source analyzer, harmonic mixers 11970A

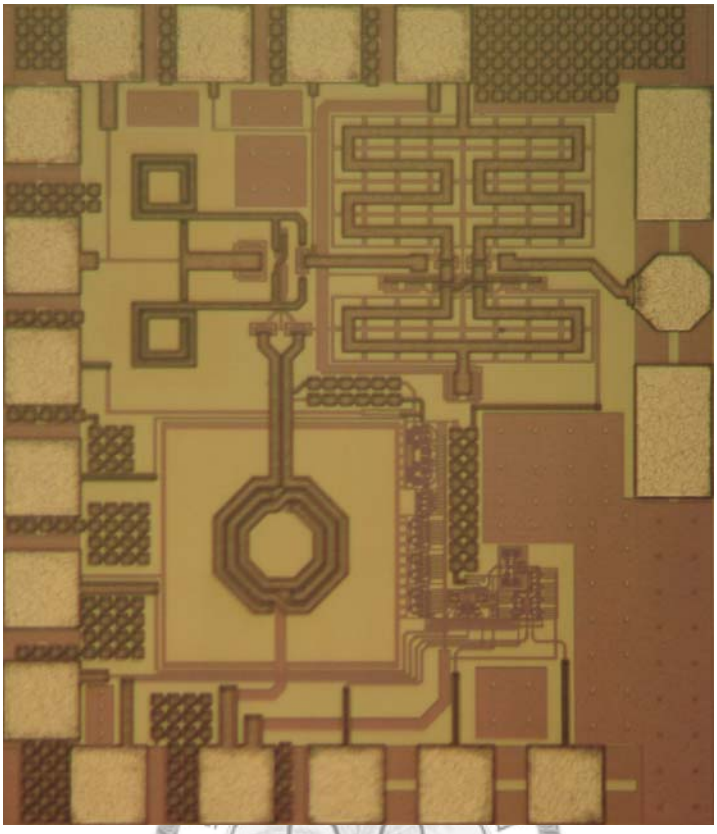


Fig. 4.1 The microphotograph of the fabricated PLL.

are required in the measurement loop. Therefore, by using external harmonic mixers, phase noise measurements above 26.5GHz can be done. An Agilent E8257D analog signal generator is used as the reference for all the closed-loop measurements. For the requirement of differential signals, one balun is inserted with an input signal generated by Agilent E8257D. In addition, a bias-T is used to set the DC bias point, as shown in Fig. 4.3, since a DC offset bias voltage cannot be provided by the Agilent E8257D analog signal generator.

Operated at a supply voltage of 1.8 V, the overall power dissipation of the fabricated circuit is 64.8 mw (excluding buffer) in which 22.14 mw is consumed by the

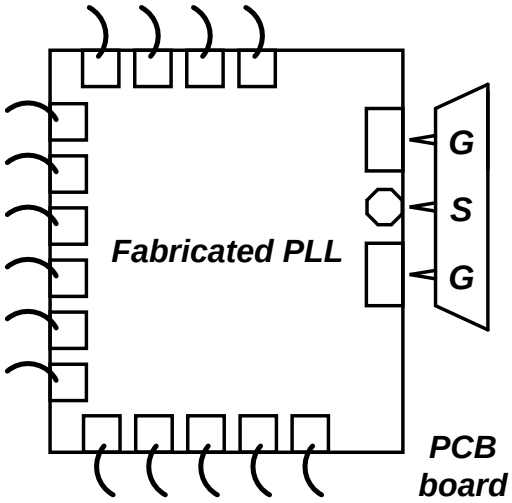


Fig. 4.2 The set-up for the measurement.

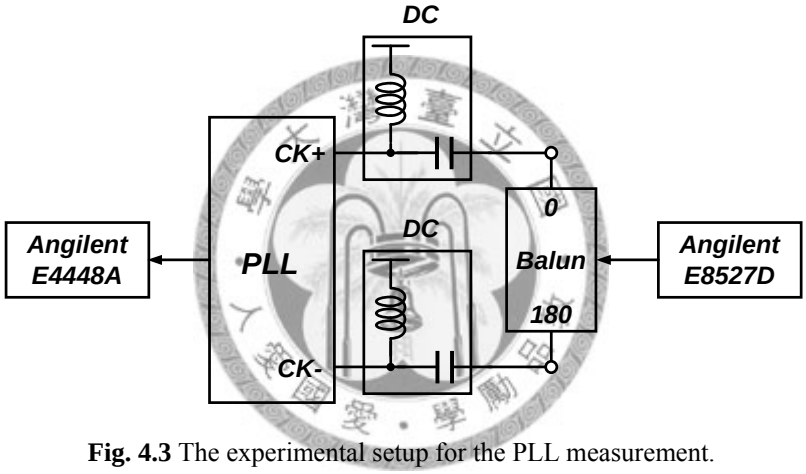


Fig. 4.3 The experimental setup for the PLL measurement.

VCO. Before evaluating the PLL performance, the proposed VCO is characterized first to verify its functionality. By providing a V_{DD} of 1.8 V, VCO draws 12-mA current to oscillate while its buffer draws 11-mA current. Fig. 4.4 shows the measured output characteristics versus the varactor controlled voltage of the VCO. Measured by on-wafer probing, the VCO exhibits a frequency tuning range from 30.01 to 30.88 GHz as the controlled voltage sweeps from 0 to 1.8 V for the various frequency bands, indicating a frequency tuning range of 2.86% and an average VCO gain (K_{VCO}) of 483

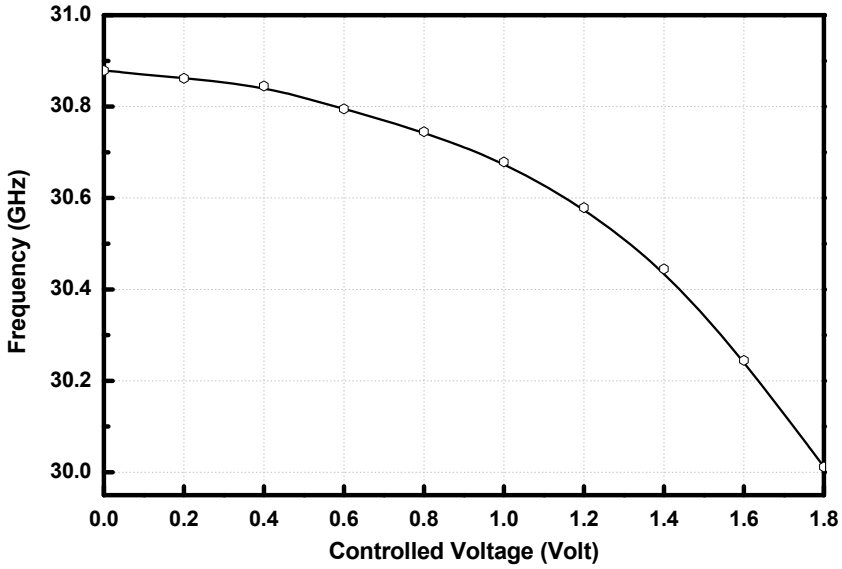


Fig. 4.4 The measured output tuning characteristics of the proposed VCO

MHz/V.

The proposed PLL can be locked from 30.08 to 30.4 GHz while consuming 64.8 mW. Using an Agilent E4448A spectrum analyzer and Agilent E8257D signal generator, the performance of the PLL can be evaluated properly. An Agilent E8257 D is used to provide a 10 dBm sine wave as the frequency reference signal between 470 and 475 MHz. With a reference frequency, the measured output spectrum is illustrated in Fig. 4.5. In this figure, the PLL can be well locked at 30.4 GHz and the spur is about -24 dB as the input frequency reference is 475 MHz. Fig. 4.6 shows the phase-noise performance of the PLL from 1 kHz to 40 MHz. The measured phase noise of the PLL output is − 89.9 dBc/Hz at an offset frequency of 1 MHz. The performance summary of the fabricated circuit along with results from previously published works [5], [7]-[8], [10] is

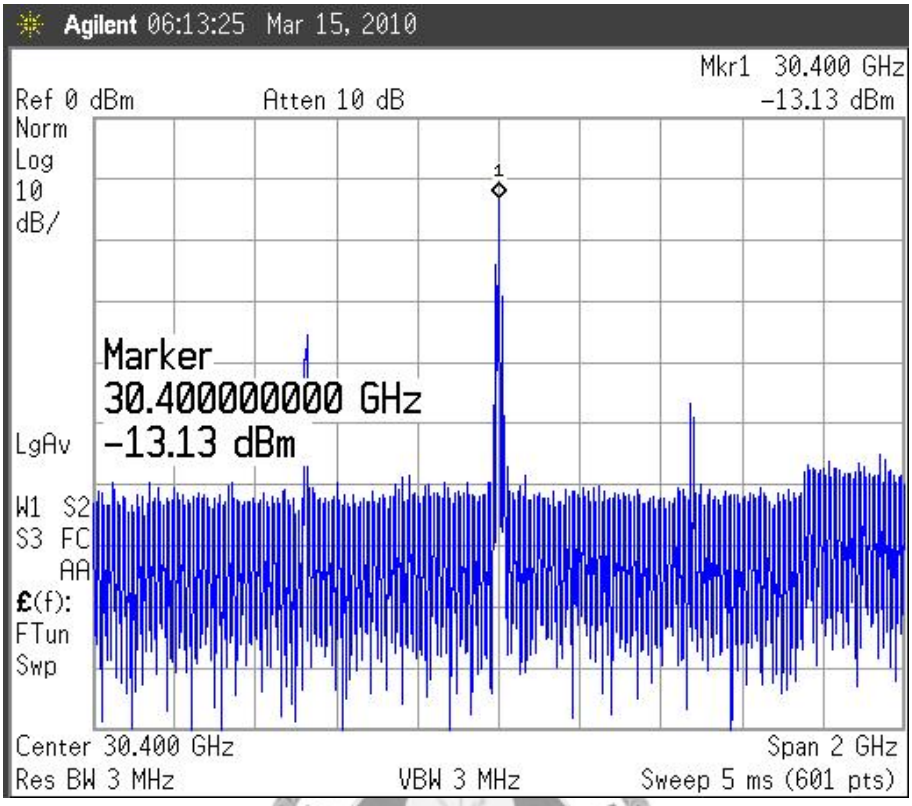


Fig. 4.5 The 30.4-GHz measured output spectrum under locking state.

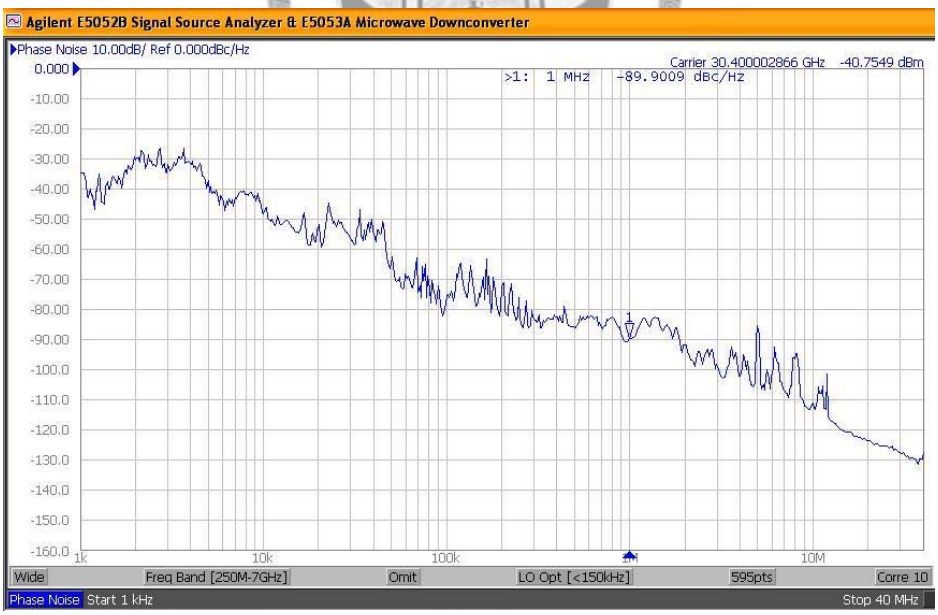


Fig. 4.6 The measured output phase noise under locking state.

tabulated in Table 4.1 for comparison.

Using a standard 0.18-μm CMOS process, a 30.4-GHz phase-locked loop is

Table. 4.1 The Performance Summary of the Phase-Locked Loop.

	This Work	**[5]**	**[8]**	**[10]**	**[7]**
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm	GaAs 0.5 μm	CMOS 0.13 μm
Supply Voltage	1.8 V	1 V	1.8 V	2.0 V	1.5 V
Output Frequency	30.4 GHz	24.2 GHz	20 GHz	30 GHz	20 GHz
Reference Frequency	475 MHz	12.1 GHz	625 MHz	3.75 GHz	78 MHz
VCO Tuning Range	867 MHz	1440 MHz	1600 MHz	2100 MHz	4.26 GHz
Phase Noise	-89.9@1M	-106.3@100K	N/A	-116@1M	-95.7@1M
VCO & Divider Power Consumption	61.3 mW	14.5 mW	N/A	61 mW	18 mW
Total Power Consumption	64.8 mW	17.5 mW	40 mW	80 mW	22.5 mW
Chip Size	0.476 mm^2	1.235 mm^2	0.64 mm^2	0.9 mm^2	0.6 mm^2

successfully developed in this work. In order to operate at high frequency, the synthetic quasi-TEM transmission line is utilized to replace the inductors of resonant tank. For the high-frequency division, the injection-locked frequency divider is involved in this circuit. The fabricated PLL consumes a dc power of 64.8 mW. It is well-suited for the wireless application at the Ka-band.

CHAPTER 5

CONCLUSION

In this thesis, design and implementation of a high-frequency PLL in standard 0.18-μm CMOS technologies is concentrated while the conclusion is provided as follows.

In Chapter 3, the general topology of a phase-locked loop for the millimeter-wave applications is presented. To ensure the high-frequency operation of the PLL, the synthetic quasi-TEM transmission line is used as the resonant tank due to the sufficient shielding effect of the electromagnetic coupling. Besides, the area of the voltage-controlled oscillator can be minimized since larger area of the spiral inductor is replaced by the transmission line, thus reduce the total area of this chip effectively. Owing to the decomposition of phase and frequency detection, the phase noise and jitter can be alleviated without lowering the operating frequency range. According to the simulation result, the proposed VCO oscillates from 29.18 GHz to 30.46 GHz at a 1.8V supply voltage. The phase noise of the VCO is below -95 dBc/Hz at an offset frequency of 1 MHz.

Following the above section, the measurement results of PLL is demonstrated in Chapter 4, Operated at a 1.8-V supply voltage, the fabricated circuit excluding the

buffer consumes a dc power of 64.8 mW. With a reference frequency of 475 MHz, the measured locking frequency of the PLL is 30.4 GHz. The measured phase noise at an offset of 1MHz is -89.9 dBc/Hz while the PLL is locked well. The proposed PLL can be locked in a frequency range from 30.08 GHz to 30.4 GHz, corresponding to a hold-in range of 320 MHz.

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