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低靜態電流且具快速暫態響應之漣波耦合固定導通時間降壓轉換器設計與實現

Design and Implementation of A Ripple-Coupling Constant On-Time Controlled Buck Converter with Low-Quiescent Current and Fast Transient Response

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本論文係阮呂政安君（學號 R06921070）在國立臺灣大學電機工程學系完成之碩士學位論文，於民國 109 年 05 月 29 日承下列考試委員審查通過及口試及格，特此證明。

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來到碩士生涯的尾聲，同時也是最後一段學生時光，心裡感到五味雜陳，在讀碩士的這段時間，深刻感受到學問的廣博以及自己的不足，所以始終提醒自己要認真學習。在研究的路上遇到了許多困難與挫折，時時會懷疑自己的能力甚至想放棄，但許多人的幫助讓我走到了這步，在此特別感謝指導老師陳景然博士，始終以最親切的語氣指導著我並讓我了解分析問題的方法，也時刻關心我們的生活。同時也感謝口試委員陳耀銘教授、劉深淵教授對於論文內容的建議與修改。

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摘要

市面上越來越多的低功率降壓轉換器被應用於手持式裝置以及物聯網裝置，像是手機、電子智慧手環、心律血壓偵測器...等。由於這類產品需要能長時間使用並且這些裝置大部分時間都處於待機且低負載的狀態，所以其降壓轉換器需要能應付寬廣的負載範圍變化以及有良好的輕載效率。然而在輕載效率下，降低控制器的功率損耗將會是低功率之降壓轉換器的一大難題。本論文提出一高度數位化之降壓轉換器控制積體電路，其動態負載範圍為 $1.25x10^5$，且在 100μA 負載電流下仍有 85%以上的效率。控制積體電路主要針對導通時間產生器、補償器以及電容電流感測器電路做改良，導通時間產生器以數位的方式實現，使其可以隨負載下降功耗。補償器則利用電荷幫浦式誤差放大器及動態偏壓電路來降低偏壓電流的消耗。電容電流感測器利用全被動元件感測電流，取代傳統放大器組成的感測器。上述所提出之電路,使用台積電 0.18μm 製程實現,晶片面積為 1.2 平方毫米。第一個版本中實現了連續導通模式並且量測之峰值效率為 88.5%。第二個版本中實現了連續導通模式以及不連續導通模式，模擬顯示控制器的總靜態電流為 3.3μA，在 10μA 的負載下，效率為 47%。當負載大於 100μA，效率皆大於 85%。

關鍵字- 低功率降壓型轉換器、高度數位化控制器、寬負載範圍、電荷幫浦、動態偏壓、電容電流固定導通時間控制之降壓轉換器。

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Abstract

The low-power buck converters are widely used in consumer electronic products and Internet of Things products, such as electronic smart bracelets, heart rate detectors, etc. Since these devices need to be used for a long time and they operate in standby mode most of the time, the low-power buck converter needs to handle the wide load range and have good light load efficiency. However, under light load efficiency, reducing the power loss of the controller will be a major problem for low-power buck converters. This thesis proposed a highly digital controller buck converter with a dynamic load range of 1.25 x 10^5, and an efficiency of more than 85% at a load current of 100μA. The controller is mainly aimed at improving the on-time generator, compensator, and capacitive current sensor circuit. The on-time generator was implemented in a digital manner so that it can reduce power consumption with the load. The compensator was replaced by a charge pump-based error amplifier and a dynamic bias circuit to reduce the consumption of bias current. The capacitor-current sensor was implemented by fully passive components, instead of the amplifier-based current sensor. The proposed control was fabricated in an integrated circuit using 0.18 μm TSMC CMOS process with the chip area is 1.2mm^2. In the first version, the CCM part was implemented and the peak efficiency was measured to be 88.5%. In the second edition, CCM and DCM were implemented. The simulation showed that the total quiescent current of the

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controller consumes 3.3 μA, and the efficiency is 47% under 10 μA load current. When the load current is greater than 100μA, the efficiency is larger than 85%.

Index Terms- low-power buck converter, charge pump, constant on-time control, highly digital control, low quiescent current, wide load range, dynamic bias

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Chapter 1

Introduction

1.1 Background: Voltage Regulators (VRs) for low power Devices

The energy efficiency of integrated circuits continues to become a major factor in determining the size, weight, and cost of portable electronic systems. They exist as autonomous or handheld objects in every environment around us and even within us, significantly improving the quality of life. These applications include mobile phones, wearable devices, wireless sensor networks, etc. With the increasing usage of these objects, battery life is getting more attention as our mobile devices. Besides, more functionality such as heart rate monitoring and body temperature measuring is required on the devices. That is, aggressive low-power circuit design and efficient power delivery are required to meet battery constraints.

On the other hand, the power converter in low-power applications needs to regulate output voltage at a wide load range and achieves fast load transient response as well. Fig. 1-1 shows the load range of the sensor devices, wearable devices, and handheld devices. In this work, we mainly focus on the wearable device. Because the load range

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of the wearable devices is from the micro-ampere level to the sub-ampere level. In order to achieve the high efficiency under the wide load range. Therefore, the multi-mode operation has been used in the buck converter for the stringent load conditions.

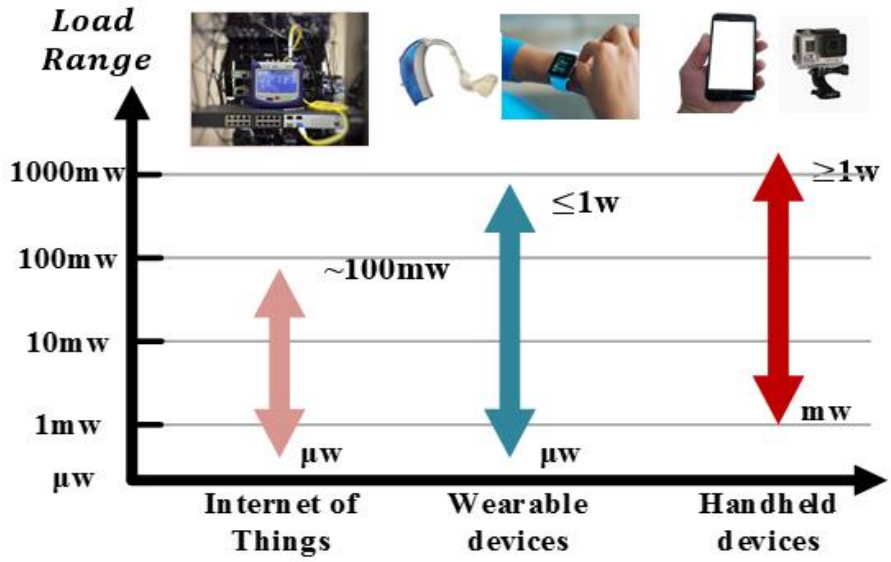

Fig. 1-1 Load range of the different devices

The power consumption over time of wearable device is shown in Fig. 1-2. Its operation mode can roughly separate into three parts: sensing mode, standby mode, and communication mode. Under normal use, the devices will perform sensing operation every fixed time and occasionally be used for communication mode. In fact, wearable devices operate in standby mode most of the time. From Fig. 1-2, we can see that the average power of the standby mode accounts for 25% of the total power loss. Therefore, mitigating the power loss in standby mode is one of the ways to extend battery life.

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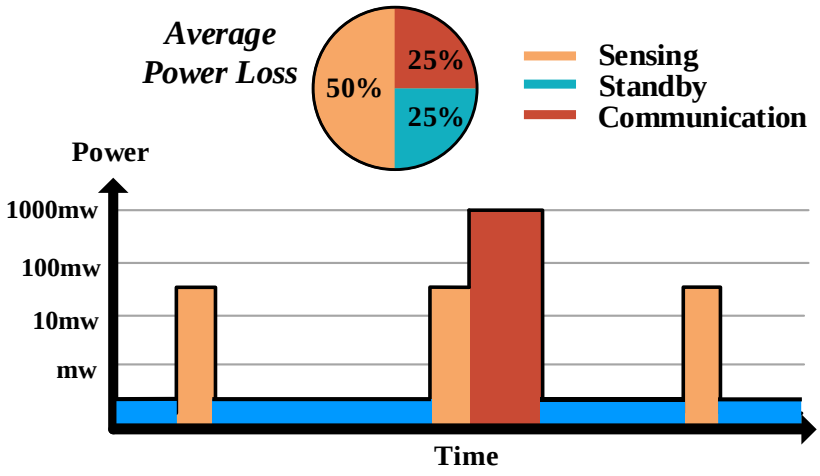

Fig. 1-2 Power consumption of a wearable device over time

In the ultra-light load condition (standby mode), the power loss is dominated by the controller loss, which can be observed in Fig. 1-3 and Fig. 1-4. The quiescent current of the controller, Controller IQ, is the limitation on ultra-light load efficiency because switching loss and conduction loss will gradually smaller than the controller loss. In other words, it is critical to reduce the quiescent current of the controller for improving the light-load efficiency.

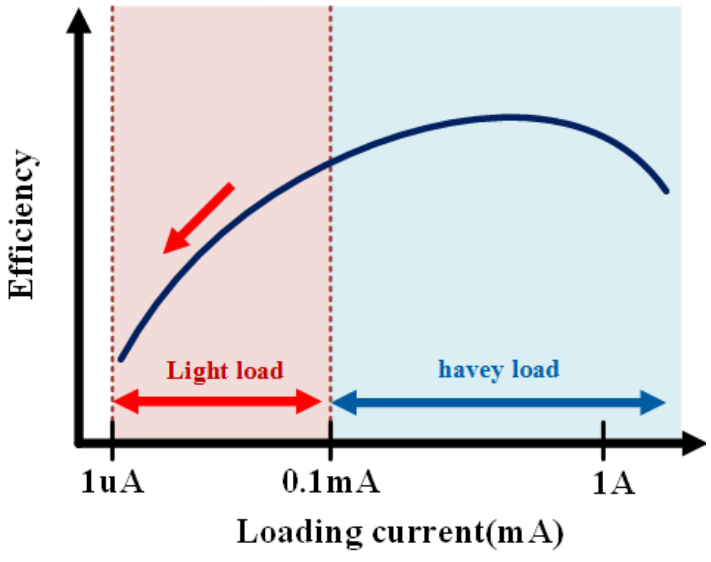

Fig. 1-3 Efficiency plot with the change in loading current

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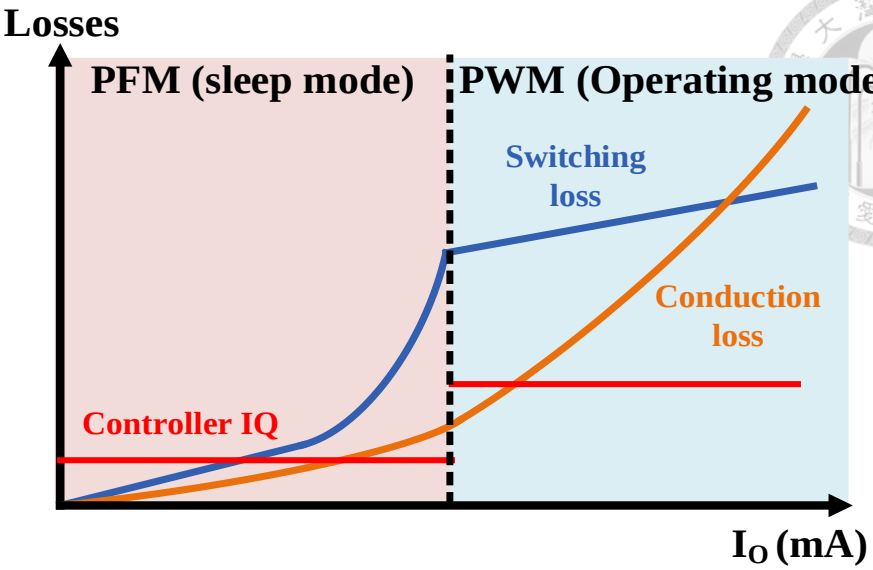

Fig. 1-4 Power losses plot versus loading current

1.2 Motivation

In recent years, more and more novel control schemes have been applied in the low power field. Because low power applications often need to handle the loads from microampere to milli-ampere, they require not only good heavy-load efficiency but also good light-load efficiency. In previous work, the low power converters were implemented with multiple operation modes [1], [2]. For example, the converter operates in pulse width modulation mode (PWM mode) under heavy load, and it changes to pulse frequency modulation mode (PFM mode) at light load. PFM mode can greatly reduce switching loss to improve light load efficiency. However, the mode transition between PFM mode and PWM mode cannot be changed automatically. Thus, the wide load transient will suffer the transition problem. In order to achieve the seamless mode transition and the fast load transient response. Therefore, COT control

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was implemented in this dissertation because there is the inherent discontinuous conduction mode (DCM) in COT control. Then, we compared the three architectures (RBCOT, V^2COT, and C^2COT) and chose an architecture that is suitable for low power converter to improve and implement.

Ripple-based constant on time (RBCOT) control has found applications in powers converter because of its simple architecture, fast load transient response, small components count, and good light-load efficiency. However, this control scheme encounters two problems. One is output voltage DC offset; the other is sub-harmonic oscillation when ceramic capacitors are used for output filter capacitors.

Another control method is V^2 constant on-time (V^2COT) with the inductor ramp that has been proposed to solve the problem of instability. However, in this architecture, the differential amplifiers used to add the current ramp into the modulation is power-hungry. Therefore, the modified C^2COT control with three proposed control blocks was implemented to alleviate these problems. The ripple coupling path (RCP), digital on/off-time generator, and charge pump-based error amplifier (CPEA) mitigated the sub-harmonic issue and power consumption problem.

1.3 Thesis outline

In Chapter 2, a literature survey about research works of constant on-time buck converters on voltage regulators (VRs) is introduced. Ripple-based COT(RBCOT),

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V^2COT,and current-mode COT(CMCOT) are analyzed in this chapter. Moreover, the previous work on low quiescent current buck converter will be reviewed in this chapter, also.

In Chapter 3, The introduction of the proposed constant on-time control buck converter will be presented. Moreover, the compensation design of the charge pump-based error amplifier (CPEA), the operation principle of the digital on/off-time generator, linear search zero current detector, and dc voltage clamper will be illustrated.

Chapter 4 presents the transistor level circuit implementation of the controller and the detailed design of the passive and active device for low quiescent current design.

Chapter 5 shows the simulations and experimental results. Finally, the chapter 6 summarizes the conclusions and Future works of this thesis.

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Chapter 2

Review of Buck Converter for Low-Power Application

2.1 Multi-Mode Low Quiescent Current Dc-Dc Buck Converter

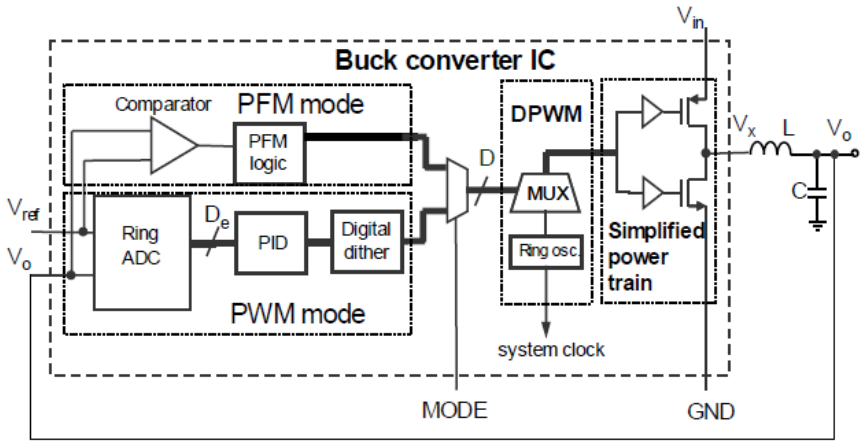

Fig. 2-1 Block diagram of the dual-mode digitally-controlled buck converter

Fig. 2-1 shows an ultra-low-quiescent-power dual-mode digitally-controlled buck converter [1]. The control method is divided into two parts including PWM mode and PFM mode. PWM mode operates the converter in continuous conduction mode (CCM). In this mode, the error between V_O and Vref is quantized by the ADC to provide a error signal to the digital compensator, PID, and generate a duty ratio D. The DPWM converts the duty ratio into a PWM signal for controlling the high-side and the low-side

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switches. On the other hand, PFM mode runs the converter in discontinuous conduction mode (DCM) with fixed sampling frequency, fixed on-time, and variable off-time. When V_O is lower than V_{ref}, the controller will introduce a fixed on-time through the DPWM to charge the output capacitor. Otherwise, the converter and controller are idling. The control utilizes two operation modes to cope with the wide load conditions. When the system is running under heavy load, the controller is operated in PWM mode. On the contrary, when the system is running under light load, the controller is operated in PFM mode. If the system operates under PWM at the light load conditions, the efficiency will become extremely poor as shown is Fig. 2-2. Therefore, the feature is that the switching frequency in PFM mode scales proportionally to the load conditions. In other words, the switching loss is greatly reduced in the light load conditions. However, the ultra-light load efficiency is limited by the controller quiescent power. The digital controller is triggered by fixed sampling frequency. According to Table 2-1, PFM mode quiescent current is 4μA in the ultra-light loads. Moreover, the load current only covers from 0.1mA to 400mA. If the system operates at i_{LOAD}=10μA, the efficiency is roughly 42%. Another drawback is that the wide load transient from heavy load to ultra-light load will suffer the mode transition problem because the mode transition between PWM and PFM mode is done manually. It cannot be changed automatically.

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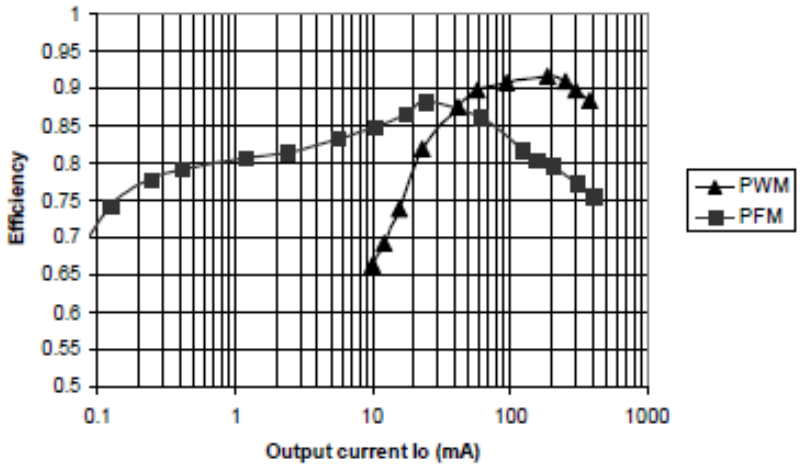

Fig. 2-2 Measured PWM and PFM mode efficiency in dual-mode buck converter

Table 2-1 Performance table of dual-mode buck converter

Technology	0.25-μm CMOS (Max. supply 2.75V)
Input Voltage	5.5-2.8V
Output Voltage	1.0-1.8V
Load Current Range	0.1mA-400mA
PFM Mode Sampling Freq.	600kHz
PFM Mode Quiescent Current	4μA
PWM Mode Switching Freq.	0.5-1.5MHz

Fig. 2-3 shows a tri-mode digital buck converter with self-tracking zero-current detection [2]. To obtain a wide output power range, the converter is operated in CCM and DCM at heavy load and light load conditions, respectively. Furthermore, there is

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an AM control which is activated in aggressive-light load conditions. When the output power is lower than 10μW, the power consumption of the controller circuits becomes critical and limits efficiency. Therefore, While AM control is activated in light load, the gate of low-side MOS, M_N, will be connected to the ground and M_N conducts the inductor current by the body diode. For minimizing the power consumption, DPWM, PFM controller, ZCD, and the NMOS driver will be disabled, and the Efficiency over output current are illustrated in Fig. 2-4.

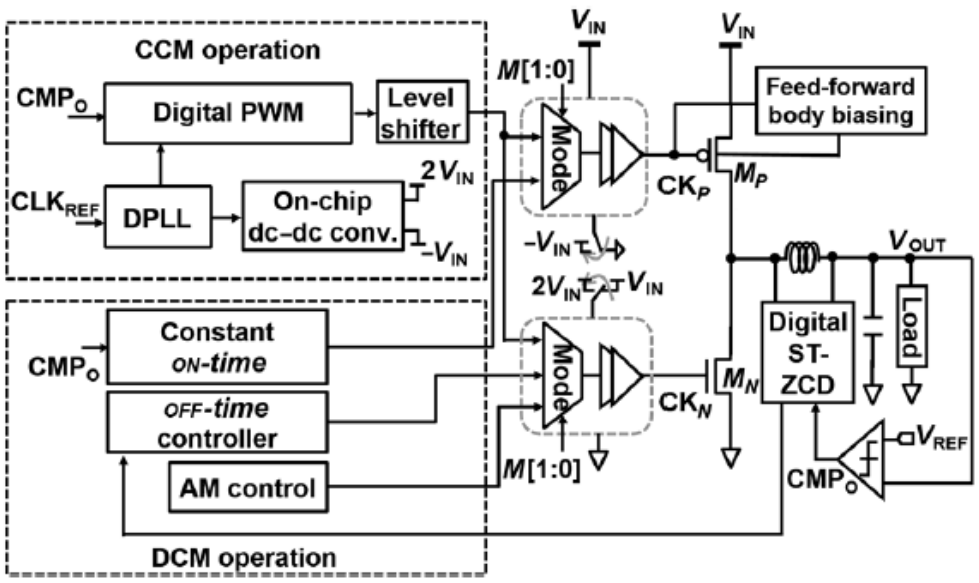

Fig. 2-3 Block diagram of the tri-mode digital buck converter

The tri-mode buck converter efficaciously improves light load efficiency, but its mode selection is done manually by the external 2-bit multiplexer. That is, When the load-step occurs from micro-ampere to milli-ampere, the mode transition cannot change automatically. This problem is also encountered in the dual-mode buck

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converter. Therefore, the proposed controller will be mentioned in the later dissertation, and then it will be improved to the automatic mode transition for a large load-step.

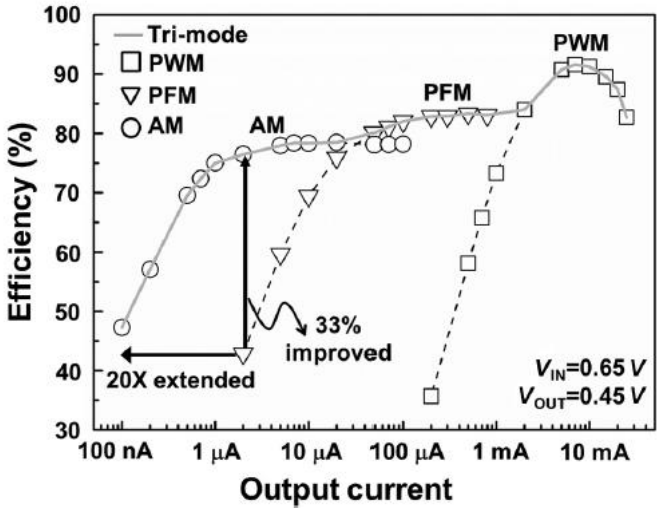

Fig. 2-4 Measured efficiency versus output loading current with tri-mode operation

2.2 Constant On-time Control

2.2.1 Review of Ripple-based Constant On-time Control

In the past several years, DC-DC converters with constant on-time (COT) control scheme have been adopted for many applications because of simplicity and high conversion efficiency [3]-[7]. Ripple-based COT controls achieve fast transient response because the output voltage directly goes into the modulation without passing through an error amplifier. No compensation is required in the RBCOT control scheme shown in Fig. 2-5. Relatively, the simple architecture means the redundant quiescent current of the controller can be saved.

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Moreover, RBCOT converter achieves good light-load efficiency. The converter is usually designed to operate in a discontinuous conduction mode (DCM) under light-load condition. Under such a condition, the switching frequency is automatically decreased with the load current level for a COT controller. Since the switching loss is dominant under a light-load condition, a reduction of switching frequency improves the overall efficiency.

However, RBCOT control encounters a DC offset issue introduced by the modulation mechanism. The reason is that RBCOT control regulates the valley of the output voltage, V_O, to reference voltage, V_{REF}, instead of regulating the average output voltage to V_{REF}. The second problem is RBCOT suffered from the sub-harmonic oscillation instability, especially when the capacitors with the low-equivalent series resistor (low-ESR) are used as the output capacitors [3]-[7]. Recently, the ceramic capacitor is often applied as the output capacitor due to the small size, but their low-ESR characteristics will make the instability place.

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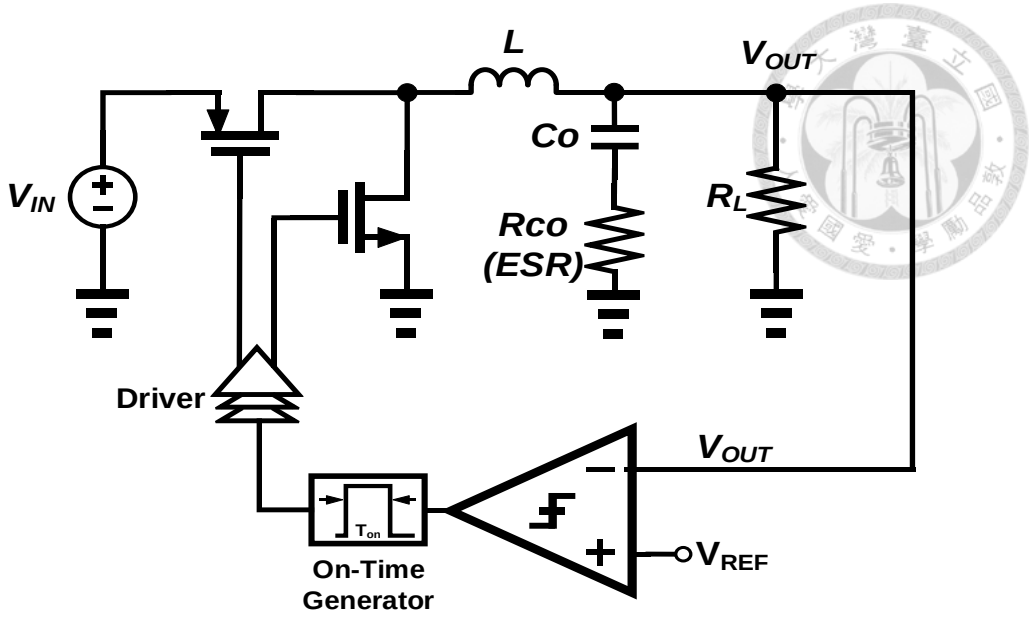

Fig. 2-5 Circuit diagram of the ripple-based constant on-time (RBCOT)

The sub-harmonic oscillation can be explained by Fig. 2-6. The output voltage consists of the ESR ripple voltage and capacitor ripple voltage. There is no phase delay between the inductor-current ripple and ESR ripple, but the delay exists between the former and the capacitor ripple. As shown in Fig. 2-6 (b), if the triangular-shaped ESR ripple dominates the output voltage ripple, the system is stable in steady state.

As shown in Fig. 2-6 (a), the capacitor ripple dominates the output voltage ripple. It is shown that when the duty turns on, the output voltage is still decreasing because of the delayed capacitor ripple. Then, the modulation mechanism forces the duty to turn on again and again until the output voltage is greater than the reference voltage.

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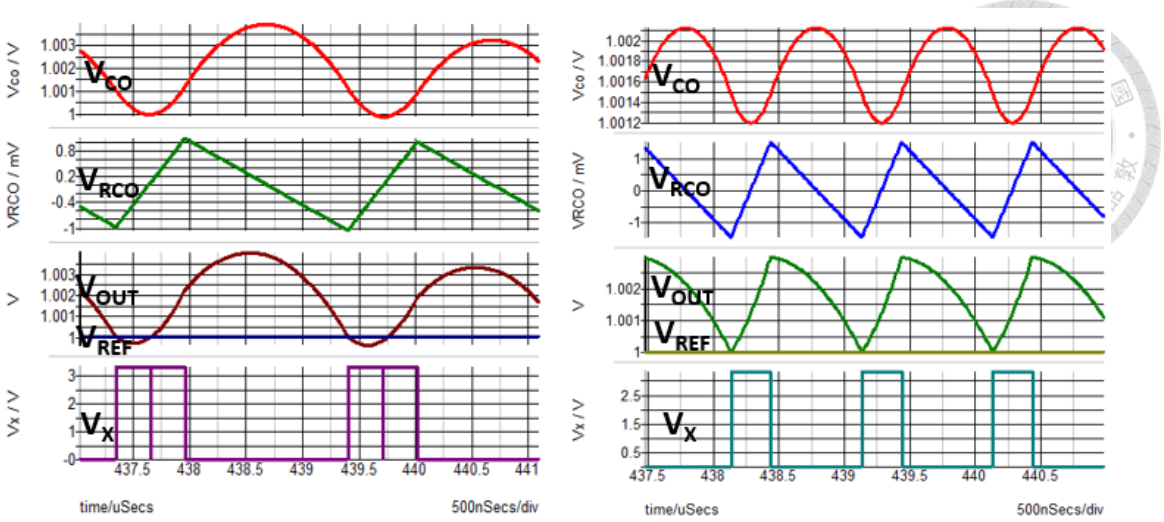

(a) (b)

Fig. 2-6 Modulation waveform of the RBCOT control: (a) the stable operation with the large-ESR capacitor, (b) the sub-harmonic waveform with the low-ESR capacitor

Such operation can also explain by equation (2.1) to (2.3). The transfer function from the reference voltage to the output voltage [6] is derived as follows:

$$\frac{v_{OUT}(s)}{v_{REF}(s)} \approx \frac{1+R_{CO}C_O \cdot s}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2})} \tag{2.1}$$

Where

$$\omega_1 = \frac{\pi}{T_{ON}},\ Q_1 = \frac{2}{\pi},\ \omega_2 = \frac{\pi}{T_{sw}}, \text{ and } Q_2 = \frac{T_{sw}}{(R_{co}C_o - \frac{T_{on}}{2})\pi} \tag{2.2}$$

If T_{ON} is sufficiently small, the transfer function can be simplified to the following equation:

$$\frac{v_{OUT}(s)}{v_{REF}(s)} \approx \frac{R_{CO}C_O \cdot s+1}{1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}} \tag{2.3}$$

In order to prevent from the undesirable right-half plane pole, we can get the

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inequality in (2.4):

$$Q_2 = \frac{T_{sw}}{(R_{co}C_o - \frac{T_{on}}{2})\pi} > 0 \tag{2.4}$$

Thus, the stability criterion is as follows:

$$R_{co}C_o > \frac{T_{on}}{2} \tag{2.5}$$

2.2.2 Review of V^2 Constant On-time Control with Inductor Current Ramp

Fig. 2-7 shows the V^2 constant on-time (V^2COT) control with inductor current ramp [8], [21]. In this architecture, there is an outer compensation loop that adjusts the average output voltage to a reference voltage. It solves the DC offset problem in the RBCOT control. To improve the instability issue, the V^2COT control adds additional inductor current information to the output voltage. The inductor current ramp is added to the output voltage via current sensing gain, R_K.

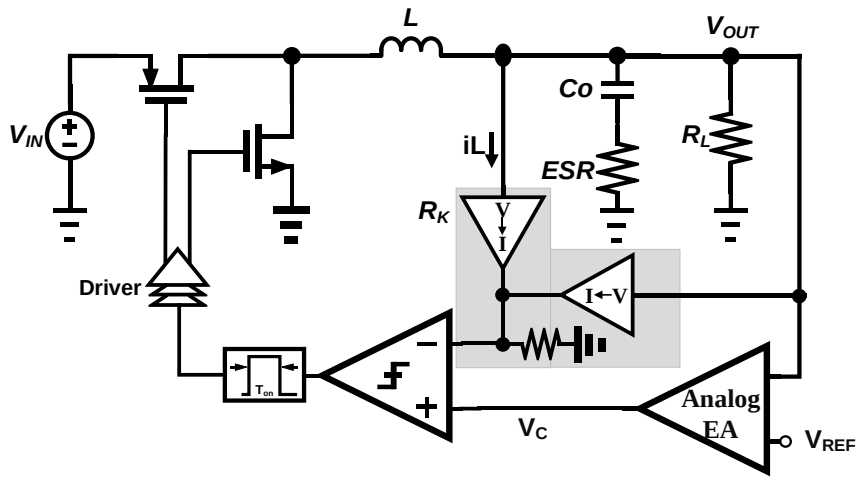

Fig. 2-7 Circuit diagram of the voltage-squared constant on-time (V^2COT) with the inductor ramp compensation

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Combining the inductor current ramp with the output voltage, the transfer function can be given as below:

$$\frac{v_{OUT}(s)}{v_C(s)} \approx \frac{1+R_{CO}C_O \cdot s}{(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^{\,2}})} \tag{2.6}$$

Where

$$Q_2 = \frac{T_{sw}}{\{(R_{co}+R_K)C_o - \frac{T_{on}}{2}\}\pi} \tag{2.7}$$

The rewritten stability criterion is as follows:

$$(R_{co}+R_K)C_o > \frac{T_{on}}{2} \tag{2.8}$$

Based on the above criterion, as the large current sensing gain, R_K, is designed, the system will become more stable. In other words, an additional current loop is introduced to enforce the current feedback information and alleviate the influence of the capacitor voltage ripple. For combining the current ramp with output voltage, the differential amplifiers will be used in this sensing circuit, which means the quiescent current of the controller cannot be suppressed very small. On the other hand, When the sensing gain is increased, the circuit's operating behaves more like current mode constant on-time (CMCOT) control. That will slow down the load transient response [9]. Thus, the following dissertation will discuss the capacitor current constant on-time (C^2COT) with proposed control scheme.

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2.2.3 Review of Capacitor Current Constant On-time Control

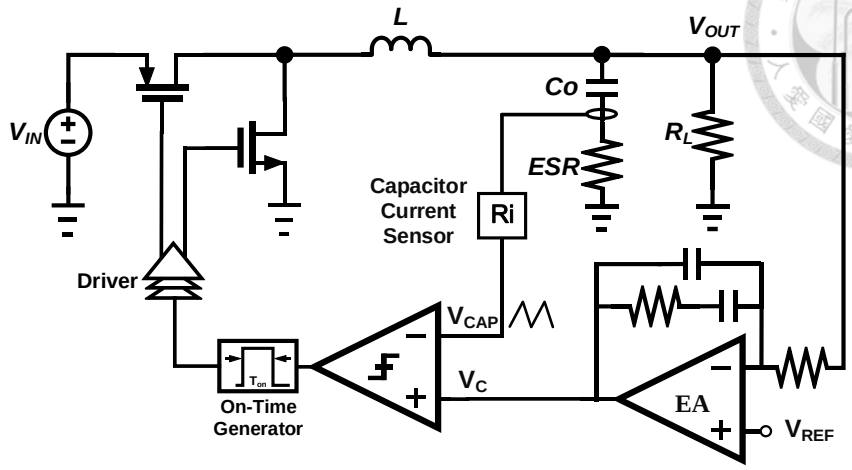

Fig. 2-8 Circuit diagram of the capacitor current constant on-time (C^2COT)

The capacitor current constant on-time (C^2COT) control [27] is shown in Fig. 2-8. The capacitor current is sensed to the modulation directly, instead of the output voltage and inductor current. The VCAP signal provides a fast loop to handle the load transient. Meanwhile, it solves the sub-harmonic oscillation issue. The control-to-output transfer function of C^2COT can be simplified to equation (2.9) where Ri represents the capacitor sensing gain. Then, we can observe that the control-to-output transfer function, $G_{VC}(s)$, exits the three left-half-plane poles (LHP pole) and one ESR-zero. The frequency of the complex pole is $1 / (2T_{on})$ which is much higher than the switching frequency, so it will not affect the stability of the system at all. From (2.10), the quality factor, Q_1, of the complex pole is not related to the capacitor current sensing gain, Ri. Moreover, ω_{P1} is always positive which means C^2COT control will not encounter the sub-harmonic instability problem.

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$$G_{vc}(s)=\frac{v_{out}(s)}{v_c(s)}\cong G_{vc\_DC}\frac{\left(1+\frac{s}{\omega_{ESR}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)} \quad (2.9)$$

Where $G_{vc\_DC}=\frac{2L}{R_i\cdot T_{on}}$, $\omega_{P1}=\frac{T_{on}}{C_O\cdot(R_i\cdot T_{on}+2L)}$, $\omega_{ESR}=\frac{1}{R_{CO}C_O}$, $Q_1=\frac{2}{\pi}$, and

$$\omega_1=\frac{\pi}{T_{on}} \quad (2.10)$$

Based on the above advantages, such as no stability problems and fast transient response, this dissertation implements CCM mode and DCM mode in C^2COT control to deal with a wide load range. However, the conventional capacitor-current sensor needs a high-bandwidth amplifier which is power-hungry. The quiescent current of the conventional compensator consumes at least 2 μA. Besides, the conventional on-time generator containing a comparator and the always-on current bias. These power-consuming blocks of C^2COT will degrade the ultra-light load efficiency.

Hence, the ripple coupling path (RCP), the charge pump-based error amplifier (CPEA), and the digital on/off-time generator are proposed to improve three power-consuming blocks of C^2COT.

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Chapter 3

Proposed Ripple-Coupling Constant On-Time (RCCOT) Controlled Buck Converter

From previous works, the research target can be formulated in Table X-X. In [1], the quiescent current of PFM mode controller is 4μA. If the quiescent current of the controller reduces 1 μA, the efficiency can improve from 40% to about 50% at i_{LOAD}=10 μA. Then, in order to meet the load conditions of the wearable devices. The proposed buck converter needs to handle the dynamic load range from micro-ampere to ampere level and achieve fast transient response. Where the figure-of-merits (FoM) [28] is defined to compare the transient response. Large FoM stands for fast transient response. On the other hand, the proposed buck converter needs to change mode from DCM to CCM automatically.

Table 3-1 Research target of the ripple coupling constant on-time control

Quiescent Current of the Controller	< 4μA [1]
Dynamic Load Range	$\mu A - A$
Load Transient Response	> FOM = $\frac{10\mu H \cdot 100mA \cdot 10^3}{47\mu F \cdot 1M \cdot 5\mu s} = 4.26$ [1]
Mode Transition	Automatic

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Where FOM = $\frac{L \cdot \Delta ILoad \cdot 10^3}{Co \cdot Fsw \cdot Tsettling}$, L=inductor, Co=output capacitor, Fsw=switching frequency, ΔILoad= load transient step, and $T_{settling}$= settling time.

3.1 Circuit Diagram of Constant On-time Buck Converter with the Proposed Control scheme

Fig. 3.X shows the circuit diagram of ripple coupling constant on-time (RCCOT) buck converter with the proposed control scheme. The charge pump-based error amplifier (CPEA) regulates the output voltage, V_{OUT}, to the reference voltage, V_{REF}, by generating compensation voltage, V_C. If the V_{OUT} is lower than $V_{REF,}$ the charge pump will go into the charging mode to increase the V_C voltage and compensate the V_{OUT}. On the contrary, the charge pump operates in the discharging mode to decrease the V_C voltage. The proposed CPEA can improve the quiescent current of controller in DCM. Because the half current bias can shut down by DCM clamp mechanism in idle time. The ripple coupling path (RCP) consisting of all passive devices provides the fast ac loop to improve the load transient response by a high pass filter. On the other hand, if RCP is completely matching with the impedance of the output capacitor, the subharmonic issue will be solved. The digital on/off-time generator consists of several delay lines and logic gates to produce the on-time by time delay. Because of its digital operation, the quiescent current can scale with the load. On the other hand, there are

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coarse-tune and fine-tune to cover the process voltage temperature variations (PVT). In order to realize the discontinuous conduction mode (DCM), the zero-current detector (ZCD) is used to control the NMOS on or off. When the RCCOT is operating in DCM, the V_C will be clamped to the threshold voltage, V_{DCM}. The power stage specifications for the implemented IC are V_{IN}= 3.3 V, V_{OUT}= 1 V, L= 6.8 μH, C_O= 10 μF, ESR=8 mΩ, and switching frequency f_{sw}=300 KHz.

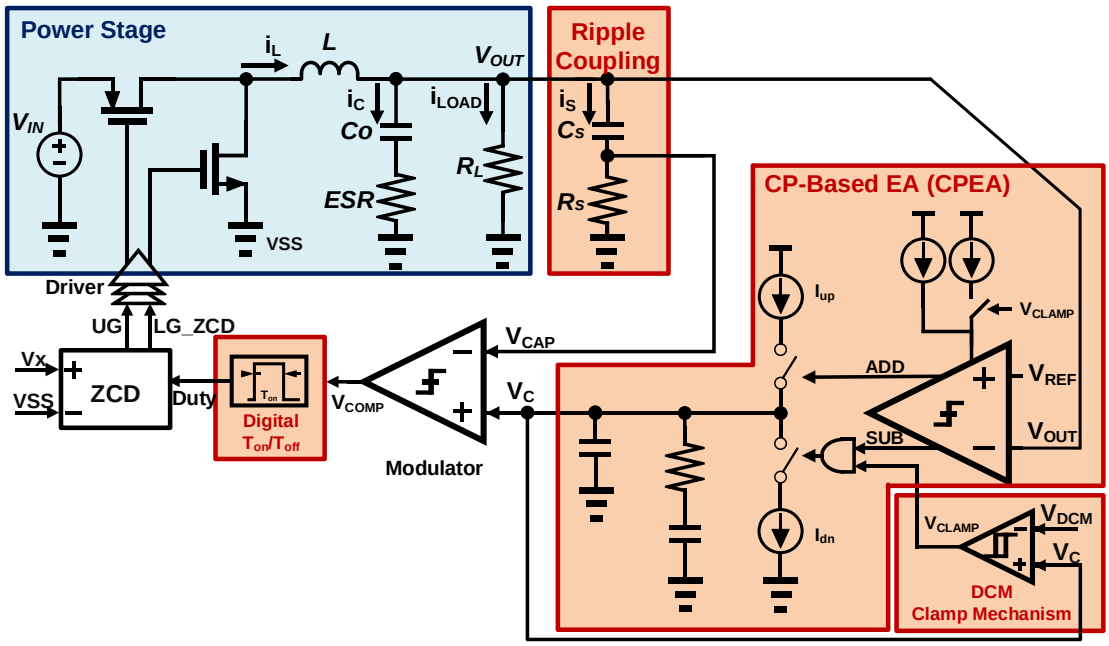

Fig. 3-1 Circuit diagram of the proposed RCCOT buck converter

3.2 Ripple Coupling Path

The RCCOT inserts the output capacitor current into the modulation by ripple coupling Path [8], [10] to achieve the fast-transient response. In a buck converter, the relation of the output capacitor current, I_C, load current, I_{LOAD}, and inductor current, I_L,

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can be express as (3.1).

$$I_C = I_L - I_{LOAD} \tag{3.1}$$

The equation demonstrates that the capacitor current is relative with the minus load current directly. The load transient waveforms of I_C, I_L, and I_{LOAD} are shown in Fig. 3-2. When the load step occurs, the output capacitor current I_C will respond immediately based on (3.1). This inner current loop phenomenon can achieve the fast-transient response.

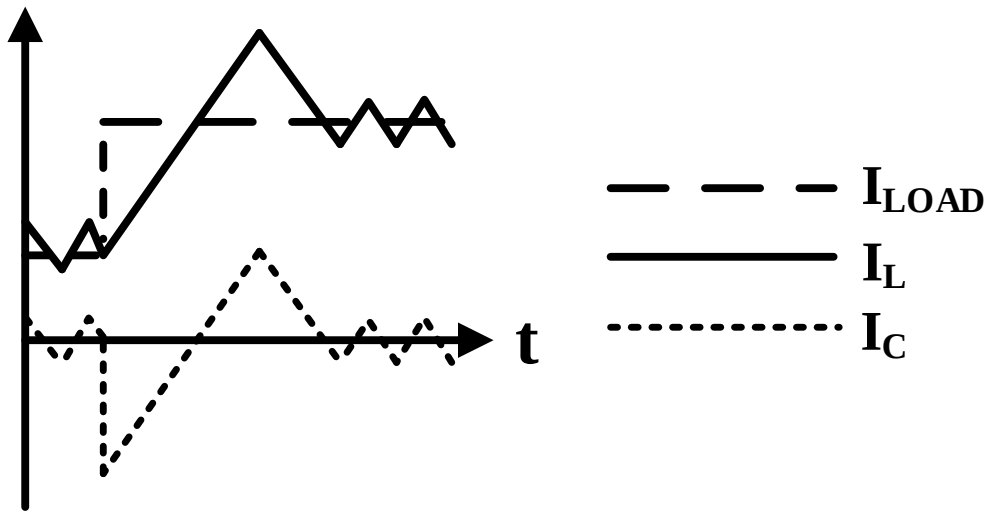

Fig. 3-2 Relation waveforms of I_{LOAD}, I_L, and I_C

In Fig. 3-2, the inductor current waveform and the output capacitor current waveform are nearly the same, except for the dc level between I_C and I_L. In the CMCOT control, inserting the inductor current ramp into the modulation can be stable against the subharmonic issue [9]. Therefore, inserting the capacitor current ramp which is the

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same phase as the inductor current ramp into modulation can improve the subharmonic issue, also [10].

As a simple way, the output capacitor current can be sensed by a current sensing resistor in series with a capacitor. Nevertheless, the resistor sensing introduces the power loss. Thus, the value of the resistance needs to larger than the resistance of ESR to reduce the power loss. As shown in Fig. 3-3, the ripple coupling path consist of a capacitor (C_S) and two resistors. The resistor divider in the ripple coupling path circuit is used to increase the dc level of VCAP voltage for solving the input common-mode range issue of the next stage.

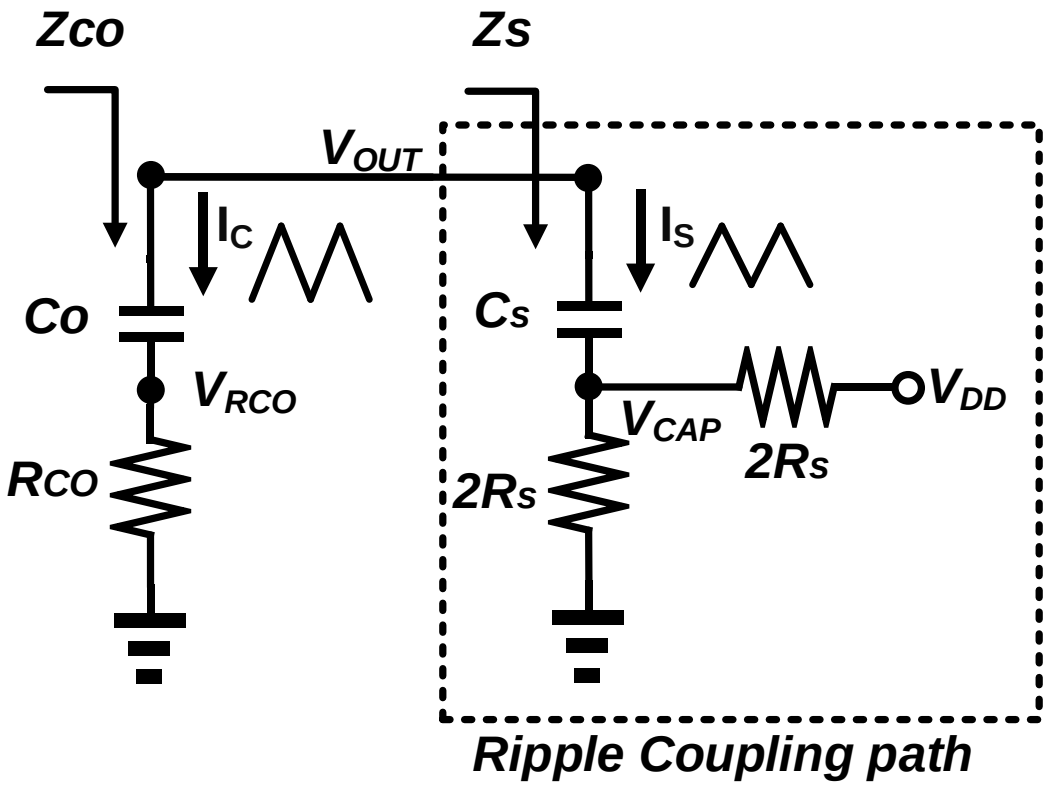

Fig. 3-3 Circuit diagram of the ripple coupling path (RCP)

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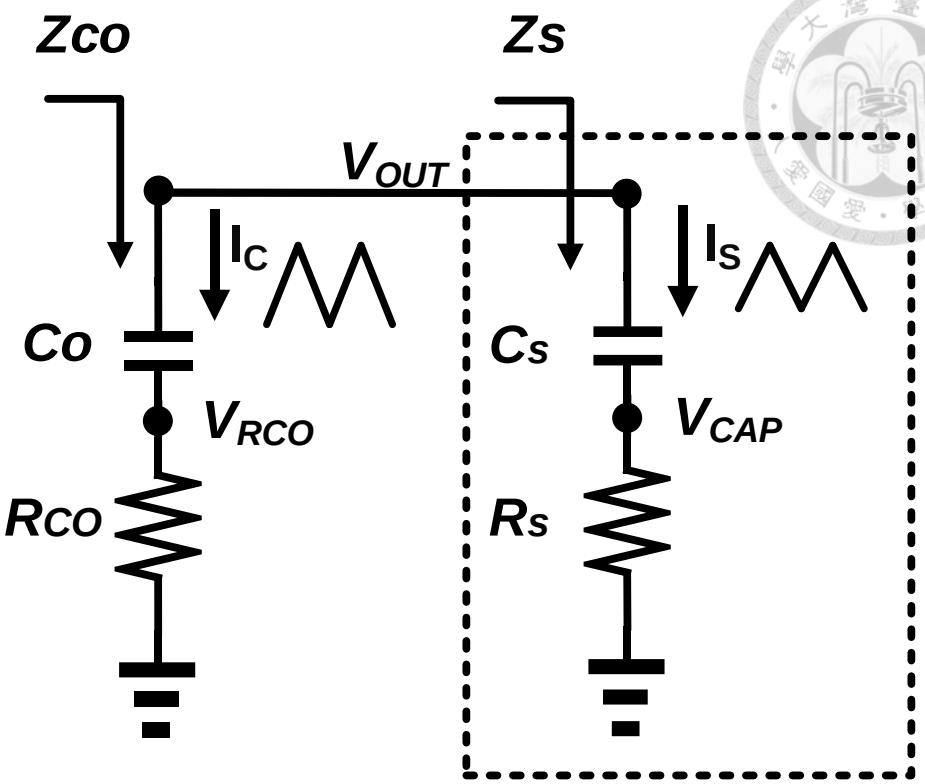

Fig. 3-4 Small signal equivalent circuit of the ripple coupling path

The small signal equivalent circuit of the RCP presents in Fig. 3-4. The capacitor C_S and the resistor R_S is given by (3.2), and the impedance of sensing branch Z_S is K times larger than the impedance of the output capacitor Z_{CO}, as shown in (3.3). From (3.2) – (3.4), it is obvious to get (3.5).

$$C_S = C_{Co} / K \ , \ R_S = K \cdot R_{Co} \tag{3.2}$$

$$Z_S = (R_S + 1/(SC_S)) = K \cdot (R_{CO} + 1/(SC_{CO})) = K \cdot Z_{CO} \tag{3.3}$$

$$I_S = I_C / K \tag{3.4}$$

$$V_{CAP} = I_S \cdot R_S = I_C \cdot R_C = V_{RCO} \tag{3.5}$$

Based on the above concept of the capacitor current sensor, the V_{CAP} voltage sensed by the ripple coupling path is the same as the V_{RCO} waveform. However, the

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sensed signal, V_{CAP} is distorted if a mismatch exists between the output capacitor and the ripple coupling path. The mismatch issue and implementation of RCP will be discussed in chapter 4.2.

3.2.1 Transient Response of RCCOT Controlled Buck Converter

Fig. 3-5 shows the schematic of RCCOT controlled buck converter in *SIMPLIS* simulation tool, including the power stage, compensator. On-time generator, minimum off-time generator, and ripple coupling path. Table 3-1 lists the specifications of power stage. In the Fig. 3-5, the on-time generator and minimum off-time generator is the traditional type. The proposed on-time generator will be discussed in Section3.3 and 4.1.

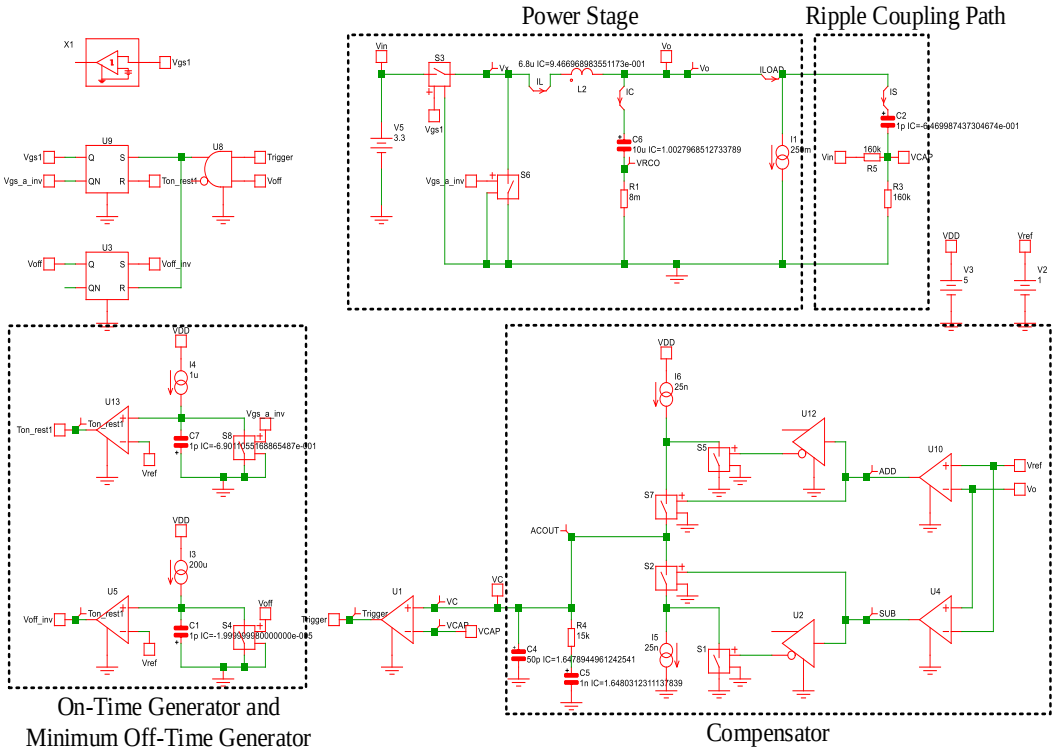

Fig. 3-5 Schematic of RCCOT controlled buck converter in *SIMPLIS*

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Table 3-2 Specifications of the power stage

V_{IN}	V_{OUT}	L	C_O	R_{CO}	Ton	F_{SW}
3.3V	1V	6.8μH	10μF	8mΩ	1μs	300kHz

Fig. 3-6, 3-7, and 3-8 show the steady-state waveform, step-up load transient waveform, and step-down load transient waveform, respectively. Because of the characteristic of IC in (3.1), the duty cycle saturates immediately to compensate the VOUT at the step-down load.

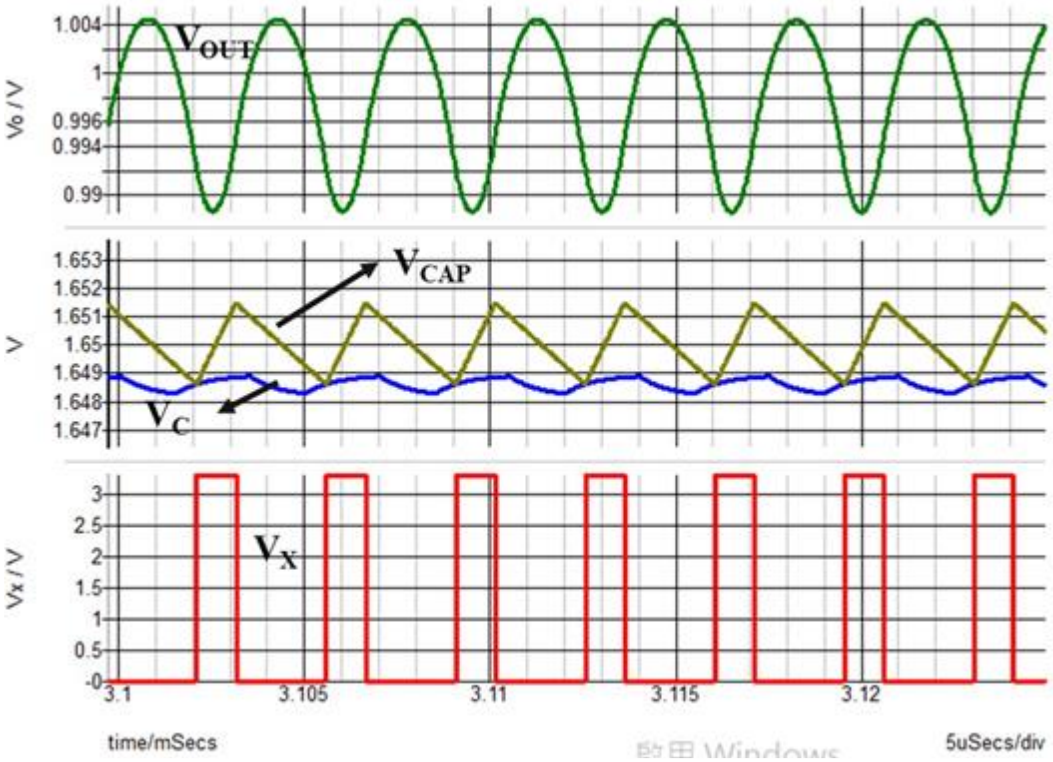

Fig. 3-6 Steady-state waveforms of RCCOT control

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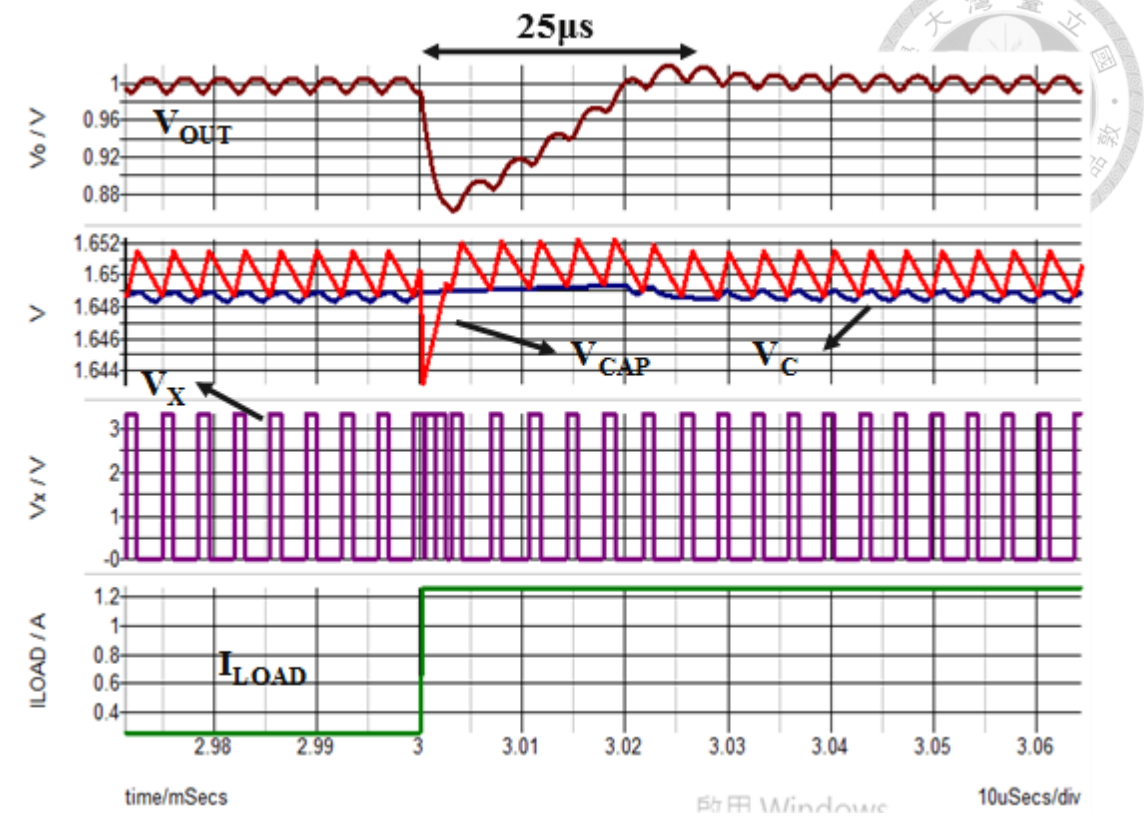

Fig. 3-7 Step-up load transient waveforms of RCCOT control (I_{LOAD}=0.25A-1.25A)

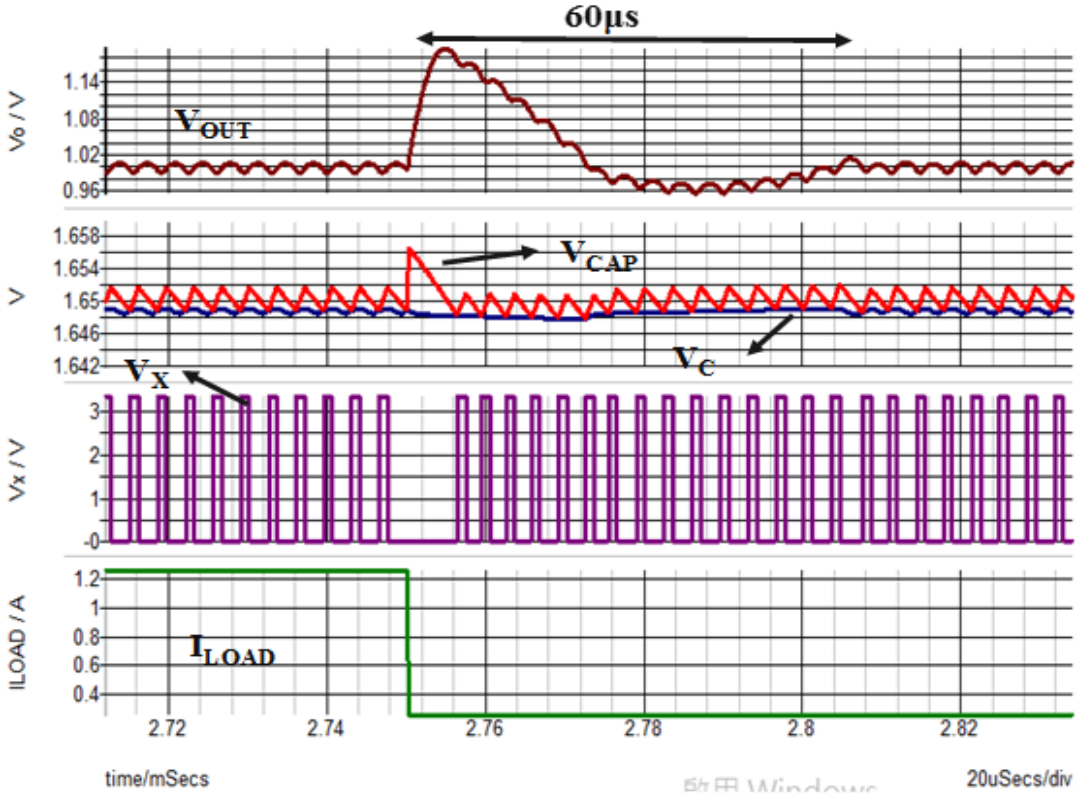

Fig. 3-8 Step-down load transient waveforms of RCCOT control (I_{LOAD}=1.25A-0.25A)

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3.3 Digital On/off-Time Generator

Figure 3-9 shows the conventional on-time generator consists of the constant current bias, a capacitor, a switch MOS, a SR-latch and a comparator. The on-time period, Ton, is designed by the following equation:

$$Q = C_{on} \cdot V_{on} = I_B \cdot T_{on} \tag{3.6}$$

$$T_{on} = \frac{C_{on} \cdot V_{on}}{I_B} \tag{3.7}$$

With the fixed Ton, Von voltage cannot set too low because the low voltage will be influenced by noise voltage. Furthermore, if the capacitance of C_{on} is too small, the C_{on} will suffer from the charge injection due to the parasitic capacitor of the switch (S1). For the power consumption, not only the I_B consuming micro-ampere level is a certain amount of power dissipation, but the continuous-time comparator consumes a large amount of power at ultra-light load.

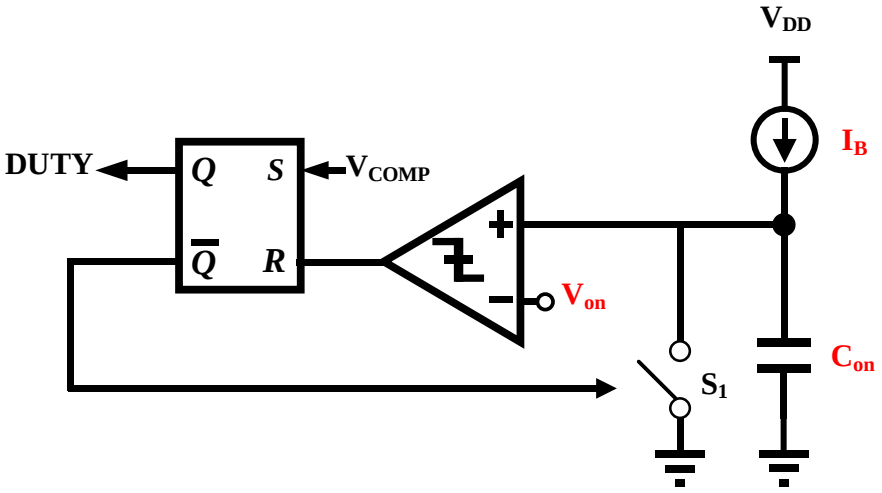

Fig. 3-9 Circuit diagram of the conventional on-time generator

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In order to decrease the power consumption at light load conditions, a proposed on/off-time generator consisting of delay cells and logic gates were implemented by digital circuitry. Obviously, the dynamic power of the proposed on/off-time generator is shown as

$$P_{dynamic} = \alpha \cdot F_{SW} \cdot C_L \cdot V_{DD}^2 \tag{3.8}$$

where α is the fraction of the bottom-plate parasitic capacitance to the actual capacitance of the capacitor. In the equation (3.8), the dynamic power can scale with the switching frequency, F_{SW}. Therefore, when the RCCOT operates in DCM, the switching frequency is scaled with the load. That is, the dynamic power can reduce with the load due to the decreased switching frequency.

Fig. 3-10 demonstrates the block diagram of the proposed on-time generator (the digital on/off-time generator) which contains the on-time generator, the off-time generator, a power-on-reset block, a D flip-flop, and the logic gates. In the on/off-time generator, the circuit input, $V_{COMP,}$ is triggered by modulator as shown in Fig. 3-1, and the circuit output is V_{Driver} which produces the duty signal to the zero-current detector (ZCD) for regulating the output voltage.

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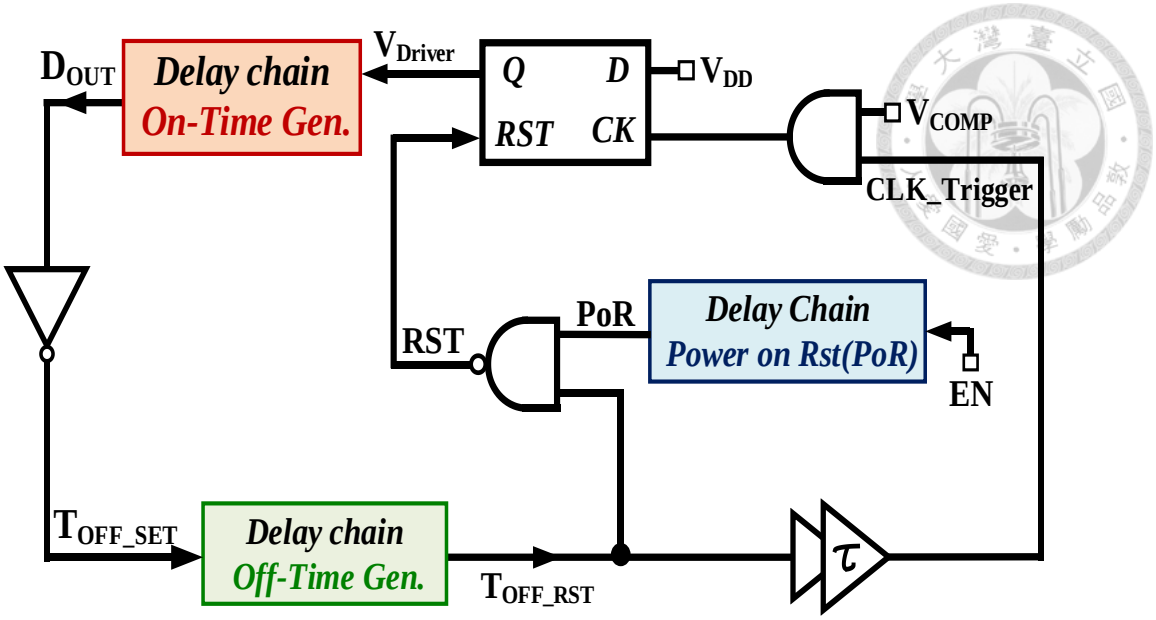

Fig. 3-10 Block diagram of the digital on/off-time generator

Fig. 3-11 shows the conceptual steady-state waveform. In the steady-state, V_{CAP} is lower than V_C to produce the V_{COMP} pulse by the modulator. At the t_1, the V_{COMP} pulse triggers the D flip-flop to change V_{Driver} from logic low to logic high and keep at the supply voltage, VDD. Then, the rising edge of V_{Driver} waveform goes into the on-time generator to introduce the on-time pulse, T_{ON}, by delay chain block. And then, in order to prevent the D flip-flop from malfunctioning. Therefore, the minimum off-time pulse, T_{OFF}, produced by off-time generator is used to reset the output signal of the D flip-flop at the t_2. The power-on-reset block is necessary for avoiding the D flip-flop from malfunctioning during startup mode. The operational principle of the power-on reset block works the same as the off-time generator. The on-time generator, off-time generator, and power-on reset block consist of delay chains which will be introduced in chapter 4.1.

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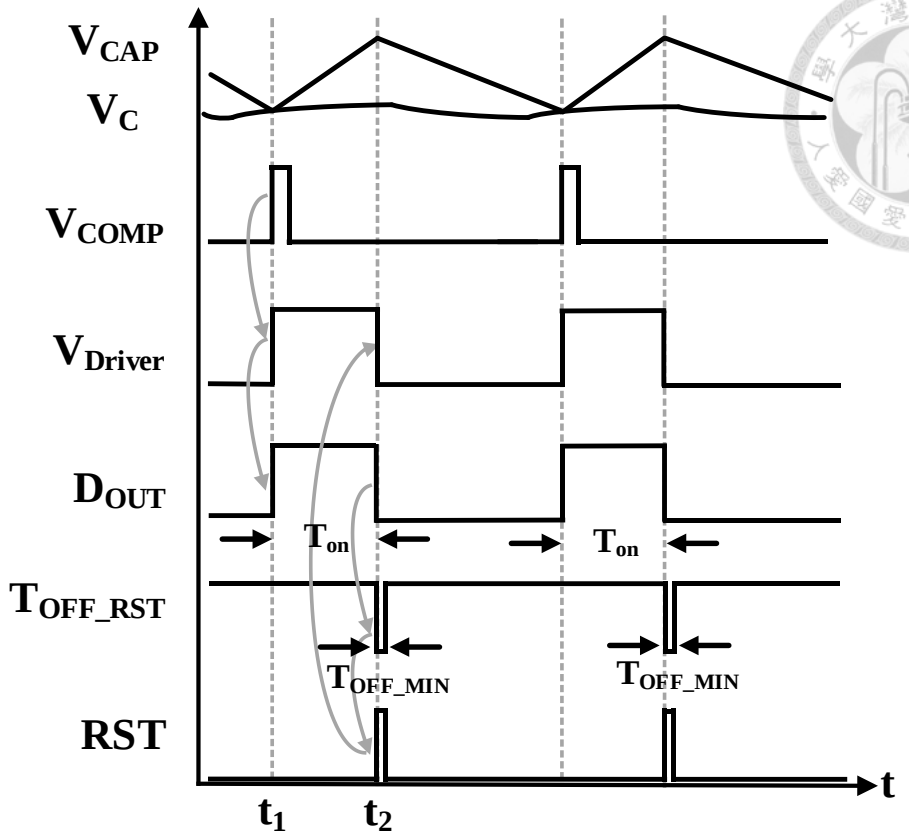

Fig. 3-11 Conceptual steady-state waveforms of RCCOT with digital on/off-time generator

In Fig. 3-12, the boosted load current causes V_{CAP} to stay below V_C for several cycles when the load current step-up condition occurs. In this way, from t3 to t4, the V_{COMP} signal is always logic high to make the V_{Driver} signal saturate for compensating. However, V_{Driver} does not always maintain a logic high voltage. Because there is a minimum off-time pulse, T_{OFF_MIN}, to reset the V_{Driver} signal. In order to achieve the saturated duty at step-up load condition, the CLK_Trigger is used to trigger D Flip-Flop to go high again. On the other hand, the step-down load current makes V_{CAP} greater than V_C. The V_{COMP} signal is a logic low level from t_5 to t_6, so until V_{CAP} is less than V_C. V_{Driver}, DOUT, and T_{OFF_RST} waveforms are always a logic low level as well.

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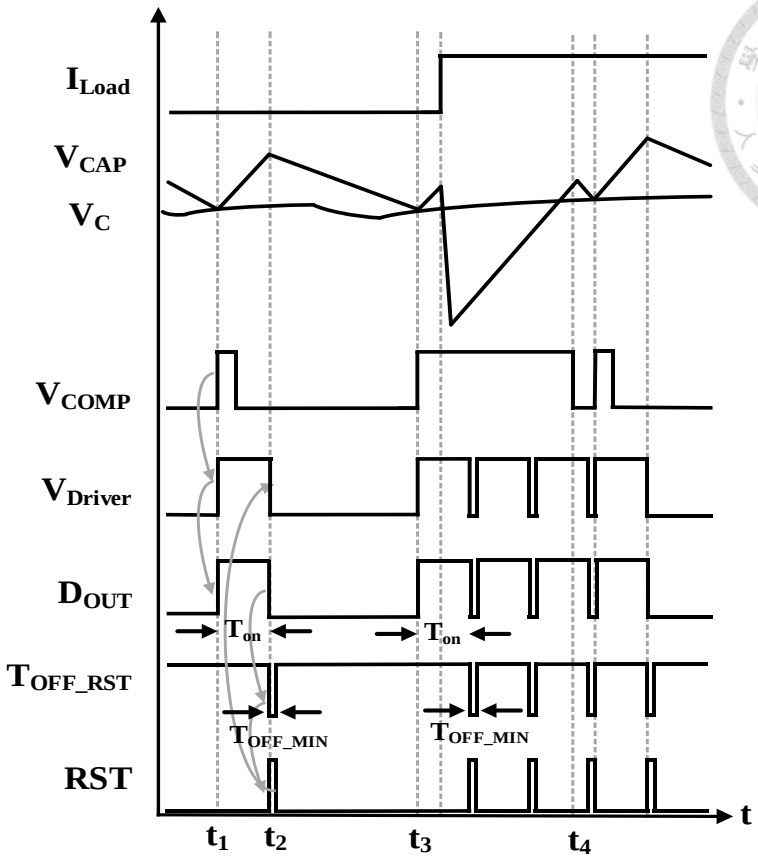

Fig. 3-12 Conceptual load transient waveforms of RCCOT with the digital on/off-time generator

3.4 Charge Pump-Based Error Amplifier

3.4.1 Charge Pump-Based Error Amplifier with A Discrete-Time Comparator

In traditional C^2COT control, a type-II compensation circuit is necessary in a closed-loop buck converter. Generally, the type-II compensation circuit shown in Fig. 3-13 consists of a continuous-time error amplifier, two resistors, and two capacitors. The higher the switching frequency of the system, the current consumption of the error amplifier will increase due to the requirement for high gain-bandwidth (GBW). When the load condition changes from the heavy load to the ultra-light load, the power

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consumption of the continuous-time error amplifier greatly degrades the efficiency at ultra-light loads. Under the simulation verification, when the two-stage amplifier with 80dB DC gain and 5MHz GBW is operated at ultra-light load (i_{LOAD} = 10μA), the quiescent current is 2.5μA. In order to reduce the current consumption of the error amplifier, we proposed two versions of the charge pump-based error amplifier, as will be shown in Fig. 3-14 and Fig. 3-17.

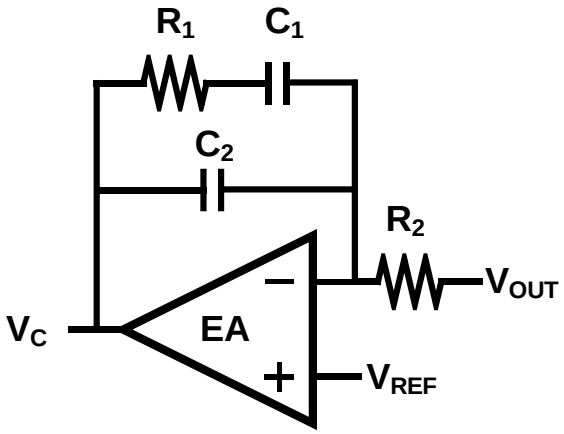

Fig. 3-13 Conventional type-II compensation

The first version of the proposed charge pump-based error amplifier (CPEA) is shown in Fig. 3-14. It is comprised of a discrete-time comparator, a SR-latch, a charge pump, and the loop filter. The control voltage, V_C, is introduced by CPEA for modulation and compensates for the dc error between V_{REF} and V_{OUT}. The discrete-time comparator [12] compares V_{OUT} with V_{REF} to produce the differential signals (logic high and logic low). Fig. 3-15 shows the conceptual steady-state waveform of the proposed CPEA. When V_{OUT} is lower than V_{REF} during the clock on, the output of the discrete-time comparator, ADD′, goes high and the other one, SUB′, goes low. Then, ADD' and SUB' pass through the SR latch to generate 1-bit differential error pulse deciding the charge pump operates

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in charging state. The charge pump current, I_{up}, charge the loop filter to makes V_C increase. On the contrary, the control voltage V_C is discharged by a current source, I_{dn}, when the charge pump operates in the discharging state.

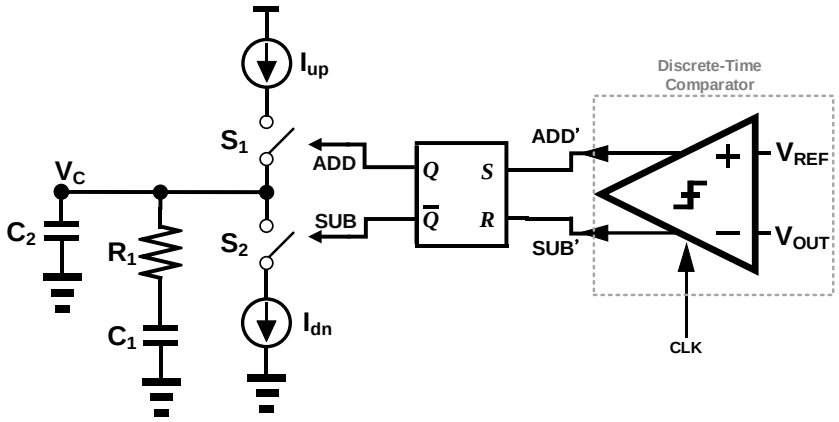

Fig. 3-14 The first version of the proposed charge pump-based error amplifier

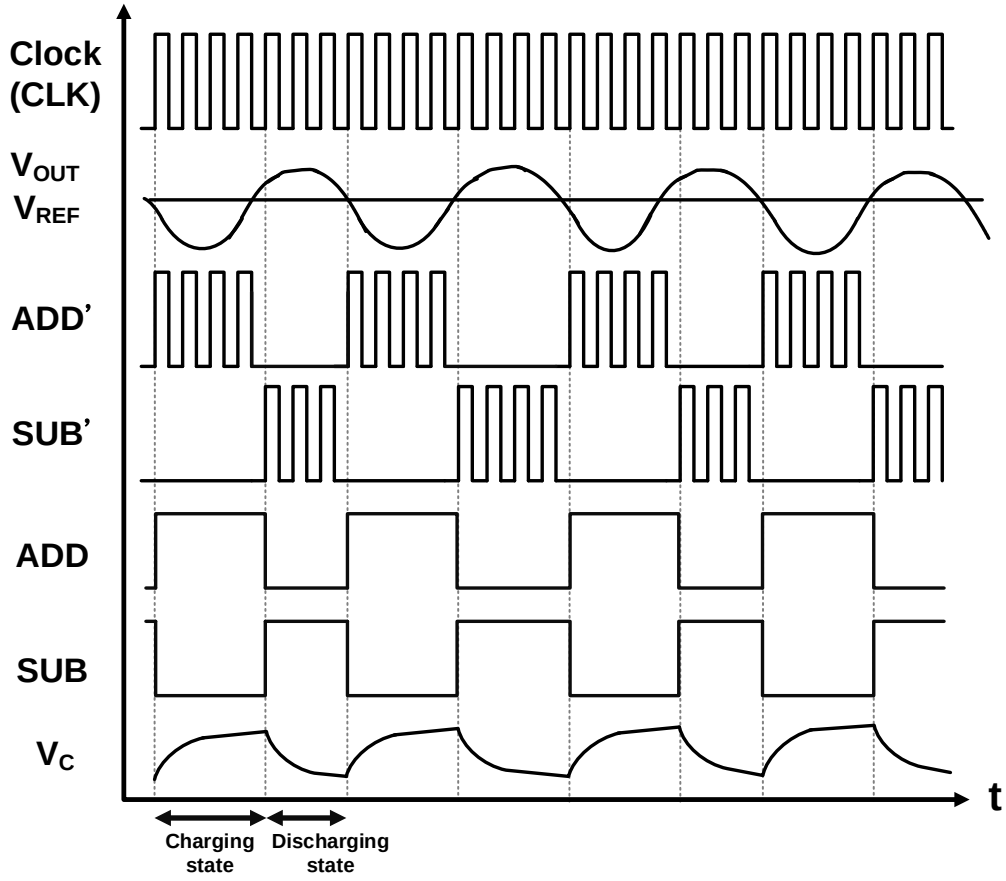

Fig. 3-15 Conceptual steady-state waveform of the proposed CPEA

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The loop filter design is similar to the type II compensation, there are two poles, and one zero. The frequency of pole1 is very low. Although there is no mathematical model of pole1, it does not affect the stability design of the system . The frequency position of pole2 and zero1 can be expressed as

$$Zero1_{frequency} = \frac{1}{2\pi R_1 \cdot C_1}, \text{ and}$$

$$pole2_{frequency} = \frac{1}{2\pi R_1 \cdot (\frac{C_1 \cdot C_2}{C_1 + C_2})} \tag{3.9}$$

The bode plot of the control-to-output is shown in Fig. 3-16, the control-to-output of RCCOT control is a single-pole system and the pole frequency is 5kHz. Thus, the zero of the loop filter, Zero1, is used to boost the dominant pole's phase drop. Then, the pole2 frequency is designed at the high frequency to suppress the noise.

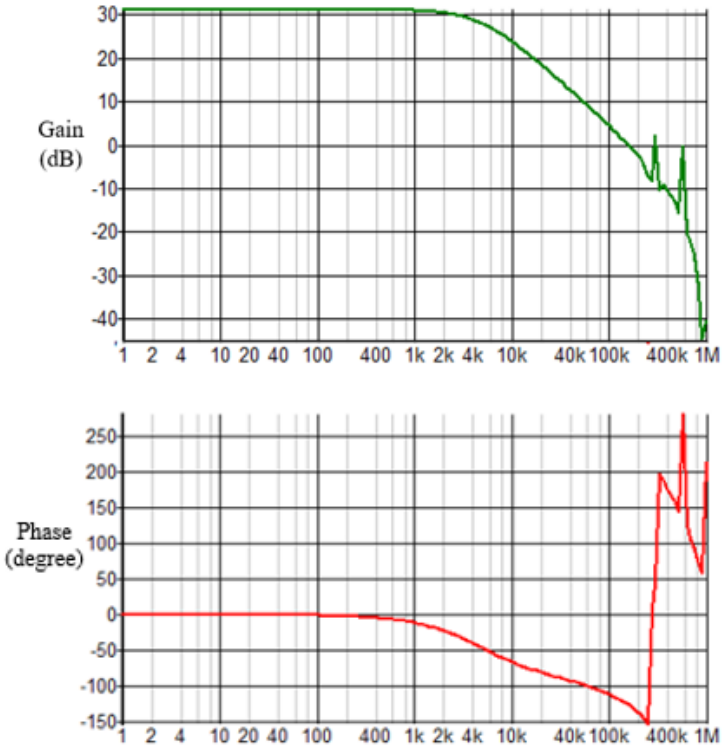

Fig. 3-16 Control-to output bode plot of RCCOT control in *SIMPLIS*

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According to the control-to-output of RCCOT and the time-domain simulation waveform in *SIMPLIS*, the frequencies of Zero1 and Pole1 are designed at 20kHz and 145kHz, respectively. The values of R1, C1 and C2 are 80kΩ, 100pF, and 16pF. The value of the current bias (Iup and Idn) is 75nA.

3.4.2 Charge Pump-Based Error Amplifier with A Dynamic Bias Comparator

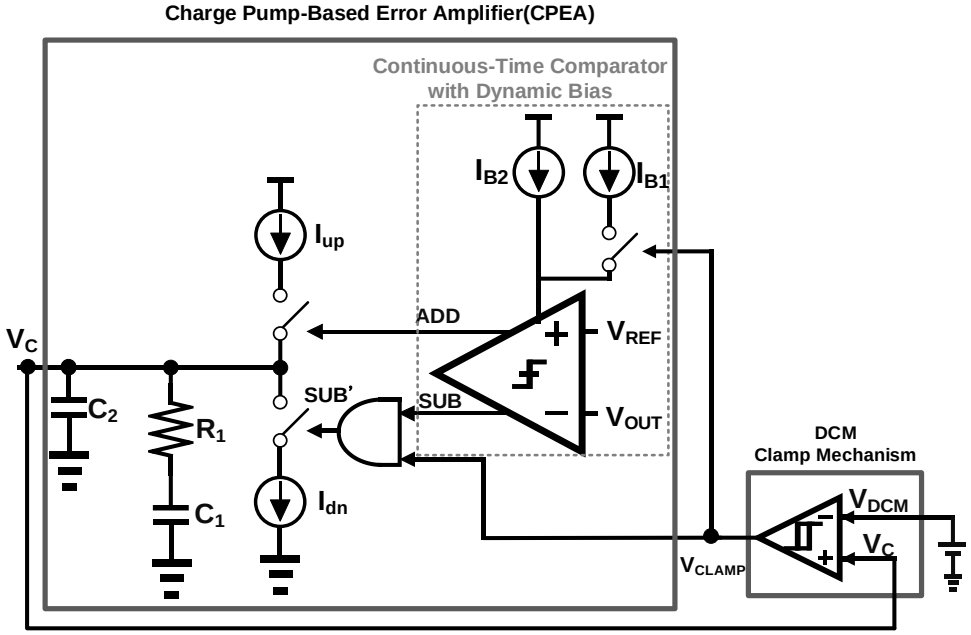

Fig. 3-17 The second version of CPEA and the DCM clamp mechanism

Fig. 3-17 shows the second version of CPEA and the DCM clamp mechanism. The discrete-time comparator is replaced by a dynamic bias comparator and the clock generator is removed for saving power in the second version of CPEA. The design of the loop filter and the charge pump is the same as the first version. Although the first version of CPEA saves 1.5uA compared to conventional type II compensation under

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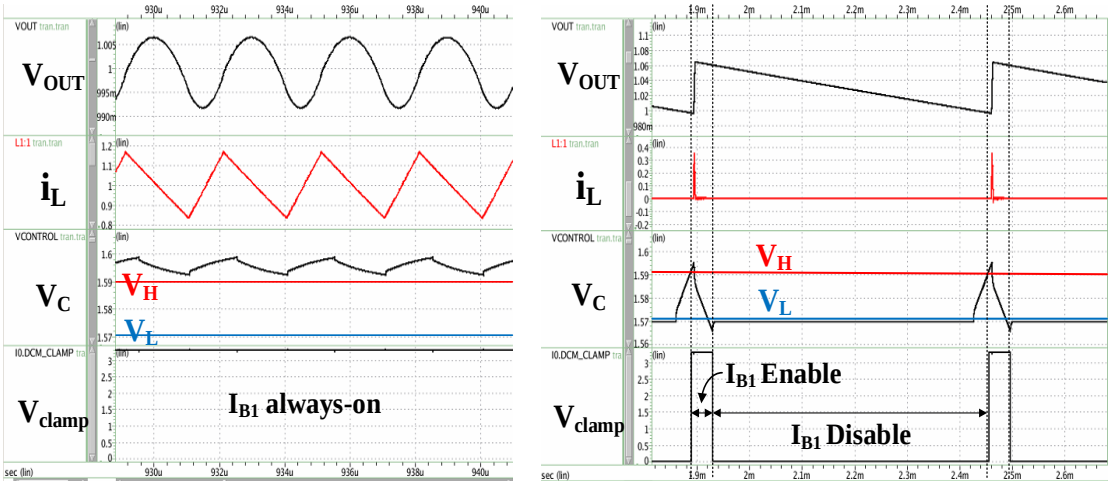
the ultra-light load. However, the disadvantage is that CPEA needs a power-hungry clock generator. If we implement a 2MHz clock generator in the buck converter, the clock generator will consume 35μA.

The operating waveform of the CPEA with the DCM clamp mechanism is illustrated in Fig. 3-18. In the DCM clamp mechanism, the hysteresis of Schmitt trigger generates the high voltage bar, V_H, and low voltage bar, V_L, according to the input voltage, V_{DCM}. V_{clamp} remains at a logic high in the CCM because V_C is always larger than V_L. In the DCM, when V_C drops below V_L, V_{clamp} goes low to turn off the current sources (Idn and I_{B1}). This force the comparator consumes only half current from t1 to t2. In other words, the half power loss of the comparator can be saved in the idle time. The DCM clamp mechanism will be discussed in Section 3.6, and the current consumption of three compensators will be compared in Section 4.5.2.



(a) (b)

Fig. 3-18 Conceptual steady-state waveforms of RCCOT with CPEA and DCM clamp mechanism: (a) the operation waveforms in the CCM, (b) the operation waveforms in the DCM

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3.5 Delay-Based Zero-Current Detector for DCM Operation

The zero-current detector is necessary to implement for turning off the low-side MOS, when the inductor current becomes negative. This approach makes the converter can operate in DCM, and the benefit is the switching frequency can scale with the load. Because when the inductor current is completely discharged, both the high-side MOS and low-side MOS are turned off. This forces the output capacitor to pass power to the load. Therefore, the lighter the load, the longer the idle time, Tidle, which is shown in Figure 3-19. This means that the switching frequency will decrease with the load. Then, the power consumption of the system can be reduced at light loads.

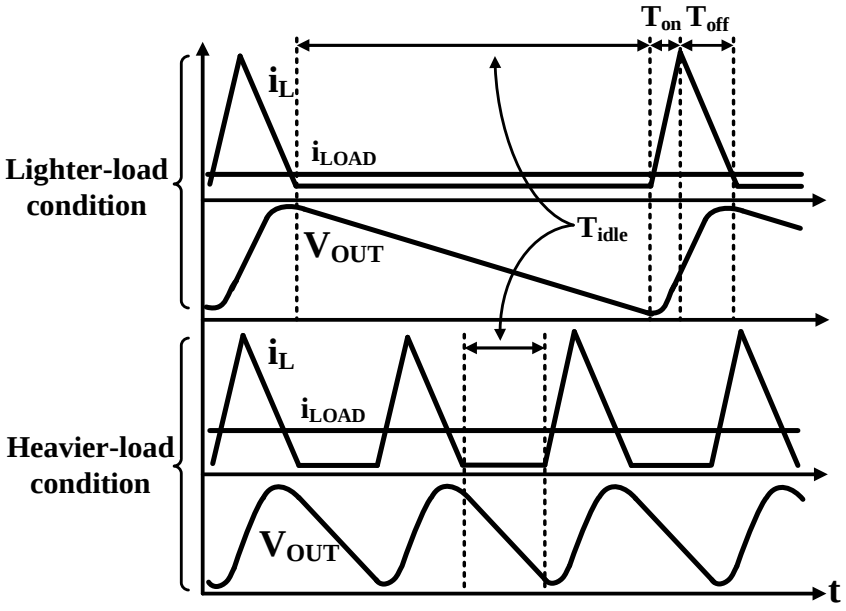

Fig. 3-19 Timing diagram of i_L and V_{OUT} in the DCM at the different loads

As shown in Fig. 3-20, the delay-based pulse width controlled ZCD [13], which is

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in digital operation, reduces a large amount of power consumption in the conventional ZCD architectures containing a continuous-time comparator. τ_D is one delay unit.

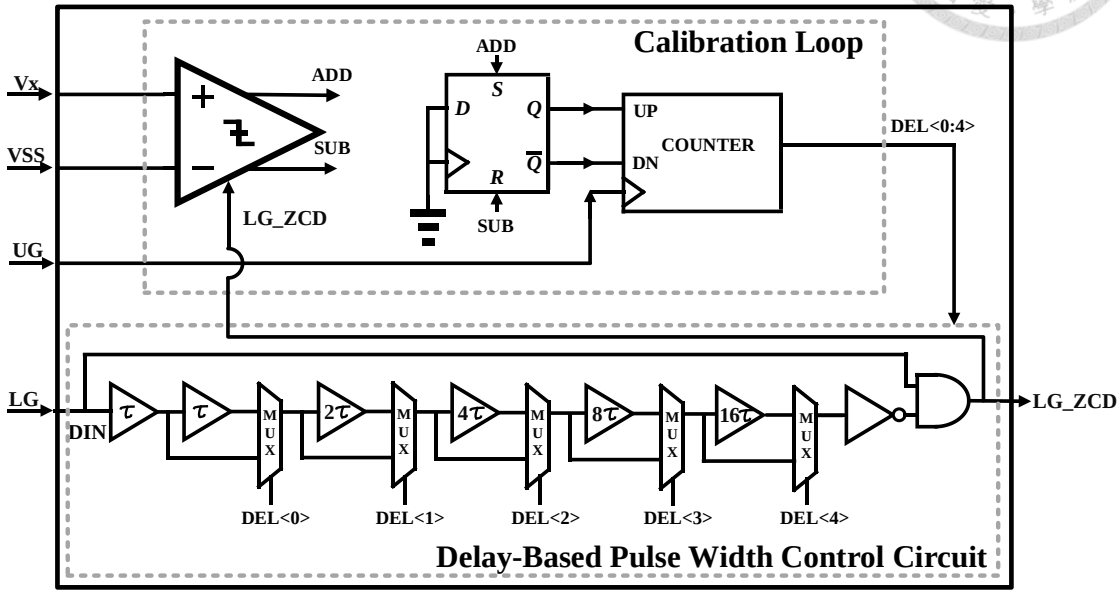

Fig. 3-20 Circuit diagram of the zero-current detector with the delay-based pulse width control

The delay-based pulse width control Circuit which consists of 32 delay units and the width of the pulse is controlled by 5-bit signal DELAY< 0 : 4 > to adjust the optimal pulse width for the NMOS.

The calibration loop operates as follows: the input voltage of the comparator, VX will compare with the ground (VSS). However, the comparison occurs instantly when the NMOS (power MOS) is turned off. As shown in Fig. 3-21(a), if the NMOS is turned off too early, the freewheeling inductor current turns on the parasitic body diode to force the VX below the ground. Therefore, the VX signal is lower than ground (VSS) at the

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falling edge of LG_ZCD signal to make the ADD signal goes high and the SUB signal goes low. In the contrary, if the NMOS is turned off too late, the reverse inductor current charge the parasitic capacitor of NMOS to force the VX higher than ground. Then, the ADD/SUB signal goes low/high, which shows in Fig. 3-21(b). Based on the above, the SUB/ADD signal goes into the up/down counter to determine the value of the DELAY< 0 : 4 > at the rising edge of UG signal. After a few cycles, the optimal pulse width will be decided by the calibration loop.

Fig 3-22(a) shows that the 5-bit signals, DELAY <0 : 4>, keep increasing or decreasing by 1 bit in the steady-state of DCM. However, in the steady-state of CCM, all 5-bit signals, DELAY <0 : 4>, are always logic high because VX is lower than VSS during Toff as shown in Fig. 3-22(b).

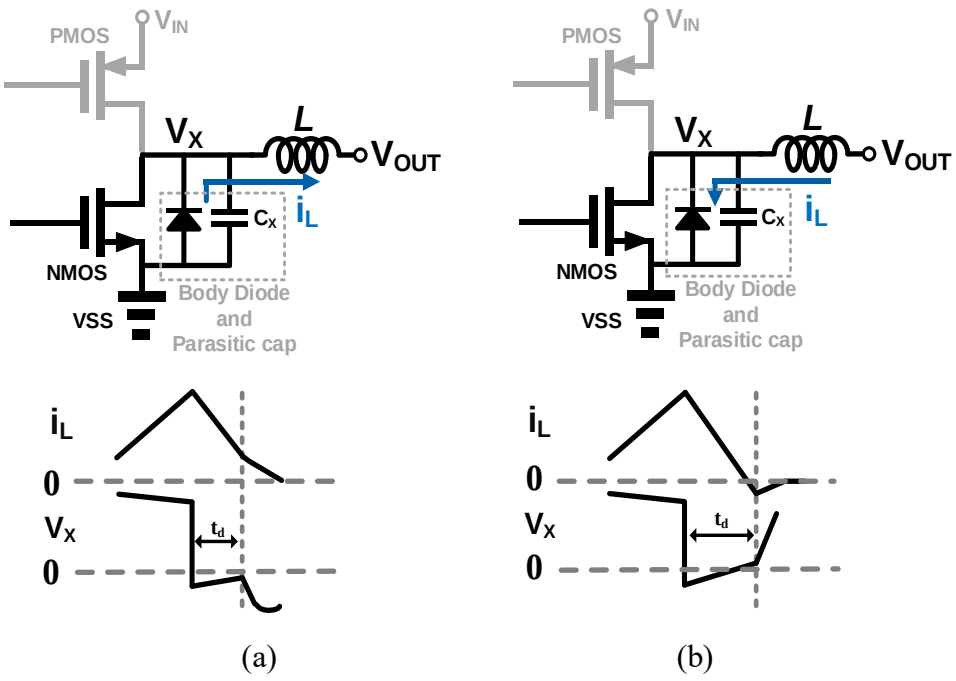

Fig. 3-21 Operation waveforms of i_L and V_X in the ZCD:

(a) turn off the low-side MOS too early, (b) turn off the low-side MOS too late[29]

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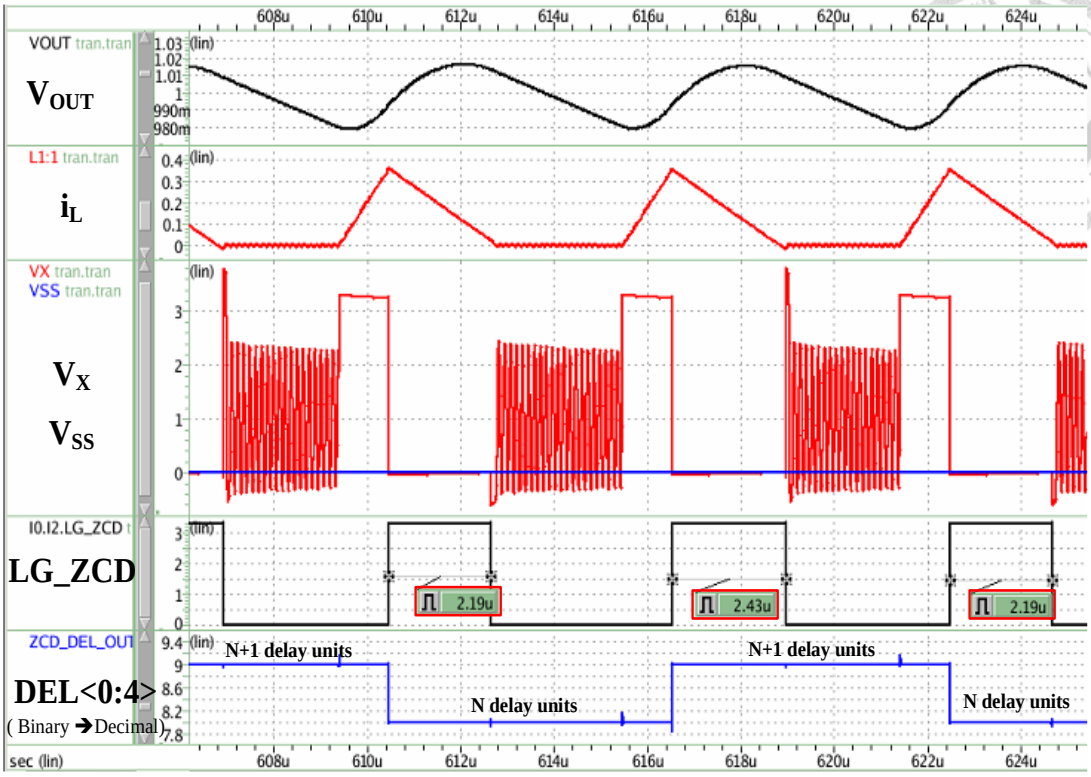
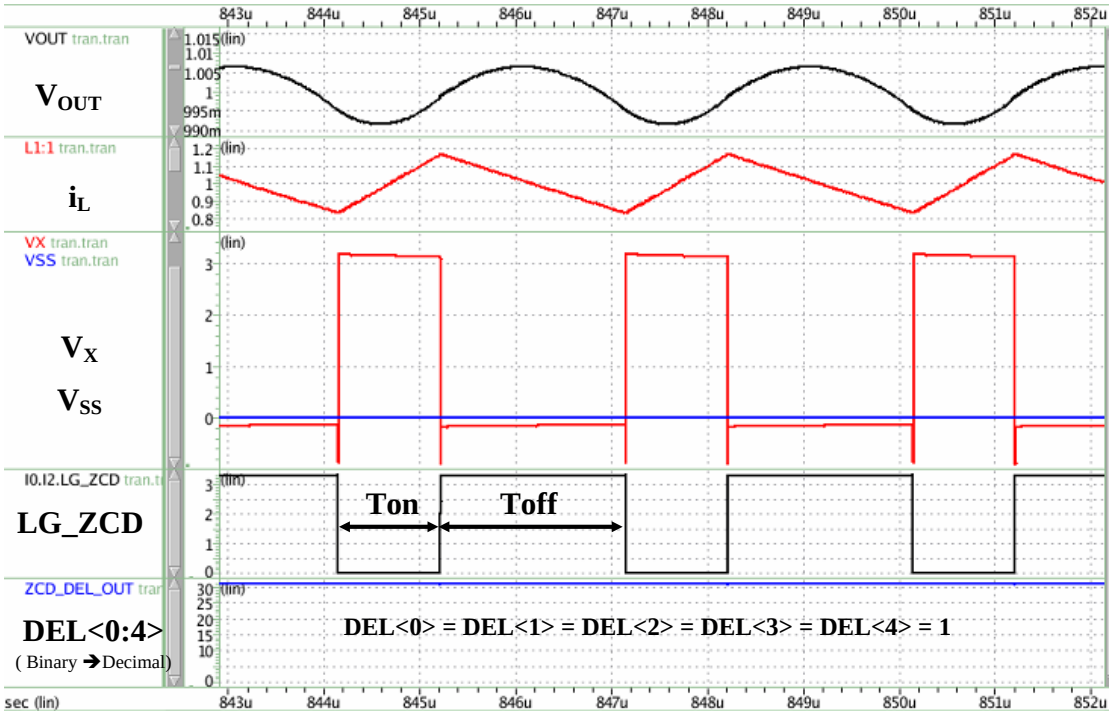


(a)



(b)

Fig. 3-22 Conceptual steady-state waveforms of ZCD: (a) the operation waveforms in the DCM, (b) the operation waveforms in the CCM

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3.6 DCM Clamp Mechanism for Very-Light to Heavy Load Transient

When the load current changes from extremely light load to heavy load, if there is no mechanism to clamp the V_C voltage, the phenomenon that the output voltage drops to ground instantly will appear as shown in Fig. 3-23. The reason is that when the circuit is operating at a light load steady-state, the V_{OUT} voltage will gradually decrease to VREF due to the output capacitor discharging. Before V_{OUT} is lower than the V_{REF}, the V_C voltage will drop, or even to ground. At the same time, if a large step-up load transient occurs, the current of Co will be completely discharged to the output load. Moreover, the response of the compensator is not fast enough. As a result, the output voltage will drop dramatically.

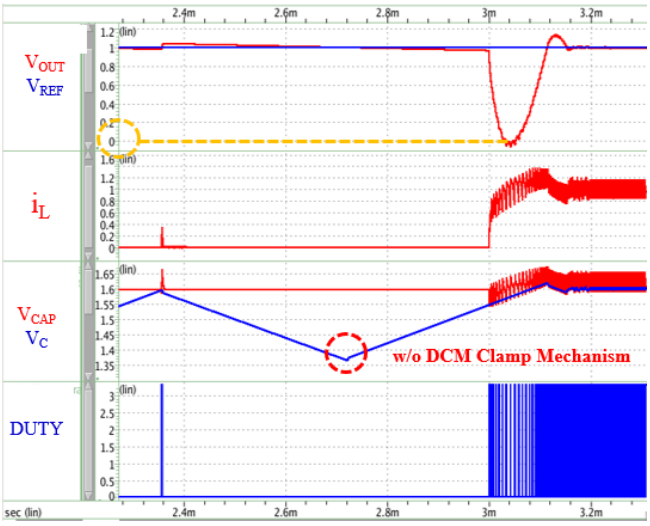

Fig. 3-23 Load transient waveform from DCM to CCM (without DCM clamp mechanism)

In order to avoid this phenomenon, the clamp mechanism is used to restrain the VC voltage to the low voltage bar, V_L, at extremely light loads. As shown in Fig. 3-1, the

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clamp mechanism circuit consists of a Schmitt trigger which is a bi-stable network. Fig. 3-24 illustrates that When the Vc is lower than the V_L, the output of the Schmitt trigger, V_{clamp}, will go low and turn off the low-side switch of the charge pump circuit. This forces the Vc voltage is limited to the V_L. Therefore, when the dramatic load transient occurs, the Vc can recover to the steady-state voltage soon. Then, the undershoot voltage of the V_{OUT} can be improved. In contrast, when the V_C is higher than the high voltage bar, V_H, the V_{clamp} goes high. Thus, the low-side switch can be controlled by the compensator output, SUB.

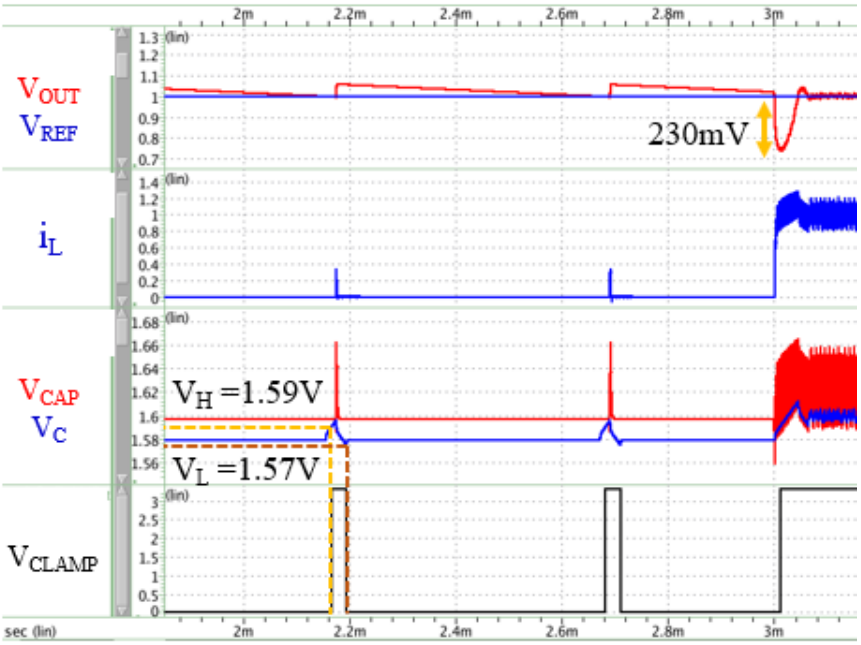

Fig. 3-24 Load transient waveform from DCM to CCM (with DCM clamp mechanism)

In this work, we set the V_H is 1.59V and the V_L is 1.57V as shown in Fig.3-24. If the V_L value is designed too low, the undershoot of the V_{OUT} will still drop a lot. Fig. 3-25(a) shows the undershoot is 500mV, because the V_L is only 1.56V. On the other

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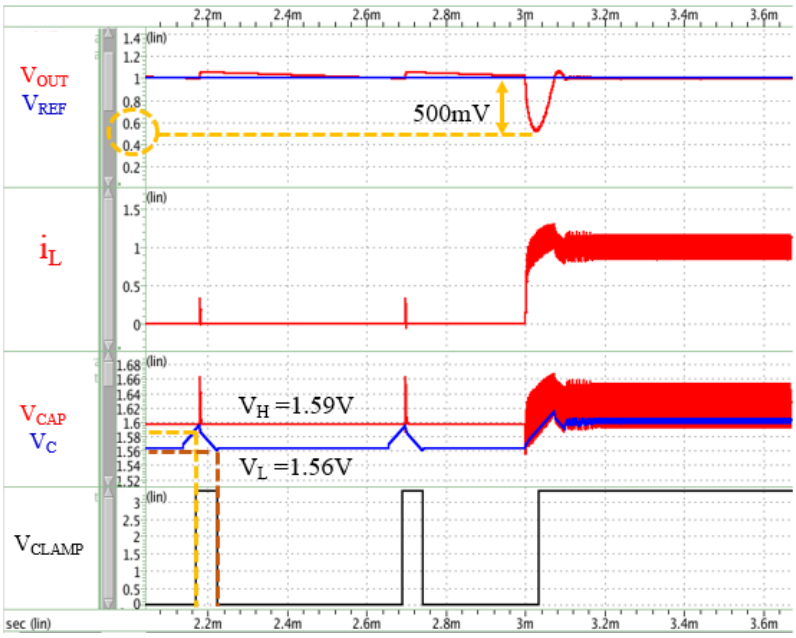
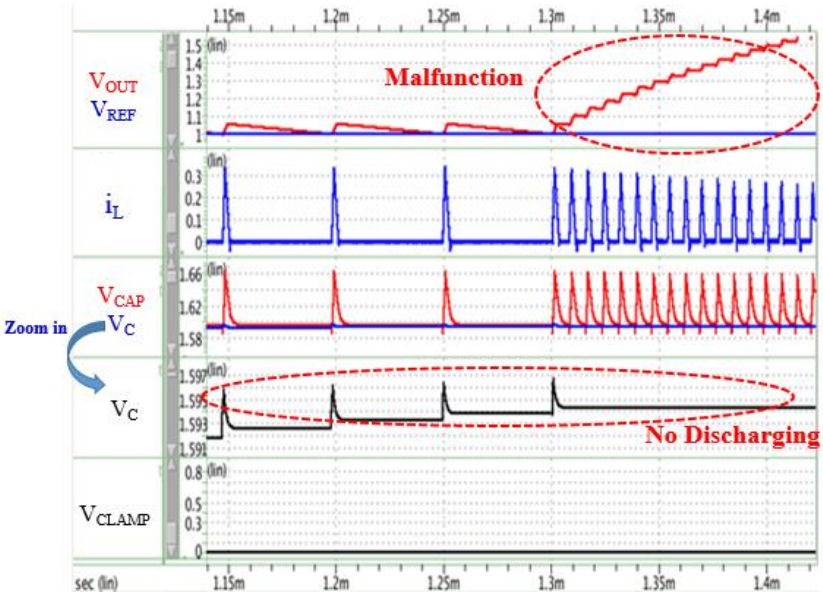
hand, if the V_H value designed too large, the low-side MOS, XX, will always be open. That forces the V_C cannot be discharged. Therefore, the malfunction will happen as shown in Fig. 3-25(b).



(a)



(b)

Fig. 3-25 Undesirable operation waveforms due to the improper design:

(a) VL is too low, (b) VH is too high

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Chapter 4

Circuit Implementation

The following chapters introduce the circuit design and power breakdown of each block. When the quiescent current of the controller is 3μA under 10μA load current, the efficiency is roughly 50% as shown in figure 4-1 below. Other losses including switching loss, conduction loss, and parasitic resistor loss on PCB. Then analyze the power breakdown of the controller in detail. The four main power-consuming blocks are the ripple coupling path, modulator, CPEA, and current bias circuit. Since the current bias will occupy a large power of the controller under an ultra-light load. To improve the power consumption problem, part of the bias current will be disabled through the Vclamp signal in idle time. Therefore, the overall controller power can be reduced at light load to promote efficiency.

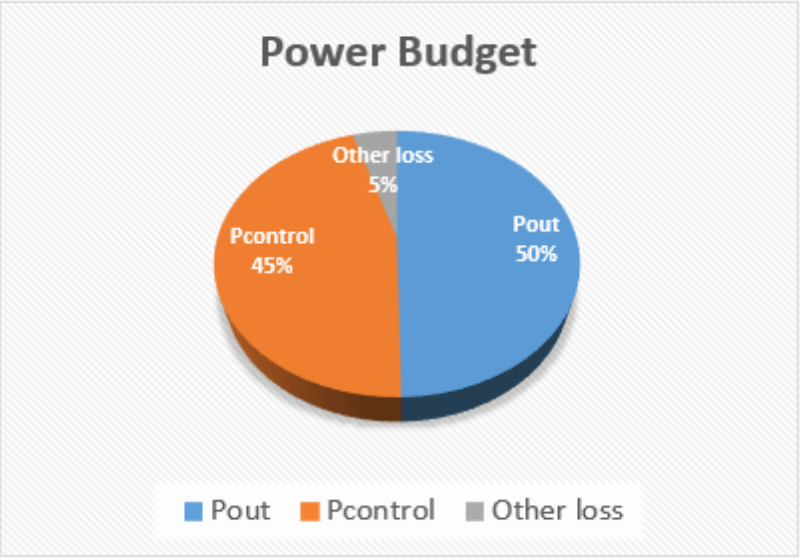

Fig. 4-1 Power budget at i_{LOAD}=10μA

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4.1 Delay Chain for Digital On/Off-Time Generator

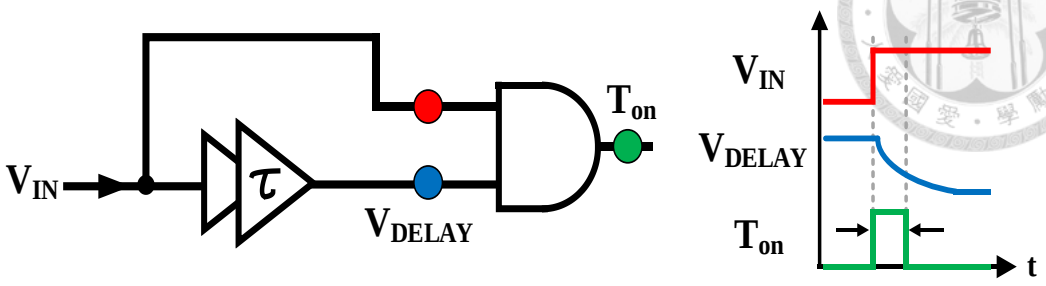

Fig. 4-2 Circuit diagram of a simple pulse width control and its timing diagram

The simple pulse width control with the delay chain is shown in Fig. 4-2. As we know, the more the delay cell, the wider the pulse width. However, the pulse width based on RC delay will be affected by PVT variations. In order to solve the PVT problem, the 2-bit on-time generator proposed in this paper includes coarse-tune and fine-tune. As shown in Fig. 4-3 and Fig. 4-4, the delay chain is composed of 7 delay units, so the delay time can be adjusted by manually changing the control bit <0: 1>.

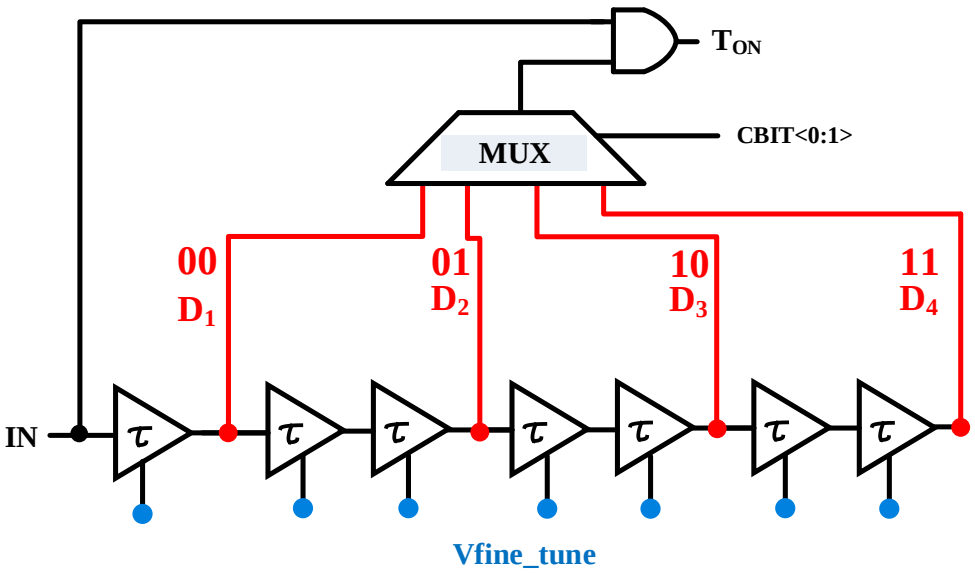

Fig. 4-3 Block diagram of the on-time generator with coarse-tune and fine-tune

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Furthermore, because the delay time is determined by a resistor, R_D, and a varactor, C_D, we can fine-tune the delay time by adjusting the top plate voltage of Varactor, Vfine_tune. The larger the voltage difference across the capacitor, the smaller the capacitance.

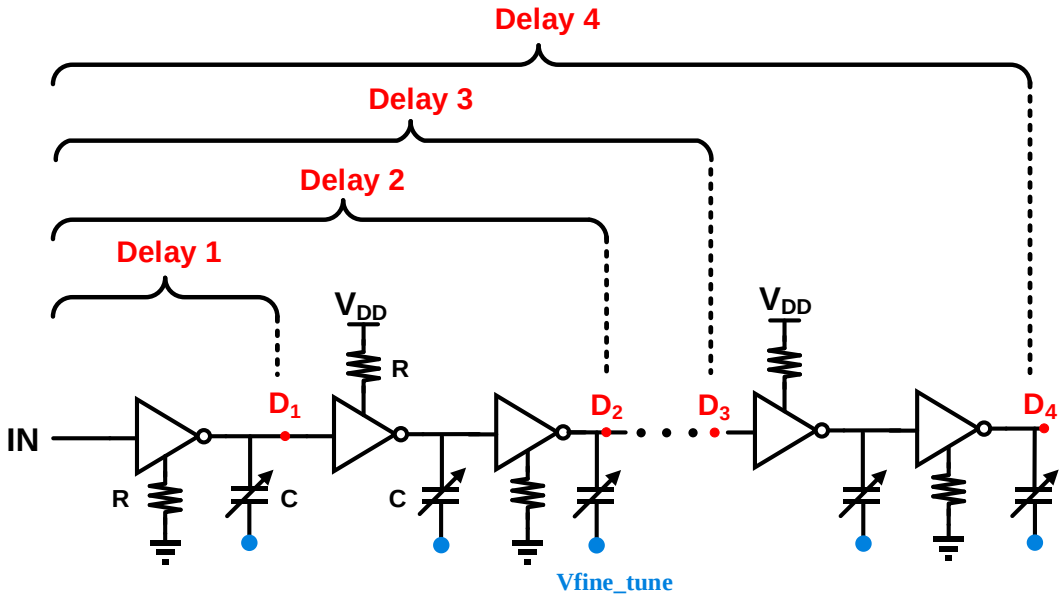

Fig. 4-4 Circuit diagram of the delay chain

Based on the equation (4.1), the duty, D, is related to the Ton and Tsw, where the Tsw is the inverse of the switching frequency. The switching frequency is 300kHz, so we can get the Ton=1 μs in equation (4.2). Then, we decide one delay unit, τ, is qual to 200ns in equation (4.3). Therefore, when the delay path, D3, is selected by control bit <0 : 1>, the on-time (Ton) pulse width is 1μs due to the 5 delay units.

$$D=\frac{V_{OUT}}{V_{IN}}=\frac{T_{on}}{T_{SW}}=\frac{1}{3.3}=0.303 \tag{4.1}$$

$$T_{on}=D\cdot T_{SW}\cong 1\mu s \tag{4.2}$$

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$$\tau = R_D C_D = 200ns \quad (4.3)$$

Where we design the R_D=235kΩ and the C_D =850fF. Note that the resistance of R_D must be designed larger and the capacitance of C_D must be designed smaller. Figure 4-5 shows a time-domain plot of the delay time and delay paths (D1-D4) through different numbers of delay units. It shows that the delay affects only the rising edge of the output waveform and does not affect the falling edge of the output waveform. The reason is that the resistor R_D is placed on the source terminal of the PMOS or NMOS, rather than on the output of the inverter. As shown in Fig.4-6, if the input signal, V_{IN}, is rising step, the time delay $\tau = R_D \cdot C_D$ will be reflected on the output signal, Vo. In contrast, if the V_{IN} is falling step, the falling delay is short due to the small parasitic resistance, Ron.

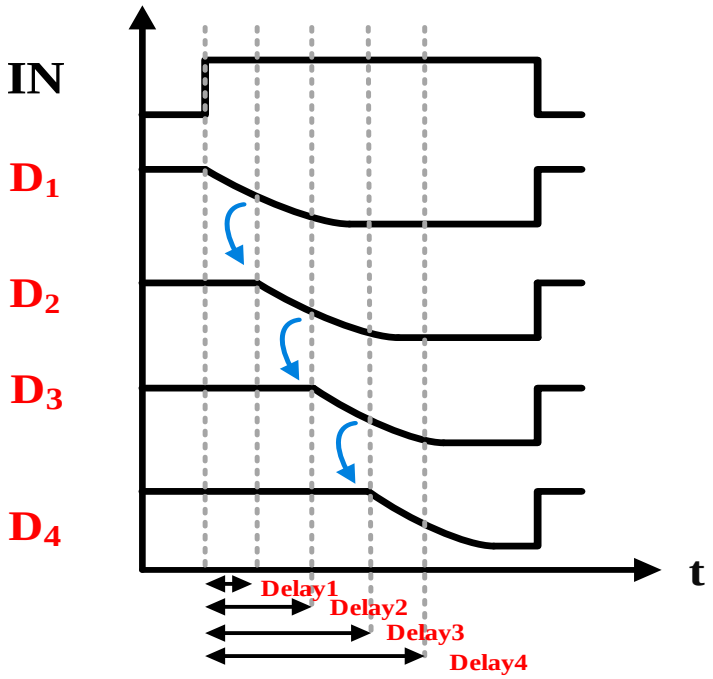

Fig. 4-5 Timing diagram of the on-time generator

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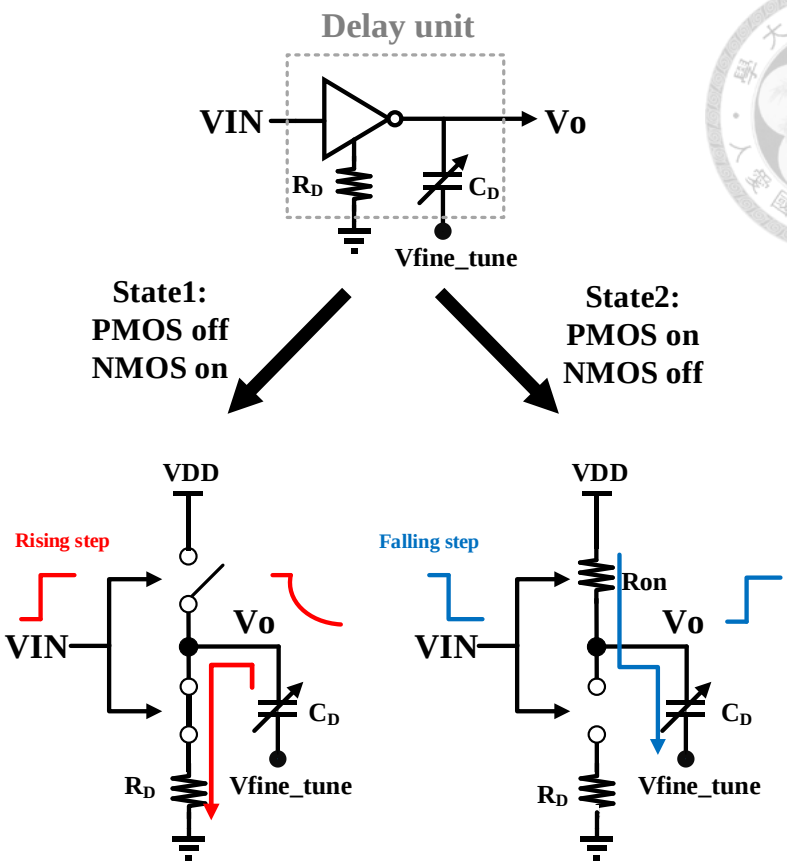

Fig. 4-6 Rising delay and falling delay of the delay unit

The Power breakdown is shown in Table 4-1. At a heavy load, the quiescent current of the on/off time generator is 9.94μA. Because of the digital operation, the quiescent current can scale with the switching frequency. Thus, the quiescent current becomes 640pA at an ultra-light load.

Table 4-1 Quiescent current of the on/off-time generator at different i_{LOAD}

	i_{LOAD}=1A	**i_{LOAD}=10μA**
Switching frequency	300kHz	19.6Hz
I_Q (Quiescent Current)	9.94μA	640pA

On-time pulse (Ton) with the change in coarse-tune and fine-tune is shown in Fig. 4-7. Based on the coarse-tune and fine-tune, we can still ensure that the on-time pulse

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can be adjusted to a desirable value (Ton=1μs) at different process corners. This result can be observed in Fig. 4-8.

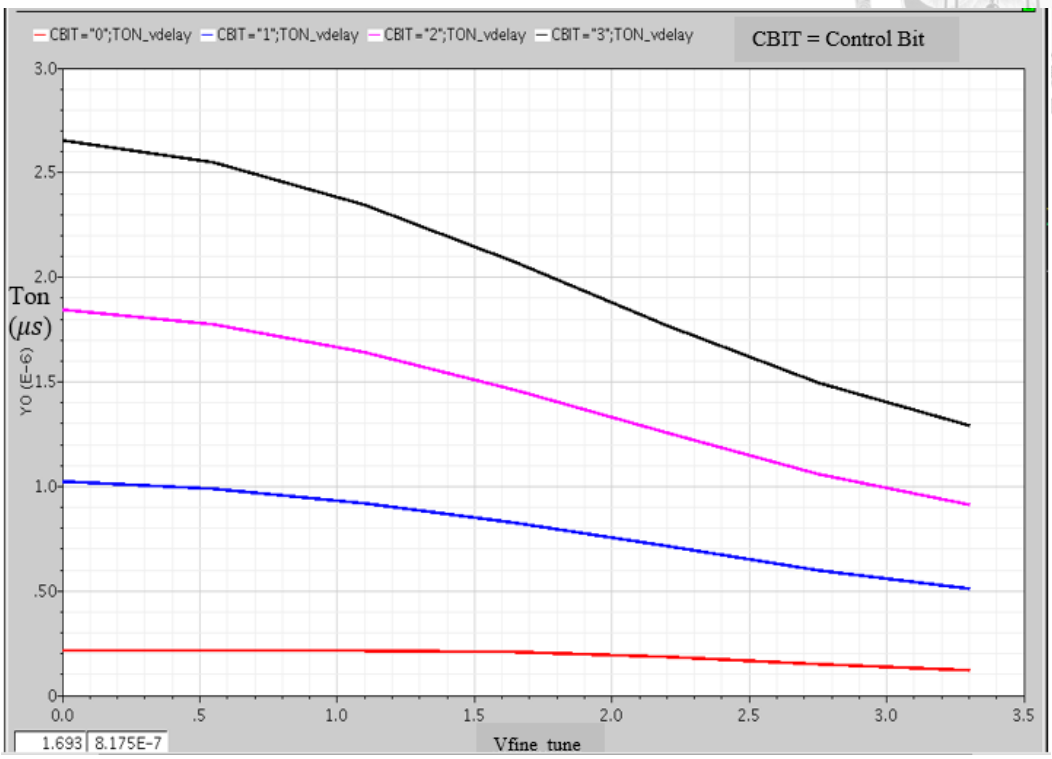

Fig. 4-7 On-time pulse width with change in the CBIT (control bits) and Vfine_tune

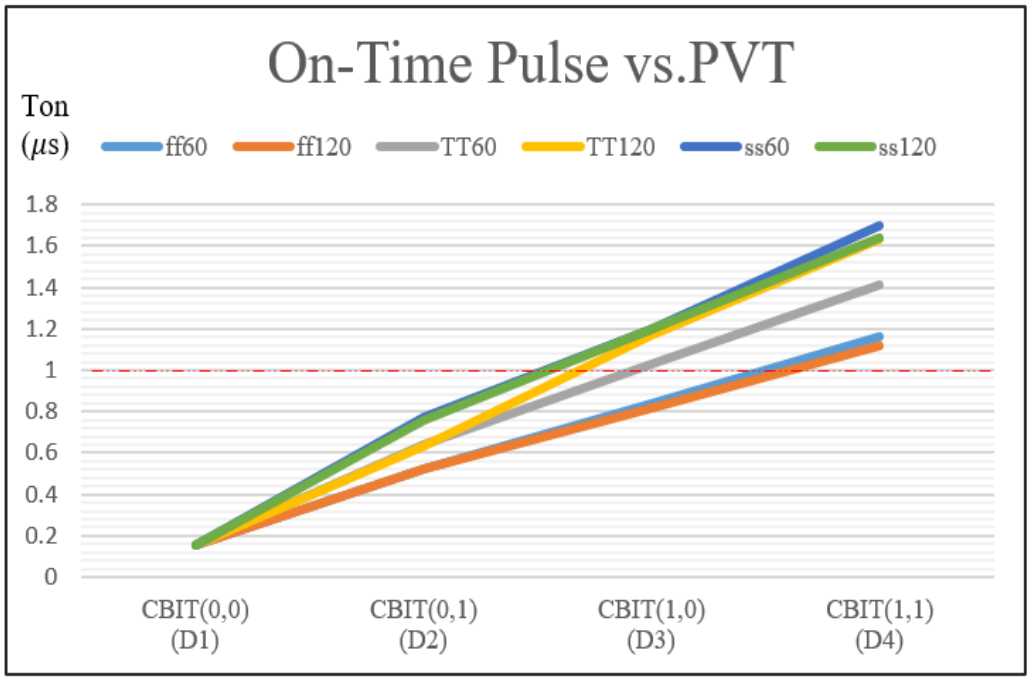

Fig. 4-8 PVT variations test of the on-time pulse width (process: TT, FF, SS; temperature: 60, 120 °C)

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4.2 Ripple Coupling Path

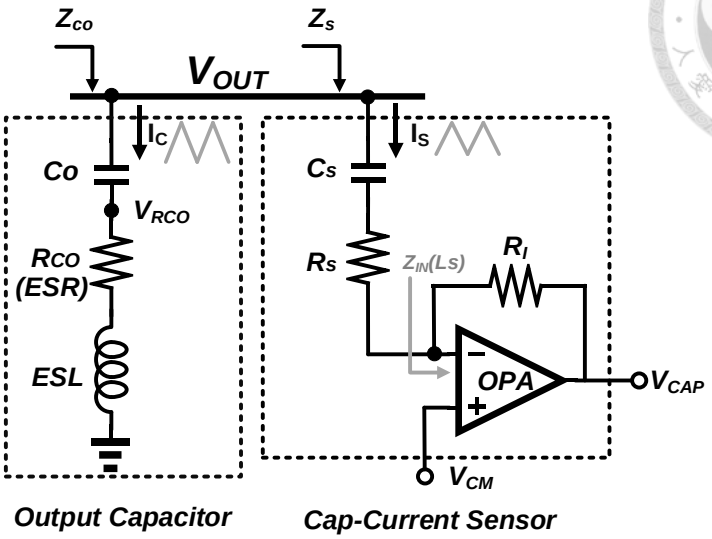

Fig. 4-9 Circuit diagram of the conventional capacitor-current sensor

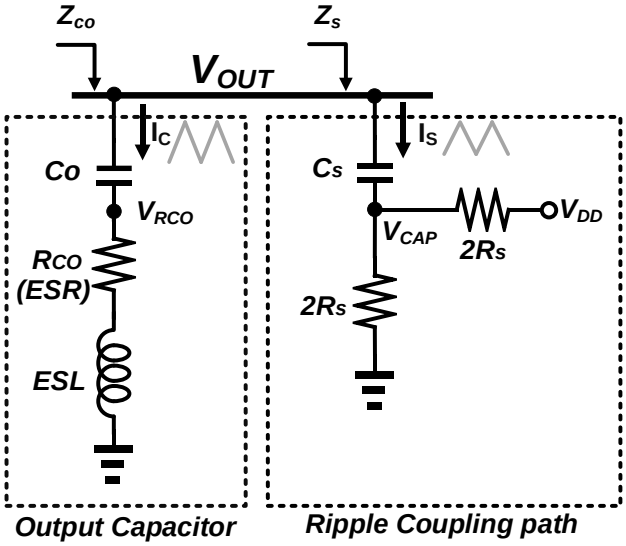

Fig. 4-10 Circuit diagram of the proposed ripple coupling path

Fig. 4-9 and 4-10 show the conventional capacitor-current sensor and the proposed ripple coupling path (RCP), separately. In conventional capacitor-current sensor, a high-bandwidth amplifier is used to imitate the equivalent inductance [10], [23]-[26] as shown in Fig. 4-9. The conventional approach causes the more power consumption on the current sensing circuit. In order to realize a low power current sensor, the ripple

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coupling path composed of the passive components only is proposed. Besides, there is no inductor used to imitate the ESL. Therefore, we must ensure that the switching frequency is less than the resonance frequency of the output capacitor. Because the circuit operates on the inductive side of the output capacitor, the system may be unstable. Figures 4-11 show the bode plot of the ripple coupling path impedance (Z_S) and output capacitor impedance (Z_{CO}). If the switching frequency of the system is greater than the resonance frequency of the output capacitor, it will cause a phase drop of nearly 90 degrees. Corresponding to the time domain waveform, it will cause instability.

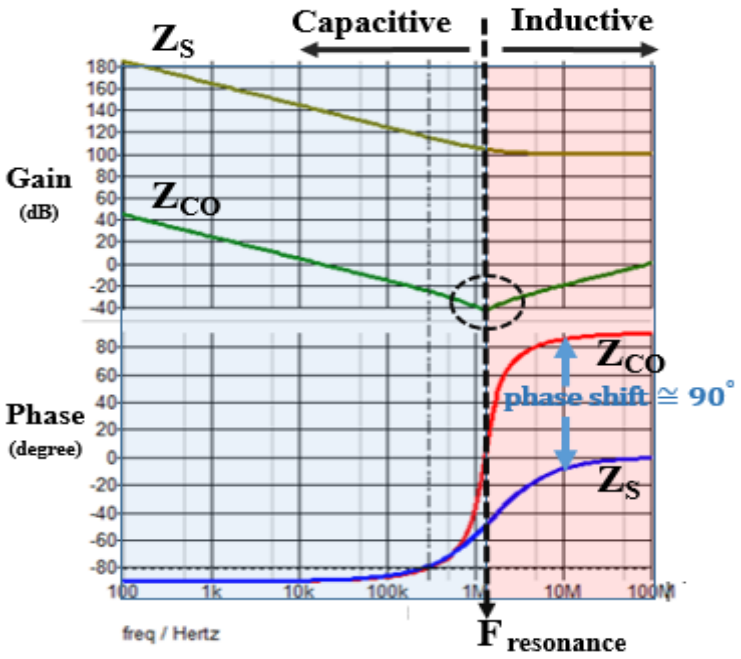

Fig. 4-11 Simulated impedance curves of the output capacitor impedance (Z_{CO}) and the ripple coupling path impedance curve (Z_S)

Design according to equation (3.3) and Table 3-1, if the Cs value is 1pF, then the Rs value should be designed to 80kΩ, this design can get the maximum stability due to only 2° phase shift as shown in Fig 4-12 (a). However, the quiescent current of RCP

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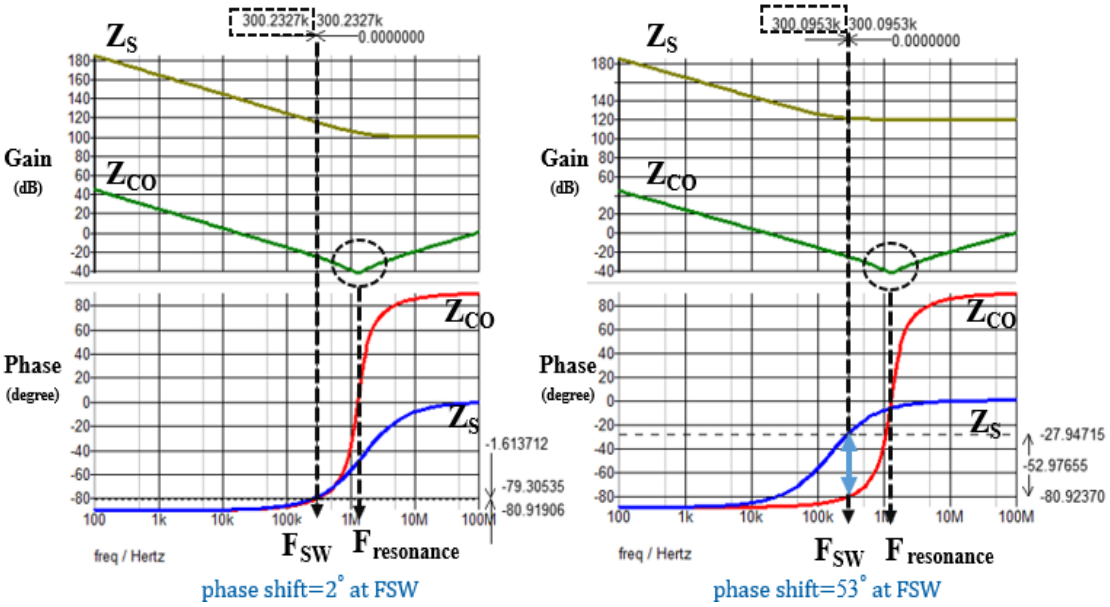
will be 10.3uA, which is unsatisfied with the power budget. In Table 4-2, we compare Rs value, current consumption, phase shift, stability, and V_{CAP} ripple. Finally, Rs is designed to be 1MΩ, and the current consumption of the ripple coupling path is 825nA. Although, the phase shift is 53° between Z_{CO} and Z_S at switching frequency, the time-domain waveform shown in Fig. 4-13 is still stable without considering the mismatch of passive devices.

Table 4-2 Relationship between R_S and other parameters

R_S Resistance	**V_{CAP} Ripple**	**Current Consumption**	**Phase Shift at Fsw**	**Stability**
80K	2.8mV	10.3uA	2°	stable
1Meg	**35mV**	**825nA**	**53°**	**stable**
1.5Meg	40mV	550nA	65°	unstable



(a) (b)

Fig. 4-12 Phase shift between Z_{CO} and Z_S at frequency=300kHz (F_{SW}): (a) Cs=1pF and R_S=80kΩ, (b) Cs=1pF and R_S=1MΩ

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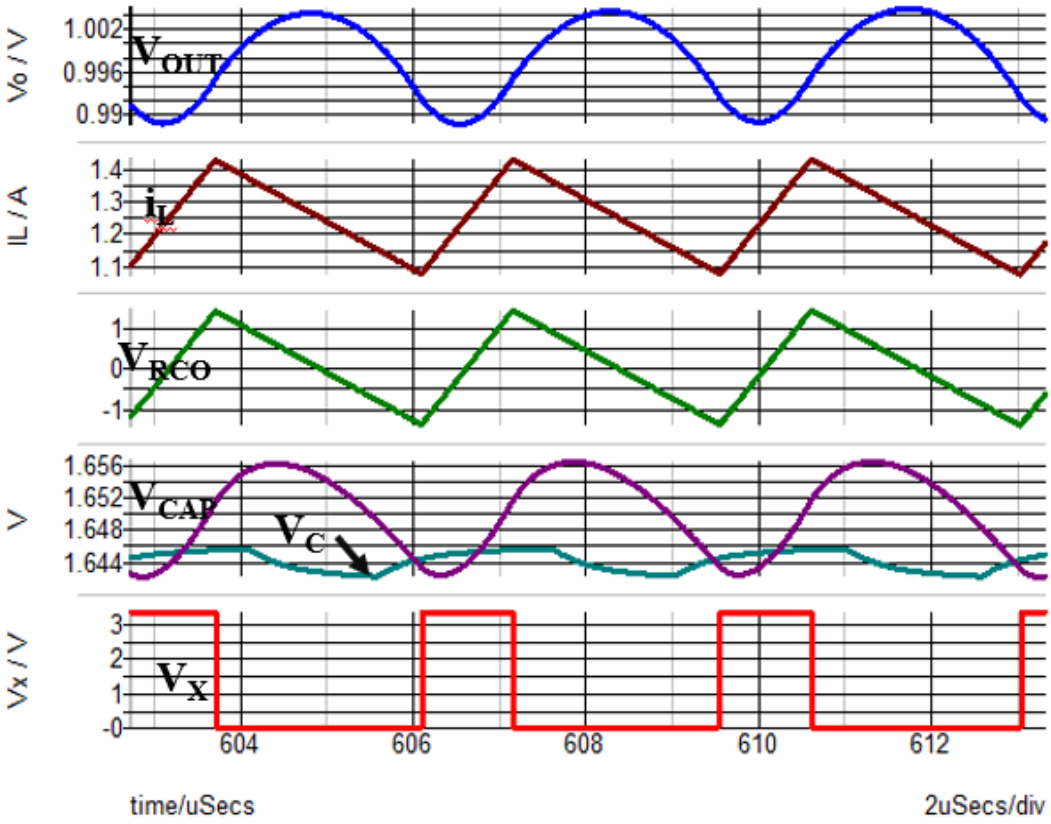

Fig. 4-13 Simulated modulation waveforms of RCCOT control

If the mismatch of the capacitor and the resistor is considered, the more phase shift will lead the system to become unstable. Figure 4-14 shows the time-domain waveform considering with the mismatch of +/- 20% in the ripple coupling path. The more phase delay due to the mismatch can cause a false trigger occasionally. Therefore, the slope compensation of the external slope is used to solve the waveform distortion caused by the phase shift.

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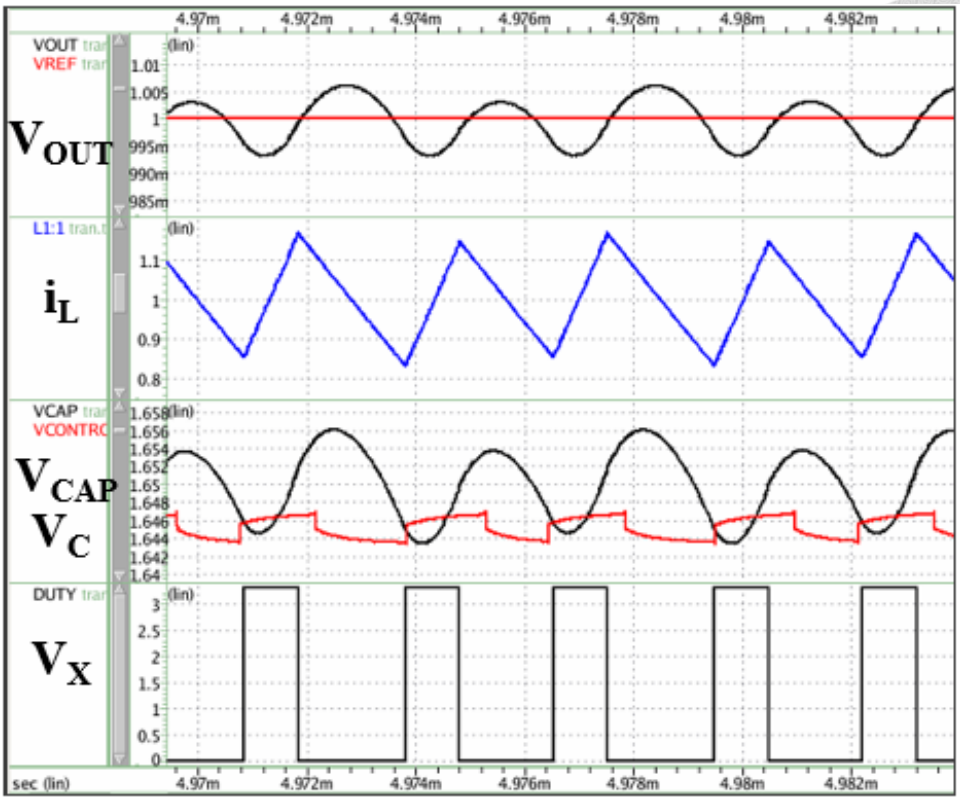

Fig. 4-14 Simulated modulation waveforms of RCCOT control considering with the mismatch of the passive devices

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4.2.1 Ripple Coupling Path with The External Ramp

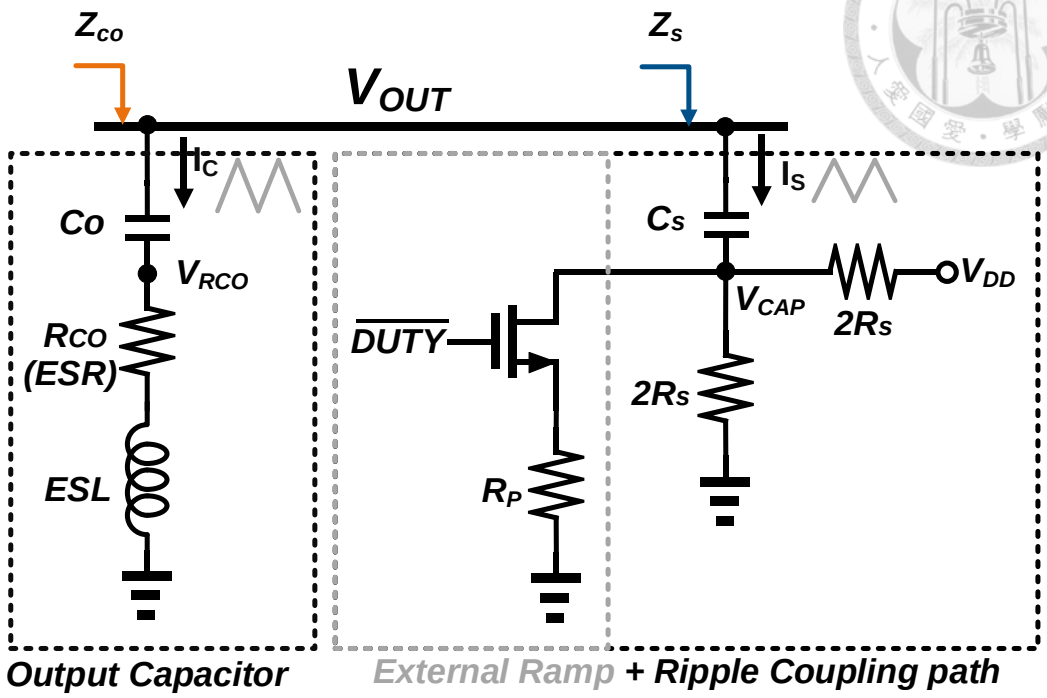

Fig. 4-15 Circuit diagram of RCP with the external ramp

The external ramp compensation used to improve the distortion of V_{CAP} is shown in Fig. 4-15. The V_{CAP} signal in the ripple coupling with the external ramp circuit can be divided into two parts, $V_{CAP}(t)|_{V_{OUT}=0}$ and $V_{CAP}(t)|_{VDD=0}$, for analysis. If we use the superposition theorem, there is only one input source, VDD, in the circuit as shown in Fig. 4-16. When $\overline{DUTY}$ goes high, the resistor R_P connects to V_{CAP}. The capacitor, Cs, is discharged to the ground through the resistor R_P. Thus, the ramp compensation voltage, V_{CAP_RAMP}, will be determined by the low pass filter and can be express as equation (4.4). When $\overline{DUTY}$ goes low, the supply voltage, VDD, charges the Cs. Thus, the ramp compensation voltage, V_{CAP_RAMP}, can be express as equation (4.5).

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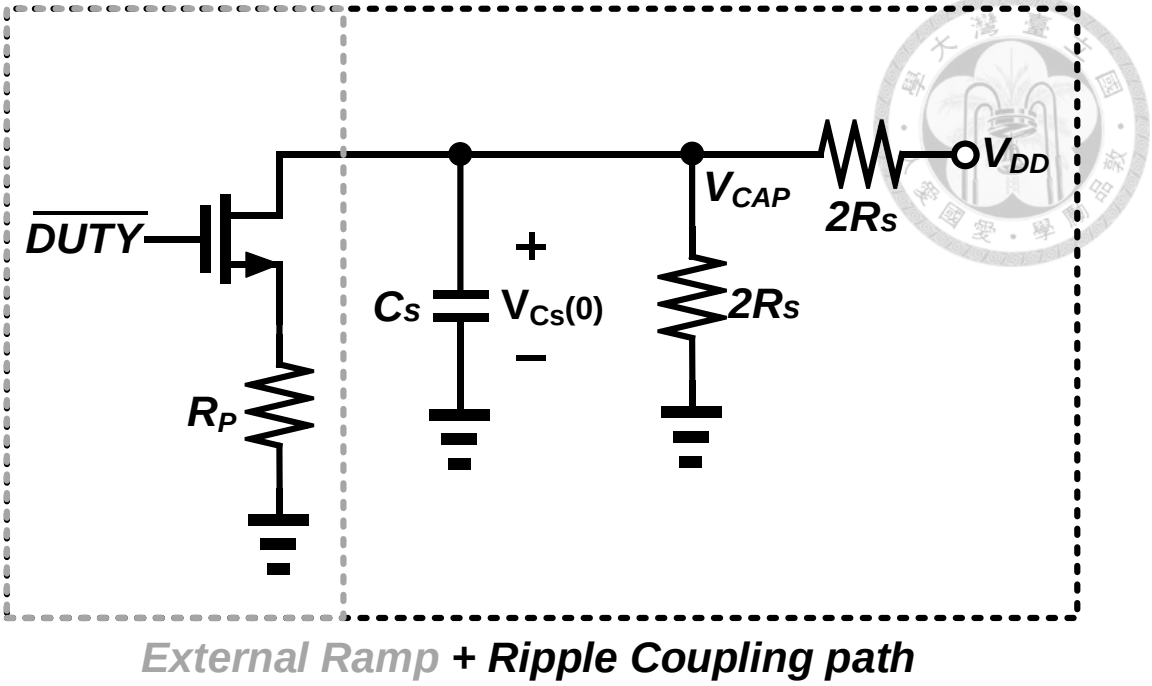

Fig. 4-16 RCP with the external ramp using superposition thorem

(1) $\overline{DUTY}$ goes high:

$$V_{CAP}(t)\big|_{V_{OUT}=0} = VDD \cdot \frac{(2R_S // R_P)}{(2R_S // R_P) + 2R_S} \cdot (1 - e^{\frac{-t}{R_{eq}C_S}}) + V_{Cs}(0) \cdot e^{\frac{-t}{R_{eq}C_S}} \quad (4.4)$$

(2) $\overline{DUTY}$ goes low:

$$V_{CAP}(t)\big|_{V_{OUT}=0} = VDD \cdot \frac{1}{2} \cdot (1 - e^{\frac{-t}{R_S C_S}}) + V_{Cs}(0) \cdot e^{\frac{-t}{R_S C_S}} \quad (4.5)$$

Where $V_{Cs}(0)$ is the initial voltage of the C_S and $R_{eq} = R_S//R_P$. Then, with the superposition theorem, we turn off the VDD and analysis the V_{CAP} signal which can be express as (4.6) and (4.7). When $\overline{DUTY}$ goes high, the resistor R_P connects to V_{CAP}.

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The distortion of $V_{CAP}(s)$ can be suppressed because the parallel resistor, R_P, decrease the phase shift between the V_{CAP} and V_{RCO}. When $\overline{DUTY}$ goes low, the equivalent circuit is the same as Fig. 4-10.

(1) $\overline{DUTY}$ goes high:

$$V_{CAP}(S)\big|_{VDD=0} = V_{OUT}(s)\cdot\frac{SC_S\cdot(R_S//R_P)}{1+SC_S\cdot(R_S//R_P)} \tag{4.6}$$

(2) $\overline{DUTY}$ goes low:

$$V_{CAP}(S)\big|_{VDD=0} = V_{OUT}(s)\cdot\frac{SC_S\cdot R_S}{1+SC_S\cdot R_S} \tag{4.7}$$

From (4.4) to (4.7), we can observe that R_P determines the magnitude of the external slope. If a smaller R_P is used, a larger external ramp will be injected into the ripple coupling path. However, due to power consumption restrain, we design R_P = 30MΩ and the current consumption of ripple coupling path is 850nA. Fig. 4-17 shows the waveform of $V_{CAP}(t)\big|_{V_{OUT}=0}$, $V_{CAP}(t)\big|_{VDD=0}$, and V_{CAP}. According to the simulation waveform in Figure 4-18, when ripple coupling considers the mismatch of +20% (worst case) on the passive devices, the external ramp circuit can effectively improve the instability caused by the mismatch.

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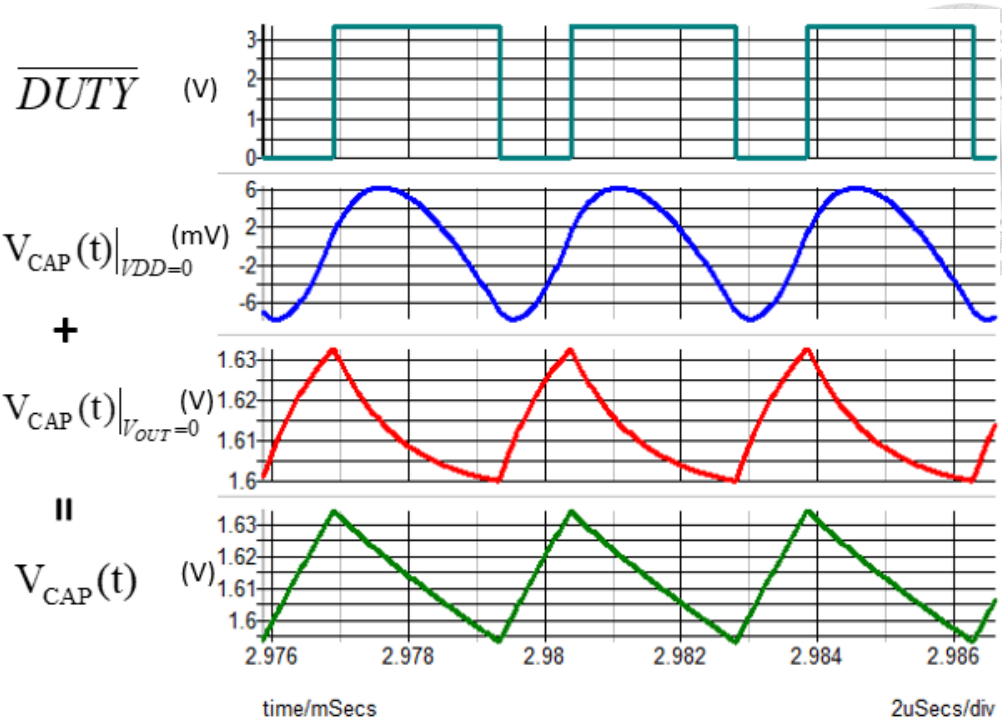

Fig. 4-17 Simulated waveforms of $V_{CAP}(t)|_{V_{OUT}=0}$, $V_{CAP}(t)|_{VDD=0}$, and V_{CAP}

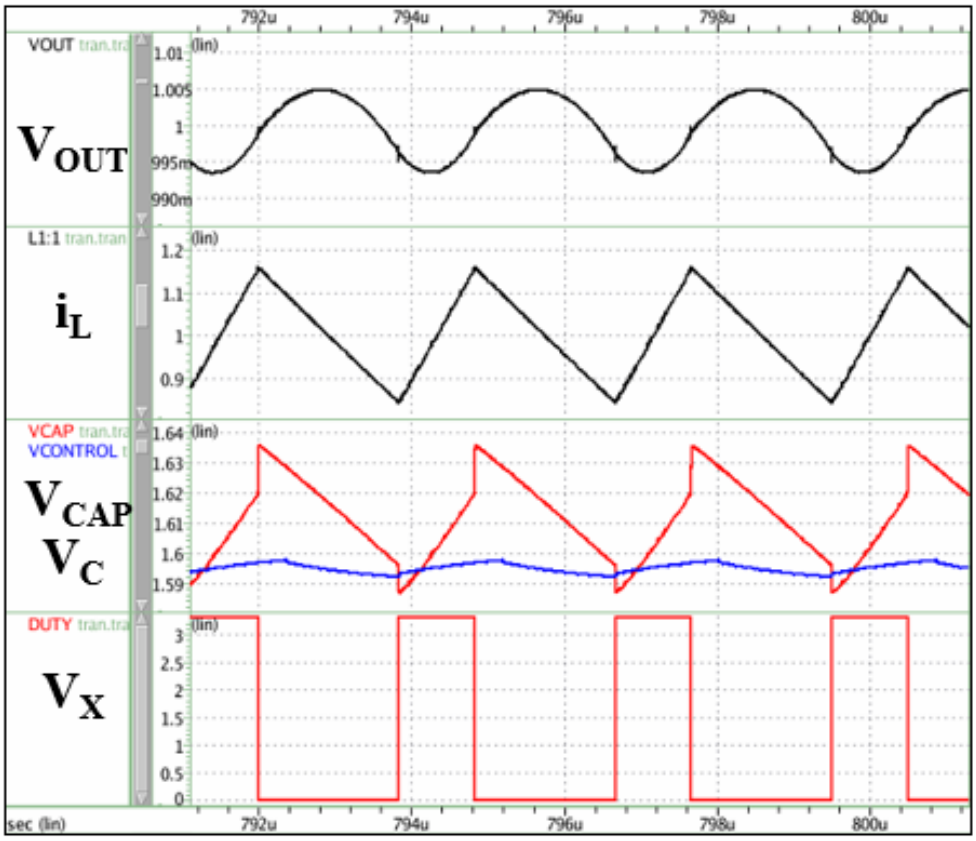

Fig. 4-18 Simulated modulation waveforms of RCCOT control with RCP adding an external ramp

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4.3 Modulation Comparator

4.3.1 The Characteristics of Modulation Comparator

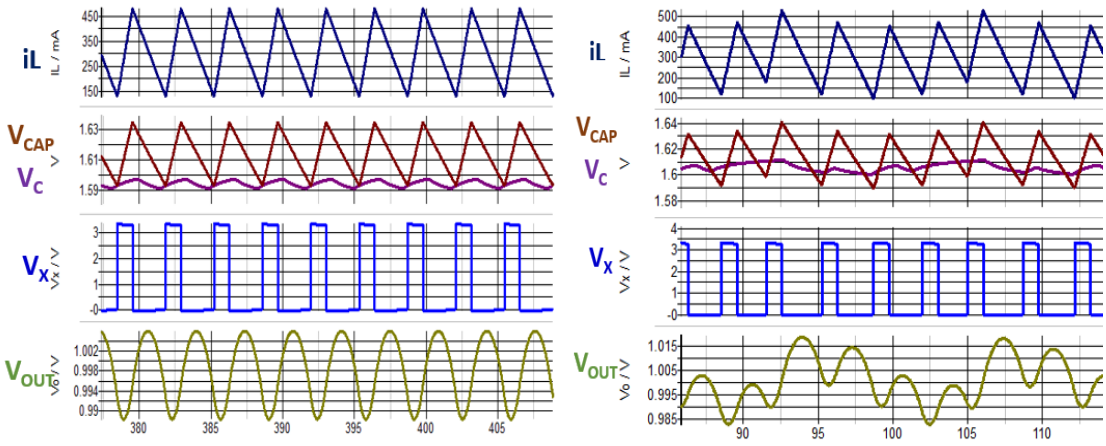

Fig. 4-19 Steady-state waveform of RCCOT control: (a) the modulation comparator with 200ns time delay, (b) the modulation comparator with 650ns time delay

From the time-domain waveform in *SIMPLIS*, we can observe that the time delay of the modulator mainly affects the stability of the system. Fig. 4-19 (a) and (b) show that when the time delay of the modulator is too large, it will also cause an unstable issue. The following section analyzes the relationship between comparator and time delay [14].

First of all, we regard the comparator as a single-pole system and it can be described as follow:

$$A_V(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{A_V(0)}{(\frac{s}{\omega_C}+1)} = \frac{A_V(0)}{(s\tau_C+1)} \tag{4.8}$$

Where $A_V(0)$ is the dc voltage gain of the comparator and ω_C equal to $\frac{1}{\tau_C}$ is the -3dB

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frequency of the comparator. Then, the Laplace-domain transfer function can be converted to the time-domain transfer function (4.9).

$$V_0(t) = A_V(0) \cdot \left[1 + e^{-t_P/\tau_C}\right] \cdot V_{in} \tag{4.9}$$

The propagation time delay (t_P) for a single-pole comparator can be expressed as follows:

$$\frac{V_{OH}-V_{OL}}{2} = A_V(0) \cdot \left[1 + e^{-t_P/\tau_C}\right] \cdot V_{in} \tag{4.10}$$

Where V_{OH} is the high-level output of the comparator and V_{OL} is the low-level output of the comparator. Finally, the propagation time delay (t_P) can be derived from the equation (4.11). From (4.11), the t_p is dominated by the pole, τ_C, which means the higher the frequency of ω_C, the shorter the propagation time delay.

$$t_P = \tau_C \cdot \ln\left(\frac{1}{1-\frac{V_{OH}-V_{OL}}{2A_V(0)V_{in}}}\right) \tag{4.11}$$

4.3.2 The Comparison of Comparator Architectures

According to Section 4.3.1, the simulation shows that the propagation time delay of the modulator must be less than 650ns to be sufficient to stabilize the system. Based on (4.8)-(4.11), the bandwidth frequency of the modulator comparator must be high enough to avoid instability issues. Under the limitation of power budget, we can

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formulate the specifications as shown in the following Table 4-3.

Table 4-3 Specification of the modulation comparator

Parameter	**Specification**
VDD	3.3V
C_L	50fF
Propagation Delay	200ns (<650ns)
Current consumption	1uA at i_{LOAD} =10μA

In order to meet the specifications, three different comparators are compared in this section as shown in Fig. 4-20 (a)-(c) [11], [15]. Fig. 4-21 shows the AC response of different comparators with the same transistor size and current bias. We can observe The current-mirror amplifier with the RC broadband technique [11] uses the zero generated by Rs and Cs to shift the -3dB bandwidth, ωc, to 4.6MHz, which is farther than the ωc of the other two comparators. Table 4-4 also shows that the propagation delays are 30ns, 10ns, and 20ns, respectively. Among them, the delay of the current-mirror amplifier with the RC broadband technique is the shortest. Therefore, it is selected as the modulation comparator, finally.

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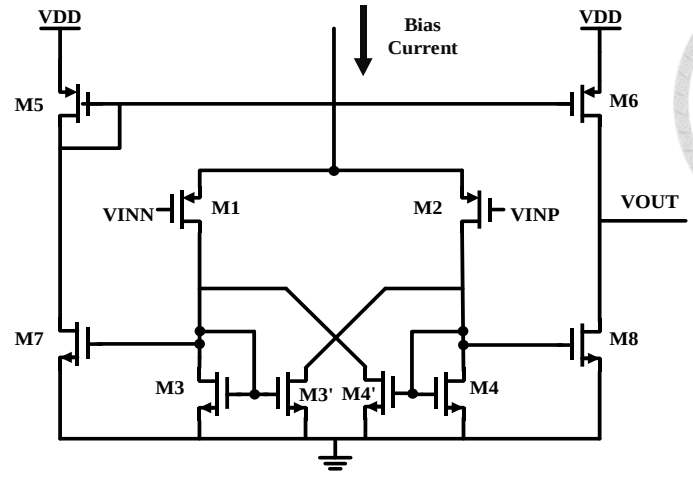
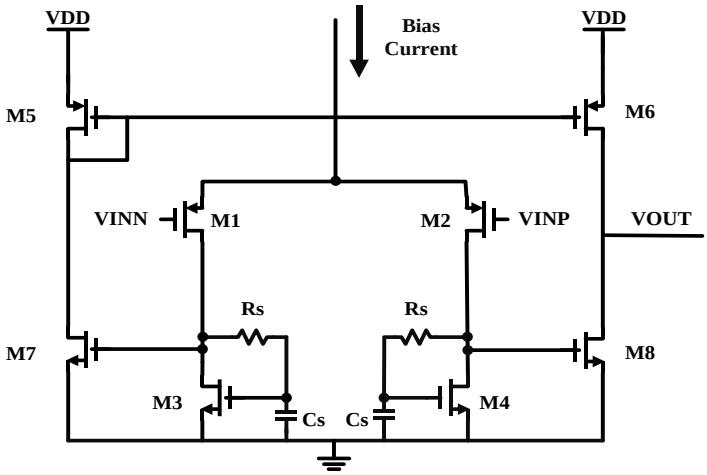
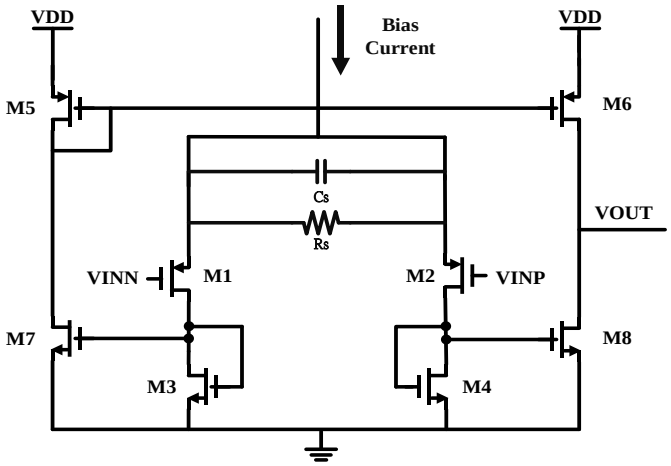


(a)



(b)



(c)

Fig. 4-20 Three comparator architectures: (a) cross-couple amp., (b) Current-mirror amplifier with the RC broadband technique, and (c) Current-mirror amplifier with the capacitive degeneration

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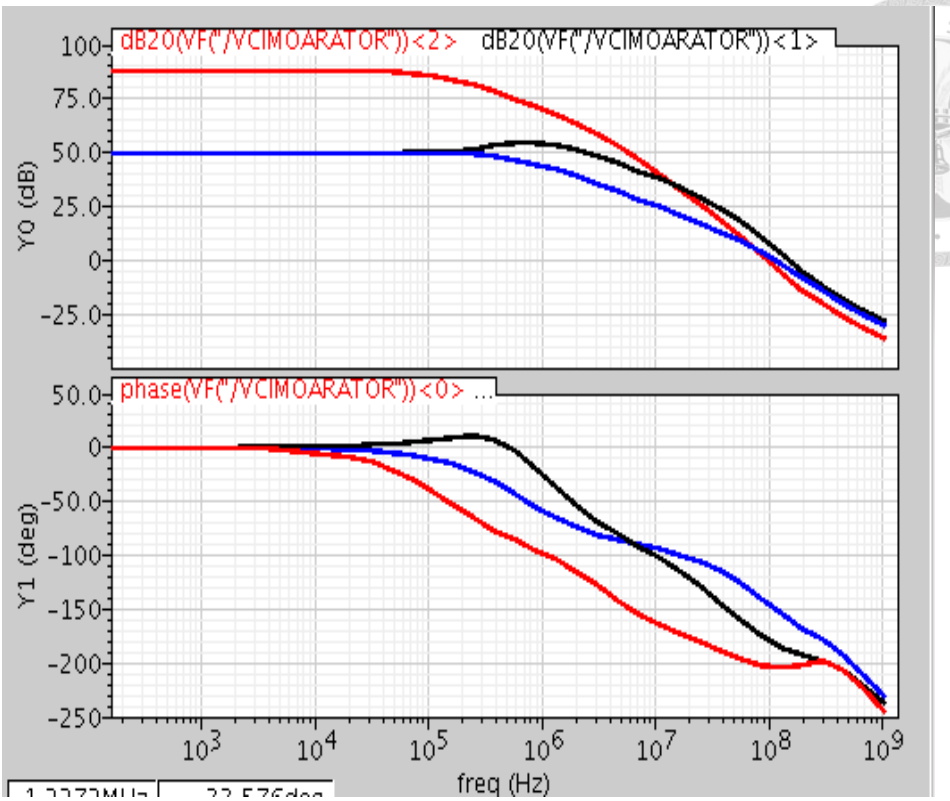

Fig. 4-21 Ac response of three comparators

Table 4-4 Comparison between three amplifier architectures

	Cross-Couple amplifier	**Current-mirror amplifier with the RC broadband technique**	**Current-mirror amplifier with the capacitive degeneration**
Current Bias	0.75uA	0.75uA	0.75uA
Propagation Delay	30n(s=2.25ns)	10ns(s=3.23ns)	20ns(s=3.87ns)
Input Offset	2.5mV(8mV)	3mV(s=11mV)	4mv(s=19mV)

4.3.3 The Modulation Comparator Design

The implementation of the modulation comparator is shown in Fig. 4-22 In the first stage of the comparator, the differential pair consists of M1 and M2 with the active

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load formed by M3, M4, two resistors (Rs), and two capacitors (Cs). Consquently, the comparator can generate a pole-zero pair to make sure the phase boost for broadband. In the second stage, the V_{OP} and V_{ON} signal are converted to the full swing voltage V_{COMP}.

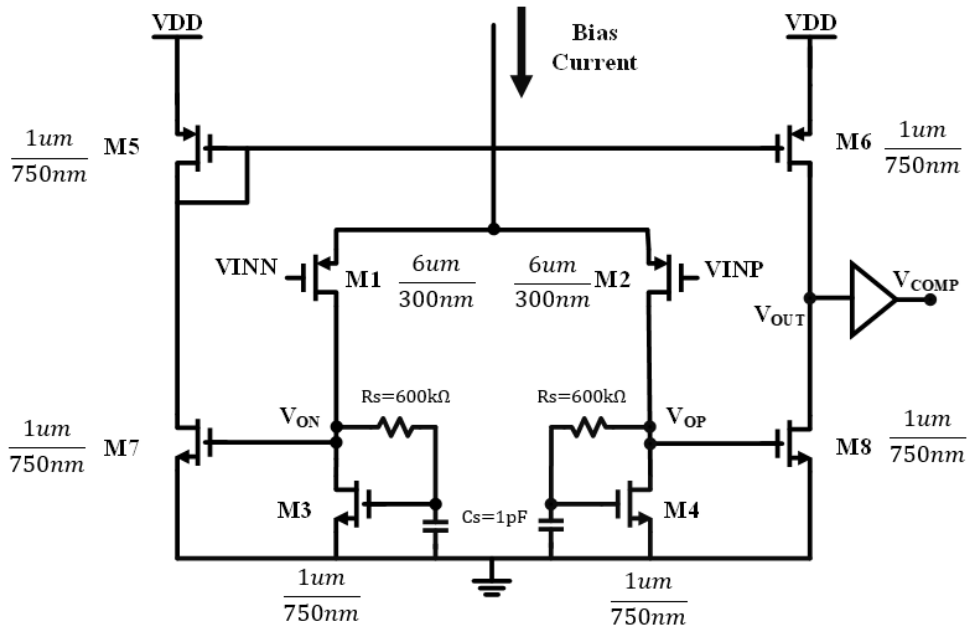

Fig. 4-22 Implementation of the modulation comparator

We use the small-signal half-circuit model of the first stage of the comparator, as shown in Fig. 4-23 to express the pole-zero pair. The test voltage V_t is applied to the V_{ON} node, and the corresponding current I_t flows into it. Thus, the equivalent output impedance Z_O can be determined.

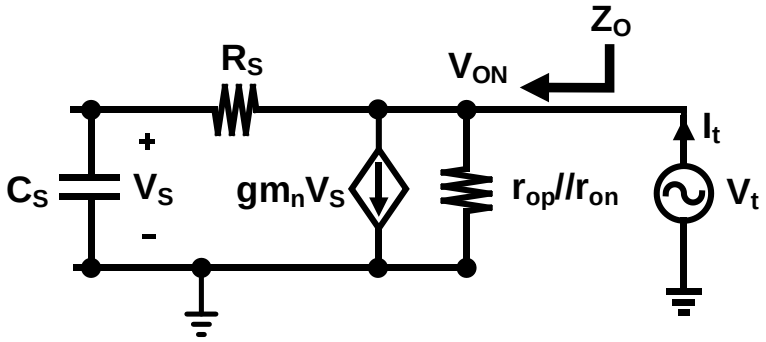

Fig. 4-23 Equivalent small-signal model of the first stage

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By the KCL theorem, the equation (4.12) can be obtained as follows:

$$i_t = \frac{V_t}{r_{op}//r_{on}} + \frac{V_t}{R_S + \frac{1}{sC_S}} + gm_n V_S \quad , \quad V_S = \frac{V_t}{1+sR_SC_S} \tag{4.12}$$

If the channel length modulation is neglected, the output impedance Z_O cam be derived as (4.13).

$$Z_O = \frac{V_t}{I_t} = \frac{1+sR_SC_S}{gm_n + sC_S} \tag{4.13}$$

Then, the transfer function can be derived as (4.14) where the pole and zero are located at gm_n/C and $1/R_SC_S$, respectively.

$$A_V(s) = \frac{gm_p}{gm_n} \cdot \frac{1+sR_SC_S}{1+s\frac{C_S}{gm_n}} \tag{4.14}$$

In this comparator design, if $R_S > 1/ gm_n$, the zero is located at lower frequency compared with the poles. The input signal will have a phase lead compared with the output signal. On the other hand, the value of the R_S set too large will make the more current consumption. Therefore, we set the R_S value to 4 times gm_n value. The R_S and Cs are set as 600kΩ and 1pF.

Finally, the simulation verification is shown in Fig. 4-24. The rising propagation delay is 10ns and the falling propagation delay is 160ns. The difference between the rising delay and falling delay is caused by the difference in the differential input signal (VINP-VINN). Table 4-5 shows the comparison between the specification and the

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simulation of the comparator.

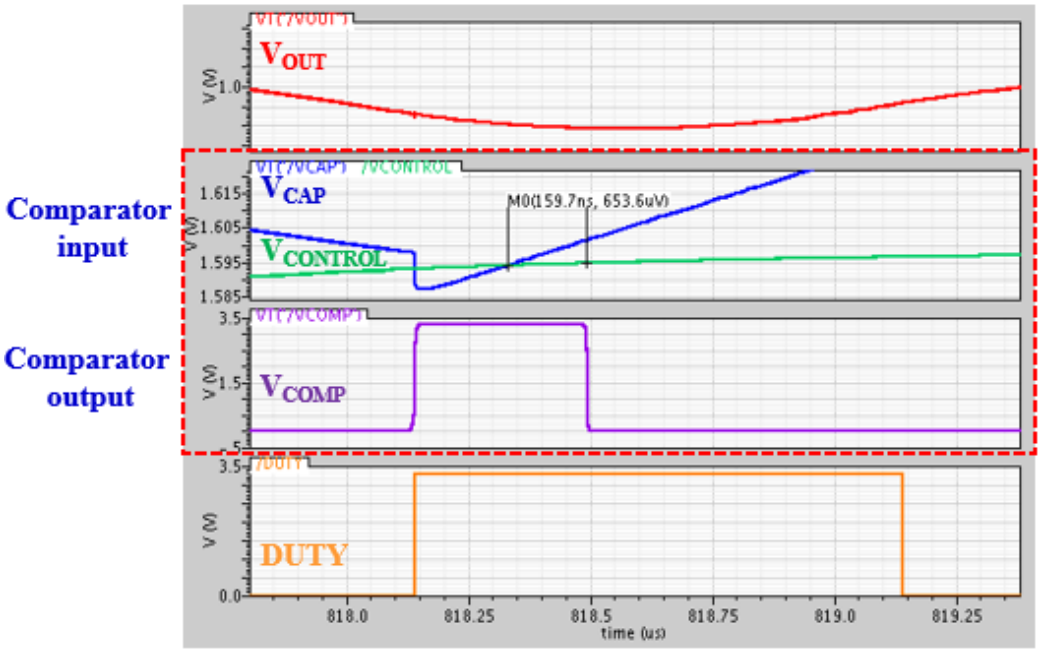

Fig. 4-24 Propagation delay of the modulation comparator in the simulated waveform

Table 4-5 Comparison between the specification and the simulation of the comparator

Parameter	**Specification**	**Simulation**
VDD	3.3V	3.3V
$V_{in,\,cm}$	1.6V	1.6V
C_L	50fF	50fF
Propagation Delay	200ns	160ns
ω_C(-3dB BW)	3.5MHz	4.6MHz
IQ	0.75μA at i_{LOAD} =10μA	0.55μA at i_{LOAD} =10μA

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4.4 Charge Pump-Based Error Amplifier

The discrete-time comparator design will be discussed in Section 4.5.1, and the two versions of CPEA will be compared in Section 4.5.2. In the first version of CPEA, we need a clock generator to trigger the discrete-time comparator. Based on the Nyquist criterium, the sampling frequency needs to be larger than 2 times the bandwidth of interest. Thus, we decide the clock frequency as 2 MHz. On the other hand, from the simulation waveform in SIMPLIS, when the propagation delay of the comparator is 800 ns, the system is still stable. However, the system becomes unstable under the 1us delay of the comparator. Therefore, specifications of the comparator were formulated in Table 4-6. In the second edition, we used a continuous-time comparator instead of a discrete-time comparator, so that the clock generator can be eliminated and the current consumption of 35μA can be saved. Although a continuous-time comparator requires a bias current which causes the more current during heavy load, we proposed the clamp mechanism which can halve the bias current to greatly reduce the power consumption in idle time.

Table 4-6 Specification of the chaege pump-based error amplifier

Parameter	Specification
Supply Voltage	3.3v

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$V_{in,\,cm}$	1v
Power Budget	<1μA at i_{LOAD} =10μA
Propagation Delay	800ns (<1us)
F_{CLK}	2MHz

4.4.1 The Discrete-Time Comparator of The First Version of CPEA

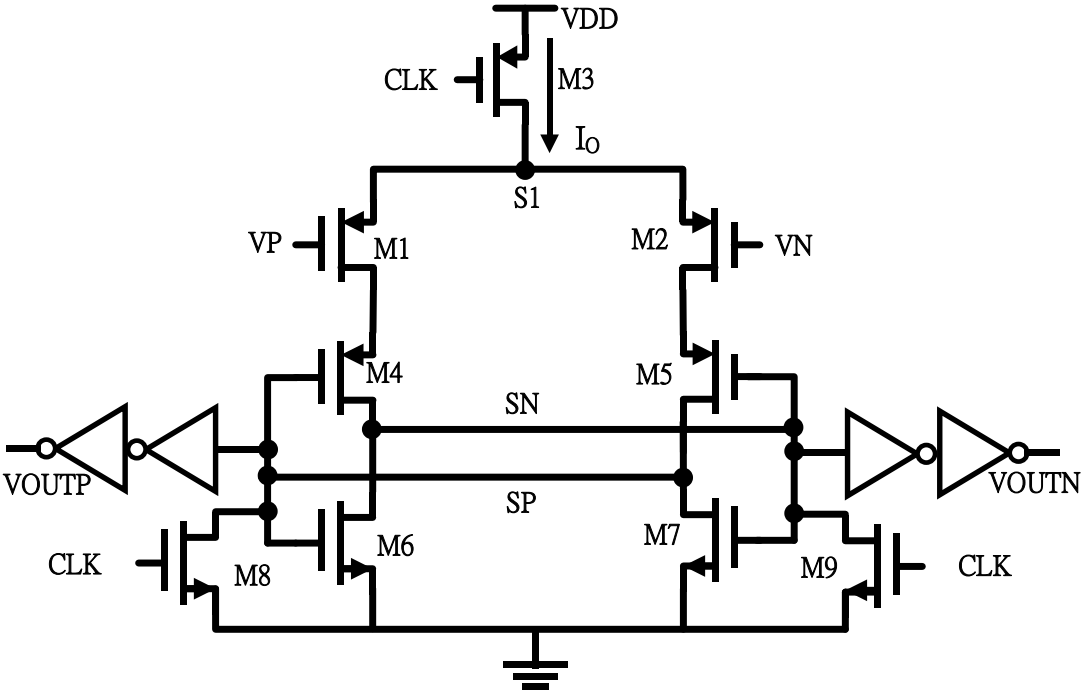

Fig. 4-25 Circuit diagram of the latch-type sense amplifier (Latch Amp.)

In the first version, a latch-type sense amplifier [12] was used to implement the comparator of the CPEA. This sense amplifier combines the strong positive feedback with high resistive input as shown in Fig. 4-25. The current flow of the input transistor controls the serially connected latch circuit. A small difference between the currents through M1 and M2 converts to a large voltage difference. Then, the output voltage

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difference can be quickly increased due to positive feedback of the latch circuit. Therefore, there is a short propagation delay in this sense amplifier. The amplifier speed can be analyzed by estimating total delay, T_D.

$$T_D = t_0 + t_{latch} \tag{4.15}$$

The total delay, T_D, can be separated into t_0 and t_{latch}. The delay t_0 represents a load capacitor C_L is charged until the n-channel transistor turns on. Since M1 has been assumed to have smaller input potential, the drain current I_P introduces more charge to output SP compared to SN which is driven by M2 with smaller current I_N. As such, the charging delay, t_0, can be expressed as

$$t_0 = \frac{C_L \cdot V_{thn}}{I_P} \tag{4.16}$$

Where

$$I_P \cong \frac{I_O}{2} \tag{4.17}$$

t_{latch} is the latching delay of the cross-coupled inverters. The value of t_{latch} is mainly determined by τ_{latch}, but output voltage swing (ΔV_{out}), input voltage difference (ΔV_{IN}), and tail current (I_O) will also affect the latch slightly. From [12], [15], we can get the following formula (4.18).

$$t_{latch} = \tau_{latch} \cdot \ln\left(\frac{1}{V_{thn}}\sqrt{\frac{I_O}{2\beta}} \cdot \frac{\Delta V_{out}}{\Delta V_{IN}}\right) \tag{4.18}$$

Where

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$$\tau_{latch} = \frac{C_L}{gm_{latch}} \tag{4.19}$$

With (4.16) and (4.18), the total delay of (X.X) becomes

$$T_D = \frac{2C_L \cdot V_{thn}}{I_O} + \frac{C_L}{gm_{latch}} \cdot \ln\left(\frac{1}{V_{thn}}\sqrt{\frac{I_O}{2\beta}} \cdot \frac{\Delta V_{out}}{\Delta V_{IN}}\right) \tag{4.20}$$

I_O value is relative to M3 size. Therefore, we sweep the width of transistor M3 from 0.5μm to 3μm as shown in Fig. 4-26 and Fig. 4-27. When the width is 0.5um, the quiescent current is the best case, and the total delay is much smaller than the specification.

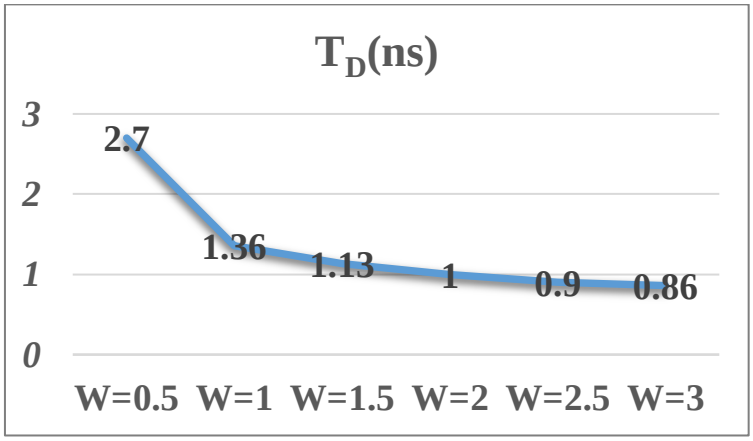

Fig. 4-26 Time delay with the change in the width of transistor M3

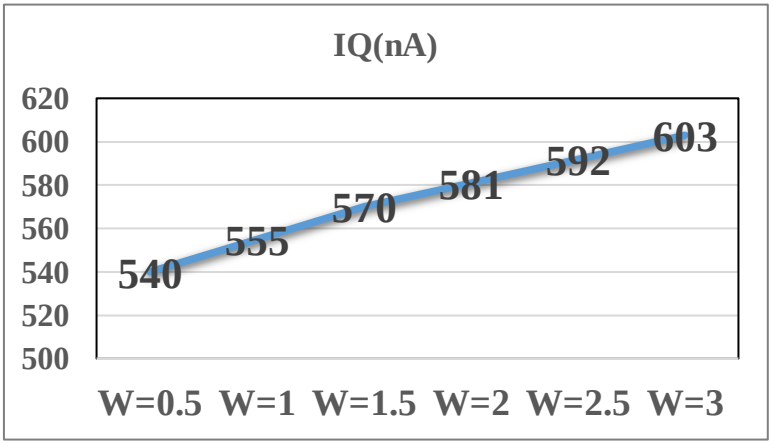

Fig. 4-27 Quiescent current with the change in the width of transistor M3

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The next step, we sweep the width of the latch circuit (M4-M7) and the width of the input pair (M1, M2). Table 4-7 demonstrates minimizing the latch size can make the current consumption smaller, but the input offset becomes larger. Because the large input offset will influence the output voltage regulation, we design the width of the transistors (M4-M7) to 2μm. Table 4-8 shows the delay, current consumption, and input offset corresponding to different input pair sizes.

Table 4-7 Relationship between the width of the latch circuit and other parameters

M4-M7 size (μm)	T_D (ns)	Current consumption (nA)	Input Offset (mV) *pre-sim *Monte Carlo run 300 times
W=1	2	486	2
W=2	2.7	540	1
W=5	3.8	725	1
W=10	5.2	1060	1

Table 4-8 Relationship between the width of the input pair and other parameters

M1 and M2 size (μm)	T_D (ns)	Current consumption (nA)	Input Offset (mV) *pre-sim *Monte Carlo run 300 times
W=4, M=2	2.6	498	2
W=5, M=2	2.7	540	1
W=10, M=2	3.17	780	1

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As a result, the final implementation of the latch-type sense amplifier is shown in Fig. 4-28, and Table 4-9 shows the comparison between the specification and the simulation of the comparator.

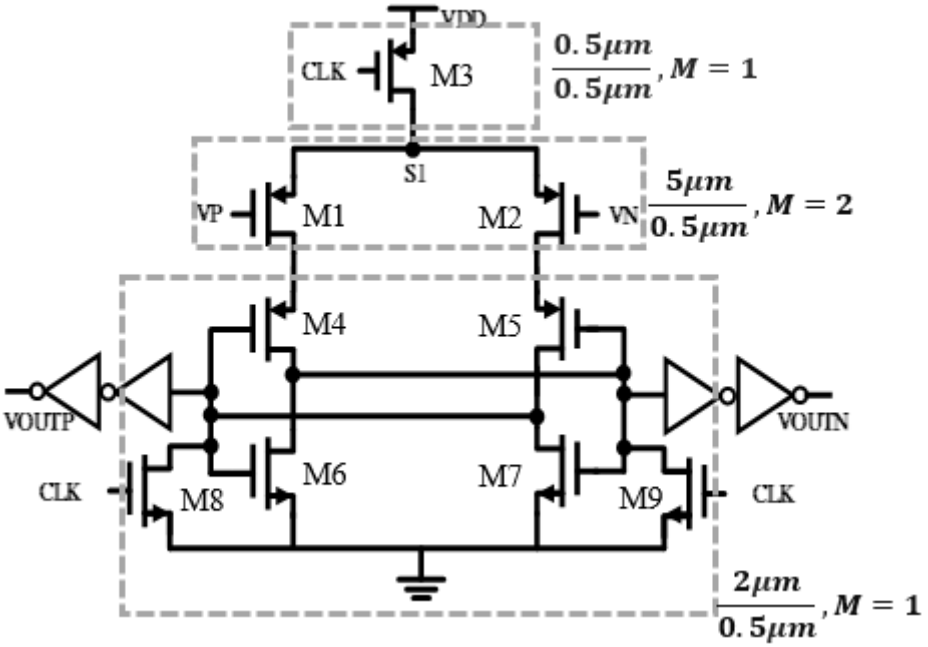

Fig. 4-28 The final size of the transistors (M1-M9)

Table 4-9 Comparison between the specification and the simulation of the comparator

Parameter	Specification	Performance
Supply Voltage	3.3V	3.3V
$V_{in,\,cm}$	1V	1V
Power Budget	<μA@iLoad =10μA	707nA@iLoad =10μA
Propagation Delay	800ns (<1μs)	2.7μs
F_{CLK}	2MHz	2MHz

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4.4.2 Comparing Two Different CPEA Architectures

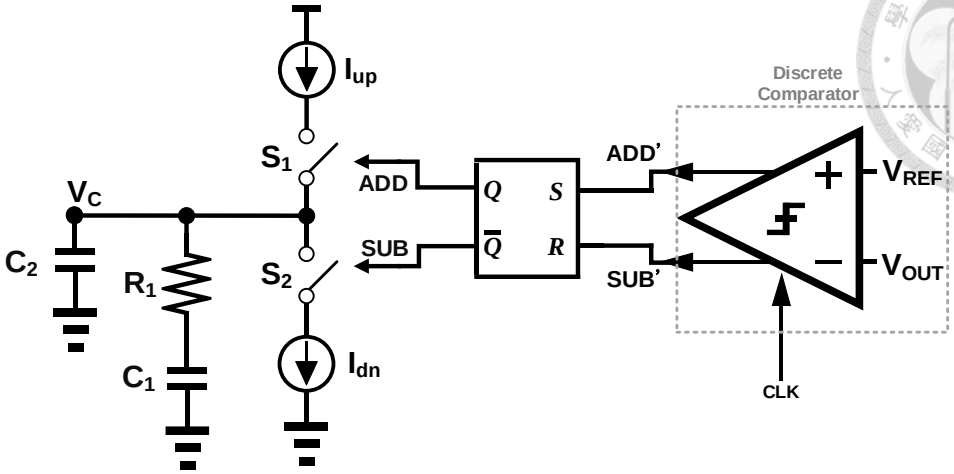

Fig. 4-29 Cicuit diagram of the first version of CPEA

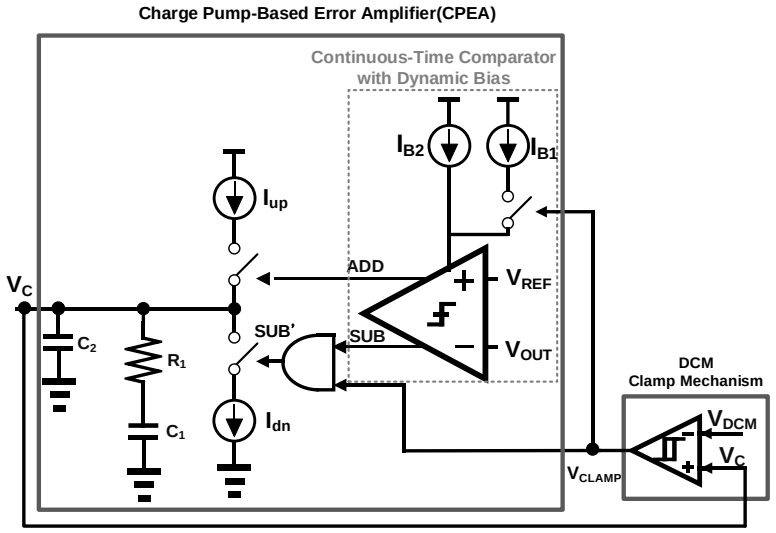

Fig. 4-30 Cicuit diagram of the second version of CPEA

Fig.4-29 and Fig.4-30 show the circuit diagrams of the first version of CPEA and the second version of CPEA, respectively. The comparator design of the second version of CPEA is the same as Section 4.4.3. Under the ultra-light load, the quiescent current of the continuous-time comparator is significantly influenced by the bias current. Thus,

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the dynamic bias controlled by the DCM clamp mechanism can greatly reduce the quiescent current. Under the ultra-light load, the comparator is not in operation for most of the time, so the quiescent current of the second version can be reduced to 350nA, and the DCM clamp mechanism only consumes 38nA. Then, we compared to three different architecture compensators in Table 4-10. Although the current consumption of the first version CPEA is reduced compared to the conventional error amplifier, it is still limited by the fixed frequency clock generator. When the load current is 10μA, the quiescent current consumes about 1μA.

Table 4-10 Comparison between three compensation architectures

	Conventional EA	**Version 1**	**Version 2**
IQ	2.5μA at i_{LOAD} =10μA	1μA at i_{LOAD} =10μA	350nA at i_{LOAD} =10μA
F_{CLK}	N/A	2MHz	N/A
Note	N/A	IQ_{CLK} =35μA	$IQ_{DCM\ Clamp\ Mechanism}$ =38nA

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4.5 Zero-Current Detector

4.5.1 The Delay-Based Pulse Width Control Circuit

Fig. 4-31 Time-domain waveforms of i_L, V_X, and VSS

To realize the DCM, the delay-based pulse width control circuit and a calibration loop are used to implement the zero-current detector in RCCOT control. According to Section 3.5, we need to design an appropriate delay time to turn off the low-side MOS. Fig. 4-31 shows the DCM waveform, where we can calculate the ΔV_X and $T_{delay,DCM}$ values through the following analysis to design a zero-current detector.

First, the peak value of the inductor current, $i_{L,peak}$, is given by

$$i_{L,peak} = \frac{V_{IN} - V_{OUT}}{L} \cdot Ton \tag{4.21}$$

Then, we can get the ΔV_X as below.

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$$\Delta V_X = i_{L,peak} \cdot R_{Nds,on} \tag{4.22}$$

Where the $R_{Nds,on}$ is the on resistance of the low-side MOS. In this work, the $R_{Nds,on}$ is about 145mΩ. Then, if we assume the $R_{Nds,on}$ is constant, ΔV_X equals to 50mV. From (4.22), the optimal delay time can be calculated by (4.23) and (4.24).

$$\frac{dV_X}{dt} = R_{Nds,on} \cdot \frac{di_L}{dt} \tag{4.23}$$

$$T_{delay,DCM} = \Delta V_X \cdot \frac{1}{R_{Nds,on} \cdot \left| \frac{Vo}{L} \right|} \tag{4.24}$$

We can calculate $T_{delay,DCM}$ = 2.3μs and ΔV_X = 50mV. If the resolution of the comparator is 5mV, a delay LSB is designed to 230ns.

In the CCM, the zero-current detector will continue to operate and the delay will be adjusted to the maximum delay time by the calibration loop operation. If the maximum delay time is too short, the low-side MOS will be erroneously turned off at the load transient state during the CCM. With the worst-case design, the maximum delay time should be larger than 6.28μs to properly control the low-side MOS as shown in Fig. 4-32. Therefore, with a delay LSB of 230ns, a 5-bit delay chain is required as shown in Fig. 4-33. The maximum time delay is designed to 7.5μs.

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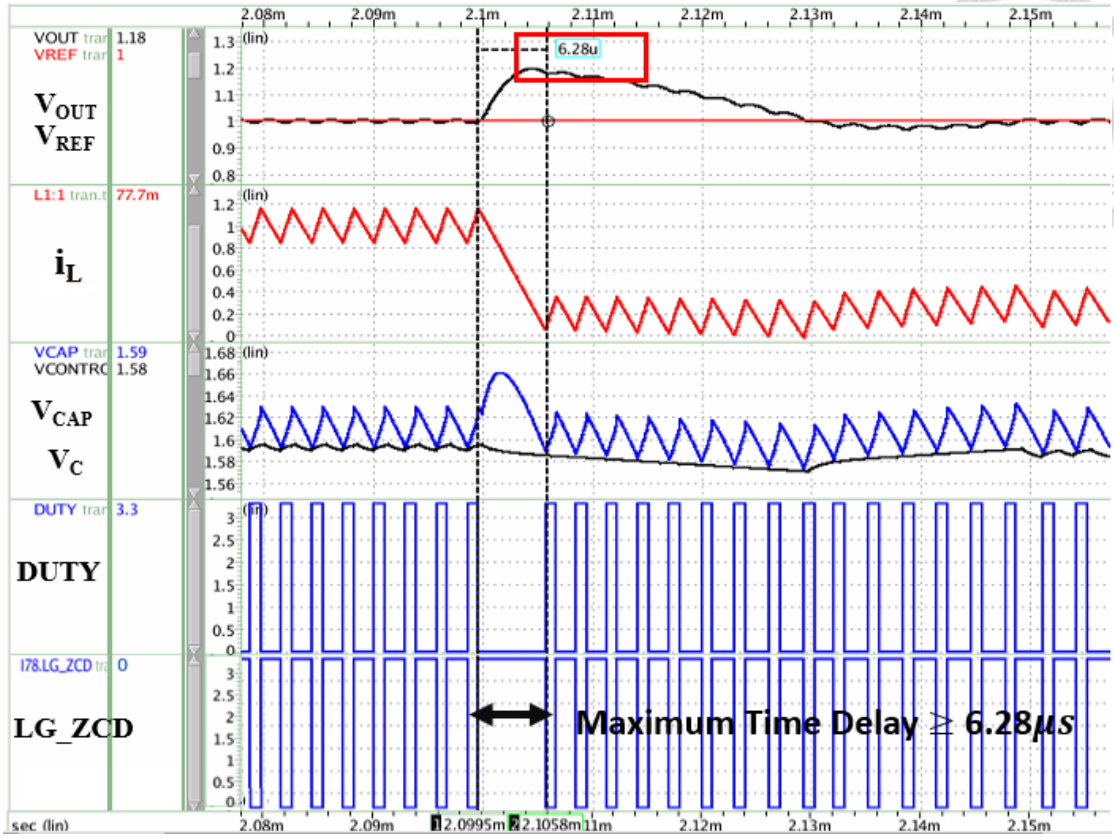

Fig. 4-32 Load transient waveform from heavy load to light load in the CCM

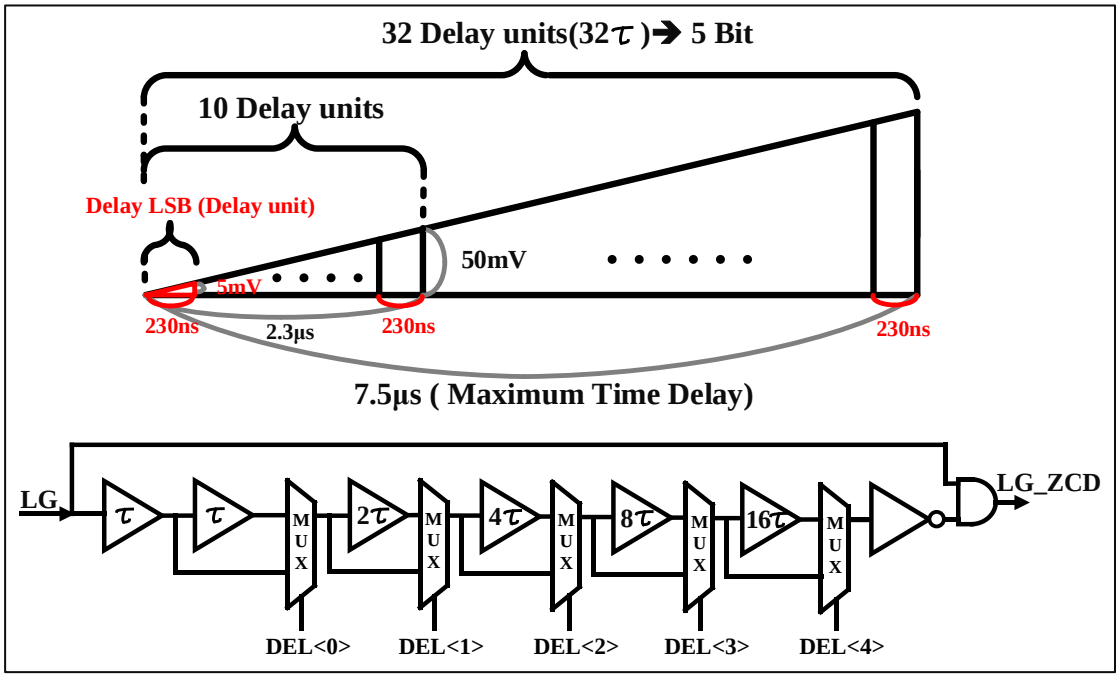

Fig. 4-33 Schematic diagram of delay time design

doi:10.6342/NTU202000931

4.5.2 The Double-Tail Comparator in Calibration Loop

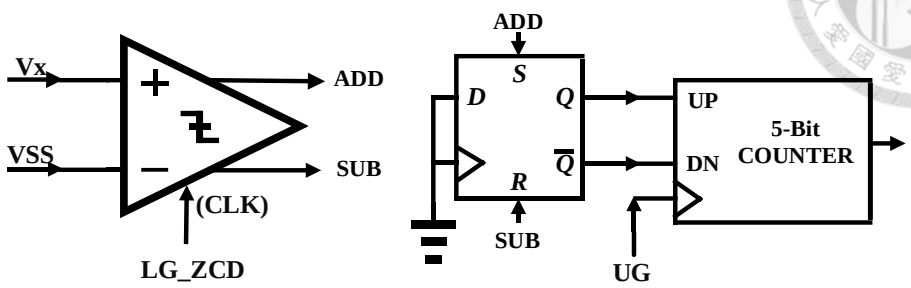

Fig. 4-34 Circuit diagram of the calibration loop

The calibration loop shown in Fig. 4-34 contains a double-tail comparator, a SR latch, and a 5-bit counter. Based on Section 4.6.1, the specification of the double-tail comparator is formulated as below.

Table 4-11 Specification of the double-tail comparator

Parameter	**Specification**
Supply Voltage	3.3V
$V_{in,\,cm}$	0V
Input offset	5mV
Propagation Delay	<100ns
F_{CLK}	20Hz~300kHz

doi:10.6342/NTU202000931

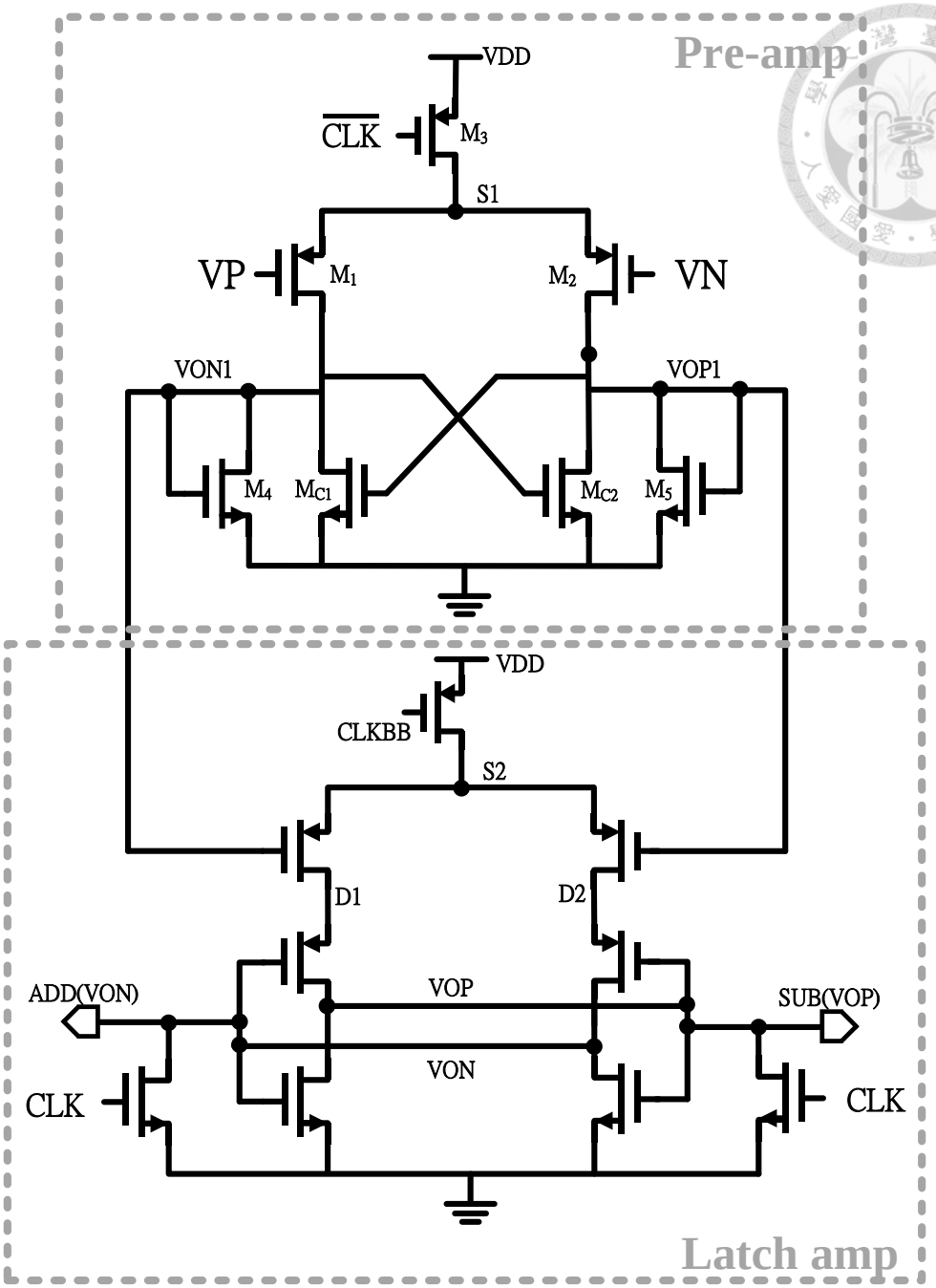

Fig. 4-35 Schematic of the double-tail comparator

Fig. 4-35 shows the schematic of the double-tail comparator. In order to implement a comparator with the low input offset, we added a pre-amplifier as the first stage to minimize the input offset of a latch type sense amplifier, and the design of the latch type sense amplifier is the same as Section 4.5.1. [16]-[18] analyze the effect of the threshold

doi:10.6342/NTU202000931

and current factor mismatches of the controlling transistors (Mc1,2) on the total input-referred offset voltage. According to the analysis, we can find a design rule for the comparator.

(1) Effect of Threshold Voltage Mismatch of MC1, MC2, i.e., $\Delta V_{thC1,2}$:

The differential current due to the threshold voltage mismatch can be given by

$$i_{diff} = g_{mc1,2} \cdot \Delta V_{thc1,2} \tag{4.25}$$

Where $g$mc1,2 is the transconductance of the controlling transistors. So, the input offset voltage due to the Mc1,2 threshold voltage mismatch is obtained as follows

$$V_{IN,OS\_\Delta Vthc12} = \frac{g_{mc1,2} \cdot \Delta V_{thc1,2}}{g_{m1,2}}$$

$$= \frac{\mu_n W_{C1,2} V_{OVC1,2}}{\mu_p W_{1,2} V_{OV1,2}} \cdot \Delta V_{thc1,2} \tag{4.26}$$

Where V_{OV} is the overdrive voltage of the transistor.

(2) Effect of Current-Factor Mismatch MC1, MC2, i.e., $\Delta\beta_{C1,2}$:

To calculate the input offset due to the current factor mismatch of the $M_{C1,2}$, βC1,2 is modeled as a channel width mismatch ΔW, i.e., $\Delta\beta/\beta = \Delta W/W$. The differential current that ΔW generates can be expressed as

$$i_{diff} = \frac{1}{2}\mu_n C_{OX} \frac{\Delta W_{C1,2}}{L}\left(V_{gsC1,2} - \Delta V_{thc1,2}\right)^2 \tag{4.27}$$

Thus, the input offset voltage due to the current factor mismatch is obtained as

doi:10.6342/NTU202000931

$$V_{IN,OS\_\Delta\beta c12} = \frac{i_{diff}}{g_{m1,2}}$$

$$= \frac{\frac{1}{2}\mu_n \Delta W_{C1,2}\left(V_{gsC1,2} - V_{thc1,2}\right)^2}{\mu_P W_{1,2}\left(V_{gs1,2} - V_{th1,2}\right)} \quad (4.28)$$

From (4.26) and (4.28), it can be concluded that the larger the ratio of the input transistor sizes to the controlling transistor sizes, the input offset is effectively reduced. Because the transconductance of the input transistors (gm1,2) is important in amplifying the input differential voltage, it relatively reduces the impact of input offset on input differential voltage. Finally, the size of the transistors in pre-amplifier is shown in Table 4-12.

Table 4-12 Size of the pre-amplifier

Transistor	size
M_1, M_2	$\frac{2\mu m}{0.3\mu m}$, M = 4
M_{C1}, M_{C2}, M_4, M_5	$\frac{2\mu m}{0.35\mu m}$, M = 2
M_3	$\frac{2\mu m}{0.35\mu m}$, M = 1

The post-layout simulation of the input offset in the double-tail comparator is shown in Fig. 4-36, and Table 4-13 shows the comparison between the specification and the simulation of the comparator.

doi:10.6342/NTU202000931

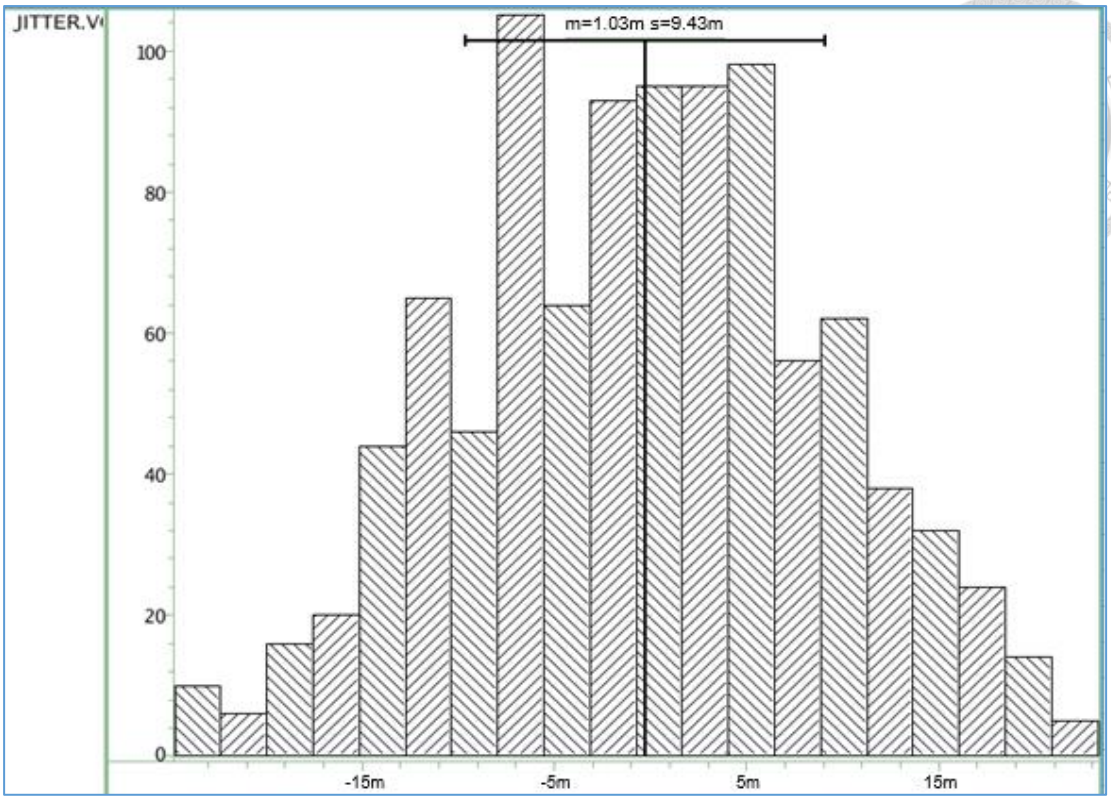

Fig. 4-36 Monte Carlo simulation of the input offset in the double-tail comparator

Table 4-13 Comparison between the specification and the simulation of the comparator

Parameter	Specification	Simulation
Supply Voltage	3.3V	3.3V
$V_{in,\,cm}$	0V	0V
Input offset	5mV	m=1.03mV (s=9.43mV)
Propagation Delay	<100ns	90ns
F_{CLK}	20Hz~300kHz	20Hz~300kHz

doi:10.6342/NTU202000931

The Power breakdown of the zero-current detector is shown in Table 4-14. At a heavy load, the quiescent current of the zero-current detector is 100μA. Because the clock signal (CLK) of the double-tail comparator is controlled by the gate terminal of the low-side MOS, LG_ZCD, the quiescent current can scale with the switching frequency. Thus, the quiescent current becomes 860pA at an ultra-light load.

Table 4-14 Quiescent current of the zero-current detector at different i_{LOAD}

	i_{LOAD}=1A	i_{LOAD}=10μA
Switching frequency	300kHz	19.3Hz
I_Q	100μA	860pA

doi:10.6342/NTU202000931

Chapter 5

Simulation and Measurement Results

The buck converter with the proposed control was fabricated into an IC using Taiwan Semiconductor Manufacturing Company (TSMC) 18-μm technology. This chapter shows the chip photo, layout photo, printed circuit board (PCB) design, simulation results and Measurement results. Table 5-1 shows the circuit parameters for experiment. In the first version of RCCOT, only CCM was implemented, where the load range was from 0.25A to 1.25A. The second chip revised the ripple coupling path circuit and CPEA circuit. In addition, CCM and DCM was implemented, and the load range can cover from 10μA to 1.25A.

Table 5-1 Circuit parameters for experiment

Parameter	**Values**
Technology	180nm CMOS
Input voltage V_{IN}	3.3V
Output voltage V_{OUT}	1V
Switching frequency F_{SW}	300kHz
Output capacitor C_O	$10\mu F$
ESR of output capacitor	8mΩ
L	$6.8\mu H$

doi:10.6342/NTU202000931

5.1 The First Version of RCCOT Controlled Buck Converter

5.1.1 Introduction

Fig. 5-1 presents the chip micrograph and Fig. 5-2 shows the layout photo. The chip area including all bonding pads is 1.192mm^2. The control circuit contains the ripple coupling path, the charge pump-based error amplifier, the digital on/off-time generator, the modulator, the current bias circuit, and the clock generator.

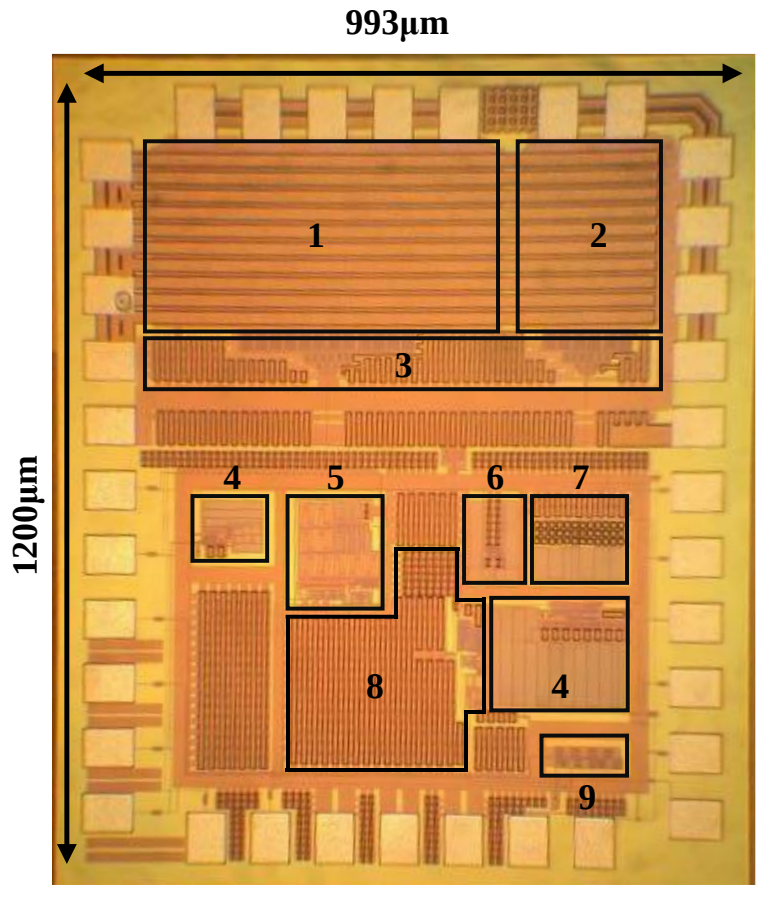

Fig. 5-1 Chip photo with the proposed techniques: (1) power PMOS, (2) power NMOS, (3) gate driver, (4) current bias circuit, (5) digital on/off-time generator, (6) modulator, (7) ripple coupling path (RCP), (8) charge pump-based error amplifier (CPEA), and (9) clock generator

doi:10.6342/NTU202000931

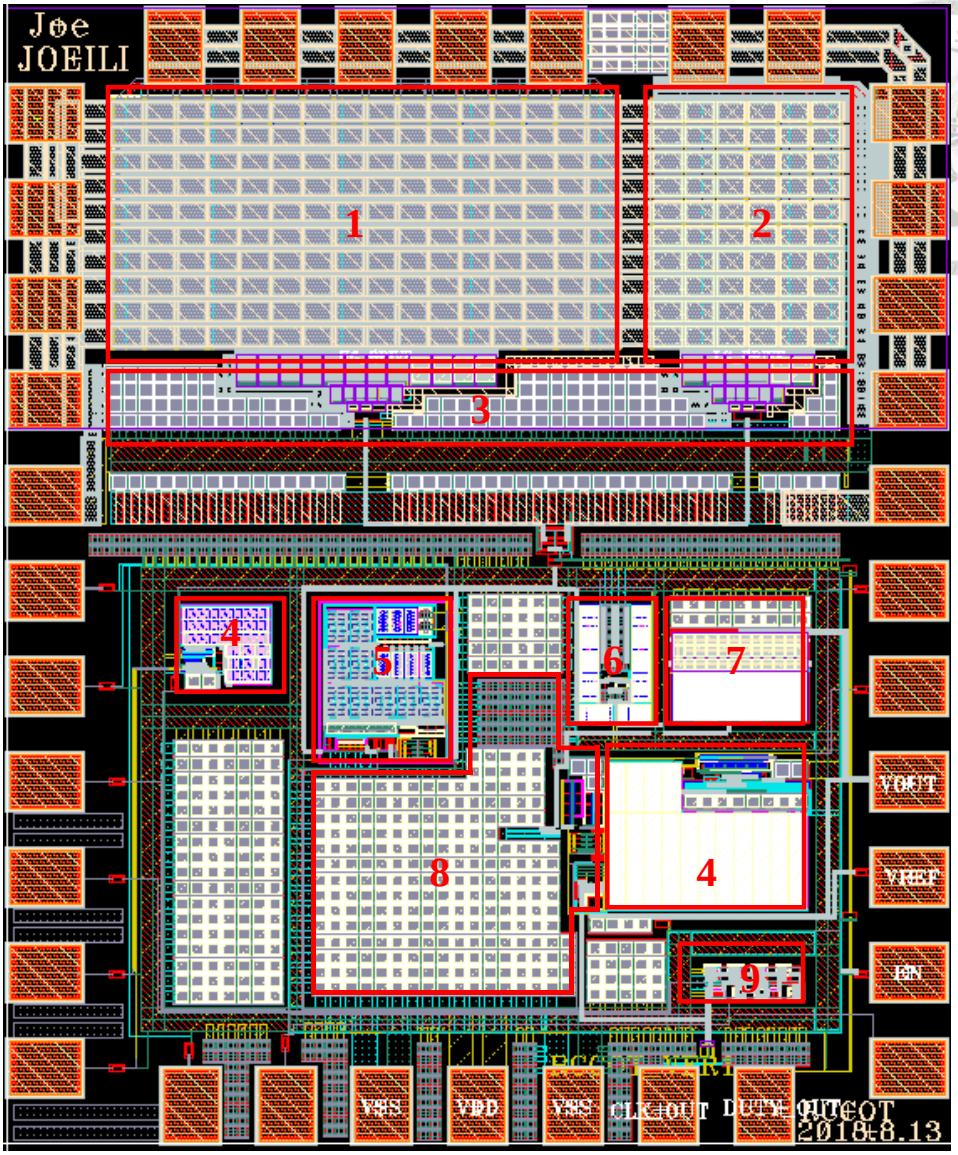

Fig. 5-2 Layout photo with the proposed techniques: (1) power PMOS, (2) power NMOS, (3) gate driver, (4) current bias circuit, (5) digital on/off-time generator, (6) modulator, (7) ripple coupling path (RCP), (8) charge pump-based error amplifier (CPEA), and (9) clock generator

doi:10.6342/NTU202000931

5.1.2 Printed Circuit Board (PCB) Design

Fig. 5-3 shows the experiment PCB board of RCCOT controlled buck converter. The test conditions are as follows. V_{IN} is 3.3 V, V_{OUT} is 1 V, the maximum I_{LOAD} is 1.25 A, the Minimum I_{LOAD} is 0.25 A, F_{SW} is 300kHz, L=6.8 μH, and C_O=10μF. (inductor part number: IHLP5050FDER6R8M01 and capacitor part number: C1206C106K4PACTU) The output capacitor is a ceramic capacitor with the mismatch of +/-20%. The measured ESR is 8mΩ and ESL is 1.5nH. Because there are the coarse-tune and fine-tune control to adjust the on-time pulse, we implemented the dc bias circuit to define the control bit <0: 1> and V_{fine_tune}. The finished board photo is shown in Fig. 5-4.

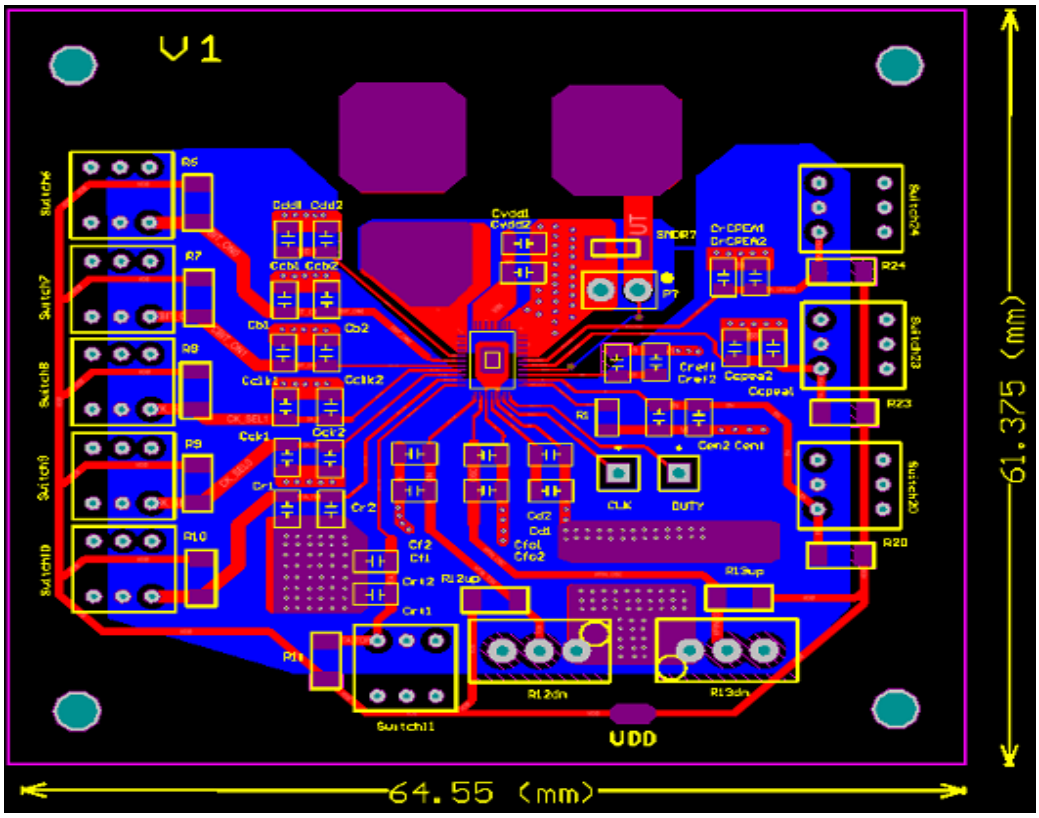

Fig. 5-3 PCB layout

doi:10.6342/NTU202000931

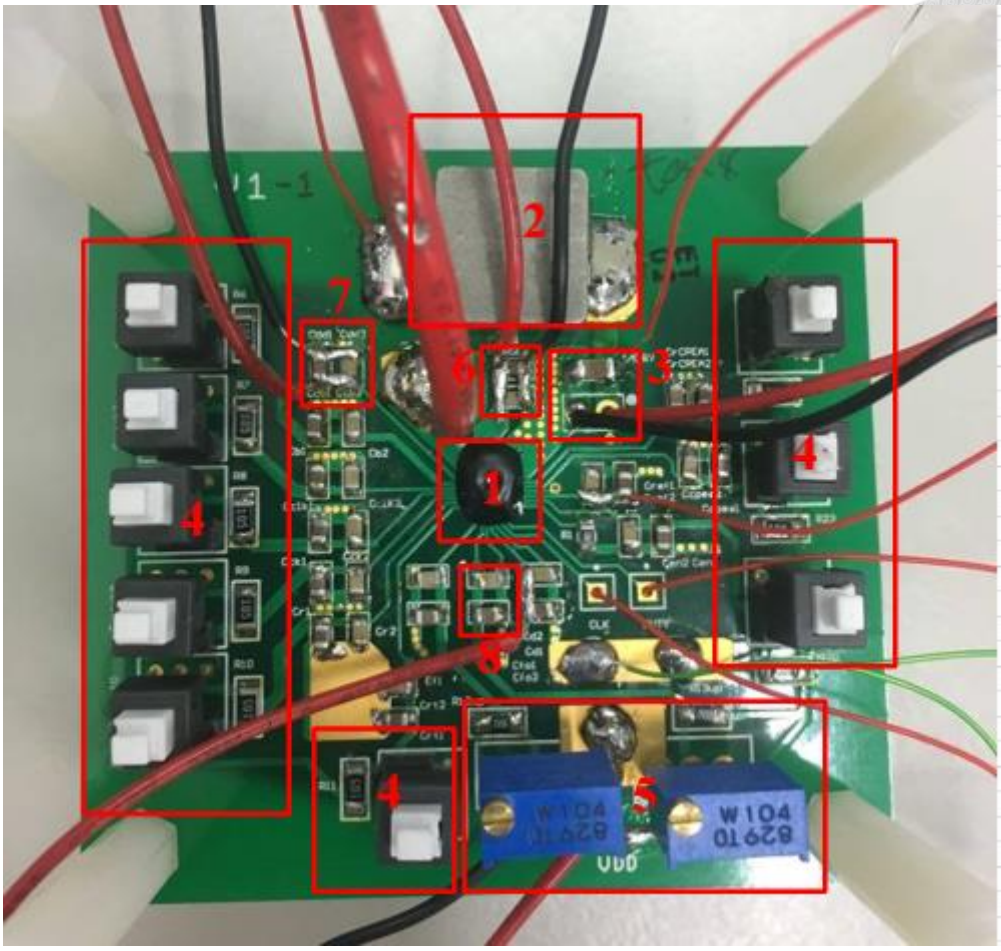

Fig. 5-4 Finished board photo: (1) fabricated chip, (2) inductor, L, (3) ceramic capacitor, C_O, (4) dc bias circuit for the coarse-tune, (5) dc bias circuit for the fine-tune, (6) V_{IN} , (7)VDD_{DRIVER}, and (8)VDD_{CTRL}

doi:10.6342/NTU202000931

5.1.3 Measurement Results

Fig. 5-5 and Fig. 5-6 show the measurement result of the steady-state waveforms at I_{LOAD}=0.25A and 0.5A, respectively. When the load current is 0.25A and 0.25A, the on-time pulse width is 1μs and the switching frequency is 300kHz. The clock frequency is 1.65MHz. The output voltage, $V_{OUT,}$ is 0.98V. However, when the load current is 1A, the system will suffer from the instability as shown in Fig. 5-7.

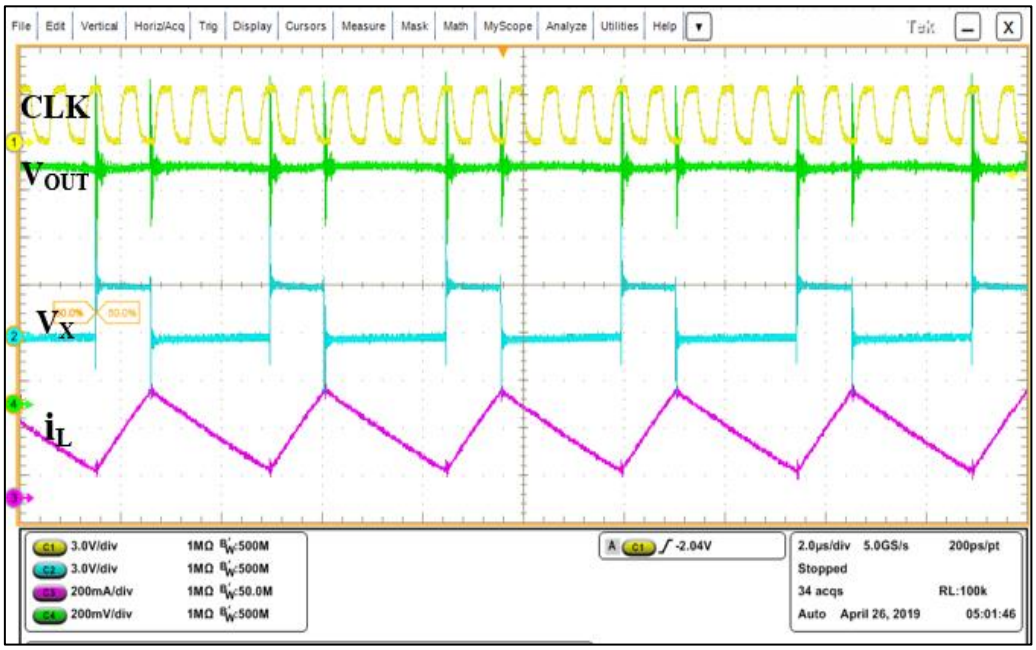

Fig. 5-5 Experimental steady-state waveforms (i_{LOAD}=0.25A)

doi:10.6342/NTU202000931

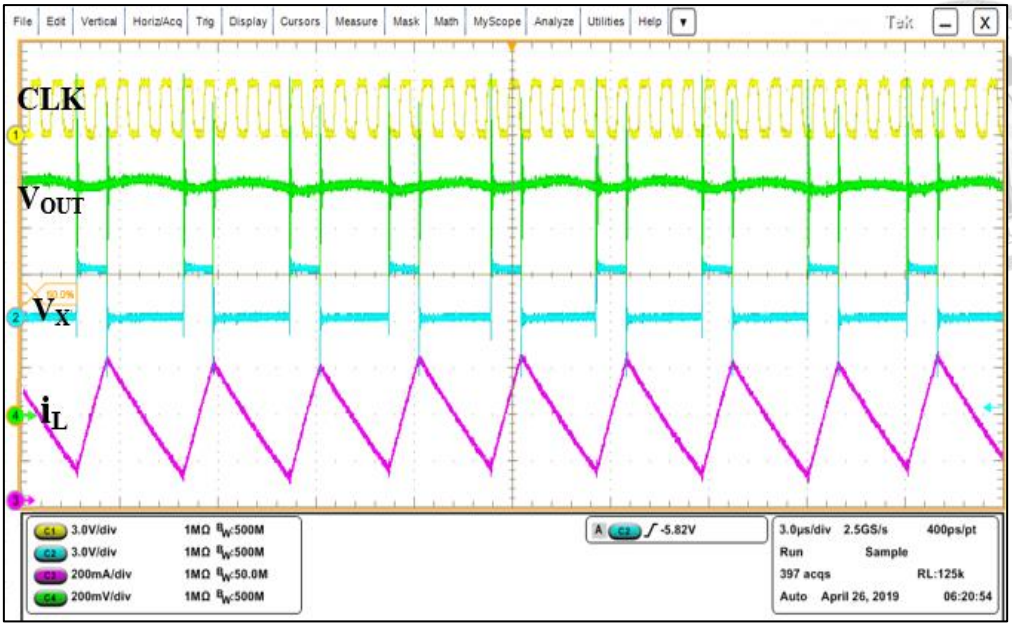

Fig. 5-6 Experimental steady-state waveforms (i_{LOAD}=0.5A)

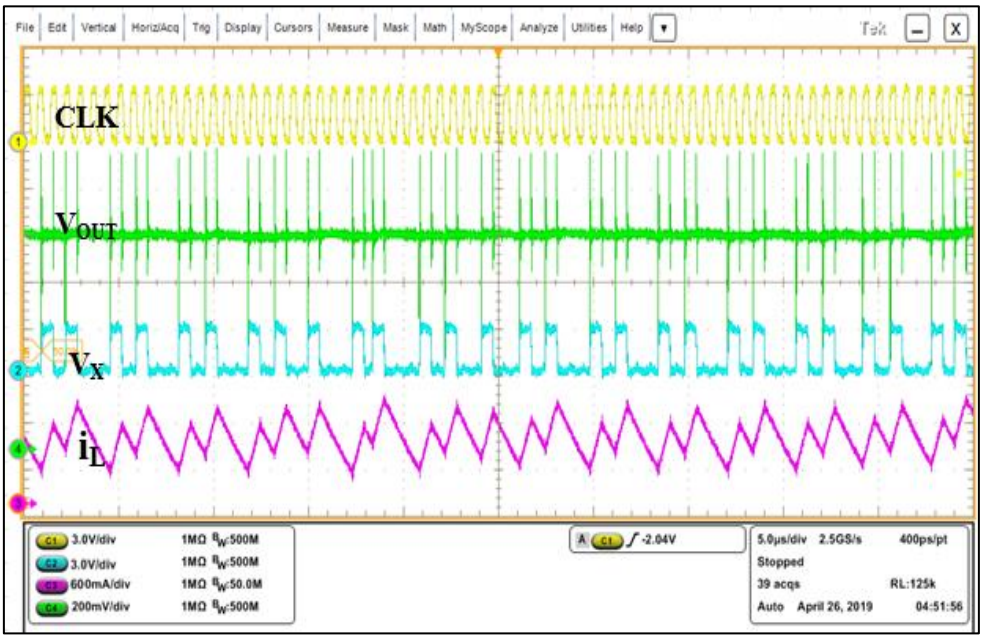

Fig. 5-7 Experimental steady-state waveforms (i_{LOAD}=1A)

Because RCCOT buck converter suffered from the instability explained in Section 4.2, we revised the ripple coupling path circuit by adding an external ramp to improve the instability. The improved simulation waveform will be presented in Section 5.2. Then, we adjusted the on-time pulse from 1µs to 1.7µs, so the switching frequency would be

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changed to 180kHz. The system would be stable because the phase shift between Zco and Z_S is smaller in this case. Fig. 5-8 and 5-9 shows the steady-state waveforms of RCCOT buck converter at iLoad=0.25A and 1A, when the on-time pulse is 1.7μs.

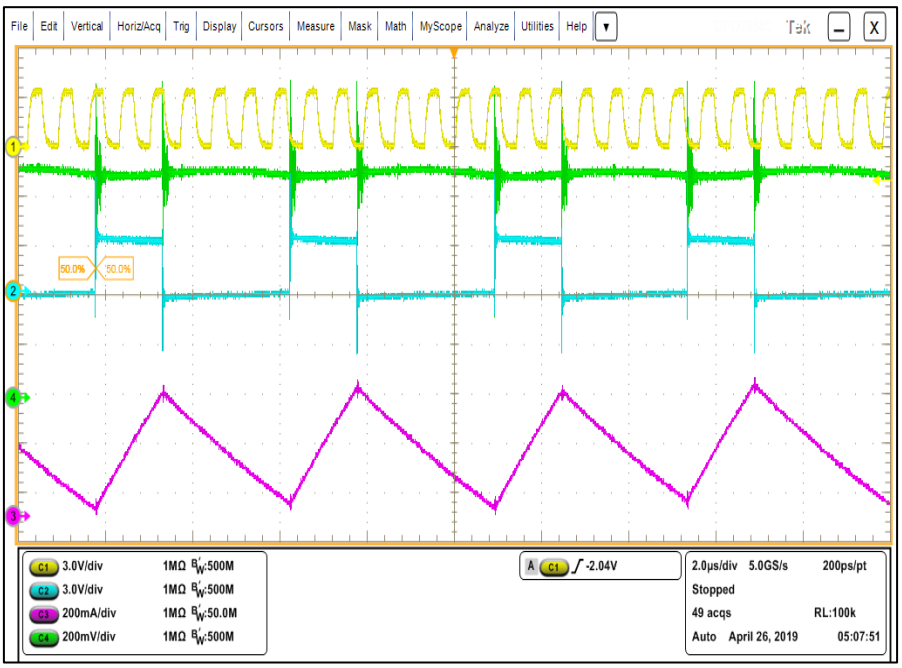

Fig. 5-8 Experimental steady-state waveforms (i_{LOAD}=0.25A and F_{SW}=180kHz)

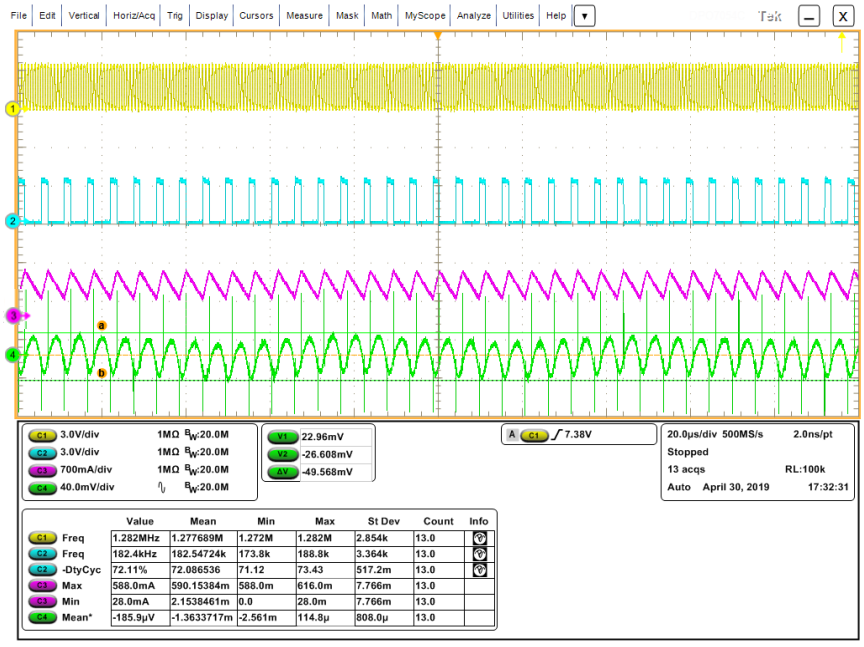

Fig. 5-9 Experimental steady-state waveforms (i_{LOAD}=1A and F_{SW}=180kHz)

doi:10.6342/NTU202000931

Fig. 5-10 shows the simulated load transient waveforms with a 1A/300nA slew rate. Under the step-up load transient, the undershoot of the output voltage is 130mV and the settling time is 43.8μA. Under the step-down load transient, the overshoot of the output voltage is 225mV and the settling time is 76μA.

Fig. 5-11 and Fig. 5-12 show the experimental load transient waveforms with a 1A/300nA slew rate. The transient load step is 1A. Under the step-up load transient, the undershoot of the output voltage is 123mV and the settling time is 45μA which is larger than the simulated value. Under the step-down load transient, the overshoot of the output voltage is 213mV and the settling time is 75μA. The experimental result is similar to the simulated result.

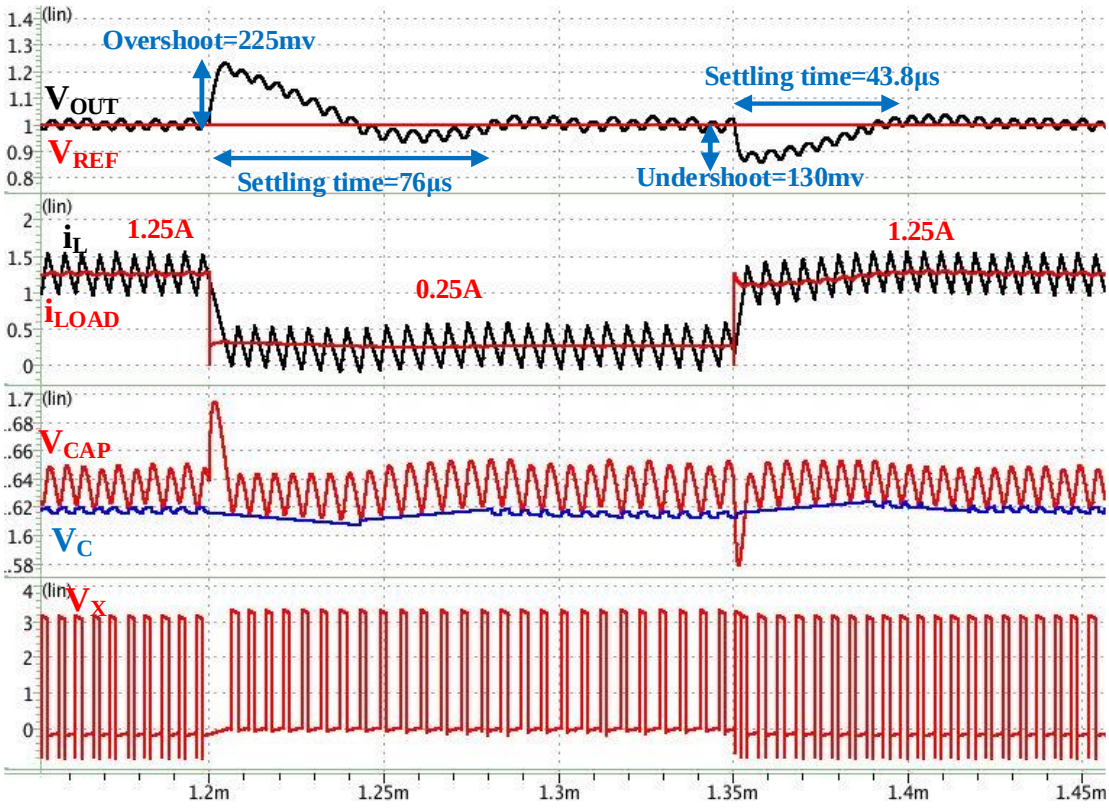

Fig. 5-10 Simulated load transient waveforms

doi:10.6342/NTU202000931

Fig. 5-11 Experimental Step-up load transient waveforms (I_{LOAD}=0.25A-1.25A)

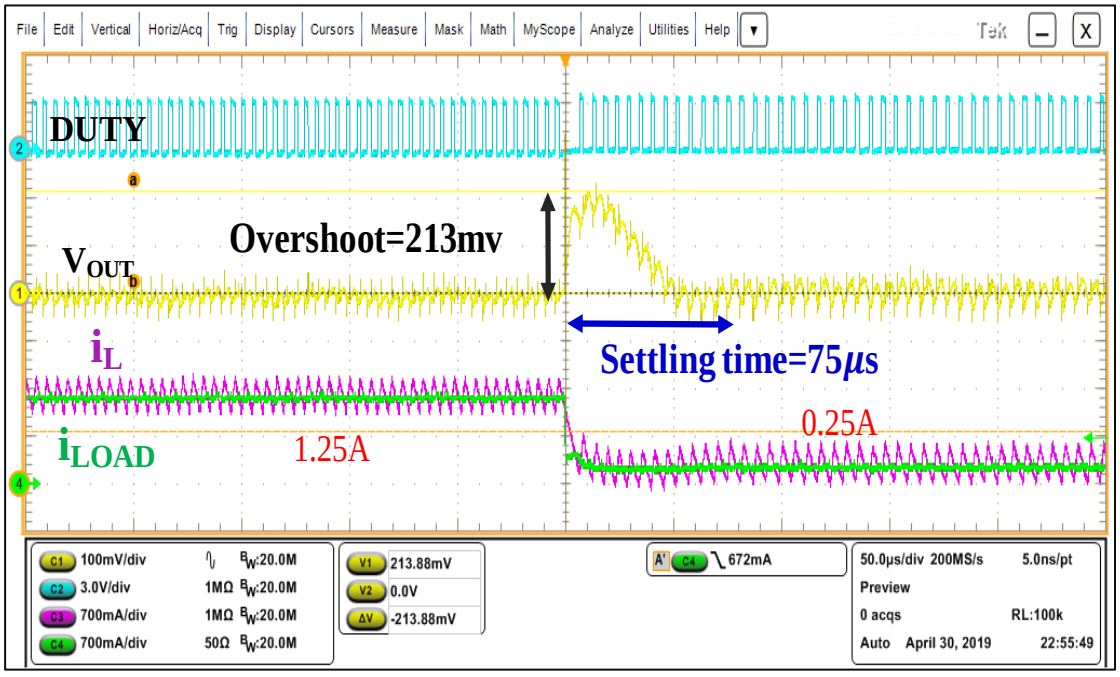

Fig. 5-12 Experimental Step-down load transient waveforms (I_{LOAD}=0.25A-1.25A)

doi:10.6342/NTU202000931

Fig. 5-13 shows the measurement efficiency and Post-sim efficiency of the proposed buck converter. The peak measurement efficiency is 88.5% when the load current is 0.4A in the CCM. The efficiency stays above 80% from 0.2A to 1A loading current. The input current is measured by the digital multi-meter. The input voltage and output voltage are measured directly probes the input voltage and output voltage node at PCB board instead of the value shows on the power supply. The measured output current is applied by the electronic load. Efficiency difference between the measurement and post-sim is about 3% - 4%. The reason for the difference may from the parasitic resistor of the bond wire, PCB trace resistor and the core loss of the inductor will cause the efficiency difference between the measurement and post-sim.

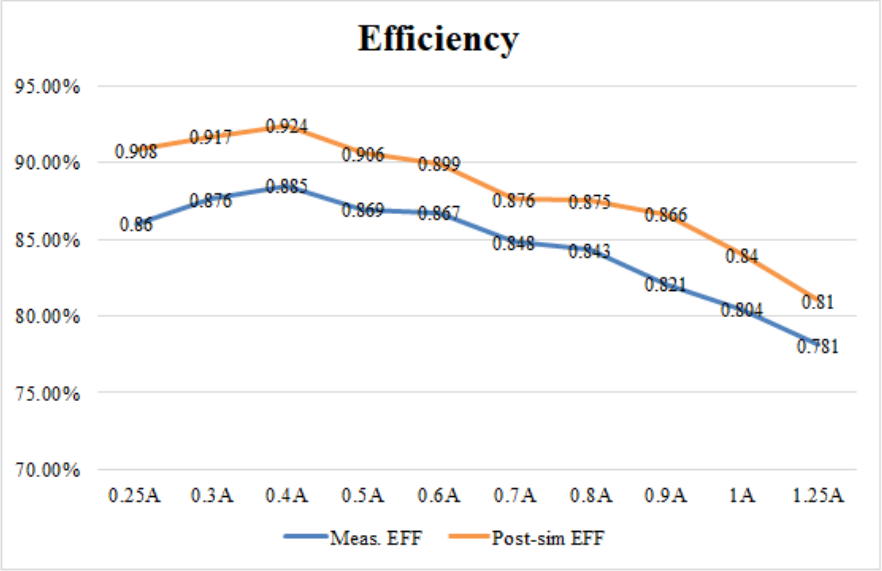

Fig. 5-13 Measurement efficiency and simulation efficiency of the buck converter

doi:10.6342/NTU202000931

5.2 The Second Version of RCCOT Controlled Buck Converter

5.2.1 Introduction

Fig. 5-14 shows the layout photo of the second version of RCCOT. In this version, we added the zero-current detector and the DCM clamp mechanism to realize the DCM for the ultra-light load conditions. Furthermore, the ripple coupling path with the external ramp circuit and the revised CPEA were implemented in this chip. The chip area including all bonding pads is 1.192mm^2.

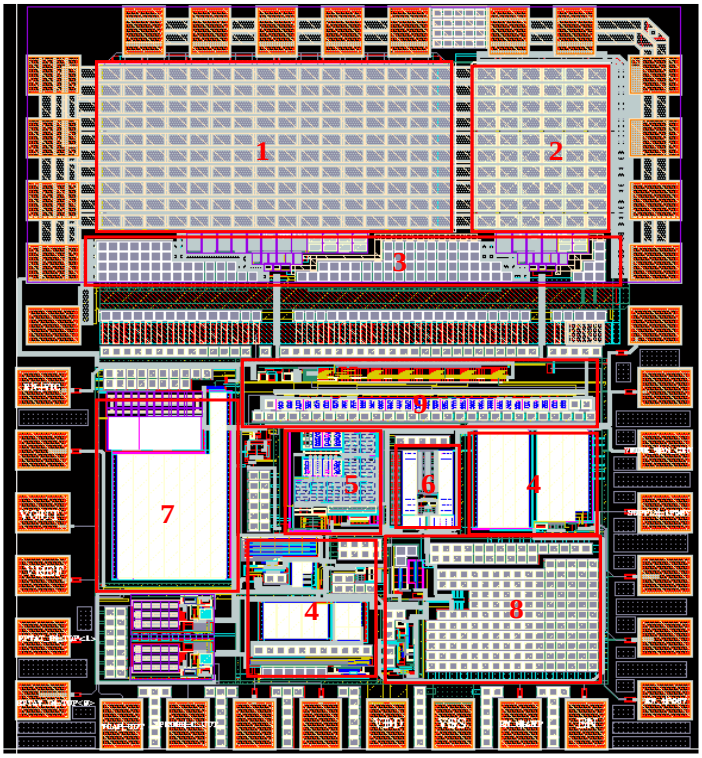

Fig. 5-14 Layout photo with the proposed techniques: (1) power PMOS, (2) power NMOS, (3) gate driver, (4) current bias circuit, (5) digital on/off-time generator, (6) modulator, (7) ripple coupling path with the external ramp circuit, (8) charge pump-based error amplifier (CPEA) with DCM clamp mechanism, and (9) zero-current detector

doi:10.6342/NTU202000931

5.2.2 Simulation Results

Fig. 5-15 to 5-18 show the post-layout simulation of the steady-state waveforms at I_{LOAD}=1A, 250mA, 1mA, and 10μA. Where the post-layout simulation is that the controller is the post-layout circuit, but the power MOS is the pre-layout circuit. This setting is to accelerate the simulation speed.

When the load current is larger than 250mA, the system will operate in the CCM. In this mode, the on-time pulse width is 1μs, the switching frequency is about 300kHz, and the output voltage, $V_{OUT,}$ is regulated to 1V. When RCCOT operates in the DCM, the switching frequency will scale down with the load current. We can observe the switching frequency is 1.8kHz at i_{LOAD}=1mA, and the switching frequency will decrease to 19.6Hz at i_{LOAD}=10μA.

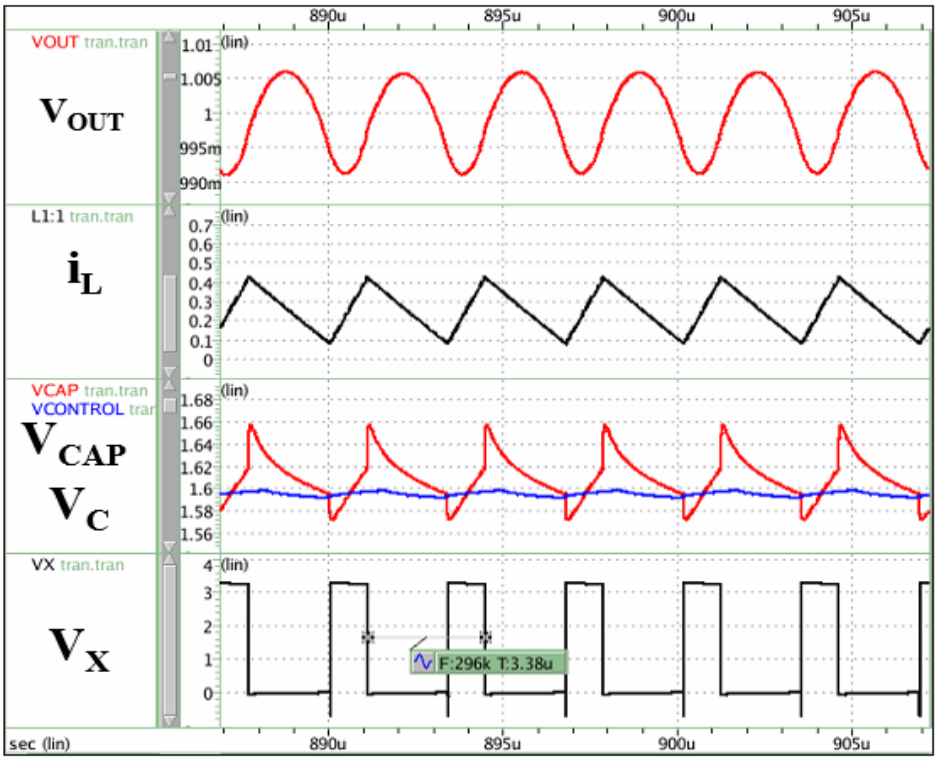

Fig. 5-15 Simulated steady-state waveforms (i_{LOAD}=0.25A)

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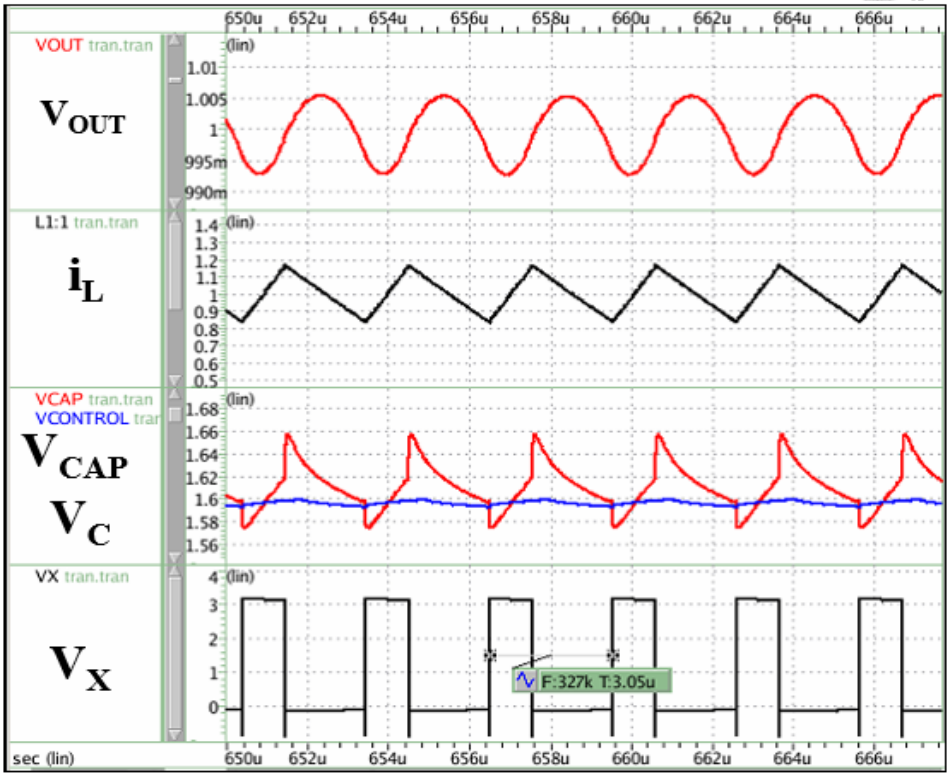

Fig. 5-16 Simulated steady-state waveforms (i_{LOAD}=1A)

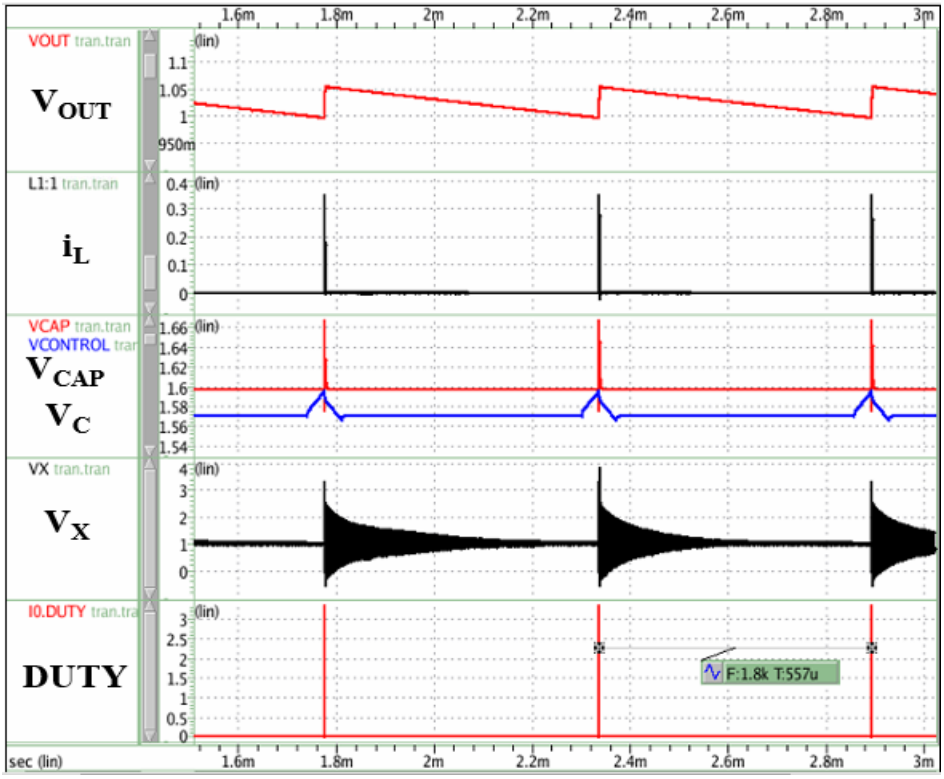

Fig. 5-17 Simulated steady-state waveforms (i_{LOAD}=1mA)

doi:10.6342/NTU202000931

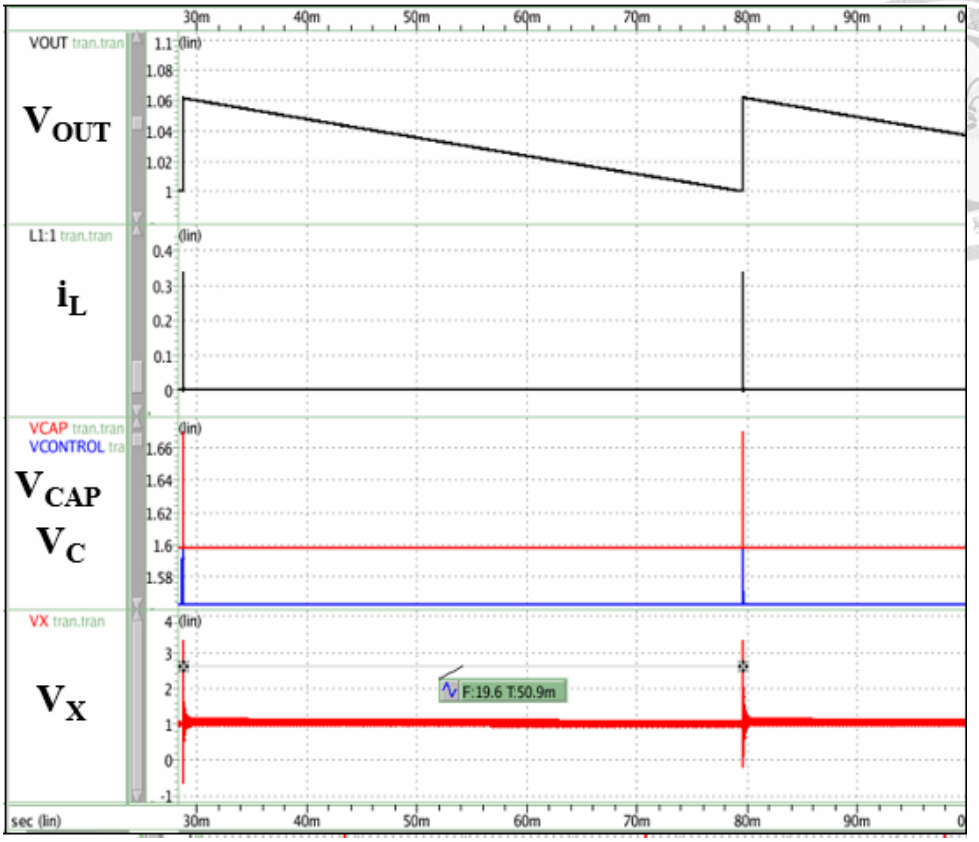

Fig. 5-18 Simulated steady-state waveforms (i_{LOAD}=10μA)

Fig. 5-19 shows the load transient waveforms of the post-layout simulation with a 1A/300nA slew rate. The transient load step is 1A. Under the step-up load transient, the undershoot of the output voltage is 160mV and the settling time is 40μA. Under the step-down load transient, the overshoot of the output voltage is 230mV and the settling time is 50μA. Fig. 5-20 shows the step-down load transient from 0.25A to 10μA. The overshoot and settling time are 20mV and 10μA. In the transitional state, the system will remain operating in the CCM until ZCD searches for the optimal $T_{delay,\,DCM}$ which is explained in Section 3.5 and 4.5.1. Fig. 5-21 shows the step-up load transient from 1mA to 0.25A. The undershoot and settling time are 170mV and 42μA, respectively.

doi:10.6342/NTU202000931

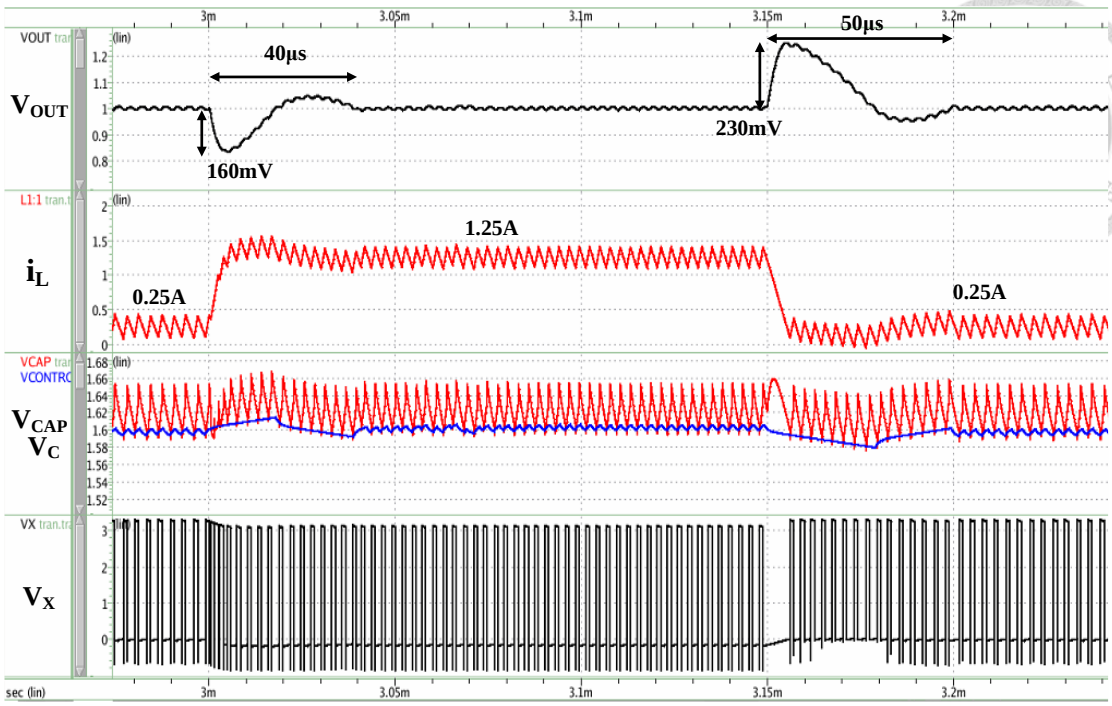

Fig. 5-19 Simulated load transient waveforms (I_{LOAD}=0.25A-1.25A)

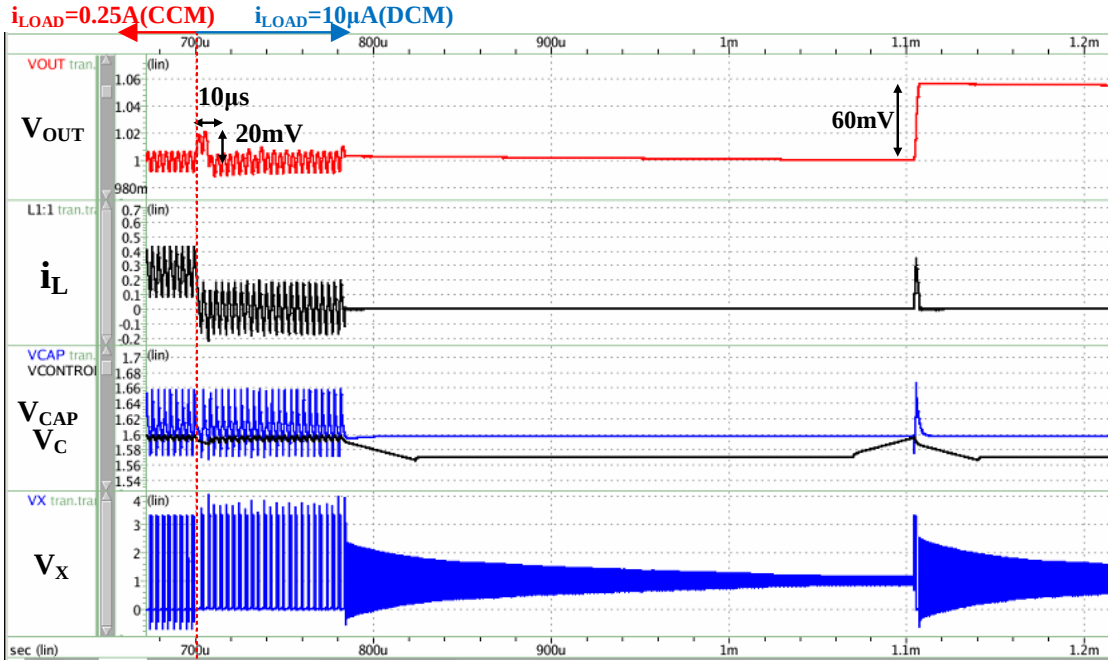

Fig. 5-20 Simulated load transient waveforms from CCM to DCM (I_{LOAD}=0.25A-10µA)

doi:10.6342/NTU202000931

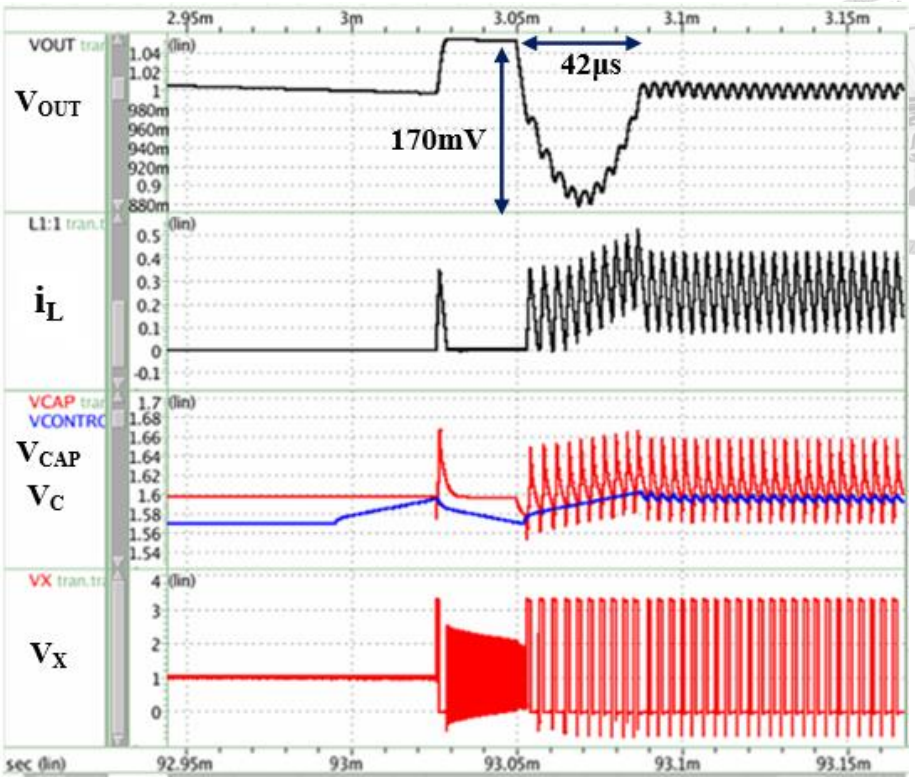

Fig. 5-21 Simulated load transient waveforms (I_{LOAD}=1mA-0.25A)

Table 5-1 demonstrates the power breakdown of the controller under different load conditions. Because of the DCM operation, the digital circuit can scale down with the switching frequency such as the digital on/off-time and the zero-current detector. These two sub-blocks consume only 1.5nA at i_{LOAD}=10μA. In addition, RCP, modulator, and CPEA can also reduce the current to 1.75μA with the switching frequency, but their quiescent current will be limited by the bias current, when the load current drops to 10 μA. Fig. 2-22 shows the efficiency versus the load current by the post-layout simulation. The efficiency all above 85% when the load current is greater than 100μA. Besides, when the load range has to deal with a wide load of 1.25A to 10μA, the

doi:10.6342/NTU202000931

efficiency is 47% at i_{LOAD} = 10μA. Then, Fig. 2-23 illustrates the controller power accounts for about 49% of the total power at I_{LOAD} = 10μA. However, compared to [1], we improved the quiescent current of the controller from 4μA to 3.3μA at the ultra-light load.

Table 5-2 Power breakdown of the control blocks at different load conditions

	i_{LOAD} = 10μA	i_{LOAD} = 100μA	i_{LOAD} =10mA	i_{LOAD} =1A
Current Bias	1440nA	1900nA	3.14μA	3.34μA
RCP	850nA	850nA	850nA	850nA
Modulator	550nA	660nA	5 μA	14 μA
CPEA	350nA	560nA	1.5 μA	6.9 μA
On/off-Time Generator	640pA	8nA	1 μA	12 μA
ZCD	860pA	9nA	9.5 μA	123 μA
Other logic circuit	100nA	300nA	820nA	1.2 μA
Total Control Current	**3.3μA**	**4.3μA**	**22μA**	**161μA**
Note	**DCM**	**DCM**	**DCM**	**CCM**

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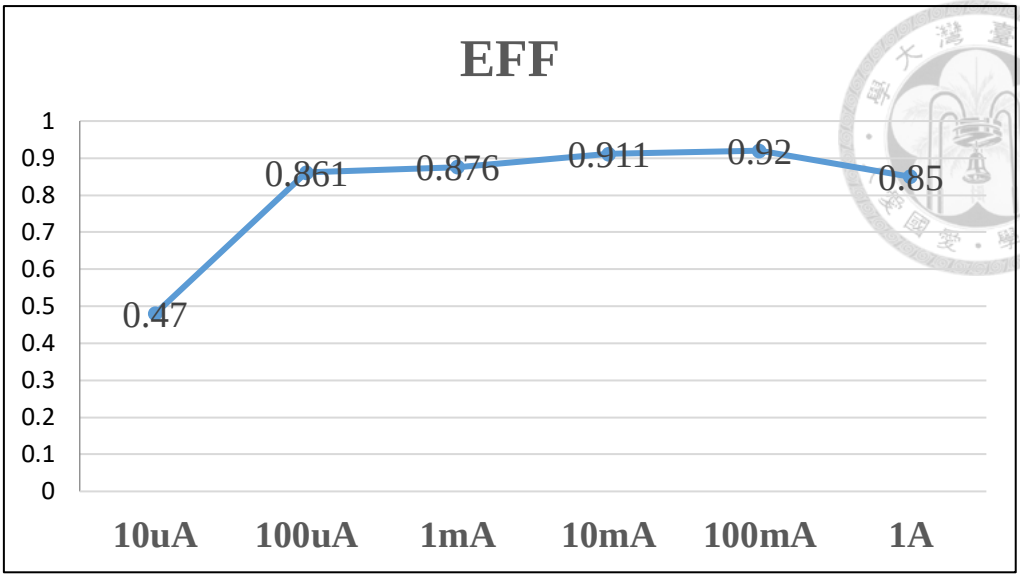

Fig. 5-22 Simulation efficiency of the second version of RCCOT buck converter

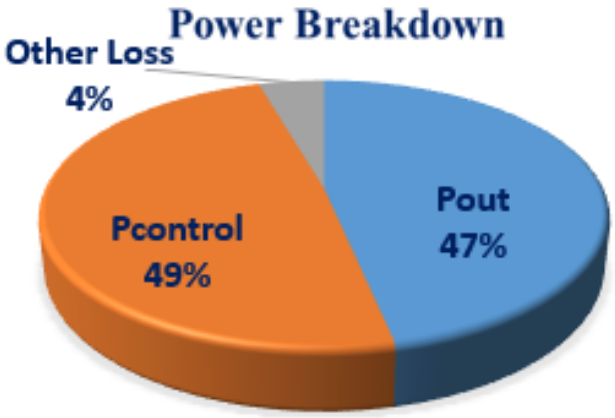

Fig. 5-23 Power breakdown of the second version of RCCOT at i_{LOAD}=10μA

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Chapter 6

Conclusions and Future Works

6.1 Conclusions

The contributions of this thesis are summarized as follows:

1. A ripple coupling constant on-time (RCCOT) control scheme is proposed. It can cope with the load range from 1.25A to 10μA. Furthermore, it achieves the seamless transition from CCM to DCM.
2. The ripple coupling path with the external ramp can solve the instability, and provide a fast-transient loop to handle the load transient response. Its current consumption consumes 850nA.
3. The DCM operation is implemented to improve the light load efficiency in RCCOT control. Because the switching frequency can scale down with the load, the power consumption of the digital on/off-time generator consumes only 640pA at i_{LOAD}=10μA.
4. CPEA with the dynamic bias consumes 350nA at i_{LOAD}=10μA. Because the DCM clamp mechanism can shut down the half bias current of CPEA at the idle time.

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5. Table 6-1 presents a performance comparison with other low-power buck converters. Compared to other low-power buck converters, this work can handle the wide load range from 10μA to 1.25A. Furthermore, when the load current drops from the heavy load to the ultra-light load, the operation mode will automatically change from CCM to DCM. At i_{LOAD}=10μA, the simulated current consumption of the controller is 3.3μA.

Table 6-1 Performance comparison with other state-of-the-art buck converters

	[1] 1SSCC'04	**[2] JSSC'16**	**[19] ISSCC'11**	**[20] JSSC'18**	**This work**
Technology	250nm CMOS	180nm CMOS	45nm CMOS	130nm CMOS	180nm CMOS
V_{IN}	5.5-2.8V	0.55-1V	2.8-4.2V	3.3-1.8V	3.3V
V_{OUT}	1-1.8V	0.35-0.5V	0.4-1.2V	1.2V	1V
L	10μH	4.7μH	10μH	18μH	6.8μH
C_O	47μF	–	2μF	56nF	10μF
Dynamic Load range	$4x10^3$	$2x10^5$	$5x10^3$	$2.65\ x10^4$	$1.25x10^5$
Load Transient $\Delta V_{OUT}/\Delta i_{load}$	12mV /100mA	N/A	10mV /40mA	40mV /2.65mA	170mV /1A
Mode Transition	manual	manual	manual	N/A	automatic
Min i_{LOAD}- Max i_{LOAD}	0.1mA-400mA	100nA-20mA	20μA – 125mA	0.1μA-2.65mA	10μA-1.25A
Quiescent Current	4μA (i_{LOAD}=0.1mA-40mA)	-	2.22μA (i_{LOAD} =20μA)	0.44μ-12.32μA (i_{LOAD}=1μA-2.65mA)	3.3μ-161 μ A (i_{LOAD}=10 μ A -1.25A)
FOM	4.26	-	4	-	45.3
Operation Mode	CCM/ DCM	CCM/ DCM	CCM/ DCM	DCM	CCM/ DCM

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6.2 Future Works

1. The first version of CPEA with a fixed frequency clock generator will limit the quiescent current at light load condition. Thus, if we replace the fixed frequency clock generator by the dynamic frequency which scales with the load, CPEA can greatly reduce the current consumption at light load.
2. The current bias consumes the half power of the controller at the ultra-light load. If the current bias can be shut down completely at the idle time. The conversion efficiency can improve at least 22%.
3. The measurement of the second version has not been included in this thesis. It will be verified and compared with the first chip in the future.
4. Small-signal model of CPEA

doi:10.6342/NTU202000931

References

[1] Jinwen Xiao, A. Peterchev, Jianhui Zhang and S. Sanders, "A 4/spl mu/A-quiescent-current dual-mode buck converter IC for cellular phone applications," in *2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No.04CH37519)*, San Francisco, CA, 2004, pp. 280-528 Vol.1.

[2] P. Chen, C. Wu and K. Lin, "A 50 nW-to-10 mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 523-532, Feb. 2016.

[3] C. Song, "Accuracy analysis of constant-on time current-mode dc-dc converters for powering microprocessors," in *Proc. IEEE APEC*, 2009, pp. 97-101.

[4] R. Redl and J. Sun, "Ripple-based control of switching regulators – an overview," in *IEEE Trans. Power Electron*., vol.24, no. 12, pp. 2669-2280, Dec. 2009.

[5] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulators modules," in *IEEE Trans. Power Electron*., vol.21, no. 2, pp. 346-353, Mar. 2006.

[6] J. Li and F. C. Lee, "Modeling of V^2 current-mode control," in *Proc. IEEE*

doi:10.6342/NTU202000931

APEC, 2009, pp. 298-304.

[7] S. Qu, “Modeling and design considerations of V^2 controlled buck regulator,” in *Proc. IEEE APEC*, 2001, pp. 507-513.

[8] Y. Yan, P. Liu, F. Lee, Q. Li and S. Tian, "V2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, 2013, pp. 117-124.

[9] Jian Li, “Current-mode control: modeling and its digital application,” Ph.D Dissertation of Virginia Polytechnic Institute and State University, Commonwealth of Virginia, Apr. 2009.

[10] S. Pan, C. Chen and C. Tsai, "A novel capacitor current constant on-time controlled buck converter at 4-MHz switching frequency," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 6008-6013.

[11] W. Chen, C. Lin and K. Chen, "Differential zero compensator in delay-ripple reshaped constant on-time control for buck converter with multi-layer ceramic capacitors," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, 2012, pp. 692-695.

doi:10.6342/NTU202000931

[12] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1148-1158, July 2004.

[13] Yogesh Kumar Ramadass, "Energy processing circuits for low-power application," Ph.D Dissertation of Massachusetts Institute of Technology, Jun. 2009.

[14] Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design 2nd Edition.* Oxford University 2002.

[15] D. Johns and K. Martin, Analog Integrated Circuit Design. New York: Wiley, 2000.

[16] C. Manoj Kumar, S. Bharath, K. Anusha and C. Ajay Kumar, "Design of a double tail dynamic comparator for low power and high speed applications," in *International Journal of Scientific & Engineering Research*, Vol. 7, Issue 3, March-2016

[17] S. Aakash, A. Anisha, G. J. Das, T. Abhiram and J. P. Anita, "Design of a low power, high speed double tail comparator," in *2017 International Conference on Circuit, Power and Computing Technologies (ICCPCT)*, Kollam, 2017, pp. 1-5.

doi:10.6342/NTU202000931

[18] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343-352, Feb. 2014.

[19] S. Bandyopadhyay, Y. K. Ramadass and A. P. Chandrakasan, "20μA to 100mA DC-DC converter with 2.8 to 4.2V battery supply for portable applications in 45nm CMOS," in *2011 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 386-388.

[20] Santoro, Francesco, Rüdiger Kuhn, Neil Gibson, Nicola Rasera, Thomas Tost, Helmut E. Graeb, Bernhard Wicht and Ralf Brederlow. “A hysteretic buck converter with 92.1% maximum efficiency designed for ultra-low power and fast wake-up SoC applications.” in *IEEE Journal of Solid-State Circuits* 53 (2018): 1856-1868.

[21] S. Tian, F. C. Lee, P. Mattavelli, K. Cheng and Y. Yan, "Small-Signal Analysis and Optimal Design of External Ramp for Constant On-Time V $^{\bf 2}$ Control With Multilayer Ceramic Caps," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4450-4460, Aug. 2014.

[22] Y. Lin, C. Chen, D. Chen and B. Wang, "A ripple-based constant on-time control with virtual inductor current and offset cancellation for DC power

doi:10.6342/NTU202000931

converters," in *IEEE Transactions on Power Electronics*, vol. 27, no. 10, pp. 4301-4310, Oct. 2012.

[23] S. C. Huerta, A. Soto, P. Alou, J. A. Oliver, O. García and J. A. Cobos, "Advanced control for very fast DC-DC converters based on hysteresis of the cout current," in *IEEE Transactions on Circuits and Systems* I: Regular Papers, vol. 60, no. 4, pp. 1052-1061, April 2013.

[24] S. C. Huerta, P. Alou, J. A. Oliver, O. Garcia, J. A. Cobos and A. Abou-Alfotouh, "A very fast control based on hysteresis of the Cout current with a frequency loop to operate at constant frequency," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, 2009, pp. 799-805.

[25] S. Huang, K. Fang, Y. Huang, S. Chien and T. Kuo, "12.6 Capacitor-current-sensor calibration technique and application in a 4-phase buck converter with load-transient optimization," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2016, pp. 228-229.

[26] Y. Li, C. Chen and C. Tsai, "A constant on-time buck converter with analog time-optimized on-time control," in *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3754-3765, April 2020.

doi:10.6342/NTU202000931

[27] S. Pan, “A novel capacitor current constant on-time controlled buck converter with a dynamic on-time generator,” Master Dissertation of National Taiwan University, Dec. 2018.

[28] W. Yang *et al*., "A constant on-time control DC–DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," in *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6187-6198, July 2018, doi: 10.1109/TPEL.2017.2746659.

[29] Ching-Jan Chen, "Power Electronics and Integrated Circuit Control: Switch Realization and Efficiency," Course Slide of National Taiwan University, Spring, 2018.

doi:10.6342/NTU202000931