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碩士論文

Graduate Institute of Communication Engineering
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Master Thesis

應用於 60 GHz 之雙向傳輸波束成型器與無開關雙向放大器之設計

Design of 60 GHz Bidirectional Beamformer and Switchless Bidirectional Amplifier

葉光聖

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中文摘要

本論文的研究主題為無開關雙向放大器與其在雙向波束成型系統的應用。論文首先說明雙向傳輸系統在通訊系統中的優勢，在雙向傳輸系統中，最關鍵的元件為雙向放大器。傳統的雙向放大器需要使用兩個單獨的放大器與開關來實現，然而多餘的開關會造成額外的損耗與占用面積。本論文提出兩個使用無開關架構的雙向放大器與一個雙向波束成型器晶片，藉由無開關與雙向的設計，降低訊號的損耗與晶片面積。

第一個雙向放大器實現在 90 奈米金氧半場效電晶體製程。在應用頻帶 57-66 GHz 內，接收模式的增益大於 18.2 dB，雜訊指數小於 8 dB，直流功耗為 15.3 mW。在發射模式下，線性增益大於 13.5 dB，直流功耗為 46 mW。在 60 GHz 時，1 dB 增益壓縮時的輸出功率為 3.6 dBm，飽和輸出功率為 6.5 dBm，最大附加功率效率為 7.3%。整體電路佈局面積為 0.44 mm^2。第二個雙向放大器實現在 40 奈米金氧半場效電晶體低功耗製程。在應用頻帶 52-62 GHz 內，接收模式的小訊號增益大於 10.1 dB，雜訊指數小於 8 dB，直流功耗為 22.3 mW。在發射模式下，線性增益大於 13.4 dB，直流功耗為 49.5 mW。在 55 GHz 時，1 dB 增益壓縮時的輸出功率為 2.7 dBm，飽和輸出功率為 9.7 dBm，最大附加功率效率為 8.5%。整體電路佈局面積為 0.21 mm^2。比起第一個雙向放大器，此電路使用差動架構降低了對旁路電容的面積需求，與使用變壓器實現了小面積的匹配網路，晶片面積可以更進一步地縮小。此外，因使用差動放大器與變壓器功率結合，輸出的功率與附加功率效率也能進一步地提升。比起已發表的文獻，本論文提出的兩個無開關雙向放大器為首次使用矽基製程實現在 60 GHz 的應用。其中 40 奈米版本的雙向放大器更具有最小的晶片面積。

藉由使用 40 奈米的雙向放大器，我們實現了一個可應用在手持裝置的雙向傳輸波束成型器晶片。藉由與四個獨立的四單元天線陣列搭配，此晶片可將收發機的訊號傳送至(接收從)選定的 16 個波束方向，以達到全向收發的功能。藉由雙向架構，此晶片上的所有被動元件與輸入輸出埠在傳送與接收模式皆可共用。此外，也因為 40 奈米版本的雙向放大器有相當小的晶片面積，此控制晶片可以縮小到 2.9 mm^2。此晶片使用金氧半場效電晶體製程，避免了異質晶片的整合；而縮小化的電

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路面積能有效改善在大數量相位陣列中，過大的輸入輸出連接數造成封裝的困難。

關鍵字：雙向放大器、雙向收發機、相位陣列、波束成型、金氧半場效電晶體、60 GHz

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ABSTRACT

The research topics of this thesis are switchless bidirectional amplifier (BDA) and its application in the bidirectional beamforming system. First, the advantages of bidirectional system in the communication are illustrated. In the bidirectional system, the most critical component is the BDA. Conventional BDAs are realized by two unidirectional amplifiers with switches. However, the switches produce extra loss and occupy large chip area. This thesis presents two switchless BDAs and a beamformer which built by the BDAs. By using the switchless topology, the loss and the chip size are minimized.

The first BDA is realized in 90-nm CMOS process. From 57 to 66 GHz, in receiving mode, the gain is above 18.2 dB and the noise figure is below 8 dB, with 15.3 mW power consumption. In transmitting mode, the linear gain is above 13.5 dB with 46 mW power consumption. At 60 GHz, output 1 dB compression point (OP_{1dB}) is 3.6 dBm, saturation output power (P_{sat}) is 6.5 dBm with peak PAE of 7.3%. The chip size is 0.44 mm^2.

The second BDA is realized in 40-nm low power CMOS process, with the transformer-coupled matching network and neutralization technique. From 52 to 62 GHz, in receiving mode, the gain is above 10.1 dB and the noise figure (NF) is below 8 dB, with 22.3 mW power consumption. In transmitting mode, the linear gain is above 13.4 dB, with 49.5 mW power consumption. At 55 GHz, the output 1 dB compression point (OP_{1dB}) is 2.7 dBm, saturation output power (P_{sat}) is 9.7 dBm with peak PAE of 8.5%. The chip size is 0.21 mm^2. Comparing with the first BDA, the chip size is reduced due to elimination of bypass capacitors in differential topology, and compact transformers as the matching networks. In addition, the output power and PAE are enhanced by using the differential power combining. Comparing with published works, the two BDAs are the

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first switchless BDA realized on Si-based process for 60 GHz application, and the 40-nm BDA demonstrate the minimum chip size.

By using the 40-nm BDA, a bidirectional beamformer which applied in the high speed communication of the mobile devices is designed. Incorporated with four separated 4-element (4×4) antenna arrays, the beamformer supports 16-beam directions. By using the bidirectional architecture, all the passive components and I/O are shared in the transmitting and the receiving paths to minimize the chip size. Moreover, due to the compact size of the BDAs, the system chip is compact as 2.9 mm^2. With the CMOS process and the minimized circuit size in the large-scale phased array, the reliability issue in high I/O connected package and heterogeneous integration can be solved.

Index Term – Bidirectional amplifier, bidirectional transceiver, beamforming, phased array, CMOS, 60 GHz.

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Chapter 1 Introduction

1.1 Background and Motivation

Phased array has been widely used in modern communication system. In order to improve the directivity and to reduce the path loss of the high-frequency carrier wave, the element quantity in the phased array has been raised in recent years. For example, a basic phased array requires at least 8 elements [1], as shown in Fig. 1.1. In high power application, it requires up to 256 elements [2], as shown in Fig. 1.2. For most of the applications, the transmitting and receiving functions are needed in phased array, separated front-end blocks for uplink and downlink are necessary. However, the large quantity of circuit blocks increases the chip area, dc power consumption, and the cost. Conventional front-end transceivers are consisted of separated transmitter (Tx) and receiver (Rx) blocks, and are designed for connecting to individual antennas. It has the advantages of optimized design for uplink and downlink, and flexible application for frequency-division duplexed (FDD) system or time-division duplex (TDD) system. However, the large physical size of the elements becomes the restriction on the limited chip area when the large quantity of circuit blocks is concerned.

Bidirectional transceivers or half-duplexed transceivers [3]-[5] are designed for amplifying and modulating the signal in two opposite paths. They are sharing all the passive components including the antennas, as shown in Figs. 1.3 and 1.4. In order to achieve the bidirectional operation, all the components must be reciprocal networks, like most non-magnetics passive components (e.g., phase shifter, Butler matrix, passive mixer, switch, etc.) However, the active components, such as power amplifier (PA) and low noise amplifier (LNA), are not reciprocal. The bidirectional amplifiers (BDA) are designed for

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this purpose. Instead of the individual PA and LNA, the BDA operated bidirectionally.

In fact, the BDA is the most critical component in the bidirectional transceiver, because it amplifies the signal in two opposite directions as desired. It has also been widely used in different aspects of communication system, from wireline [6] to wireless system [3]-[5], among digital [7], analog [8], and RF signals.

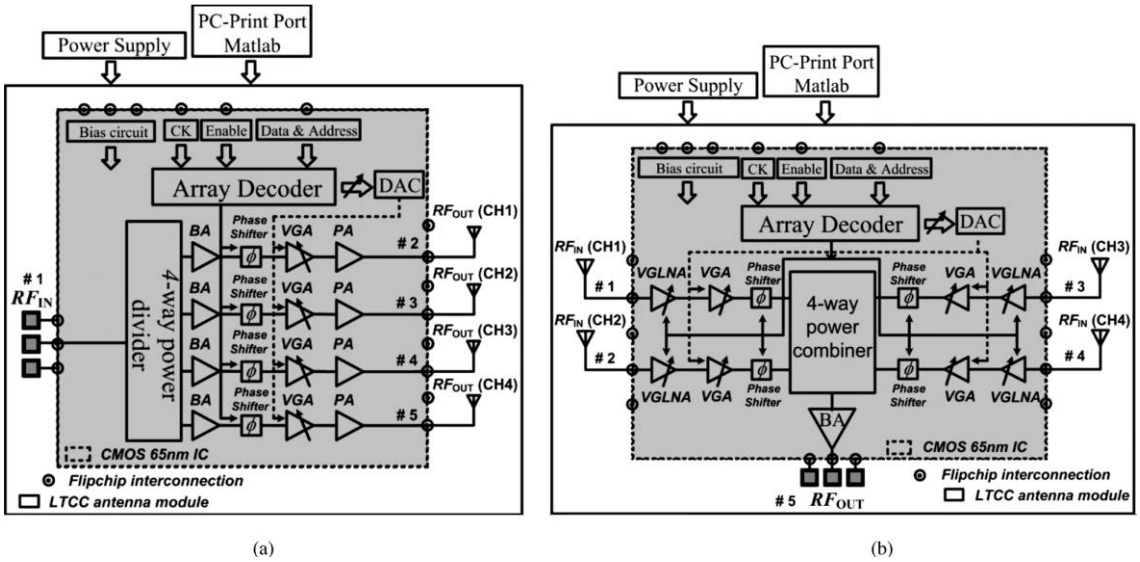

Fig. 1.1. 8-element (4T4R) phased array [1].

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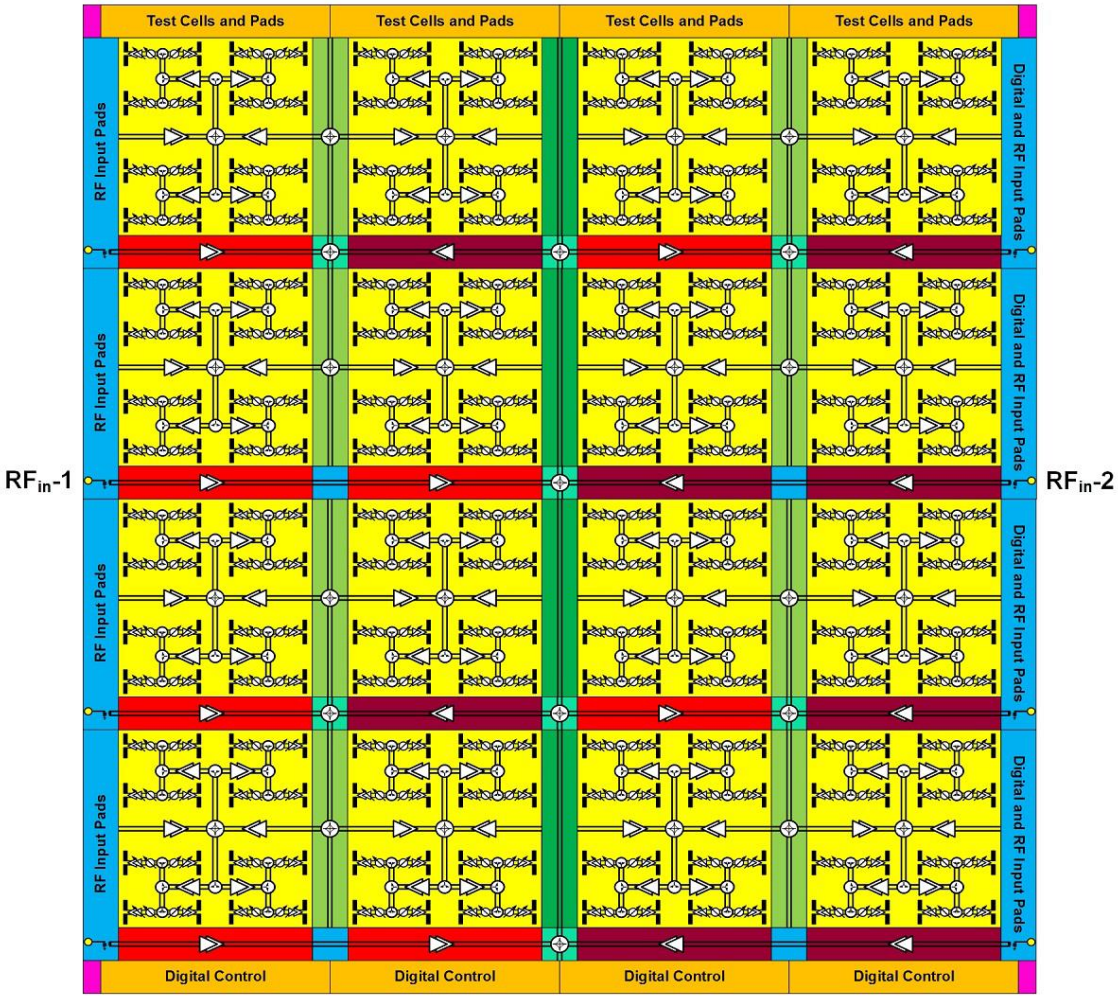

Fig. 1.2. The 256-element phased array [2].

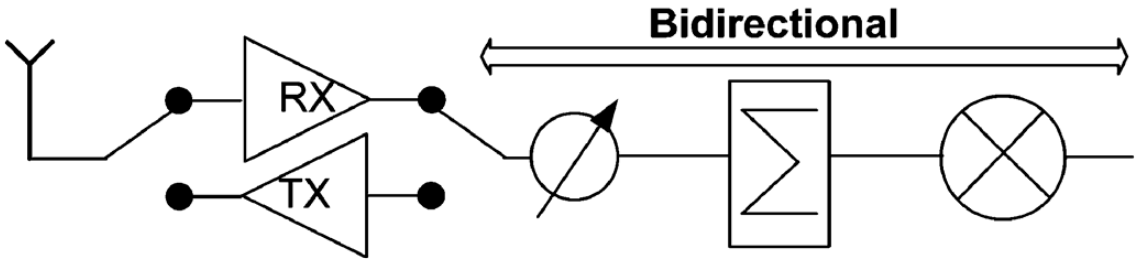

Fig. 1.3. Bidirectional transceiver [3].

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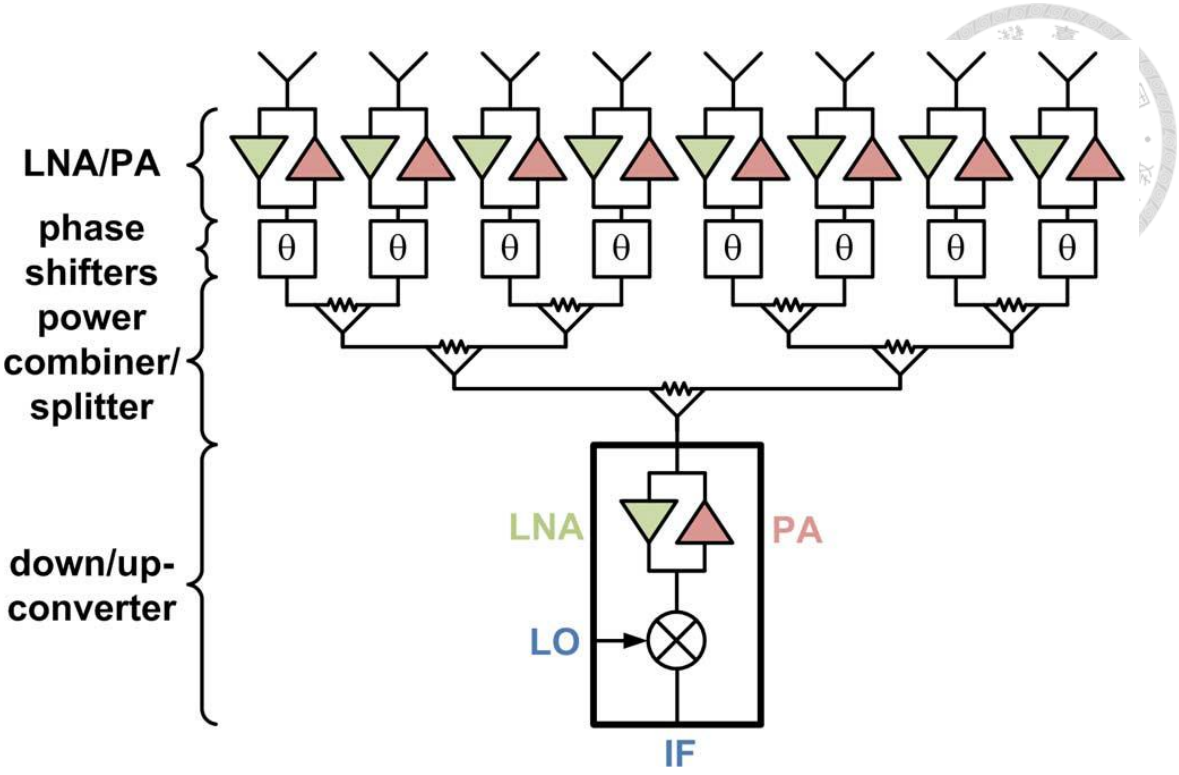

Fig. 1.4. Phased array built by bidirectional front-end blocks [4].

1.2 Literature Survey

The BDAs can be classified into full-duplex and half-duplex, which are applied in FDD and TDD system, respectively.

The full-duplex BDA amplifies the signal in two opposite directions simultaneously. However, the stability is the most critical concern due to the gain loop forming the positive feedback. In order to avoid the oscillation, the isolation network is necessary. The circulator is the ideal functional block for this purpose. Conventional circulator is realized by the ferromagnetism material, which has the properties of low loss and high power capability. However, it is large in size and incapable to be integrated on chip. For the full-duplex application, the quasi-circulator is sufficient, thus the active circulator is a possible solution for integrated-circuit design. The CMOS quasi-circulators have been

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developed in recent years [9]-[11]. However, the active circulators suffer from high loss, low power capability, and large layout size.

To avoid the drawbacks of the circulator, another topology built by the reflection-type amplifier is proposed [12]. It contains two reflection-type amplifiers and a 3-dB 90º coupler, as shown in Fig. 1.5. The coupler helps the incident signal to be coherently combined at the output port. Ideally the gain of the BDA is equal to the reflection-type amplifier. However, the gain and isolation are sensitive to the imbalance of the two reflection-type amplifiers. Besides, the gain and bandwidth are restricted by the single-stage transistor and the 90º hybrid, respectively.

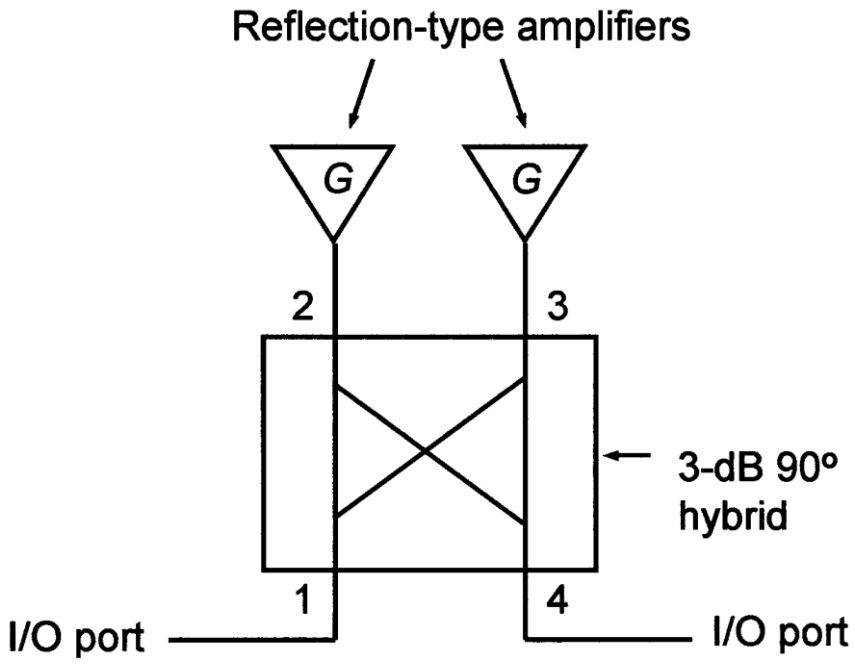

Fig. 1.5. Full-duplex BDA built by the reflection-type amplifiers [12].

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The half-duplex BDA amplifies the signal in only one direction at a time, and the direction of amplification can be switched as desired. The switched function is easy to realize by the single-pole double-throw (SPDT) switches, which offers the pass-through in the active path and the isolation in the disable path. These BDAs are built by a pair of SPDT switches and two opposite-direction amplifiers [13]-[15], as shown in Fig. 1.6. Another switching method is switching the input and output port, and hence the amplifier can be reused in two-direction amplification [16], as shown in Fig. 1.7. However, the switches suffer from a non-neglected loss in high operation frequency. For instance, at 60 GHz, the state-of-the-art CMOS SPDT switches are with at least 2-dB insertion loss [17], [18]. In brief, the 2-dB insertion loss rises up the noise figure of receiver around 2 dB and degrades the efficiency of transmitter around 37 %. In other words, the phased array needs to add extra elements that is more than a half of the original quantity to compensate the degradation. For this reasons, using the switches to realize the bidirectional function is not very practical.

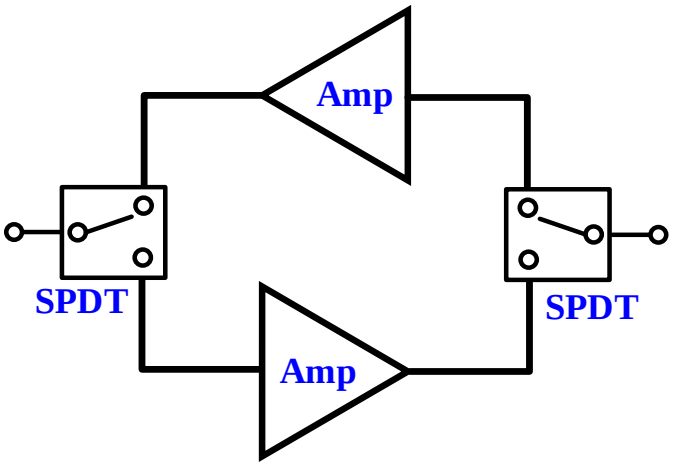

Fig. 1.6. Conventional BDA.

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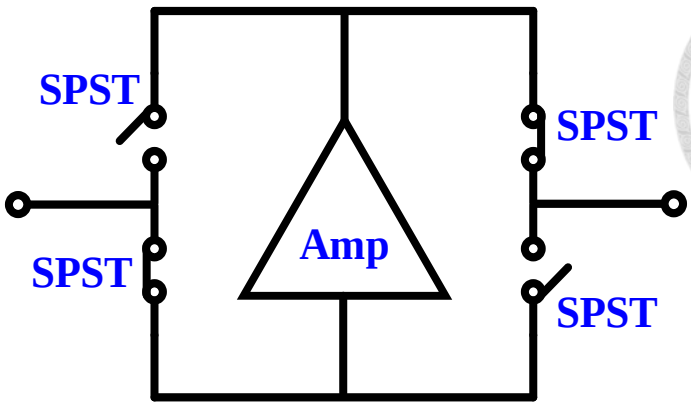

Fig. 1.7. Component-reused BDA.

To improve the drawbacks of the switch-switching topology, the "switchless" topology is proposed. That is, the designs absorb the switches into the amplifiers and optimize the junction matching network. Compared with the switch-switching topology, the loss can be reduced to improve the power efficiency and the noise performance. Besides, owing to the integrated functional blocks, the chip area and cost can be reduced.

In the previous works, the switchless BDAs can be classified into 4 categories: common-gate (CG), common-source (CS) or common-emitter (CE), bidirectional distributed amplifier (BDDA), and bidirectional constructive wave amplifier (BCWA).

The CG BDA [19]-[21] uses the identity of drain and source terminal in the transistor. While the dc bias of drain and source are interchanged, the direction of amplification can be switched, as shown in Fig. 1.8. The CG BDA takes the advantages of simple design and natural property of symmetry. However, the performance of gain, noise, and power handling are poor due to the CG stages.

The CS BDA [20], [22] and CE BDA [4], [23]-[25] are realized on FET and HBT process, respectively. As shown in Fig. 1.9, two of CS-based or CE-based amplifiers are used and placed in opposite directions, which are similar to the switch-switching topology. The difference is the SPDT switches are replaced by the passive networks, or called

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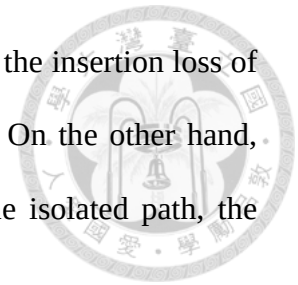

"junction network". It offers the function as the SPDT switches, but the insertion loss of the pass-through arm is reduced due to the absence of transistors. On the other hand, although the junction networks will not offer more isolation at the isolated path, the stability is confirmed by turning off the unused amplifier.

The BDDA [26]-[28] uses two anti-parallel gain cells to replace the single gain cell in the conventional distributed amplifier (DA). The topology is two individual DAs in opposite directions, and shares the passive components as shown in Fig. 1.10. The same feature of broadband is as the conventional DA; however, both drawbacks are low gain and poor power efficiency. Besides, in each direction of amplification, the turned-off gain cells contribute the extra capacitance, thus results in a lower cut-off frequency.

The BCWA [29], [30] is realized by the constructive-wave concept [31], the feedback amplifiers are built by the quarter-wave transmission line with cascode amplifiers as shown in Fig. 1.11. In each amplification mode, the inactive amplifiers are tuning off, and the feedback path can be reused for the two directions of amplification by tuning off the inactive amplifiers. However, the gain of the BCWA is affected by the loss of feedback quarter-wave transmission line [31]. Thus, the high performance active device (0.12-μm SiGe process in [29]) or low-loss substrate (45-nm CMOS SOI process in [30]) is needed to compensate the passive loss. Besides, due to the quarter-wave transmission line, the gain cell occupies more area than other types of BDA.

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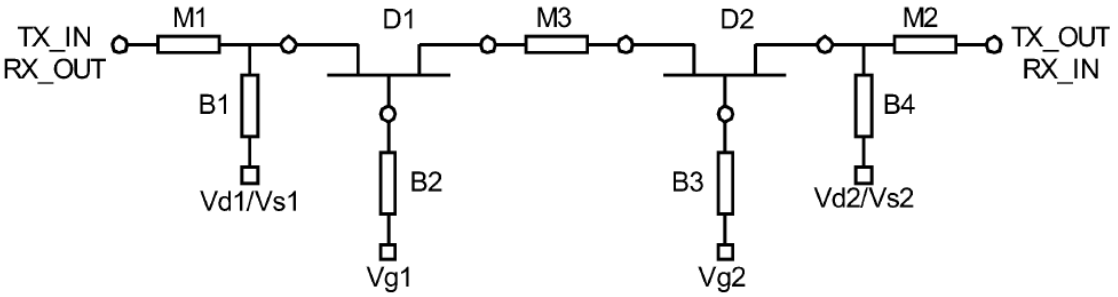

Fig. 1.8. CG BDA [20].

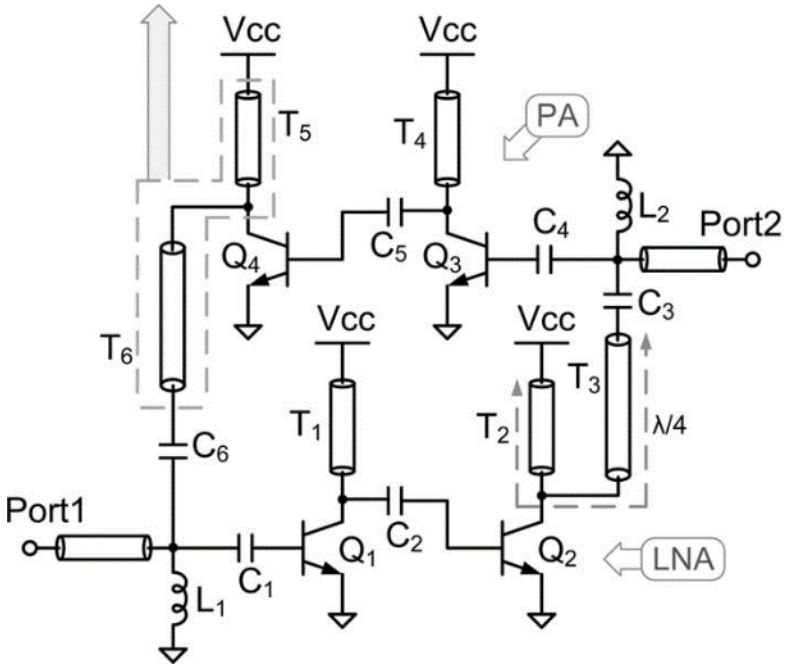

Fig. 1.9. CS/CE BDA [4].

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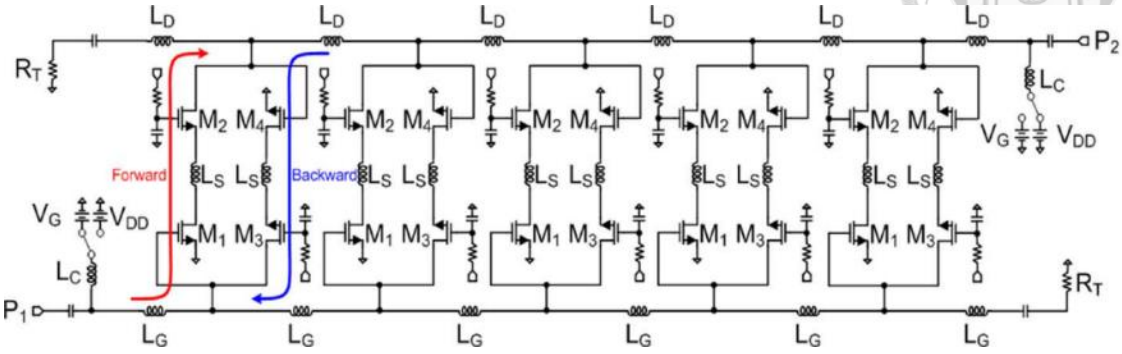

Fig. 1.10. Bidirectional DA [26].

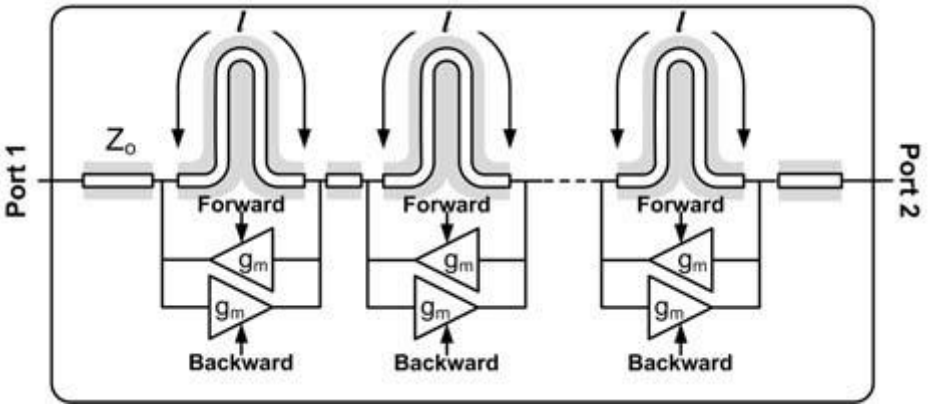

Fig. 1.11. BCWA [29].

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Table 1.1 listed the performance comparison of the cited previous works. From this table, the CS-type has the better gain performance, which is based on the un-equal signal path in each direction of amplification. The amplifiers can be optimized for noise and power applications while operated in receiving (Rx) and transmitting (Tx) mode, respectively. For the above reasons, in this thesis, the research is focused on the CS-type switchless BDA and two CS-type switchless BDAs are proposed by using different processes and topologies.

Table 1.1. Previous reported MMW switchless bidirectional amplifiers.

Ref.	Process	Topology	Frequency (GHz)	Rx Mode Gain (dB)	NF (dB)	Tx Mode Gain (dB)	OP_{1dB} (dBm)	P_{sat} (dBm)	P_{dc} (mW)	Chip Size (mm^2)
[20]	GaAs	CG	32-37	13	4.7	13	N/A	10	N/A	2.6
[21]	75-nm InP	CG	90-140	12	5	9	1*	5	15	0.46
[4]	0.12-μm SiGe	CE	41.7-45.8	34**	4.7	35**	8.5	9.5	26(R) 91(T)	1.28***
[23]	90-nm SiGe	CE	66-73	9.6	8.6	14.5	N/A	7.2	21(R) 85(T)	0.65
[25]	0.13-μm SiGe	CE	94	5.7	9.5	5.7	-2.8*	N/A	9.9	0.31
[20]	GaAs	CS	26-43	17	4	13	N/A	17	N/A	1.3
[22]	65-nm CMOS	CS	77.3	42**	9	42**	N/A	9.2	20.2(R) 71.5(T)	0.69***
[26]	0.13-μm CMOS	DA	3-20	10	6.5	10	8	16	68	0.81
[28]	0.18-μm CMOS	DA	21.6-31	6.4	9.1	6.4	4.3	12	46.8	0.28
[29]	0.12-μm SiGe	BCWA	77-90	16	N/A	16	N/A	N/A	65.8	0.47
[30]	45-nm CMOS SOI	BCWA	40/85	4.6	N/A	4.5	-2.9	3.9	N/A	0.48

*Inference from the measured IP_{1dB} with the gain in Tx Mode.
**Including the IF amplifiers.
***Total transceiver area.

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1.3 Contributions

This thesis presents two switchless BDA and a bidirectional beamformer for 60-GHz application, the contributions of these researches are illustrated as follows.

The first switchless BDA is realized in 90-nm CMOS process. By using the compact T-network as matching network, the chip size and core size are only 0.44 mm^2 and 0.18 mm^2, respectively. From 57 to 66 GHz, it demonstrate less than 8-dB noise figure with above 18.2-dB gain in receiving mode, and above 13.5-dB gain with maximum output power of 6.5 dBm with 7.3% peak PAE in transmitting mode.

The second switchless BDA is realized in 40-nm CMOS process, by using the differential common-source amplifiers with transformer-based matching network, the size is reduced improvably. The chip size and core size are only 0.21 mm^2 and 0.12 mm^2, respectively. From 52 to 62 GHz, it demonstrate less than 8-dB noise figure with above 10.1-dB gain in receiving mode, and 13.4-dB gain with maximum output power of 9.7 dBm with 8.5% peak PAE in transmitting mode. Comparing with the first BDA, the chip size is reduce improvably due to the differential topology reduce the required capacitance of bypass capacitors. In addition, the output power and PAE are enhanced by using the differential power combined. The 40-nm CMOS BDA demonstrate the minimum chip size by comparing with the published switchless BDAs.

The two switchless BDAs are the first switchless BDA that realized on Si-based process in 60 GHz. The CMOS front-end bidirectional gain blocks in compact chip size demonstrate a practical solution that helps to solve the problems of high I/O connected packaging, heterogeneous integration, and low area efficiency in the large phased array.

The beamformer is realized in 40-nm CMOS process, by taking the advantages of compact BDA and sharing components, the beamformer demonstrates the minimized chip

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size. The beamformer is designed to cooperate with 4 individual antenna array and transceiver to build up the phased array module, functions a Tx or Rx by T/R mode switching. The antennas are sharing at Tx and Rx modes, and the reduced I/O ports minimized the effort of assembly. Moreover, bidirectional transmission and omnidirectional beam-steering can be simultaneously realized by this beamformer.

1.4 Thesis Organization

The thesis is organized as follows. In chapter 2, a 60-GHz switchless bidirectional amplifier using 90-nm CMOS process is demonstrated. The design procedures, simulation, and experiment results are exhibited.

In chapter 3, the other 60-GHz switchless bidirectional amplifier using 40-nm CMOS process is demonstrated. Based on the 90-nm BDA, the advanced design techniques such as transformer-coupled and neutralization have added in the circuit to improve the performance and reduce the layout size.

Based on the 40-nm BDA, the 60-GHz beamformer is demonstrated in Chapter 4. The application in the phased array module for mobile devices is proposed. The link budget of the whole system, and gain/power budget of the beamformer is formulated. The design procedures of the functional blocks and the system chip are illustrated.

Finally, the conclusions are given in chapter 5.

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Chapter 2 Design of a 60-GHz Bidirectional Amplifier in 90-nm CMOS process

In this chapter, a 60-GHz switchless bidirectional amplifier using 90-nm CMOS process is demonstrated. The design concepts and steps are presented in the following sections.

2.1 Circuit Design

2.1.1 Introduction

By using the CS BDA topology, the two opposite amplifiers are connected by junction network, as shown in Fig. 2.1. The circuit design can be divided into three parts, (1) PA part, (2) LNA part, and (3) junction network. The BDA functions as a PA in Tx mode and as a LNA in Rx mode. The BDA is designed for TDD system, and the Tx and Rx modes are alternatively switched by turning on/off the PA and LNA, respectively. In each time slot, only one of the two amplifiers is turned on, while the other is turned off. The turn-off amplifier is operated as a part of matching network for the turn-on one.

In each operation mode, the turn-on path amplifies the signal, and the turn-off path loads the turn-on one. In order to reduce the loading effect, the turn-off one must be in high impedance to avoid degrading the performance. Fig. 2.2 plots the extra loss caused by loading effect. The extra loss caused by loading is more than 2 dB while the loading impedance is less than 100 Ω, which makes the switchless topology meaningless because the insertion loss of the state-of-the-art 60-GHz CMOS SPDT switches are around 2 dB

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[17], [18]. In this BDA, the design target is less than 2 dB loading loss. In other words, the off-state impedance of each amplifier should be higher than 100 Ω.

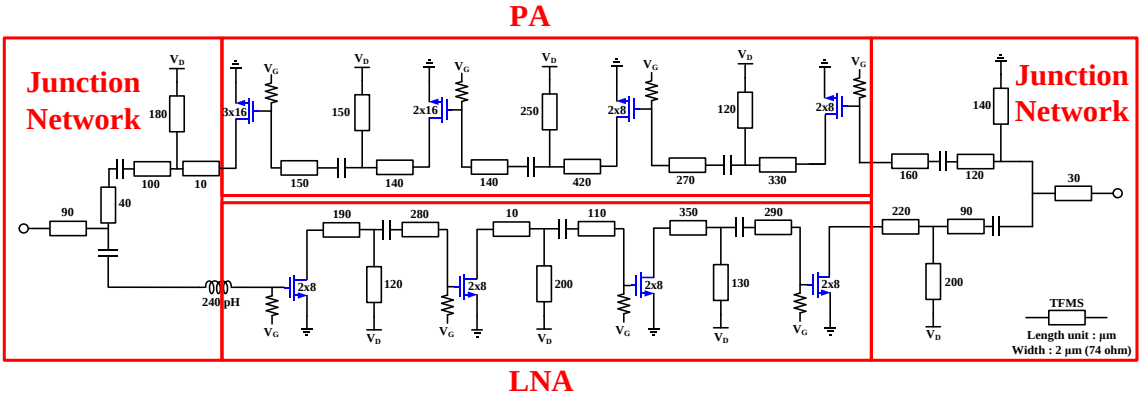

Fig. 2.1. Schematic of proposed BDA.

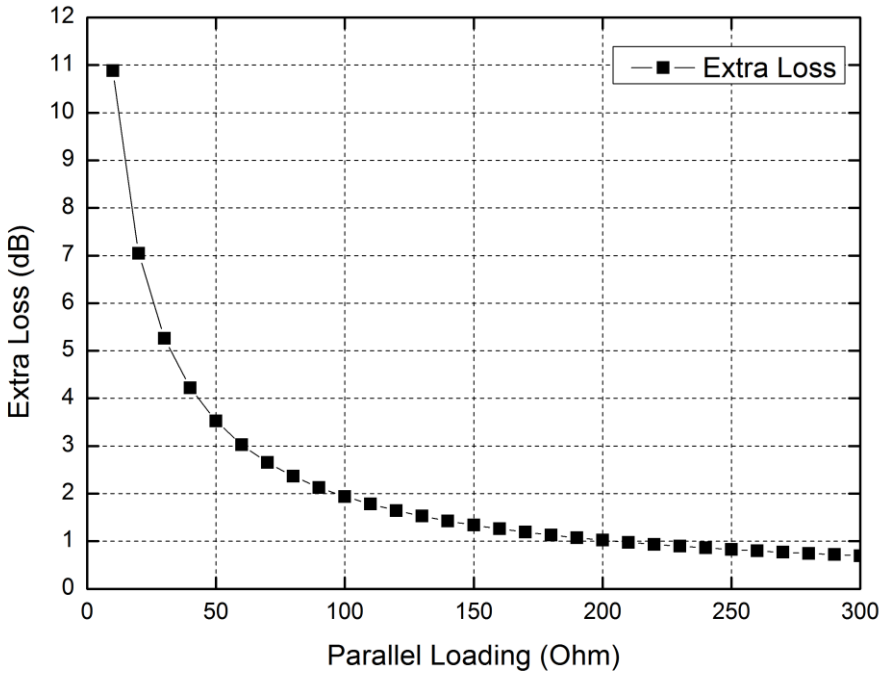

Fig. 2.2. The extra insertion loss caused by loading effect.

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2.1.2 PA part

The PA part consists of 4 common-source stages. The maximum gain of each gain cell is around 9 dB at 60 GHz, as shown in Fig. 2.3. Considering the loss introduced by the inter-stage matching network, 5-dB gain is achieved for each stage. The last stage of PA is the most critical part which restricts the performance of output power and linearity. Device with larger gate width has higher power capability and better linearity. On the other hand, the lower output impedance that requires higher impedance transformation ratio, produces more loss, and puts restriction on the bandwidth. The 3 μm×16 finger device is a compromise for adequate output power (OP_{1dB} is 8.75 dBm in load-pull simulation) with adequate large off-state impedance (above 100 Ω after T-network matching). The driver stage uses 2 μm×16 finger device that offers sufficient power to drive the last stage. The first and the second stage uses 2 μm×8 finger devices as gain stages. The device size ratio among the 4-stage is 1:1:2:3. All the devices are biased at drain voltage of 1 V, and gate voltage of 0.8 V. Fig. 2.4 shows the PA schematic, where the T-network is used in the inter-stage matching for compact layout size.

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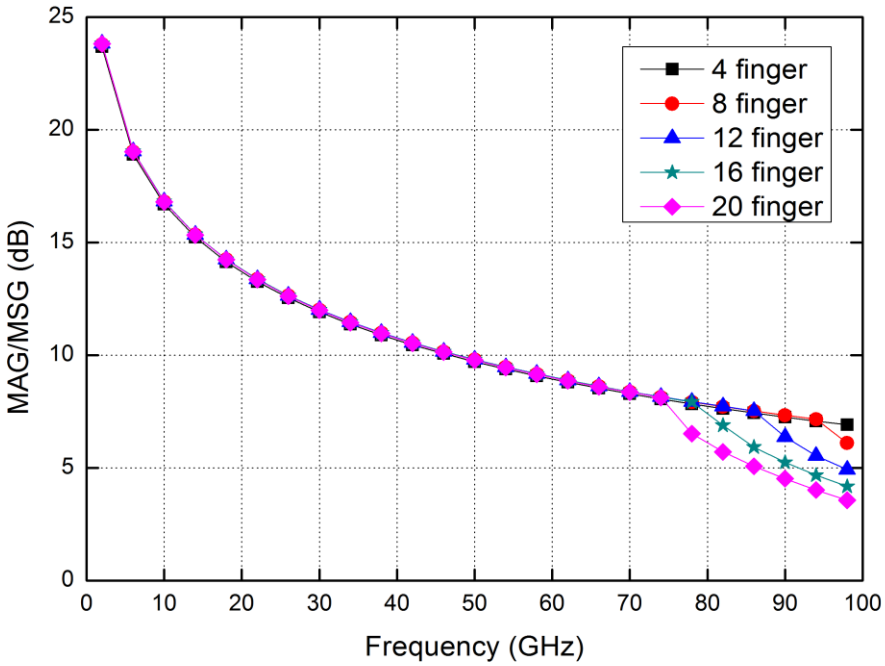

Fig. 2.3. Maximum gain of the transistors.

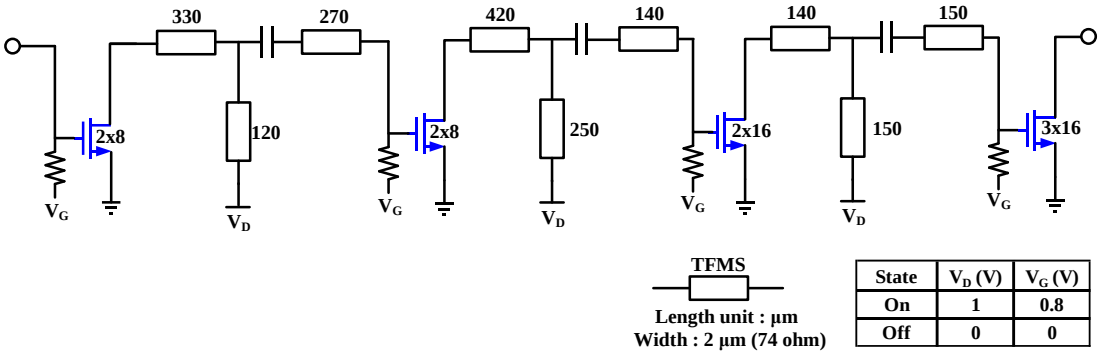

Fig. 2.4. Schematic of the PA part.

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2.1.3 LNA part

Same as the PA part, the LNA is also built by 4 common-source stages. Different from the previous PA designs, it is proposed for small-signal operation, so the large-width devices is not necessary. Fig. 2.5 shows the schematic of the LNA. The 4 common-source stages are all 2 μm×8 finger NMOS device which is selected for low noise matching and compact inter-stage matching network. They have around 20-Ω real part impedance at gate and drain terminals while simultaneously conjugate matched, and it is easy to use T-network to match the imaginary part impedance and achieve the drain bias at the same time. This design reduces the matching network complexity, loss and layout size.

As the last stage in PA, the first stage design is the most critical part in LNA. The 2 μm×8 finger device is chosen for the minimal noise figure impedance (Z_{opt}) equal to 56+135j Ω, which has around 50-Ω real part impedance. Thus, a series 240-pH inductor with 50-Ω junction impedance can achieve the minimal noise figure condition. Besides, the simulated minimal insertion loss of the spiral inductor is only 0.8 dB. By comparing with using the thin-firm microstrip (TFMS) line as matching network, it has the lower loss that avoid the poor noise performance. The structure of the spiral inductor as shown in Fig. 2.6.

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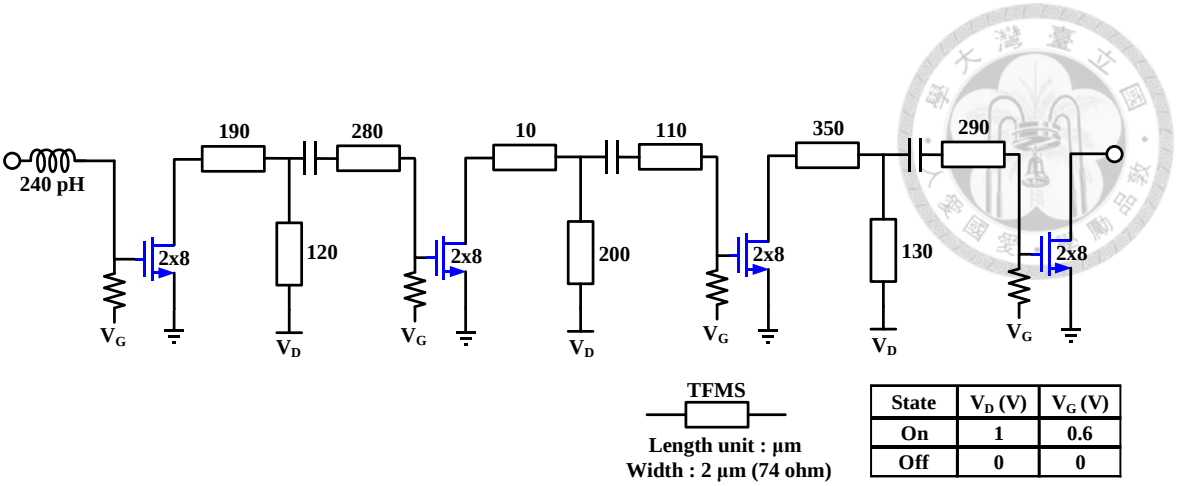

Fig. 2.5. Schematic of the LNA part.

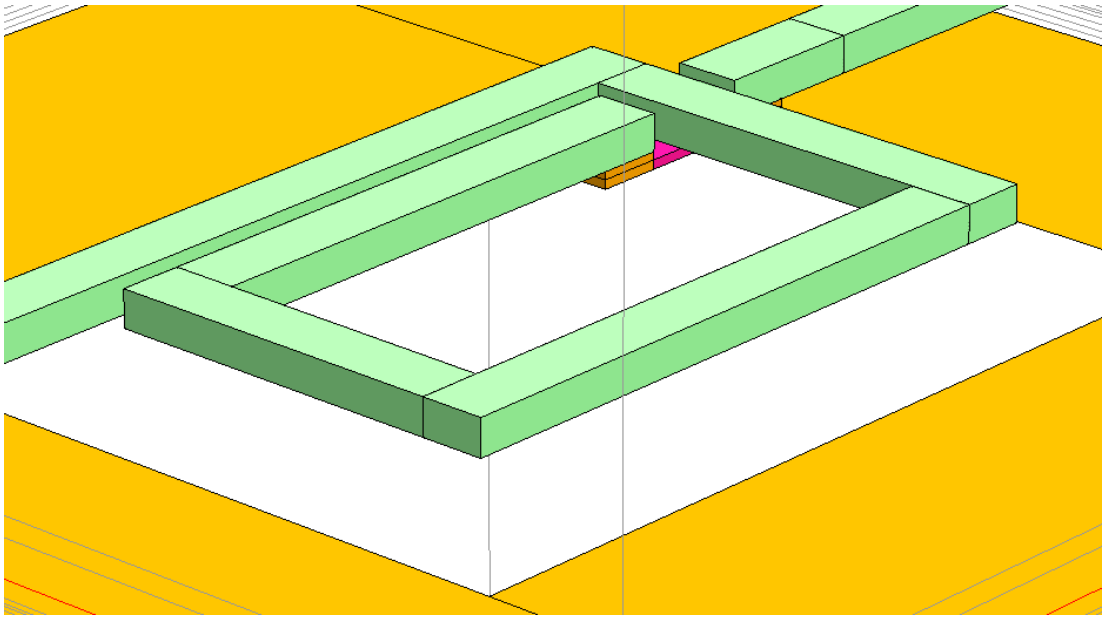

Fig. 2.6. EM structure of spiral inductor for noise matching.

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2.2 I/O Junction Network

The most critical part in this BDA is the junction between PA and LNA. The junction network should offer the noise matching for LNA in Rx mode and power matching for PA in Tx mode, as shown in Figs.2.7 and 2.8, respectively. At the same time, the 3-port network should have the 50-Ω impedance in the I/O terminal to avoid the return loss from previous or next stage circuit. However, the design goal is hard to achieve for the different conditions in the two operated mode. Alternatively, the 3-port junction network can be divided into two individual matching networks, as shown in Figs. 2.9 and 2.10 in Rx and Tx mode, respectively. By designing the junction network individually, the design procedure is simplified. The individual junction network offers the impedance matching while amplifier is tuned on and the adequate isolation (in high impedance) while amplifier is tuned-off.

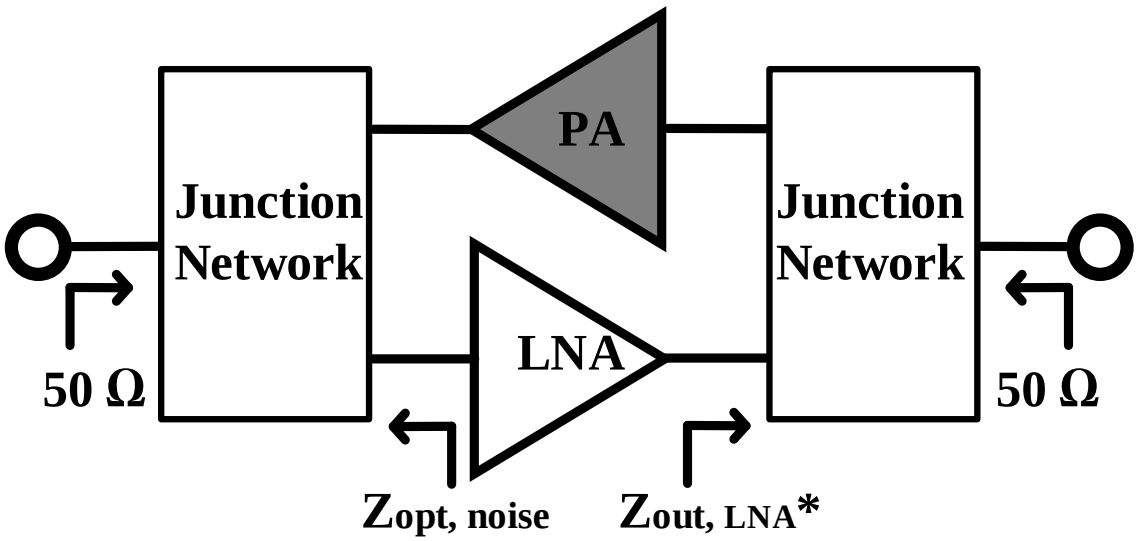

Fig. 2.7. Design goal of the junction network in Rx mode.

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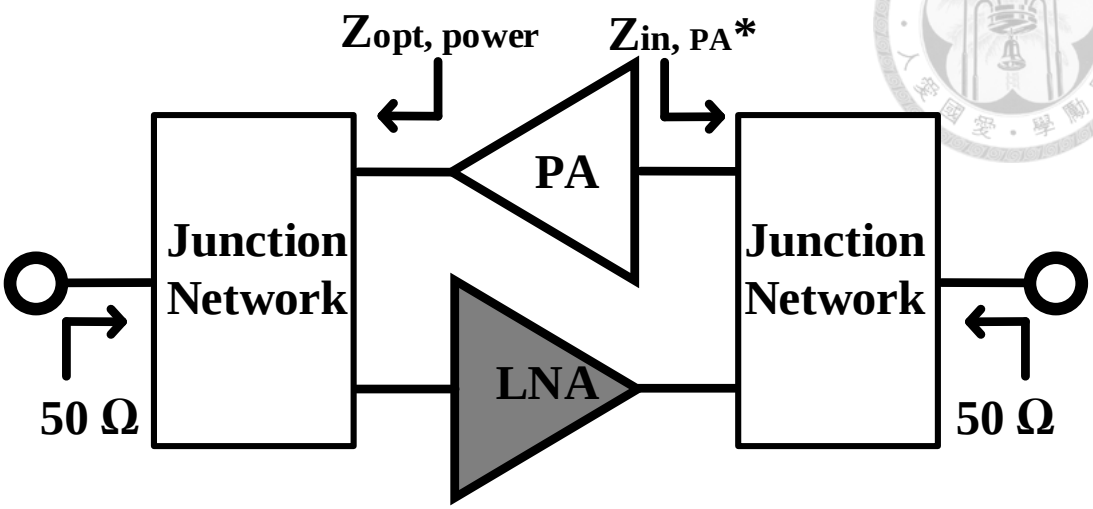

Fig. 2.8. Design goal of the junction network in Tx mode.

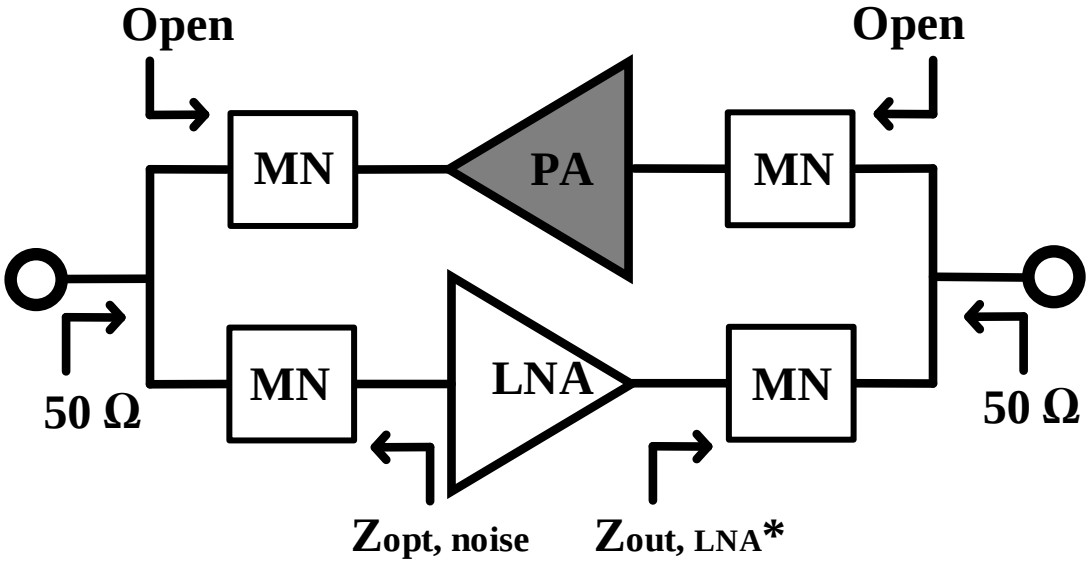

Fig. 2.9. Design goal of individual matching network in Rx mode.

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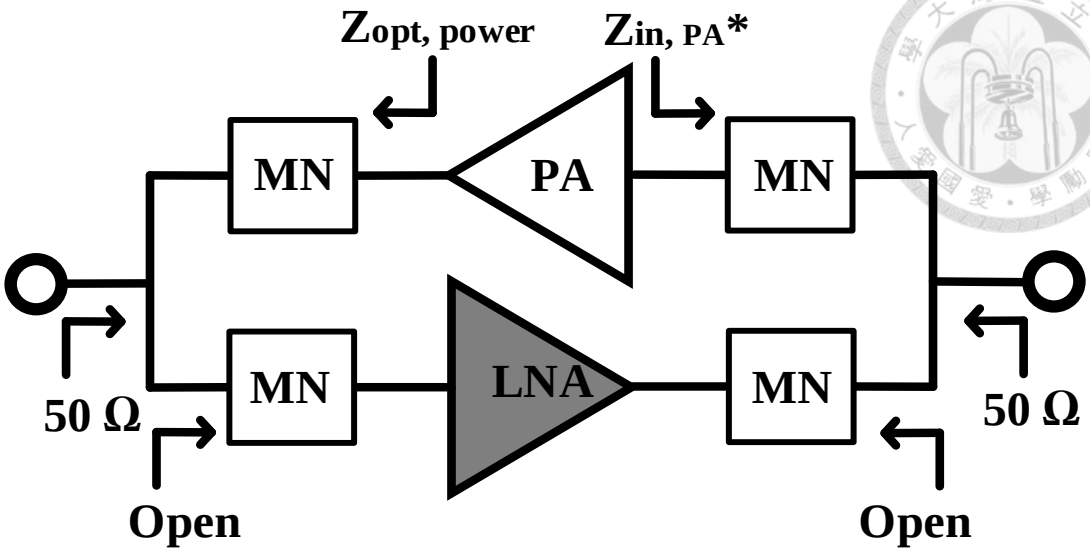

Fig. 2.10. Design goal of individual matching network in Tx mode.

In brief, the 3-port network is converted to two 2-port networks, which are the same as individual PA or LNA design, but the tuned-off amplifier causes the loading that produces extra loss. While the amplifier is tuned-off, the transistor still contributes the parasitic impedance, and it can be modeled as shunt resistor and capacitor. Figs. 2.11 and 2.12 show the junction networks design and equivalent circuit in each operated mode, the parasitic resistance and capacitance can be considered as a part of matching network.

In order to achieve the maximum power of the PA, the T-network of PA output is designed to convert the 50 Ω to the load-pull impedance in the on-state, and convert the transistor to high impedance in the off-state. In LNA part, the input matching network uses a series inductor to meet the minimal noise condition. Note that the simple series-inductor might not offer high impedance in off-state, which is a trade-off between noise and isolation.

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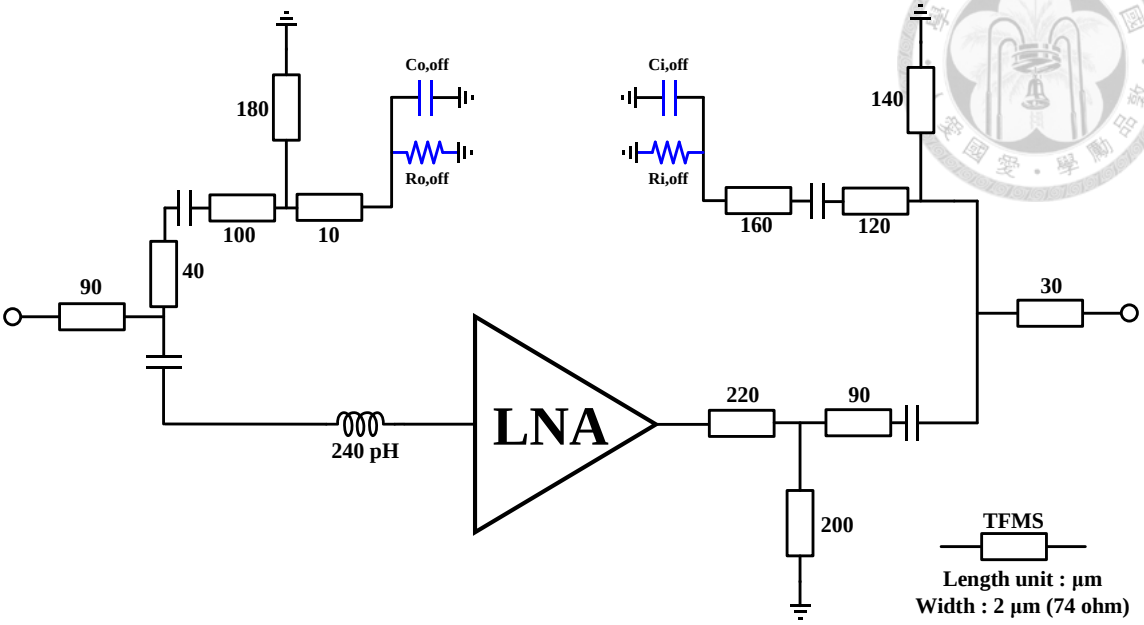

Fig. 2.11. Equivalent circuit in Rx mode.

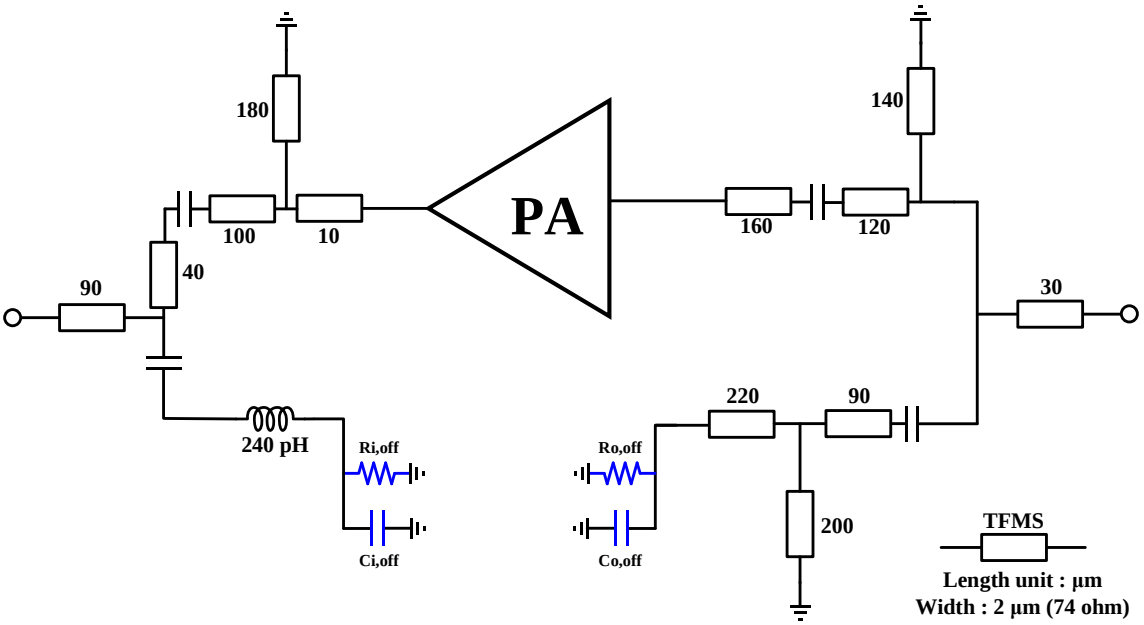

Fig. 2.12. Equivalent circuit in Tx mode.

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The impedance transformation between the I/O junction of PA and LNA are listed in Tables 2.1 and 2.2, respectively. It can be observed that, at the PA output, the T-network transforms the low impedance to 50 Ω in the on-state, and transforms to around 156 Ω in the off-state. At the LNA input, the series inductor works as the lowest-loss matching network for minimal noise figure in the on-state, and transforms to higher imaginary impedance in the off-state. Comparing with the PA part, the impedance differences between on/off state in LNA are not obvious since the device size is relatively small, which is another design challenge.

Tables 2.3 and 2.4 list the simulated insertion loss and isolation of the junction networks in each mode at 60 GHz. The isolation range is from 6.8 to 12.1 dB. Although the isolation is worse than the individual switches, the turned-off amplifier offers an extra isolation of more than 30 dB; as the result, the limited isolation will not affect the stability because the loop gain is smaller than 1. Besides, the insertion loss is around 4 dB which includes the loss of matching network, and thus the total loss is better than the discrete design which includes the individual switches and amplifiers.

Another concern is the LNA input impedance variation as the PA provides high output power. Fig. 2.13 plots the input impedance of turned-off LNA versus the PA output power in Tx mode at 60 GHz. It can be observed that the resistance is almost not affected by the amplitude of the PA output power, and the reactance decreases as the PA output power increases. However, this will not restrict the PA output power because the impedance variation is relatively small before the power reaches 15 dBm.

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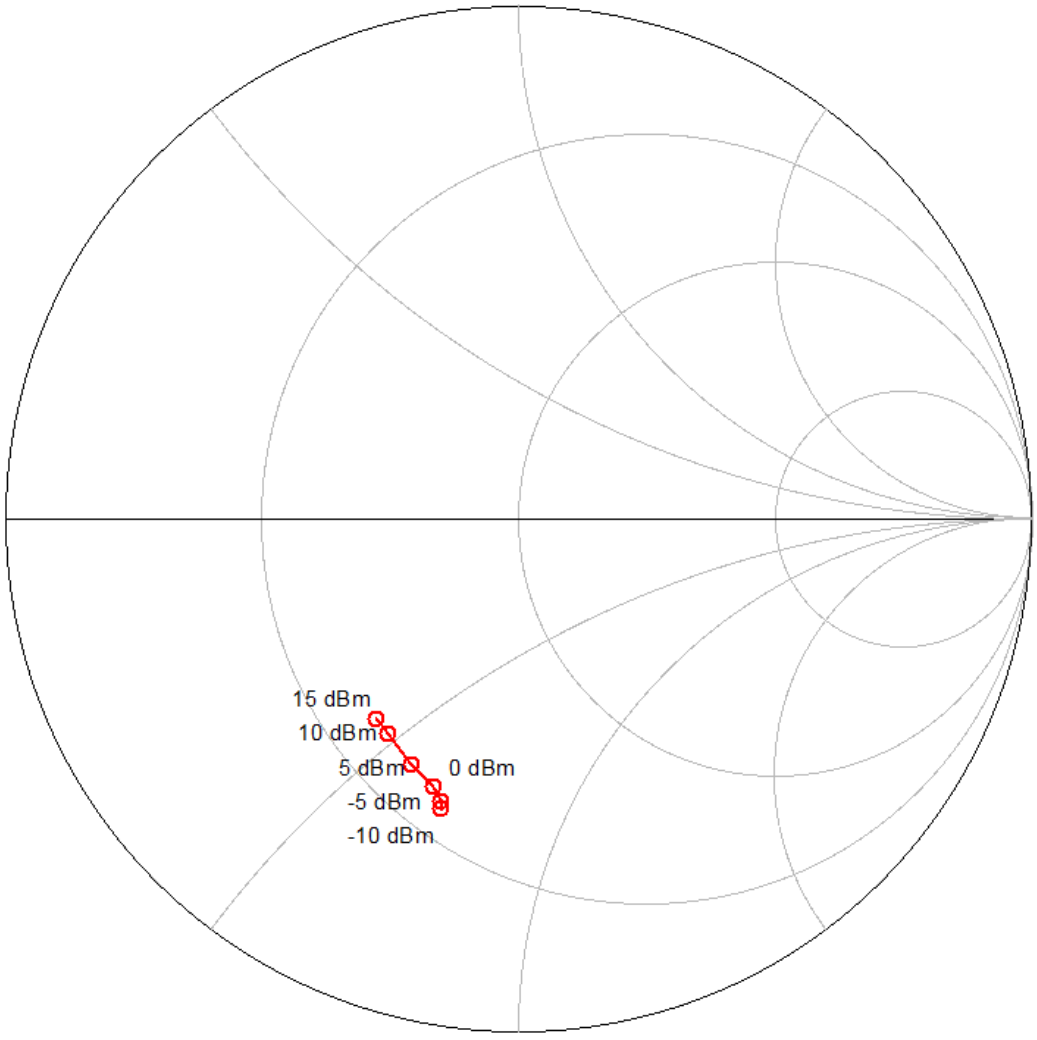

Frequency = 60 (GHz)

Pin_Rx (dBm)	Zin_LNA (ohm)
-10.000	19.951 - j34.405
-5.000	20.704 - j33.833
0.000	21.356 - j32.030
5.000	21.459 - j28.269
10.000	21.683 - j24.058
15.000	21.580 - j21.850

Fig. 2.13. Input impedance of LNA versus the PA output power in Tx mode.

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Table 2.1. Impedance transformation by the junction network in Rx mode.

Rx Mode	PA (Off)		LNA (On)	
Impedance (Ω)	Input	Output	Input	Output
without matching	70-148j	39-76j	18-100j	18-94j
with matching	53+26j	156+2j	11-12j	52-11j

Table 2.2. Impedance transformation by the junction network in Tx mode.

Tx Mode	PA (On)		LNA (Off)	
Impedance (Ω)	Input	Output	Input	Output
without matching	27-88j	21-27j	45-153j	46-174j
with matching	27-3j	50	20-35j	90+89j

Table 2.3. Insertion loss and isolation of the junction network in Rx mode.

Rx Mode	Isolation of PA arm (dB)		Insertion Loss of LNA arm (dB)	
	Input	Output	Input	Output
	6.8	11.1	4.3	6.1

Table 2.4. Insertion loss and isolation of the junction network in Tx mode.

Tx Mode	Insertion Loss of PA arm (dB)		Isolation of LNA arm (dB)	
	Input	Output	Input	Output
	3.5	3.8	7.5	12.6

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2.3 Layout and Simulated Performance

The circuit is designed with Agilent Advance Design System (ADS), and all the passive components including MIM capacitors and TFMS lines are simulated by Sonnet EM solver. The chip layout as shown in Fig. 2.14, the chip size is 0.68 mm × 0.65 mm.

Fig. 2.15 shows the simulated S-parameter in Rx mode. The gain is above 16 dB from 49 to 68 GHz, and above 17.9 dB from 57 to 66 GHz. Fig. 2.16 shows the simulated noise figure, the noise figure is below 8 dB from 57 to 66 GHz. Fig. 2.17 shows the simulated S-parameter in Tx mode. The gain is above 16 dB from 49 to 68 GHz, and above 16.2 dB from 57 to 66 GHz. Fig. 2.18 shows the simulated large-signal performance at 60 GHz, the OP_{1dB} is 3 dBm, and saturated output power is 6.2 dBm with peak PAE of 7.8 %. The bias condition of simulation as shown in Table 2.5.

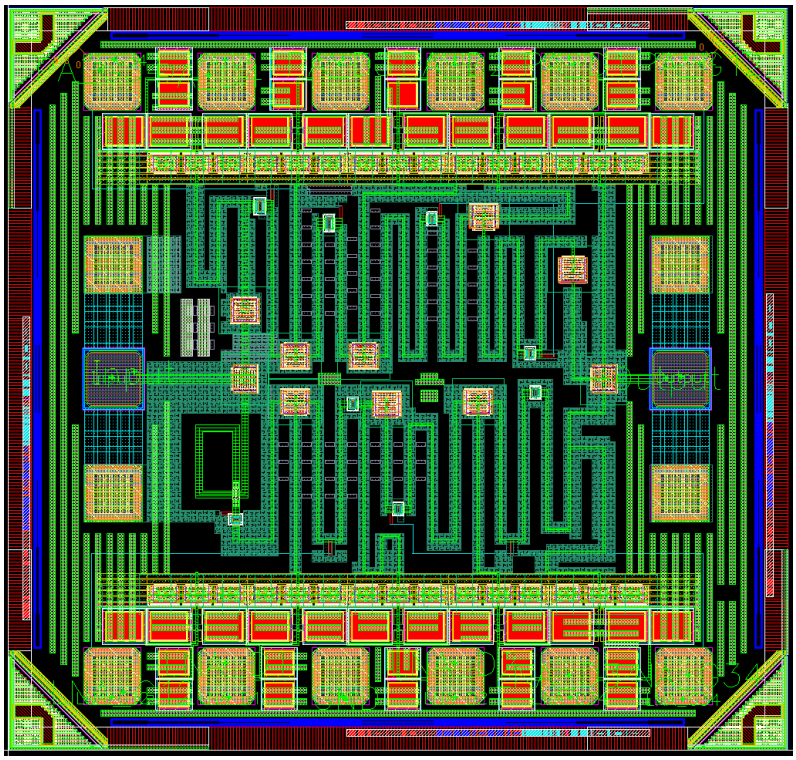

Fig. 2.14. Chip layout of the BDA.

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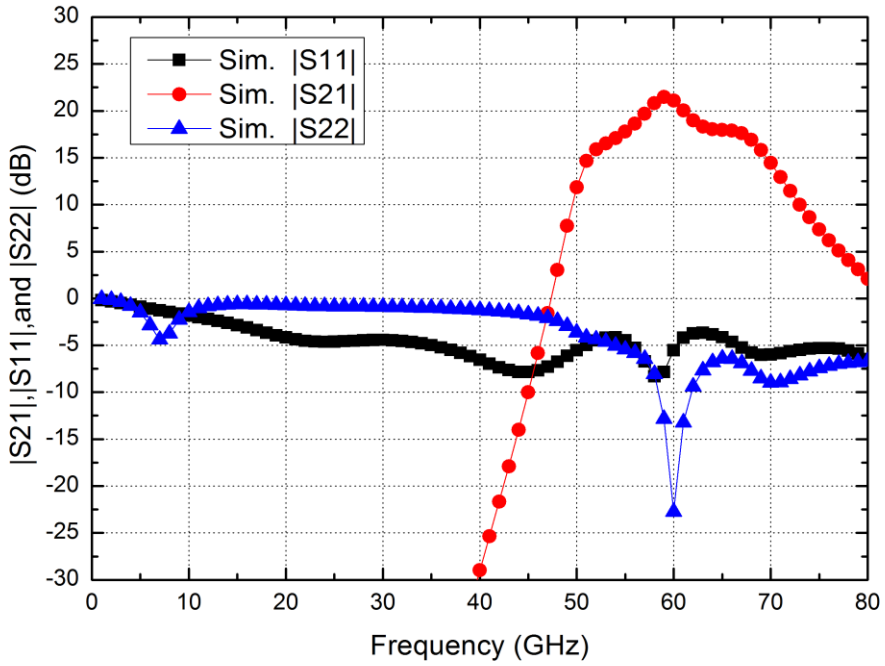

Fig. 2.15. Simulated S-parameters in Rx mode.

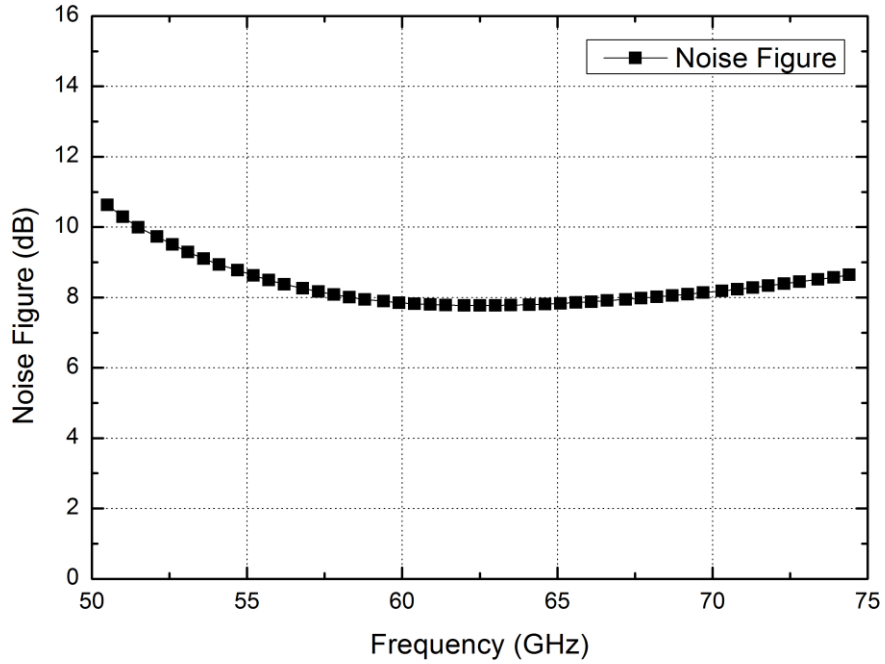

Fig. 2.16. Simulated noise figure in Rx mode.

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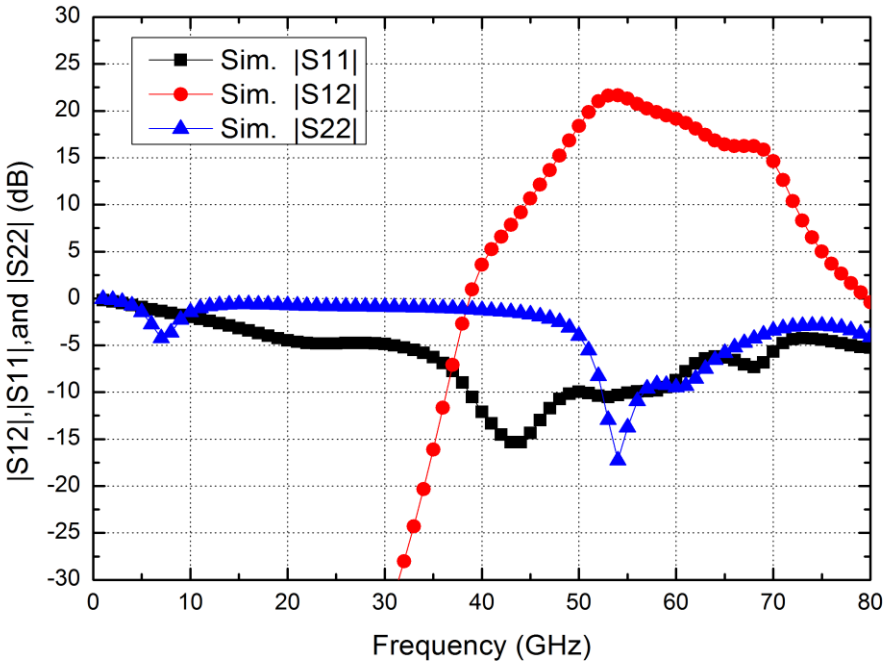

Fig. 2.17. Simulated S-parameters of the BDA in Tx mode.

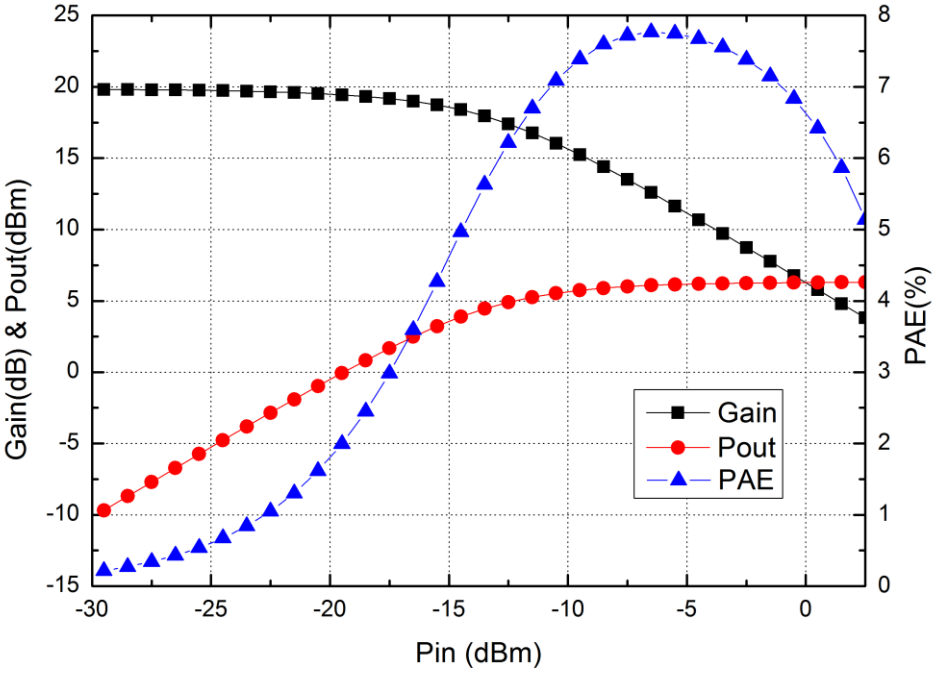

Fig. 2.18. Simulated large-signal performance in Tx mode at 60 GHz.

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Table 2.5. Simulated bias condition in each mode.

	$V_{G,\,LNA}$ (V)	$V_{D,\,LNA}$ (V)	$I_{D,\,LNA}$ (mA)	$V_{G,\,PA}$ (V)	$V_{D,\,PA}$ (V)	$I_{D,\,PA}$ (mA)	P_{dc} (mW)
Rx Mode	0.6	1	14.7	0	0	0	14.7
Tx Mode	0	0	0	0.8	1	49.3	49.3

2.4 Stability Analysis

In the multi-stage amplifier, the typical stability factors (e.g. K-factor and μ-factor) are not sufficient since they are only defined for passive terminations of a 2-port device with no feedback or active loads. The conventional method of the stability check in the multi-stage amplifiers utilizes stability circle. By separating the inter-stage, the stability can be confirmed whether the stability circles have overlapped at the same frequency. However, the bias networks form feedback paths, thus the conventional method may ignore the effect of feedback produced by the bias networks. To provide an accurate stability analysis for the multi-stage amplifiers, Texas Instruments Incorporated (TI) proposed a method without loading or affecting the circuit [32]. The tool is called "S-Probe". By sensing the reflection coefficient at the I/O of the active devices, the stability can be confirmed while the reflection coefficient (stability index) is less than 1 in magnitude.

The stability check is simulated by Agilent Advance Design System (ADS) with build-in component "S-Probe" as the follows. Figs. 2.19 to 2.22 show the check results among the 4-stage of LNA in Rx mode. Figs. 2.23 to 2.26 show the check results among the 4-stage of PA in Tx mode. All the stability indices are smaller than 1 in magnitude, and thus the BDA is stable in each mode.

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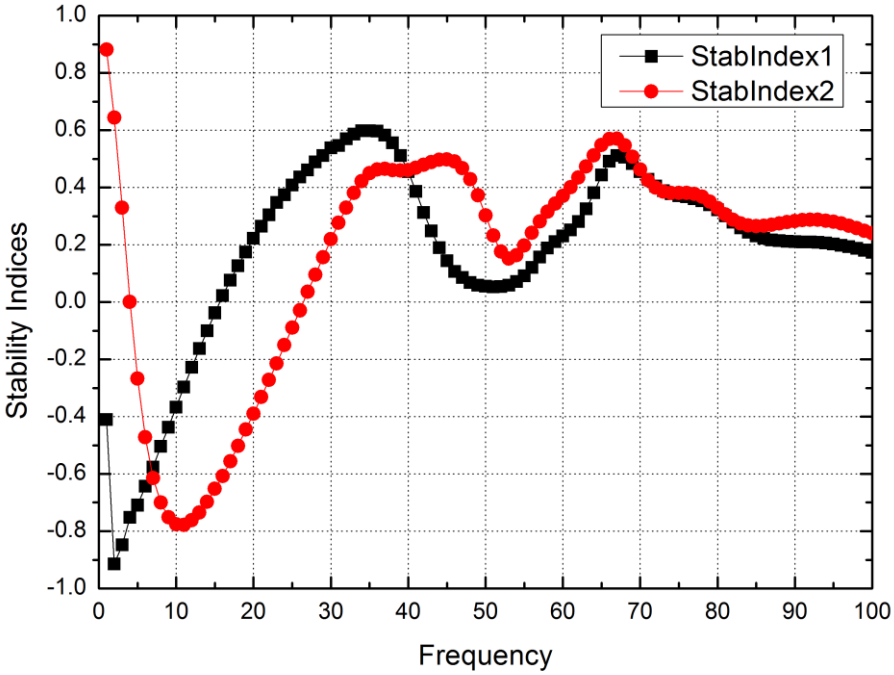

Fig. 2.19. Stability indices of LNA 1st stage.

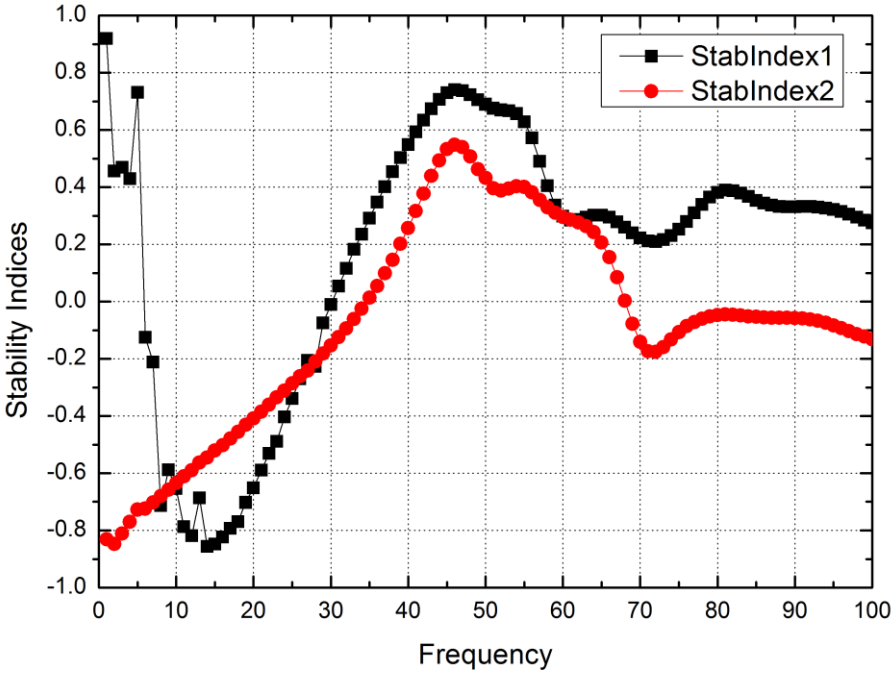

Fig. 2.20. Stability indices of LNA 2nd stage.

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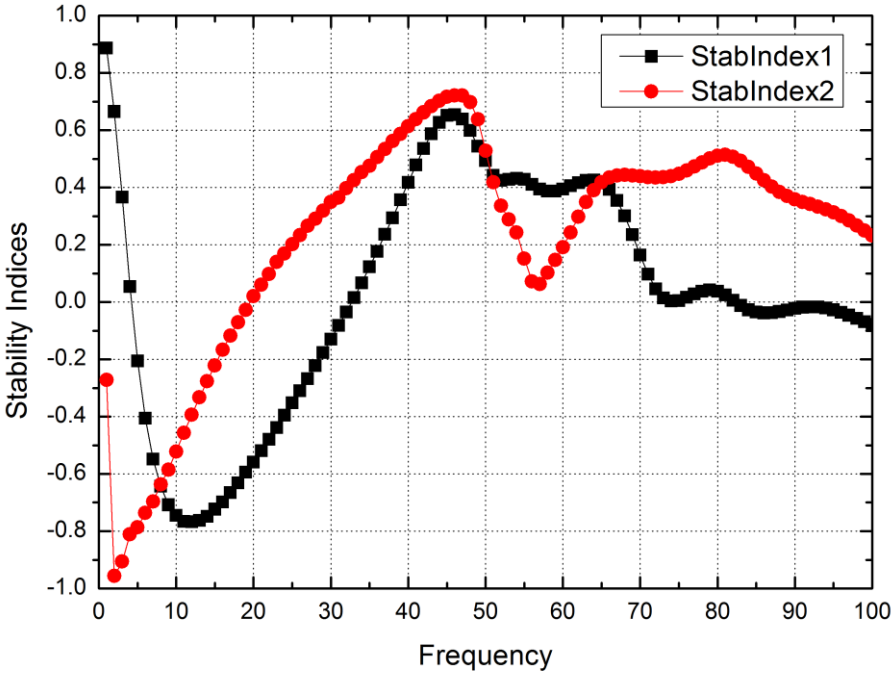

Fig. 2.21. Stability indices of LNA 3rd stage.

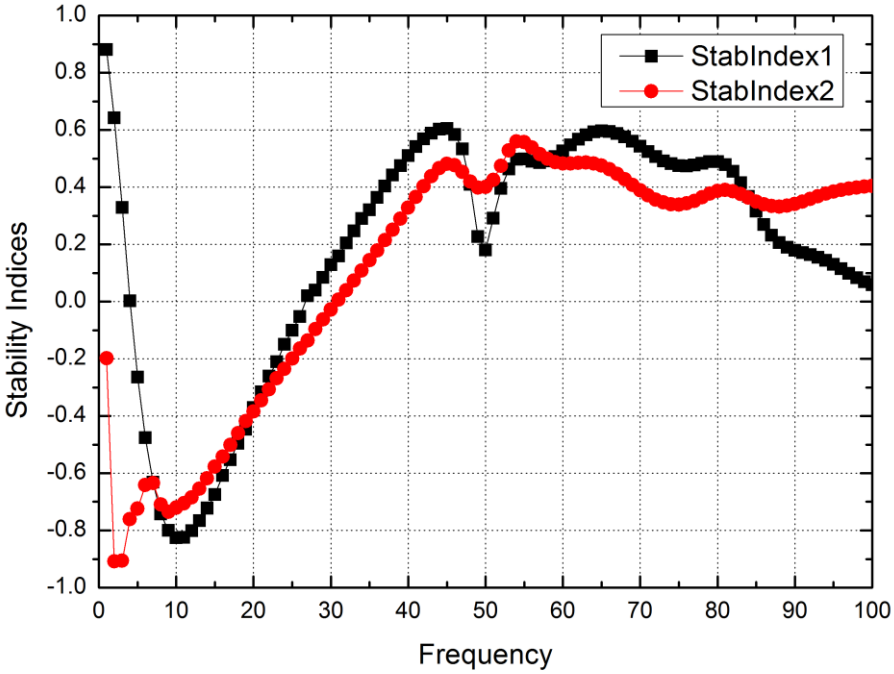

Fig. 2.22. Stability indices of LNA 4th stage.

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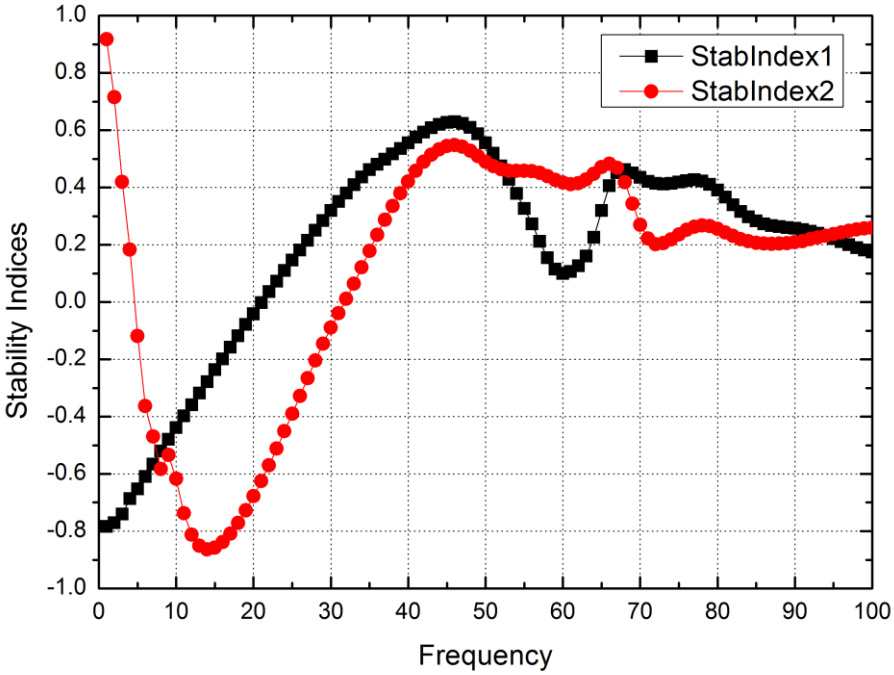

Fig. 2.23. Stability indices of PA 1st stage.

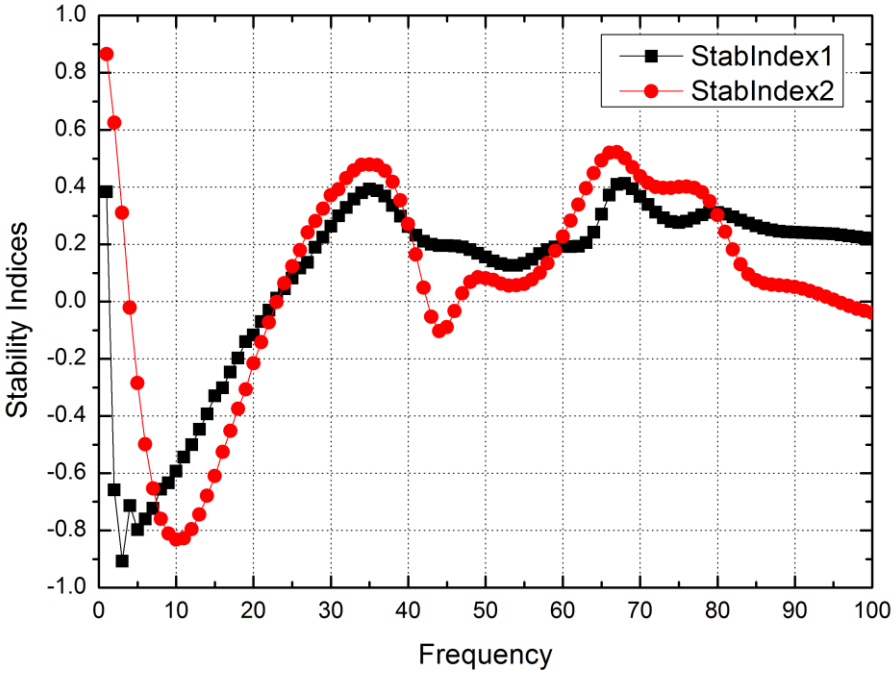

Fig. 2.24. Stability indices of PA 2nd stage.

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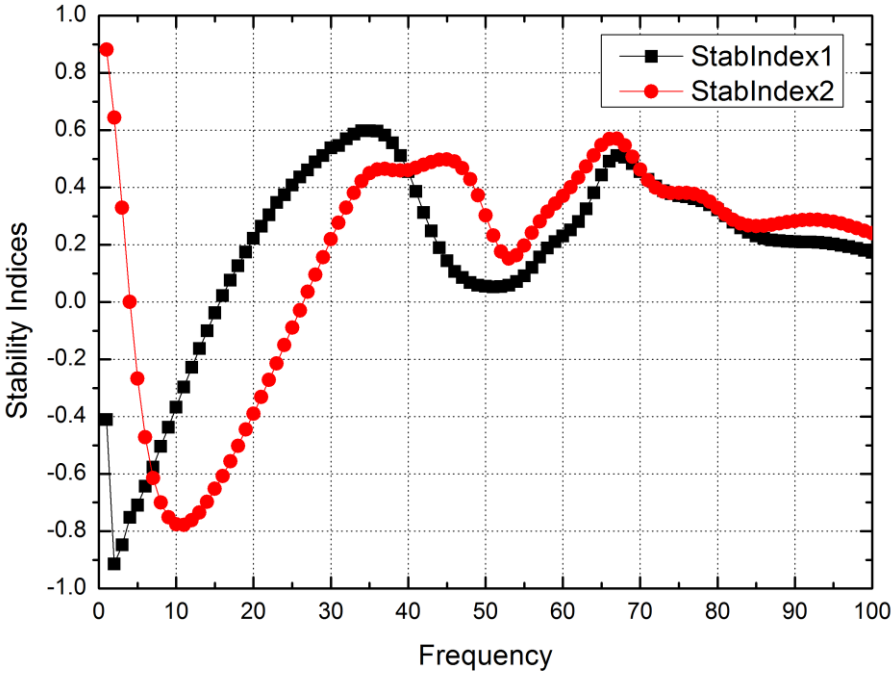

Fig. 2.25. Stability indices of PA 3rd stage.

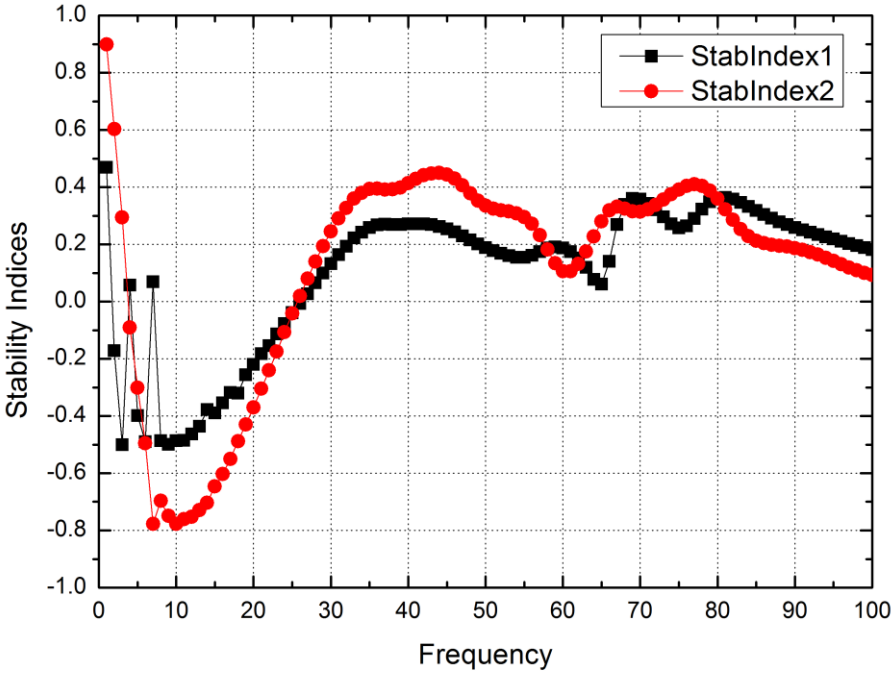

Fig. 2.26. Stability indices of PA 4th stage.

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2.5 Experiment results

The BDA is fabricated in TSMC 90-nm GUTM CMOS process. The chip photo is shown in Fig. 2.27. The chip size is 0.44 mm^2 including all pads and the cell ring, and the core size is 0.18 mm^2.

The chip measurement is taken via on-wafer probing. The S-parameter is measured by Agilent E8361C vector network analyzer. The noise figure is measured by Agilent N8975A noise figure analyzer with N8975AZ-K63 and N8975AZ-K75 downconverters. The large-signal measurement is taken by Agilent E8257D vector signal generator and Agilent E4419B power meter with Agilent V8486A V-band power sensor.

The measured gain in Rx mode is above 18.2 dB and noise figure is below 8 dB from 57 to 66 GHz, as shown in Figs. 2.28 and 2.29, respectively. The measured gain in Tx mode is above 13.5 dB from 57 to 66 GHz, as shown in Fig. 2.30. The measured large-signal performance is shown in Fig. 2.31. At 60 GHz, the measured OP_{1dB} is 3.6 dBm, and saturated output power is 6.5 dBm with peak PAE of 7.3 %. The quiescent power consumption in Rx mode and Tx mode are 15.3 mW and 46 mW, respectively. The bias condition in the measurement as shown in Table 2.6.

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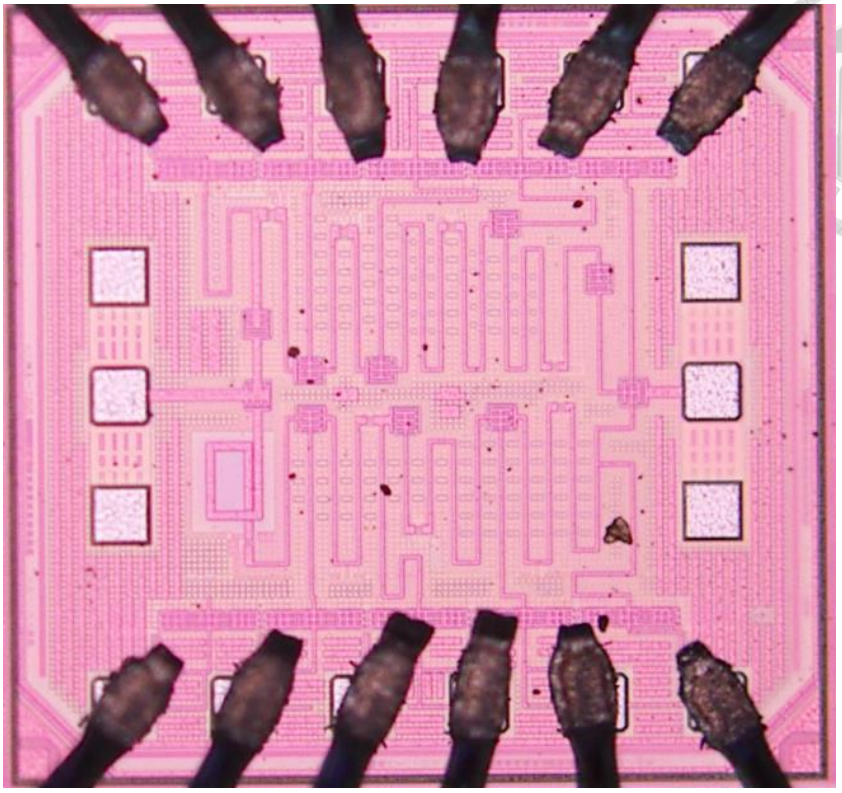

Fig. 2.27. Chip photo of the BDA.

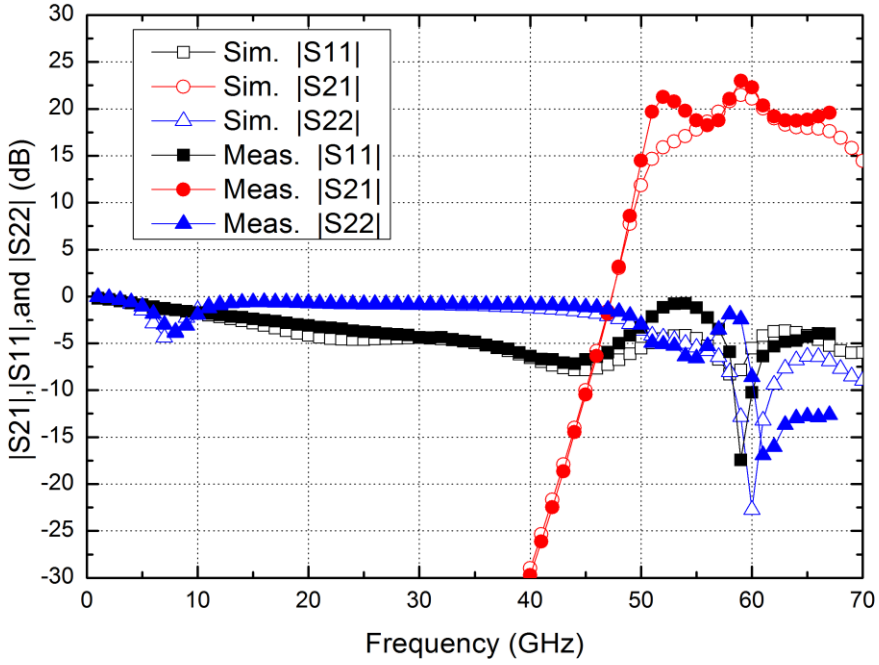

Fig. 2.28. Measured S-parameters in Rx mode.

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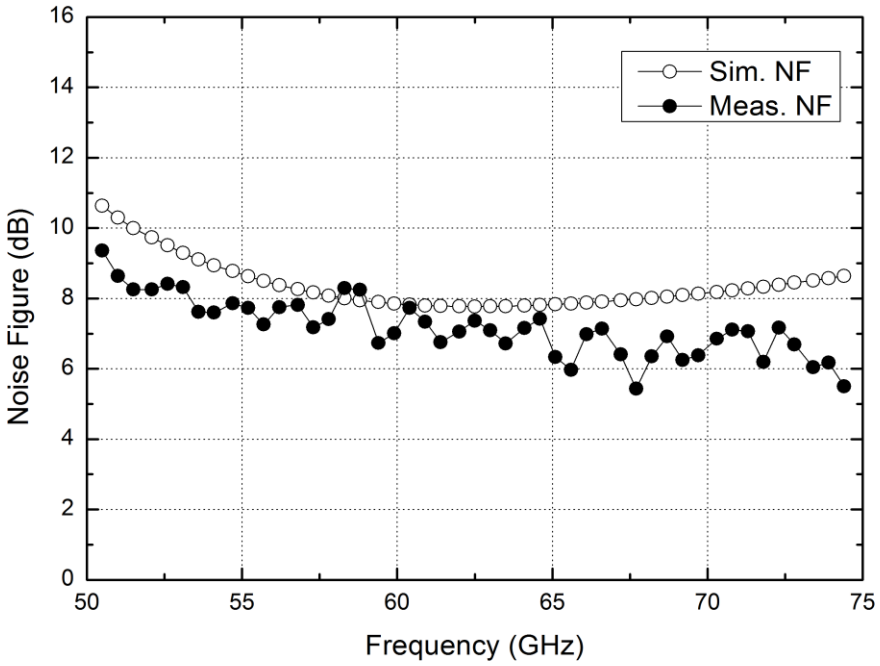

Fig. 2.29. Measured noise figure in Rx mode.

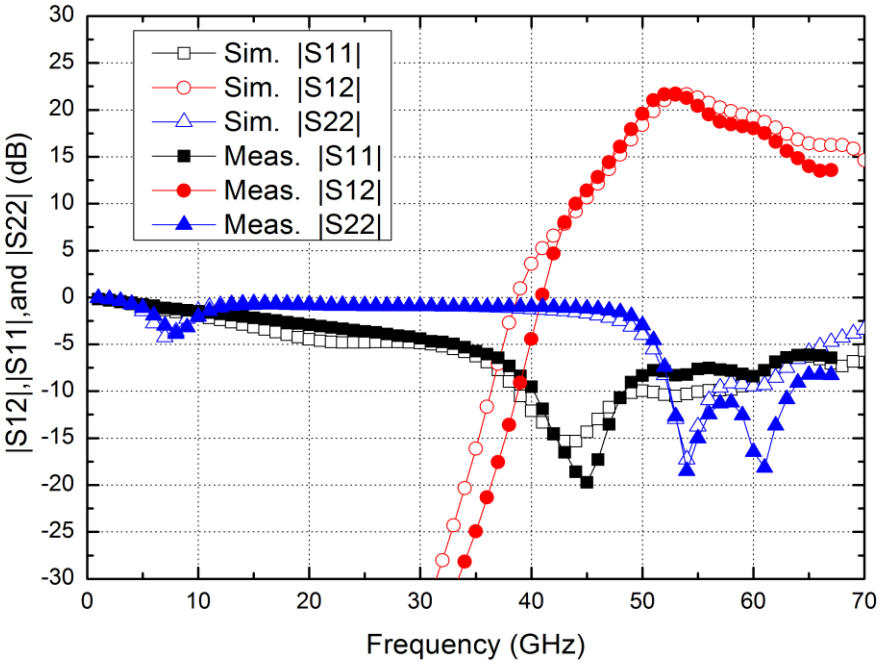

Fig. 2.30. Measured S-parameters in Tx mode.

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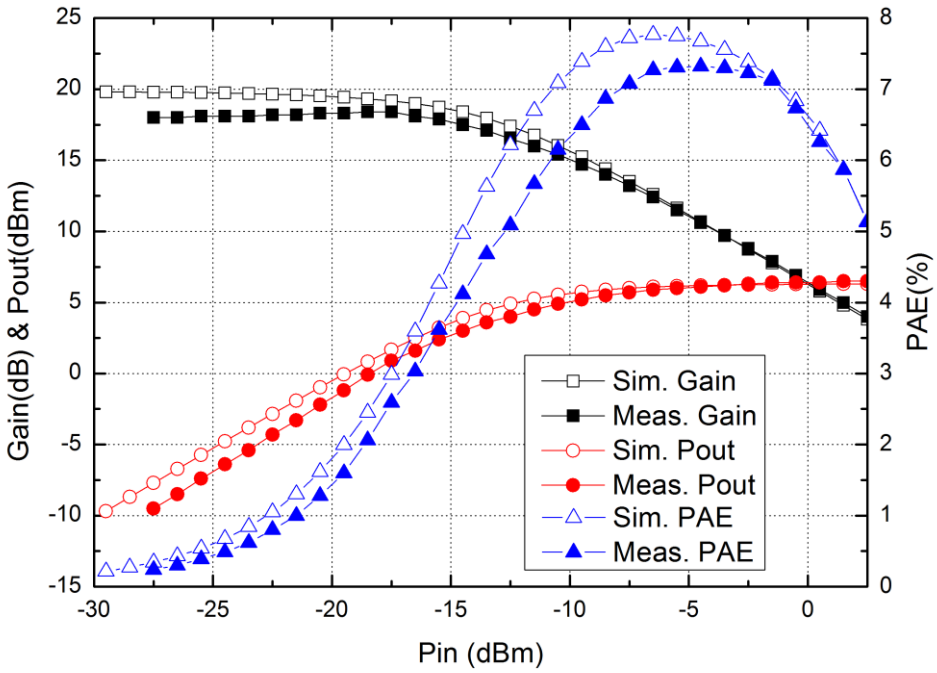

Fig. 2.31. Measured large-signal performance in Tx mode at 60 GHz.

Table 2.6. Measured bias condition in each mode.

	$V_{G,\,LNA}$ (V)	$V_{D,\,LNA}$ (V)	$I_{D,\,LNA}$ (mA)	$V_{G,\,PA}$ (V)	$V_{D,\,PA}$ (V)	$I_{D,\,PA}$ (mA)	P_{dc} (mW)
Rx Mode	0.6	1	15.3	0	0	0	15.3
Tx Mode	0	0	0	0.8	1	46	46

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From the measured *S*-parameters in Fig. 2.28, the gain around 52 GHz shows some differences between simulation and measurement. The reason is that the process variation degrades the performance of the bypass capacitor. In the 90-nm CMOS process, the capacitance of metal-insulator-metal (MIM) capacitor suffers a variation up to 20 %. In this design, the self-resonant frequency (SRF) of the bypass capacitor is 73 GHz. As the bypass capacitance is enlarged by 20% to estimate the process variation, the SRF will be 55 GHz. Note that the operated frequency is from 57 to 66 GHz in this BDA.

A long test line to verify the bypass network over wide frequency range has been added to simulate all possible impedance of bias path after the bypass capacitor. The original design shows a very low in-band gain variation when the test line is present. However, as the bypass capacitance is enlarged by 20%, the in-band gain variation is much higher due to the abrupt frequency response of the test line impedance. In this situation, the bypass capacitor does not offer a good in-band ac-short performance.

Fig. 2.32 shows the thru response of the shunt bypass capacitor. It can be observed that when the bypass capacitor is with process variation, the valley (SRF of the bypass capacitor) of frequency response moves toward lower band (from 73 GHz moves to 55 GHz). The ac-short performance is degraded in the operated frequency range (57-66 GHz), and the depth decreases up to 10 dB at high band (66 GHz). The original design did not consider the process variation. This can be avoided by adding the multi-way bypass capacitors to cover wider ac-short frequency to against the process variation for more robust design. However, adding the multi-way bypass capacitors occupies more chip area that becomes a design trade-off.

Fig. 2.33 shows the re-simulated results which the bypass capacitance is enlarged by 20% to estimate the process variation. Comparing with Fig. 2.28, the results are closer to the measured results.

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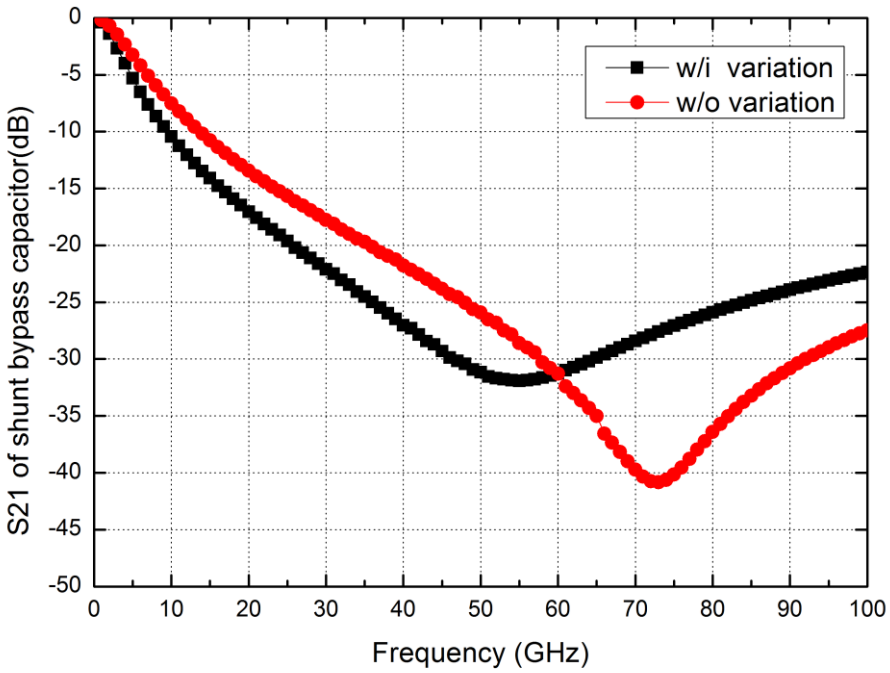

Fig. 2.32. Thru response of shunt bypass capacitor.

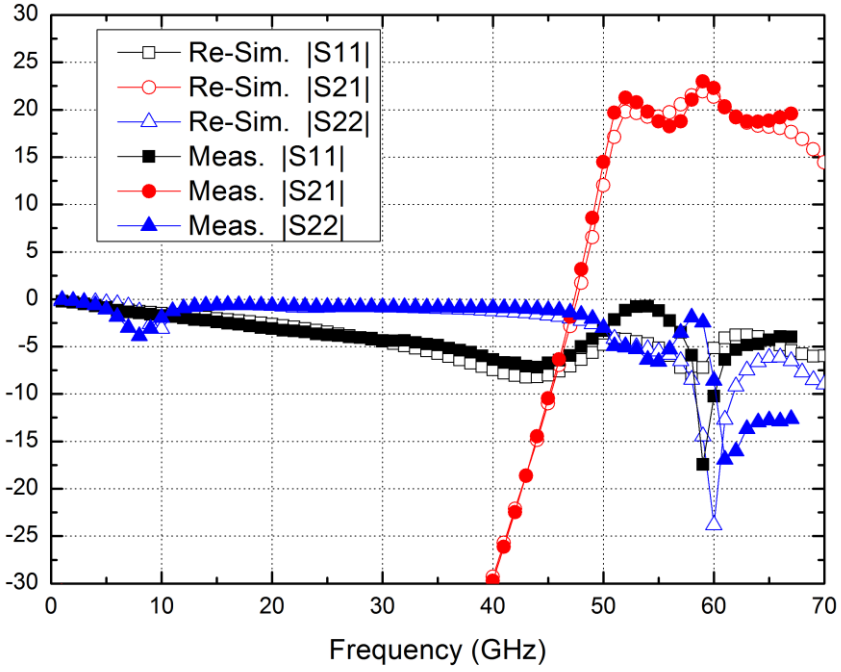

Fig. 2.33. Re-simulated S-parameters in Rx mode.

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2.6 Summary

In this chapter, a V-band switchless bidirectional amplifier based on common-source topology is presented. It consists a power amplifier, a low noise amplifier, and input/output junction networks. By using the impedance difference in the on-state and off-state of amplifiers, the junction networks are designed to transform the impedance into matched and isolated condition, respectively. Comparing with conventional bidirectional amplifiers realized by unidirectional amplifiers with SPDT switches, the loss is reduced, and hence the noise and power performance is improved. The chip size is 0.44 mm^2 with core size of 0.18 mm^2. The compact size improves the area efficiency while applied in large-scale phased array. Table 2.7 shows the comparison between the published switchless bidirectional amplifiers. In receiving mode, it demonstrate the highest gain and lowest noise figure above 50 GHz, except the work in [20] which is realized on InP process. In transmitting mode, it demonstrates the highest output power above 50 GHz, except in [22] and [23] which are realized in 65-nm CMOS and SiGe process, respectively. The bidirectional amplifier realized on CMOS process takes the advantages of lower cost and smaller chip area. It demonstrates competitive performance by comparing with the works realized in the high-cost (InP, GaAs, SiGe, and CMOS SOI) process. To the author's knowledge, this CMOS switchless bidirectional amplifier is the first Si-based switchless bidirectional amplifier in 60 GHz.

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Table 2.7. Performance comparison of the reported MMW switchless BDAs.

Ref.	Process	Topology	Frequency (GHz)	Rx Mode Gain (dB)	NF (dB)	Tx Mode Gain (dB)	OP_{1dB} (dBm)	P_{sat} (dBm)	P_{dc} (mW)	Chip Size (mm^2)
[20]	GaAs	CG	32-37	13	4.7	13	N/A	10	N/A	2.6
[21]	75-nm InP	CG	90-140	12	5	9	1*	5	15	0.46
[4]	0.12-μm SiGe	CE	41.7-45.8	34**	4.7	35**	8.5	9.5	26(R) 91(T)	1.28***
[23]	90-nm SiGe	CE	66-73	9.6	8.6	14.5	N/A	7.2	21(R) 85(T)	0.65
[25]	0.13-μm SiGe	CE	94	5.7	9.5	5.7	-2.8*	N/A	9.9	0.31
[20]	GaAs	CS	26-43	17	4	13	N/A	17	N/A	1.3
[22]	65-nm CMOS	CS	77.3	42**	9	42**	N/A	9.2	20.2(R) 71.5(T)	0.69***
[26]	0.13-μm CMOS	DA	3-20	10	6.5	10	8	16	68	0.81
[28]	0.18-μm CMOS	DA	21.6-31	6.4	9.1	6.4	4.3	12	46.8	0.28
[29]	0.12-μm SiGe	BCWA	77-90	16	N/A	16	N/A	N/A	65.8	0.47
[30]	45-nm CMOS SOI	BCWA	40/85	4.6	N/A	4.5	-2.9	3.9	N/A	0.48
This work	**90-nm CMOS**	**CS**	**57-66**	**18.2**	**8**	**13.5**	**3.6**	**6.5**	**15.3(R) 46(T)**	**0.44**

*Inference from the measured IP_{1dB} with the gain in Tx mode.
**Including the IF amplifiers.
***Total transceiver area.

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Chapter 3 Design of a 60-GHz Bidirectional Amplifier in 40-nm CMOS with Transformer-Coupled and Neutralization Technique

3.1 Introduction

In the previous chapter, a switchless BDA using TFMS line matching network is proposed. In this chapter, another BDA realized in 40-nm CMOS process and based on differential common-source topology is demonstrated. In this BDA, we use transformer to constitute the matching network. Comparing with the TFMS line, the transformer is compact in size and suitable for differential topology. Besides, the operated bandwidth and stability are enhanced by adding the neutralized capacitors.

In [22], the antenna is shared by the 77-GHz PA and LNA. By using the impedance difference between on/off states of the amplifiers, the junction transformers work as a matching network and isolation network, respectively. Besides, the differential topology and transformer-coupled method are used in each amplifier design, as shown in Fig. 3.1. In this chapter, the 60-GHz BDA design refers to the PA/LNA of [22]. In [22], the input of PA is connected to modulator, and the output of LNA is connected to the demodulator, thus the balun is not necessary in the back-end side. In this application in the system, the BDA is applied in the bidirectional phased array, thus both the antenna port and back-end port are shared.

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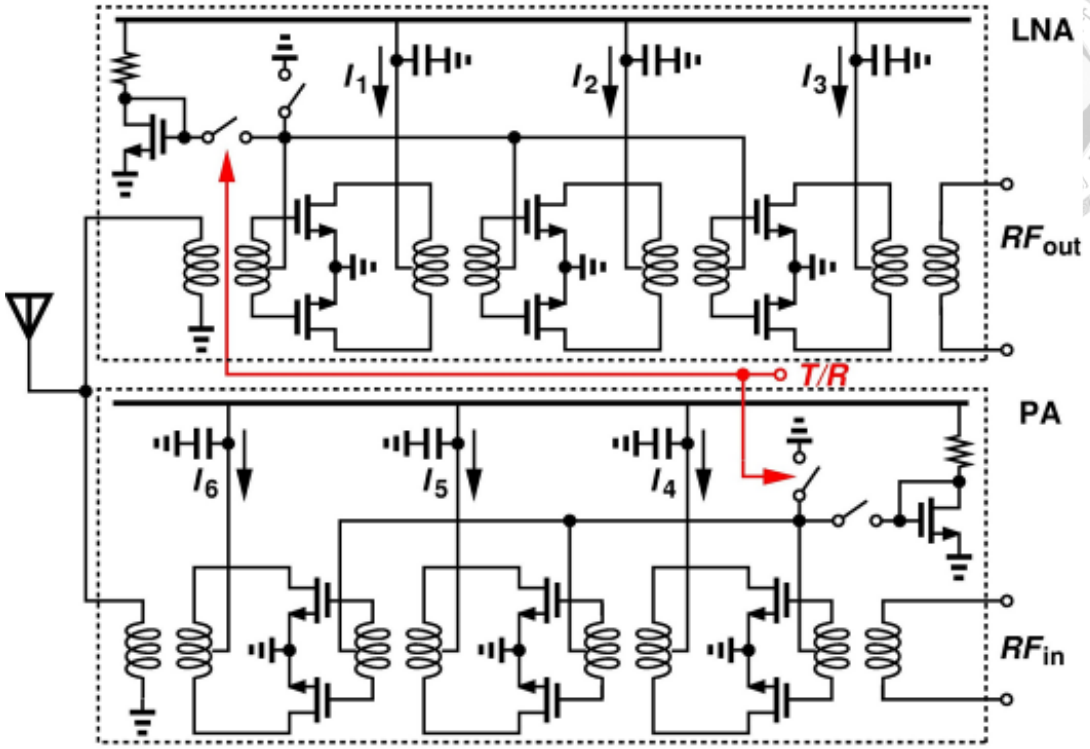

Fig. 3.1. The PA/LNA sharing the antenna port [22].

3.2 Circuit Design

In the TSMC 40-nm LP process, the transistor have three different threshold voltage options: low threshold voltage transistor (LVT), standard threshold voltage transistor (SVT), and high threshold voltage transistor (HVT). Table 3.1 shows the performance comparison of the three devices in the same power consumption. The LVT device shows that it is the most suitable choice to constitute the PA because it has the highest power capability in the same dc current. The HVT device shows less advantage by comparing with the other two, but its high I/O impedance is a useful property that it can reduce the loading effect. These will be discussed in the design of LNA part (section 3.2.2).

The differential topology is commonly used in analog amplifiers, which has the following advantages: (1) rejection of the common mode noise, (2) natural virtual short

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property at the center point that eliminate the odd order harmonics, and (3) extension of the voltage swing range that achieve effective power combining. These properties are very useful for improving the linearity and power efficiency. Besides, differential amplifier is especially suitable to be integrated with the transformers. Comparing with single-ended topology, the differential topology not only offers higher gain but higher output power. In the driver and power stage, the effective power combining enhances the linearity and power capability. In the BDA design, the differential topology is used for constituting each gain stage, and the transformers are used for constituting the inter-stage matching and the dc biasing network. Fig. 3.2 shows the total schematic of the proposed BDA. The circuit can be divided into PA part, LNA part, transformers design, and neutralized capacitors design, which will be described in the following sections.

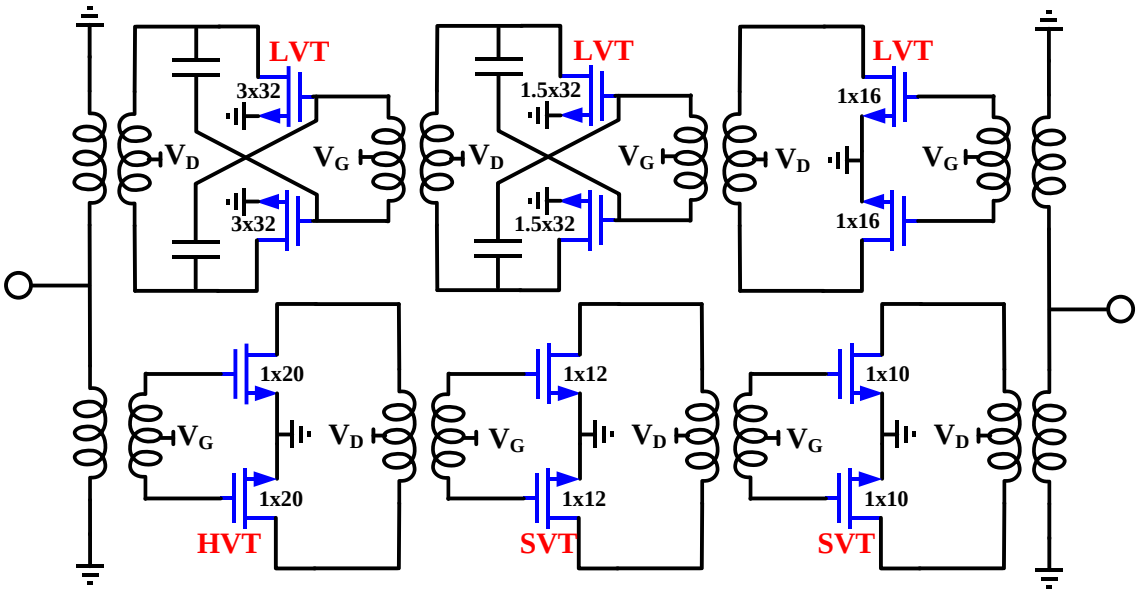

Fig. 3.2. Schematic of proposed BDA.

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Table 3.1. Performance comparison of the device options.

Device Type	HVT	SVT	LVT
Device Size	1 μm × 16 finger		
Drain Current (mA)	2		
Gate Voltage (V)	0.864	0.694	0.563
MaxGain (dB)	9.13	9.29	9.86
NF_{min} (dB)	1.93	1.46	1.7
OP_{1dB} (dBm)	-0.48	2.18	3.07
$Z_{opt,power}$ (Ω)	148+148j	75+136j	78+123j

3.2.1 PA part

The PA part is consisted of three differential common-source stages. Comparing with the 90-nm version BDA which is consisted of 4-stage gain cells in each amplifier, the 40-nm version BDA only needs 3-stage to achieve 16-dB gain due to the better transistor performance of the 40-nm device. Fig. 3.3 shows the PA schematic.

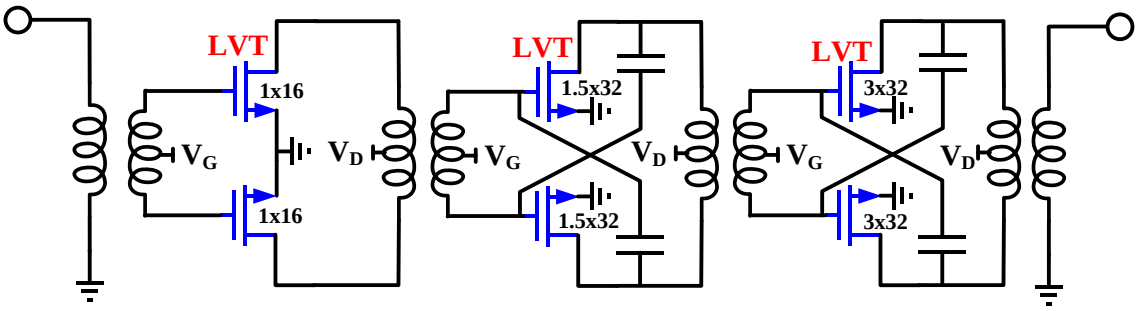

Fig. 3.3. Schematic of the PA part.

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A. Device Selection

As mentioned in previous chapter, the device selection in the output stage of PA is much critical due to the trade-off between many parameters. In individual PA design, the off-state impedance is not very critical. However, in the BDA design, we must think of this in advance.

The LVT devices are used for constituting each stage in the PA part due to the best large-signal performance as mentioned before. In the output stage, and the 3 μm×32 finger device is chosen for 9-Ω real part impedance in the off-state, and the impedance of the differential topology is equivalent to the series of the two terminals, thus total real part impedance is 18-Ω, which can be converted to around 200 Ω by a transformer. Besides, in the load-pull simulation, the single-ended 3 μm×32 finger device can offer OP_{1dB} of on up to 8 dBm. In other words, the OP_{1dB} can achieve 11 dBm in an ideally differential combining.

The driver stage uses 1.5 μm×32 finger device, which is chosen to half width of the output stage to offer adequate power to drive the output stage. The input stage is a gain cell to provide a high gain with low power consumption. Consider the power capability to drive the driver stage, 1 μm×16 finger device is chosen as one third of the width for the driven stage.

Table 3.2 lists the design parameters of the chosen devices. The size ratio among the stages is 1:3:6. All the transistors are biased at gate voltage equal to 0.65 V which makes the transistor operated in the class A region for linearity. At the inter-stage, the transformers function as the matching and biasing networks, and the design is introduced in section 3.3.2.

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Table 3.2. Design parameters among the stages.

Stage	1st	2nd	3rd
Device Type	LVT	LVT	LVT
Device Size (μm)	1x16	1.5x32	3x32
Drain Current (mA)	3.29	9.62	18.8
Gate Voltage (V)	0.65		
Drain Voltage (V)	1.1		
Z_{in} (Ω)	10-150j	4-45j	6-21j
$Z_{out,on}$ (Ω)	0-99j	5.6-48j	2-21j
$Z_{out,off}$ (Ω)	27-227j	10-84j	9-45j
$Z_{opt,power}$ (Ω)	57+86j	18+45j	20+24j
OP_{1dB} (dBm)	4.14	6.79	7.96

B. Neutralized Capacitor Design

Neutralization mitigates the intrinsic gate-drain feedback of each transistor for increased power gain and reverse isolation [32]. The concept of neutralization is using a pair of cross-coupled capacitors that produces the negative capacitance, thus the gate-to-drain capacitor (C_{gd}) of the transistor is eliminated, as shown in Fig. 3.4. By reducing the capacitance of the main feedback path, the stability is improved. Besides, the gain can be boosted to close the unilateral condition. The technique is especially useful in the wider devices which has larger parasitic capacitance.

In this BDA, we use the neutralization in the last two stages of PA, which have the largest two devices in the circuit. The capacitors are implemented by horizontal interdigital metal plates, as shown in Fig. 3.5. The top 5 metal layers (M6 to M10) are

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used for composing the capacitors, the designed cross-coupled capacitance are 10 fF and 40 fF, which are used for neutralizing the 1.5 μm×32 finger and 3 μm×32 finger devices, respectively.

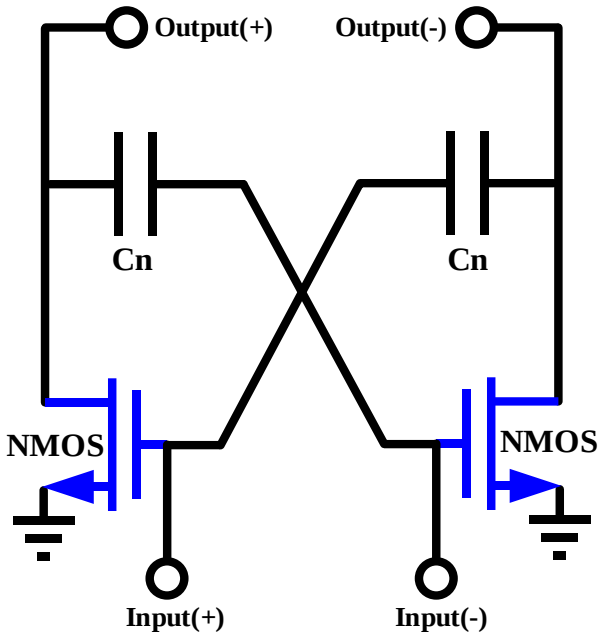

Fig. 3.4. Neutralized differential pair by cross-coupled capacitors.

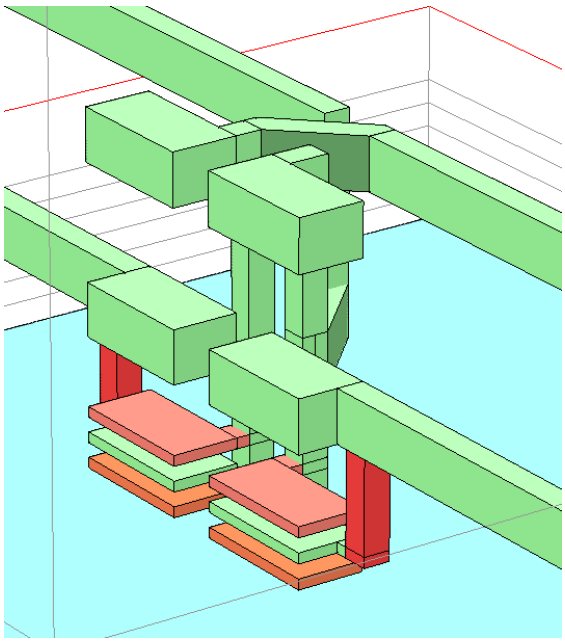

Fig. 3.5. EM structure of the neutralized capacitors.

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3.2.2 LNA part

As the PA part, the LNA part consists of three differential common-source stages. The LNA schematic is shown in Fig. 3.6.

In LNA design, the most critical parameter is the noise figure. However, in the bidirectional application, the loading effect cannot be ignored, thus the off-state impedance of devices must be considered. The selection of LNA input stage is as important as the PA output stage. The design target is high impedance in the off-state and minimizes the noise figure in the on-state.

According to Table 3.1, the SVT device has the lowest noise figure. However, the well-optimized performance of Tx mode in this application is expected, thus the loading effect is the first consideration. Table 3.3 lists the parameters comparison over different size of HVT/SVT devices. The HVT device has the highest impedance transformation ratio with an acceptable noise figure, and thus HVT device is chosen to design the input stage. The smaller device size has the higher gain and impedance. But it needs a larger inductor to match the parasitic capacitor. The larger inductor will produce higher loss due to its larger parasitic resistance. Furthermore, the larger parasitic capacitance results in the lower self-resonant frequency (SRF), and hence restricts the operated bandwidth of the inductor. The larger device will have the lower off-state impedance and higher current, which is not helpful for the small-signal operation. From the considerations mentioned above, the 1 μm×20 finger device is chosen to compose the input stage, which has the lower minimum noise figure (NF_{min}), medium impedance and medium current consumption.

The LNA is designed for operating in the small-signal region, thus the linearity is not a main concern. There is more freedom for the device selection than that for the PA,

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thus we can pay more attention on the gain flatness and reduce the loading effect. A 1 μm×12 finger SVT device is used in the second stage to achieve the balance of gain flatness and impedance matching. 1 μm×10 finger SVT device is chosen for the third stage. It is smaller than the previous stage due to its higher off-state impedance and the compensation of the gain flatness in the previous two stages.

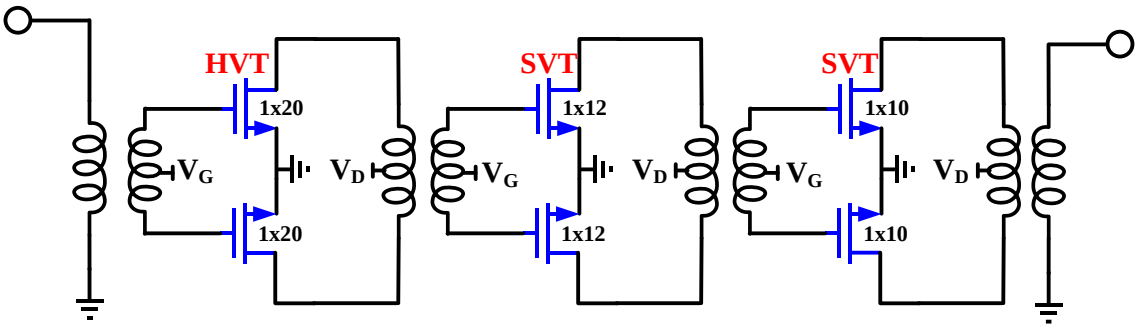

Fig. 3.6. Schematic of the LNA part.

Table 3.3. Design parameters of HVT/SVT devices.

Device type	HVT					SVT		
Device Size (μm)	1×12	1×16	1×20	1×24	1×28	1×12	1×16	1×20
Gate Voltage (V)	0.93							
Drain Voltage (V)	1.1							
NF_{min} (dB)	1.923	1.916	1.915	1.918	1.924	1.598	1.592	1.592
MaxGain (dB)	9.833	9.808	9.79	9.773	9.757	10.783	10.765	10.751
Drain Current (mA)	2.12	2.83	3.52	4.22	4.91	4.13	5.49	6.84
$Z_{s,opt}$ (Ω)	8+208j	7.2+158j	2+125j	3.1+106j	2.5+91j	4.2+197j	3.5+149j	2.6+120j
$Z_{in,on}$ (Ω)	12.3-205j	11-155j	3.1-125j	4.6-104j	3.7-90j	6.7-195j	5.5-147j	4-119j
$Z_{in,off}$ (Ω)	32-326j	25-248j	17+200j	16-167j	14-144j	26-324j	20-246j	16-199j

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3.3 Transformer Design

In conventional RF CMOS amplifier design, TFMS or co-planar waveguide (CPW) has been commonly used for impedance matching and realizing the biasing path. Recently, the RF amplifiers designed with the on-chip transformers become popular [32]-[40]. These designs use two magnetic-coupled coils to realize the impedance matching and biasing. Moreover, by using the transformer as the power combiner, it demonstrates higher efficiency and better operating bandwidth than conventional direct-combine or Wilkinson-combine [34]. Besides, the transformer has the properties of bidirectional conversion between single-ended and differential signal, and natural dc-blocking between stages that avoid the extra loss produced by the dc-block capacitors. Therefore, the transformer is widely used in modern PA design.

3.3.1 Introduction

The transformer is composed of two magnetic-coupled coils, as shown in Fig. 3.7. When the time-varying current i_1 flows into the primary coil L_1, the time-varying magnetic field is induced by L_1. The time-varying magnetic field induces current i_2 in coil L_2. And thus the signal and power have transmitted across the coils. The induced voltage or induced electromotive force (EMF), is proportional to the circumference of the coil, thus the induced voltage to current ratio can be controlled by using different coil turn ratio $N_1 : N_2$, then the impedance transformation is achieved. The sinusoidal steady-state behavior of the transformer can be expressed as:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega M \\ j\omega M & j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3.1}$$

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and

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{N_1}{N_2} = n \tag{3.2}$$

Thus the impedance transformation ratio is:

$$\frac{v_2 / i_2}{v_1 / i_1} = n^2 \tag{3.3}$$

The relationship between coupling factor *k* and mutual inductance *M*:

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{3.4}$$

Designing the transformers for high frequency operation, especially in integrated circuits, the parasitic effect cannot be ignored. The integrated transformer model proposed by [41] have been commonly used, as shown in Fig. 3.8. By including the parasitic effect on the integrated circuit process, this model is more realistic than the ideal model in Fig. 3.7. The main part of the model is composed by two individual inductors with the series resistance R_1 and R_2 as the lossy terms. The coupled terms are mutual inductance *M* and mutual-capacitance C_m. By winding the coils for compact layout, the self-capacitance C_p of each inductor is included. The substrate relative lossy terms are R_{si}, C_{si} and C_{ox}, which express the parasitic resistance, parasitic capacitance of silicon substrate, and the parasitic capacitance of oxide, respectively.

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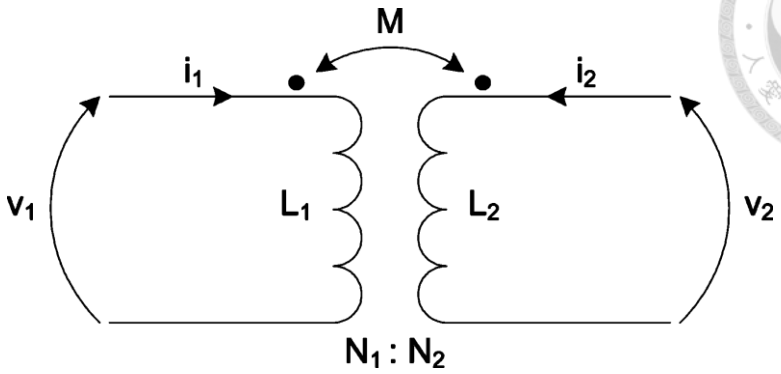

Fig. 3.7. Ideal transformer model [41].

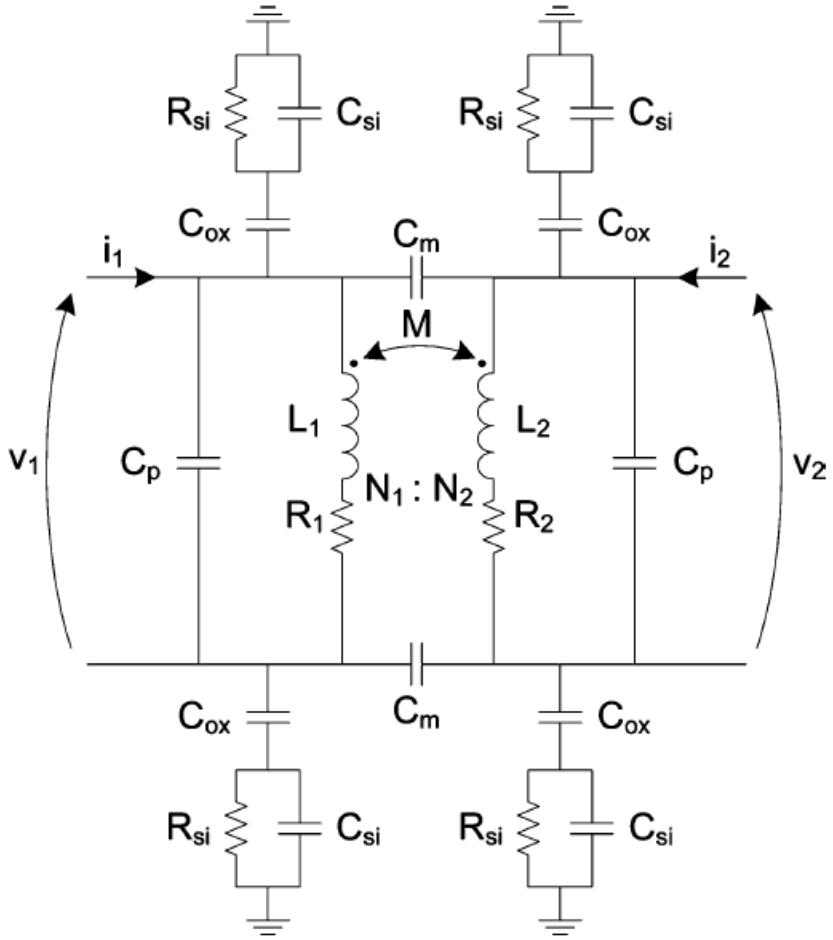

Fig. 3.8. Integrated transformer model [41].

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The coupling factor is relative to the line width and the spacing of the two inductors. The higher coupling factor results in lower loss for signal coupling. Considering the efficiency, *k* must be as large as possible. The different designed *k* might cause different mutual inductance and impedance, which can be designed for optimizing the trade-off between the efficiency and impedance matching.

The coupling factor could be raised by increasing the line width and reduce the spacing. However, the larger coupling area raises the mutual capacitance C_m that pushes the self-resonant frequency (SRF) toward lower band. Beyond the SRF, the small-signal property of the transformer become capacitive, which is not desired. The transformer must be inductive to match the capacitive transistor. As a results, operating below SRF must be confirmed.

As shown in Fig. 3.9, there are two coupled methods for the integrated transformers, edge-coupled (interleaved) and broadside-coupled (stacked), express the horizontally and vertically coupled, respectively. The edge-coupled takes the advantage of using the same metal layer, the metal loss can be minimized by realizing the coils on the ultra-thick-metal (UTM) layer which is 3.5 μm thickness. However, the minimal horizontal spacing is restricted by foundry design rules from reliability concern. The minimum allowed horizontal spacing is 1 μm on UTM layer. The testing structure of edge-coupled transformer is shown in Fig. 3.10, which uses minimum line width (2 μm) and spacing (1 μm) in order to achieve the maximum coupling. The coupling factor can be derived from simulated Z-parameters with equation (3.1) and (3.4):

$$k = \frac{M}{\sqrt{L_1 L_2}} = \sqrt{\frac{|Z_{21} \times Z_{12}|}{|Z_{11} \times Z_{22}|}} \tag{3.5}$$

doi:10.6342/NTU201603106

By using Sonnet EM solver, the simulation shows the maximum coupling factor is around 0.3, with 3.8 dB minimum insertion loss. On the other hand, the broadside-coupled has the nearer distance between the two coupled lines, the vertical distance between the top two metal layers is 0.74 μm, which is less than the limitation of edge-coupled. The tested structure of broadside-coupled transformer is shown in Fig. 3.11, which uses the top two metal layers with 0.74-μm vertical spacing. The simulation shows that, the coupling factor is 0.87 with 1.7 dB minimum insertion loss while operated near the SRF. Figs. 3.12 and 3.13 show the coupling factor and minimum loss (maximum gain) comparison between the two structures. In order to realize higher mutual coupling and reduce coupling loss, we use the topology of broadside-coupled in all the transformers design in this BDA.

Note that in Fig. 3.12, in order to confirm the transformer is operated below the SRF, the imaginary part of Z-parameters is used to calculate the coupling factor. In this situation, the parasitic resistance is ignored, thus the abrupt variation of coupling factor at the SRF due to the LC resonance can be easily observed. This ignored resistance does not affect the accuracy of the coupling factor much for the frequency below SRF. In fact, the self-resonant phenomenon is not very obvious if there is the parasitic resistance. The frequency response of the transmission coefficient (S_{21}) plotted in Fig. 3.13 includes the parasitic effect, thus the frequency response is smoother than that of the coupling factor (Fig. 3.12).

doi:10.6342/NTU201603106

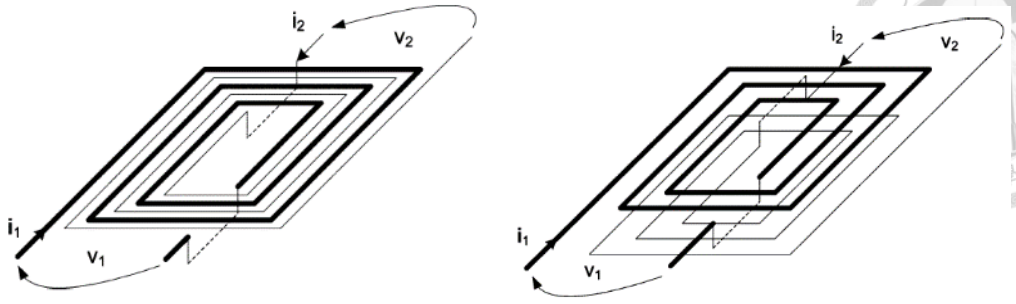

Fig. 3.9. Edge-coupled (left) and Broadside-coupled (right) transformer [41].

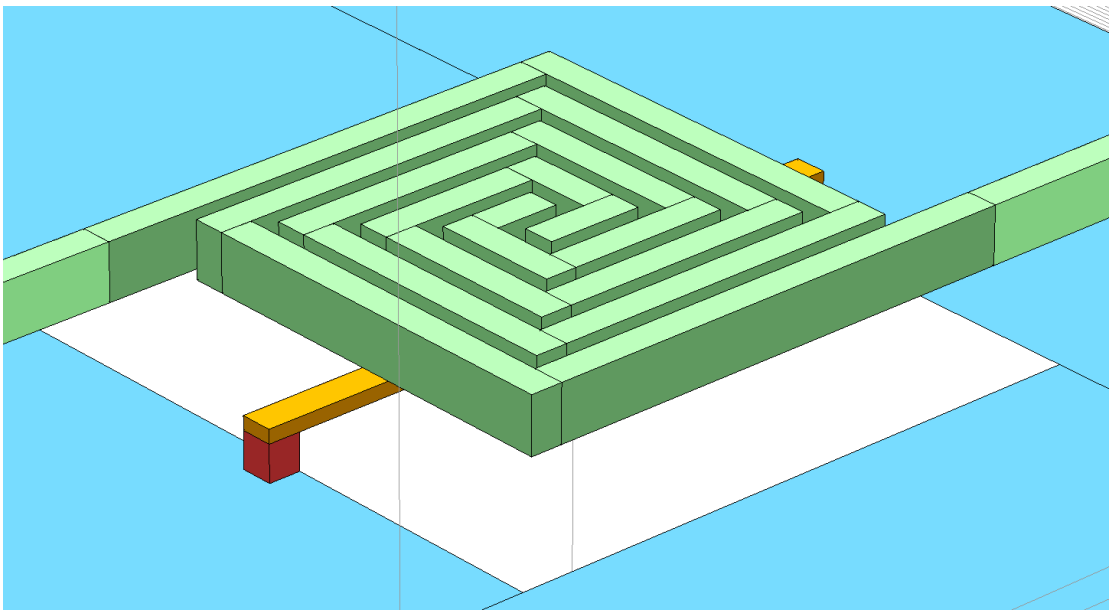

Fig. 3.10. EM structure of the edge-coupled transformer.

doi:10.6342/NTU201603106

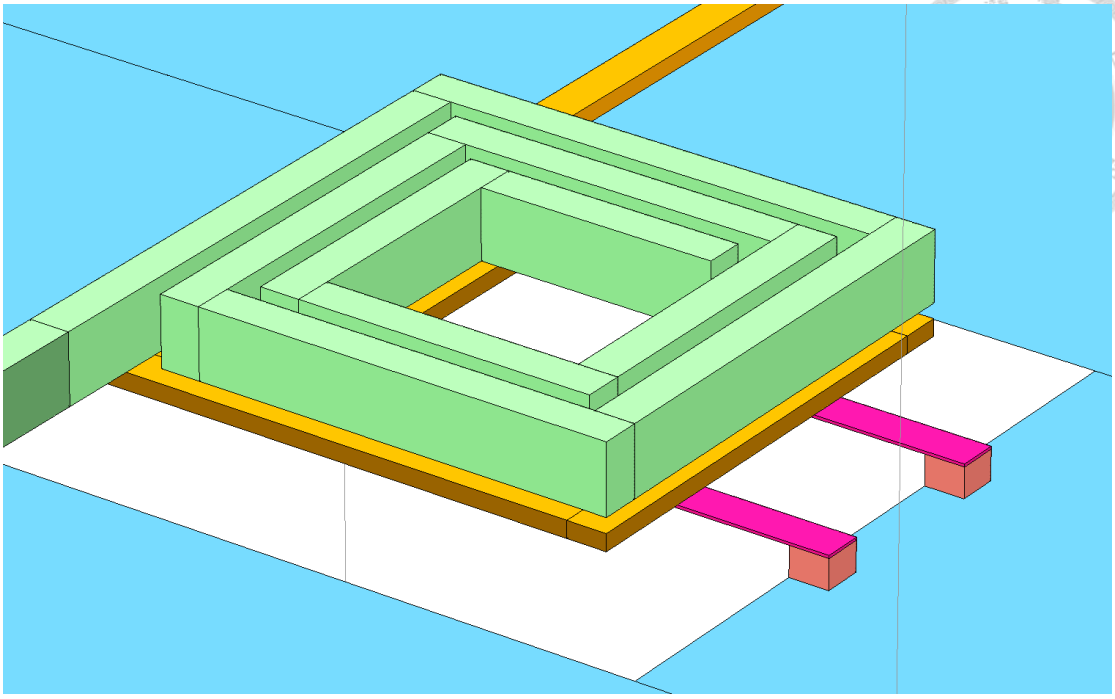

Fig. 3.11. EM structure of the broadside-coupled transformer.

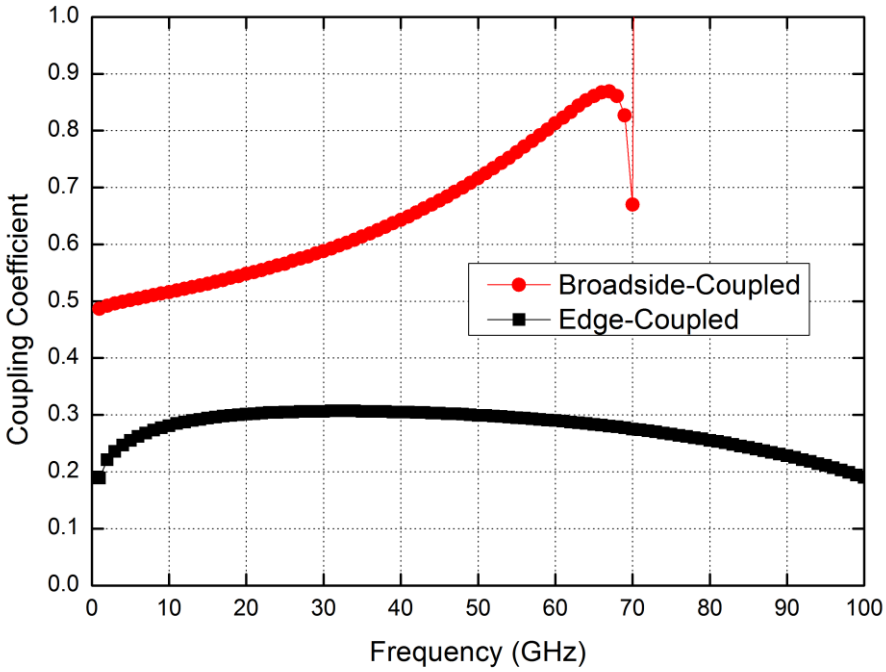

Fig. 3.12. Comparison of the coupling factor.

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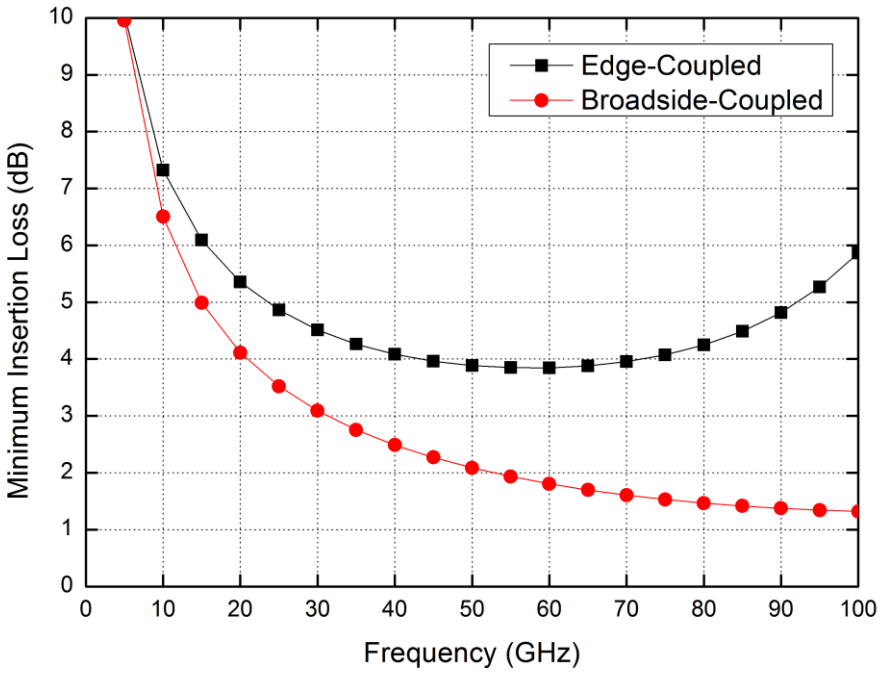

Fig. 3.13. Comparison of the minimum insertion loss.

In the TSMC 40-nm LP CMOS process, there are 1 poly and 10 metal layers (1P10M) for interconnection, and it is possible to realize a transformer with up to 1:10 turn ratio by using broadside-coupled. However, the coupling loss may dramatically increase with such a large turn ratio. Fortunately, in this BDA design, the impedance transform ratio is smaller than 10, thus the turn ratio is smaller than 1:3. Two top thick metal layers can be used to reduce the metal loss and keep the distance away from the lossy substrate.

3.3.2 Inter-stage Transformer

By matching the differential gain cells, the inter-stage transformers are designed in differential type. The differential transformer takes the advantage of the ground

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connection being enhanced by the virtual short. Besides, the dc bias can be injected into the center tap of the differential transformers, and the fundamental-short bypass capacitors can be replaced by the harmonic-short bypass capacitors, which have only half capacitance and half chip area by comparing with the single-ended circuits.

According to the device selection as mentioned before, the turn ratio could be designed by the I/O impedance of each stage. In the inter-stage, the design steps as following:

(1) select the devices type, size, and bias condition,

(2) extract the devices impedance for gain, noise, or power matching,

(3) decide the coils turn ratio from the real part impedance of the gain stages,

(4) decide the coils radius or circumference from the imaginary part impedance of the devices. In brief, using the "coupled" part to match the real impedance, and using the "uncoupled" part to match the imaginary impedance.

(5) accomplish the perfect match condition between devices and transformers, as Fig. 3.14. However, it is hard to achieve for wideband operation. Considering the gain flatness, the matching frequency has some mismatch among the inter-stage networks for wideband response.

(6) fine-tune the transformer for better performance (e.g. gain, noise figure, stability, linearity, or gain flatness).

As the results, the 3-D plot of the final design for four inter-stage transformers (two for PA, and two for LNA) as shown in Figs. 3.15 to 3.18.

doi:10.6342/NTU201603106

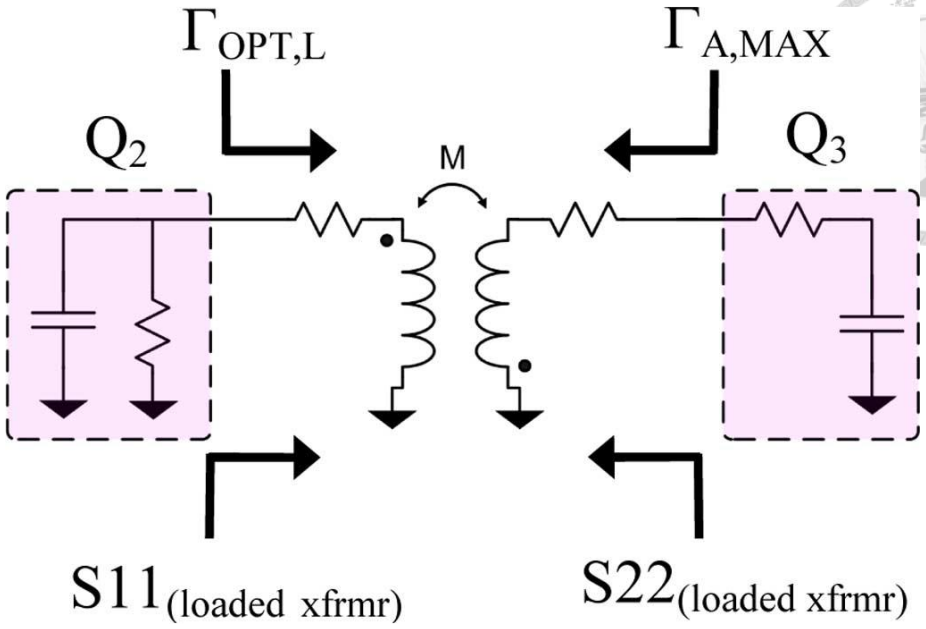

Fig. 3.14. Design goal of the inter-stage transformer [40].

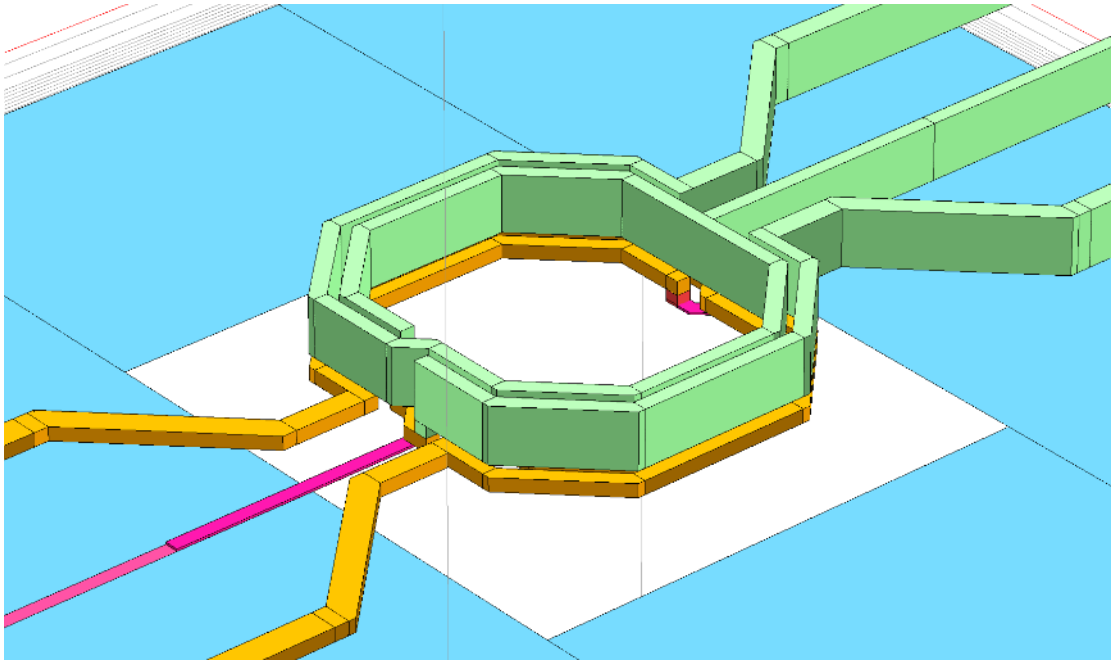

Fig. 3.15. Differential 2:2 transformers between 1st and 2nd stage of PA.

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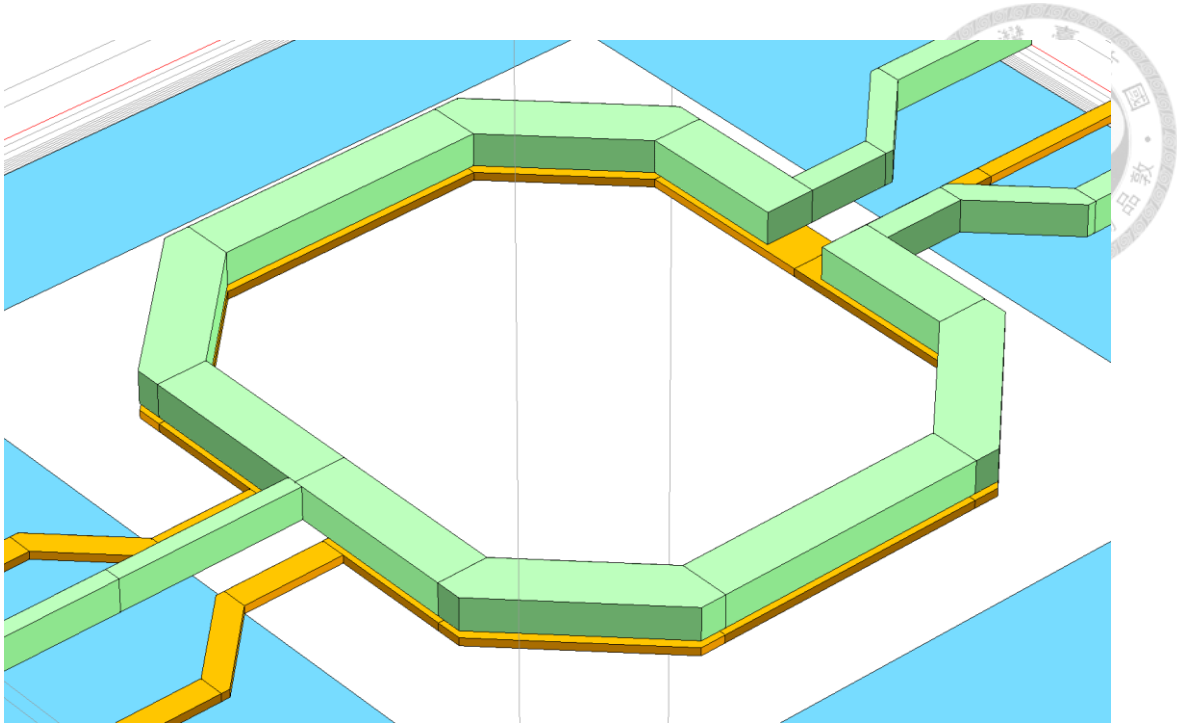

Fig. 3.16. Differential 1:1 transformers between 2nd and 3rd stage of PA.

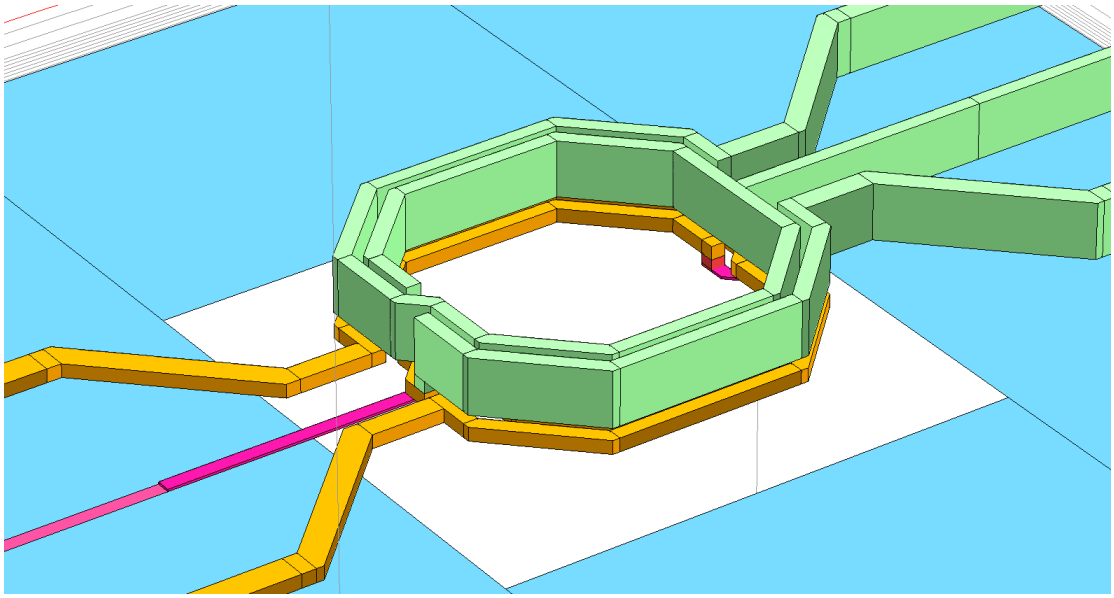

Fig. 3.17. Differential 2:2 transformers between 1st and 2nd stage of LNA.

doi:10.6342/NTU201603106

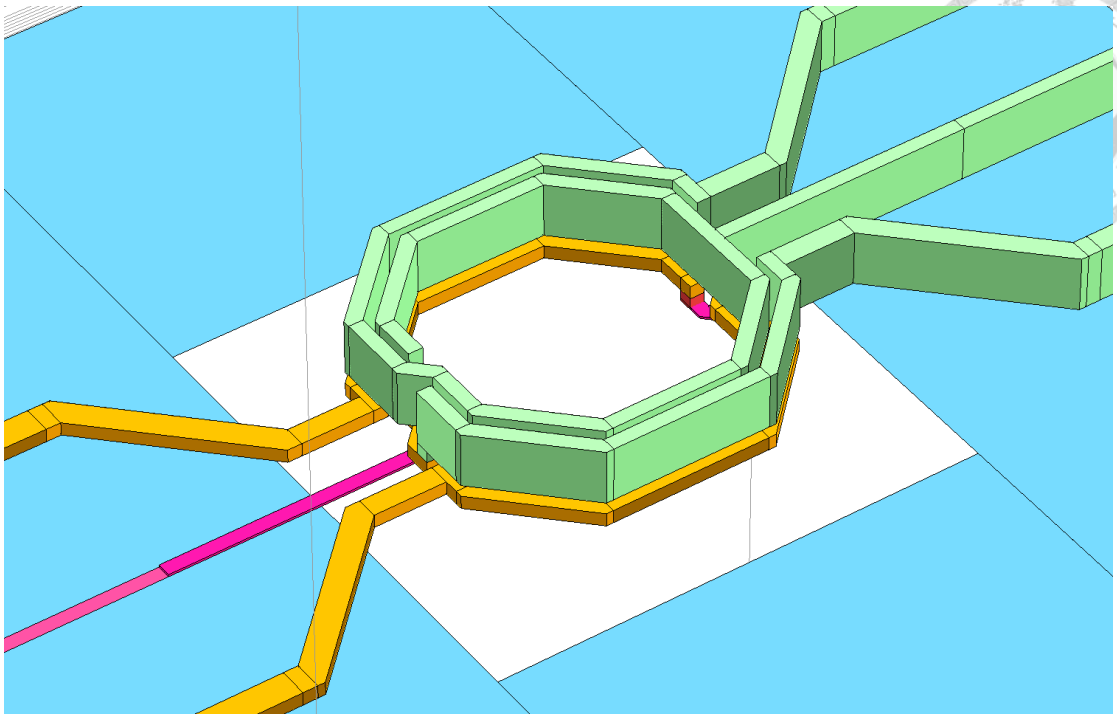

Fig. 3.18. Differential 2:2 transformers between 2nd and 3rd stage of LNA.

3.3.3 I/O Junction Transformer

The most critical part in the BDA is the junction network between the PA and LNA. As mentioned in chapter 2, the design targets of the junction network are transforming the I/O impedance of the (1) turned-on amplifiers to 50 Ω, and (2) turned-off amplifiers to high impedance. Besides, the junction network offers the noise matching or power matching in each mode. The design targets in Rx mode and Tx mode are described in Figs. 3.19 and 3.20, respectively.

In order to achieve the maximum power of the PA, the junction transformer of PA output is designed to convert the 50 Ω to the load-pull impedance. In the junction transformer design, the differential output of the PA is converted to single-ended with higher impedance for the PA arm. In the LNA arm, the single-ended input is converted to differential with the noise matching. The design steps are the same as those in the inter-

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stage, which were descripted in previous section. However, in the junction design, the off-state impedance is an additional restriction. Tables 3.4 and 3.5 show the amplifier impedance in Rx mode and Tx mode, respectively. It can be observed that the most difficult part is the small impedance difference between on-state and off-state of the PA, and it is a big challenge to achieve the design targets by a passive network. For less than 2 dB loading loss, the impedance must be larger than 100 Ω. It means the transformation ratio should be greater than 10, and it will cause higher loss and sharper frequency response, which restricts the PA power efficiency and gain flatness. Same as the LNA input, the input impedance must be transformed to higher impedance. Fortunately, the device size in LNA first stage is much smaller than that of PA output stage, so the off-state impedance is high enough. Thus the impedance transformation ratio is low enough to realize. Figs. 3.21 to 3.24 show the junction matching network design.

Tables 3.6 and 3.7 list the simulated insertion loss and isolation of the junction transformers in each mode. Using the same analysis of section 2.2, the isolation range is from 8.2 to 12.7 dB, and the insertion loss is around 5 dB. Note that the insertion loss is higher than that of the 90-nm BDA in section 2.2 because the differential topology introduces extra combined/divided loss.

Another concern is the LNA input impedance variation as the PA operates in high output power. Fig. 3.25 plots the input impedance of turned-off LNA versus the PA output power in Tx mode. It can be observed that the LNA remains in enough high input impedance ($|Z| > 100\ \Omega$) while the PA output power is below 15 dBm, thus the LNA with the junction transformer will not restrict the output power of PA.

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Table 3.4. Impedance transformation by the junction network in Rx mode.

Rx Mode	PA (Off)		LNA (On)	
Impedance (Ω)	Input	Output	Input	Output
w/o matching	45.9-549j	7.4-54j	104-142j	124-451j
w/ matching	45.6+80.2j	90.5-76.2j	45.7+12.8j	70.3+0.1j

Table 3.5. Impedance transformation by the junction network in Tx mode.

Tx Mode	PA (On)		LNA (Off)	
Impedance (Ω)	Input	Output	Input	Output
w/o matching	58.8-360j	10.4-72.3j	171-346j	77.5-811j
w/ matching	76.9+11.8j	213-37.5j	94.2+55j	103+89.8j

Table 3.6. Insertion loss and isolation of the junction network in Rx mode.

Rx Mode	Isolation of PA arm (dB)		Insertion Loss of LNA arm (dB)	
	Input	Output	Input	Output
	12.5	8.4	2.8	4.9

Table 3.7. Insertion loss and isolation of the junction network in Tx mode.

Tx Mode	Insertion Loss of PA arm (dB)		Isolation of LNA arm (dB)	
	Input	Output	Input	Output
	5.7	5.2	8.2	12.7

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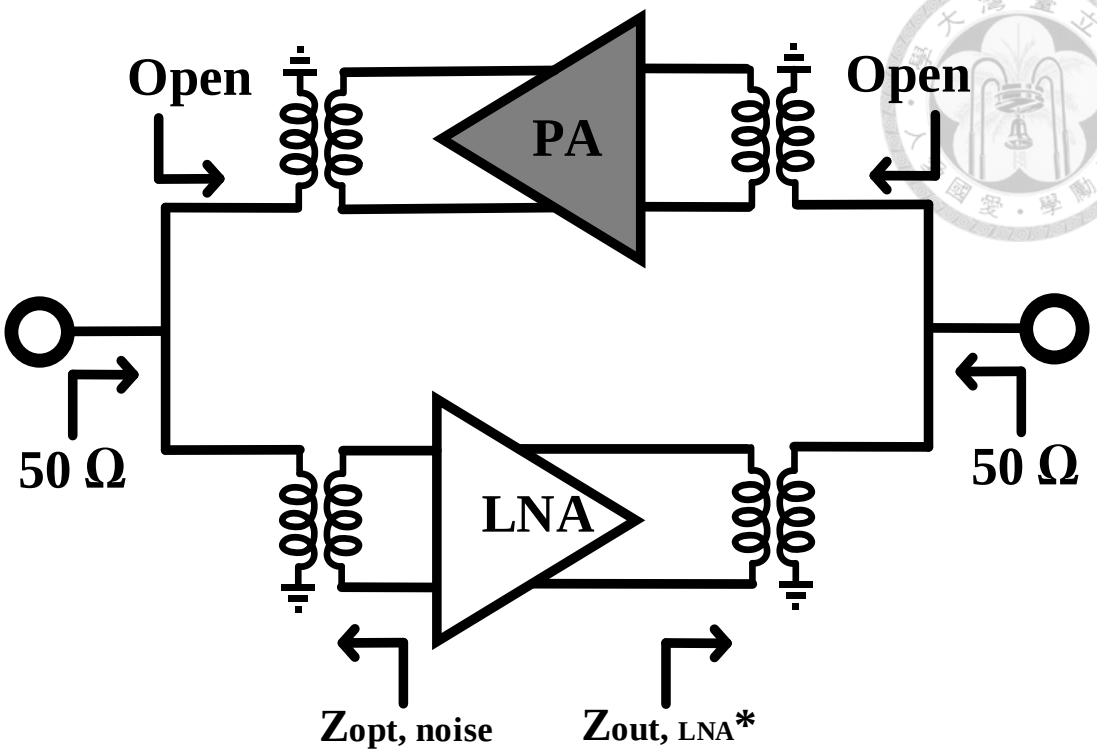

Fig. 3.19. Design goal of the junction transformer in Rx mode.

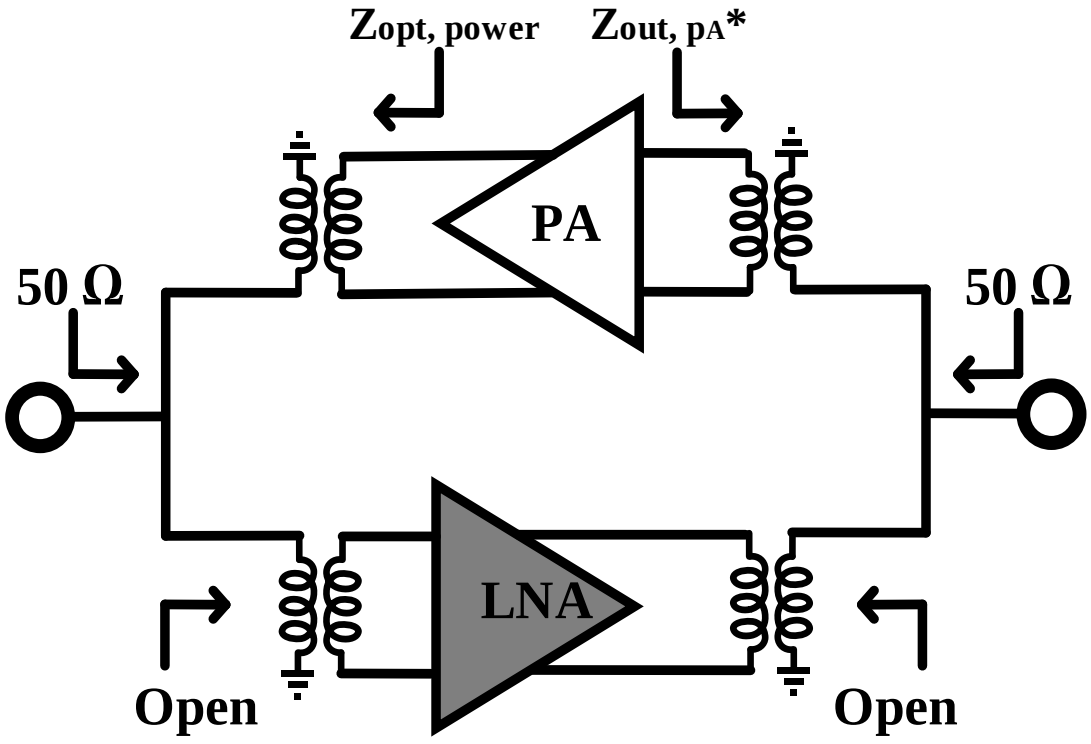

Fig. 3.20. Design goal of the junction transformer in Tx mode.

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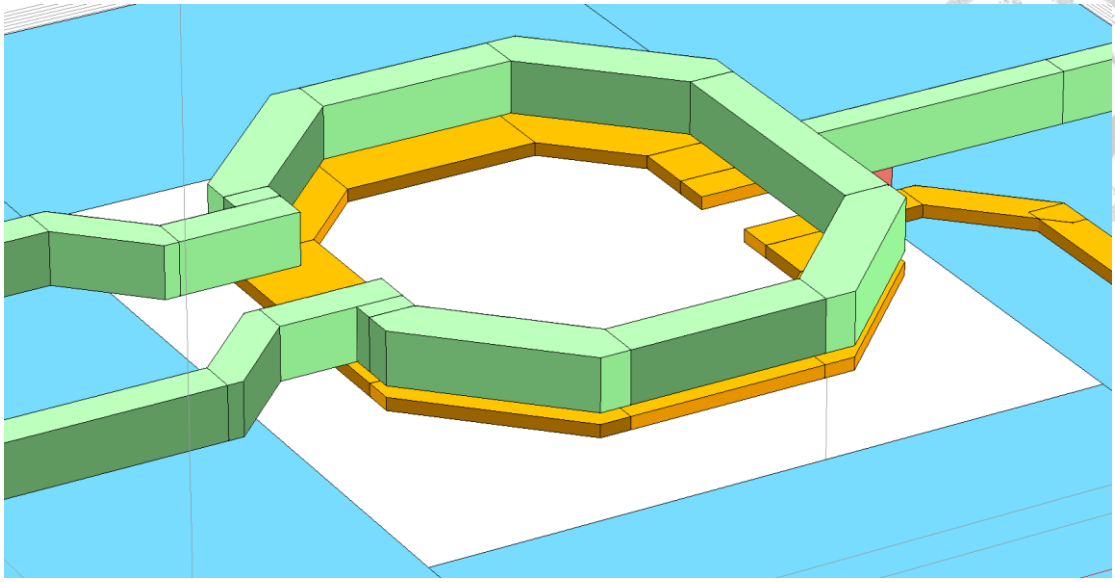


Fig. 3.21. Single-ended to differential 1:1 transformer at PA output junction.

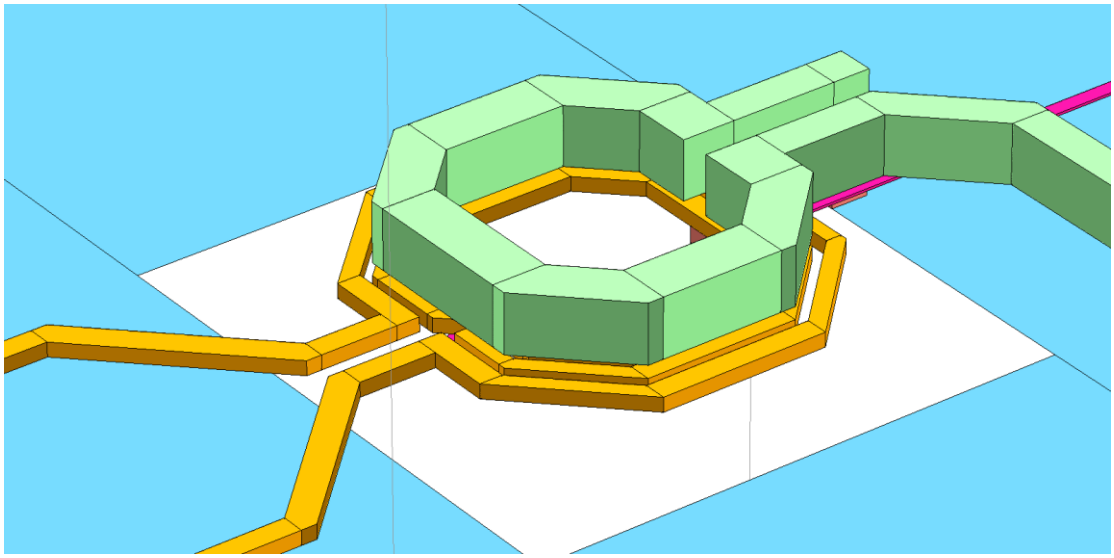


Fig. 3.22. Single-ended to differential 1:3 transformer at PA input junction.

doi:10.6342/NTU201603106

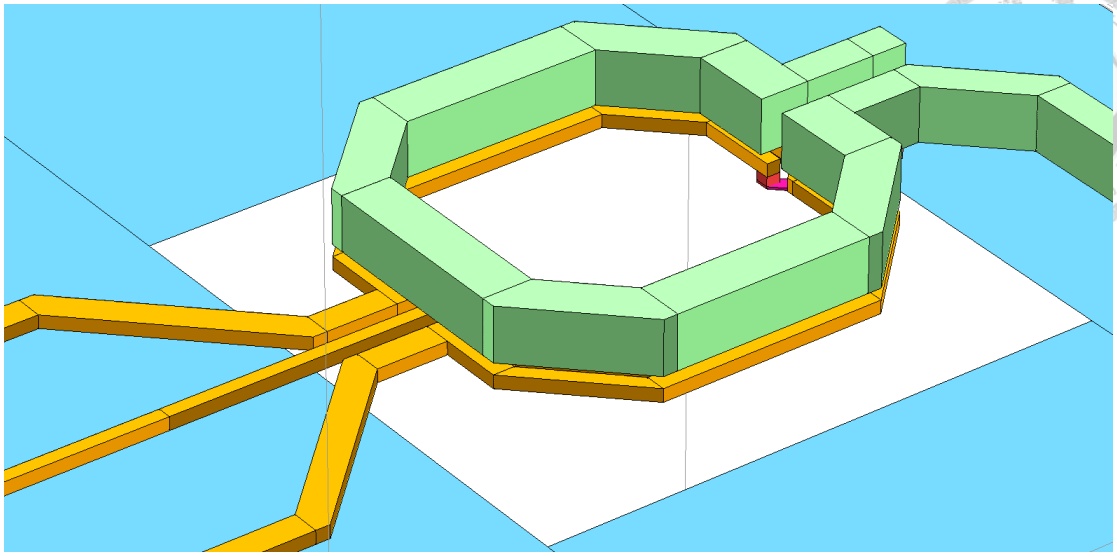


Fig. 3.23. Single-ended to differential 1:2 transformer at LNA input junction.

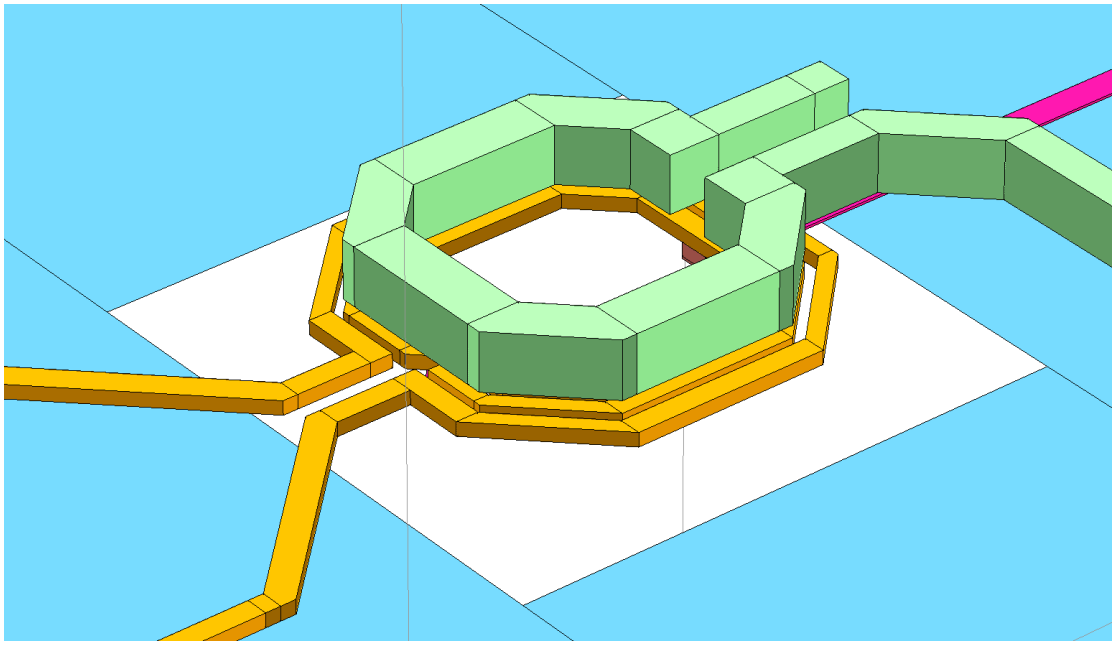
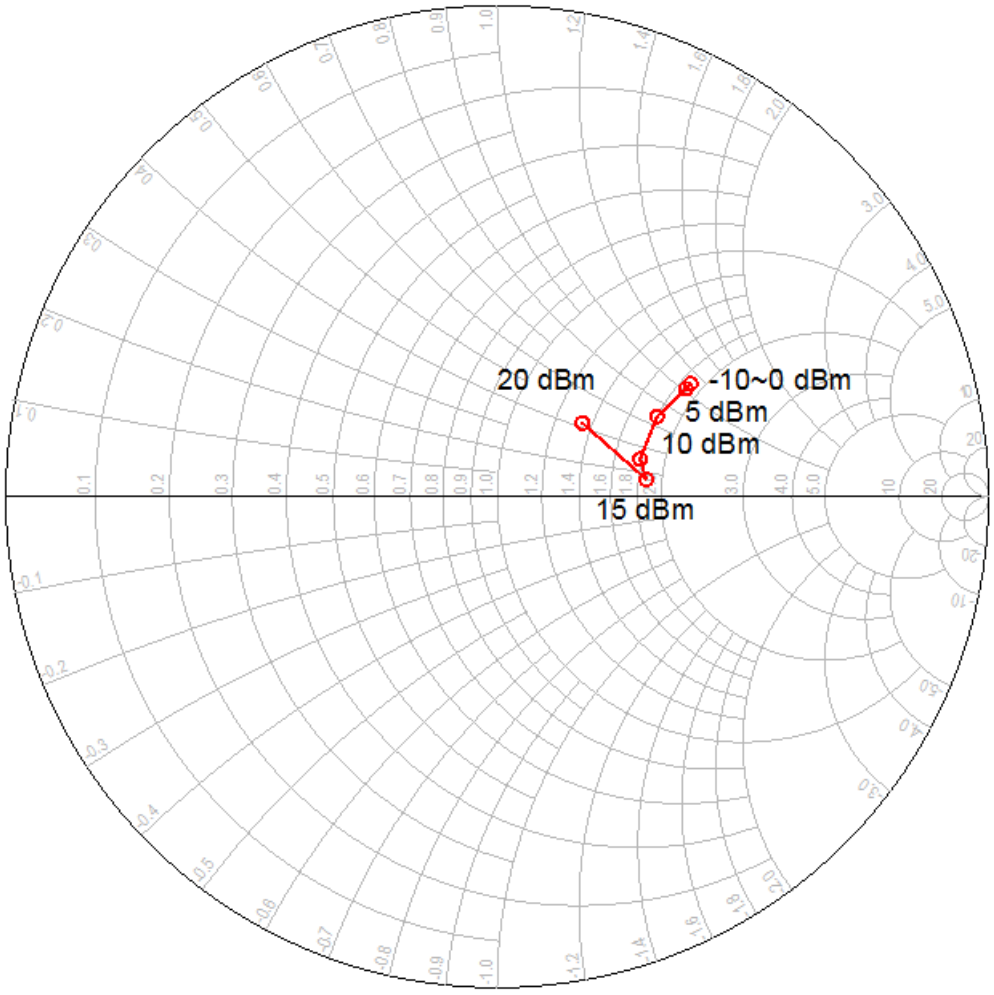


Fig. 3.24. Single-ended to differential 1:3 transformer at LNA output junction.

doi:10.6342/NTU201603106



Frequency = 60 GHz

Pin_Rx (dBm)	Zin_LNA (Ohm)
-10.000	94.117 + j54.671
-5.000	94.034 + j54.363
0.000	94.047 + j51.425
5.000	90.025 + j33.898
10.000	89.313 + j15.024
15.000	93.233 + j7.288
20.000	67.124 + j21.264

Fig. 3.25. Input impedance of LNA versus the PA output power in Tx mode.

doi:10.6342/NTU201603106

3.4 Chip Layout and Simulation Performance

The circuit is designed with Agilent Advance Design System (ADS), and all the passive components including transformers and neutralized capacitors are simulated by Sonnet EM solver. The chip layout is shown in Fig. 3.26, and the chip size is 0.57 mm × 0.36 mm.

Fig. 3.27 shows the simulated S-parameters in Rx mode. The gain is above 14 dB from 57 to 66 GHz. Fig. 3.28 shows the simulated noise figure, the noise figure is below 8 dB from 57 to 66 GHz.

Fig. 3.29 shows the simulated S-parameters in Tx mode. The gain is above 16 dB from 45 to 66 GHz, and above 16.2 dB from 57 to 66 GHz. Fig. 3.30 shows the simulated large-signal performance at 60 GHz, the OP_{1dB} is 4.6 dBm, and saturated output power is 11.1 dBm with peak PAE of 12.1 %. The bias condition of the simulation as shown in Table 3.8.

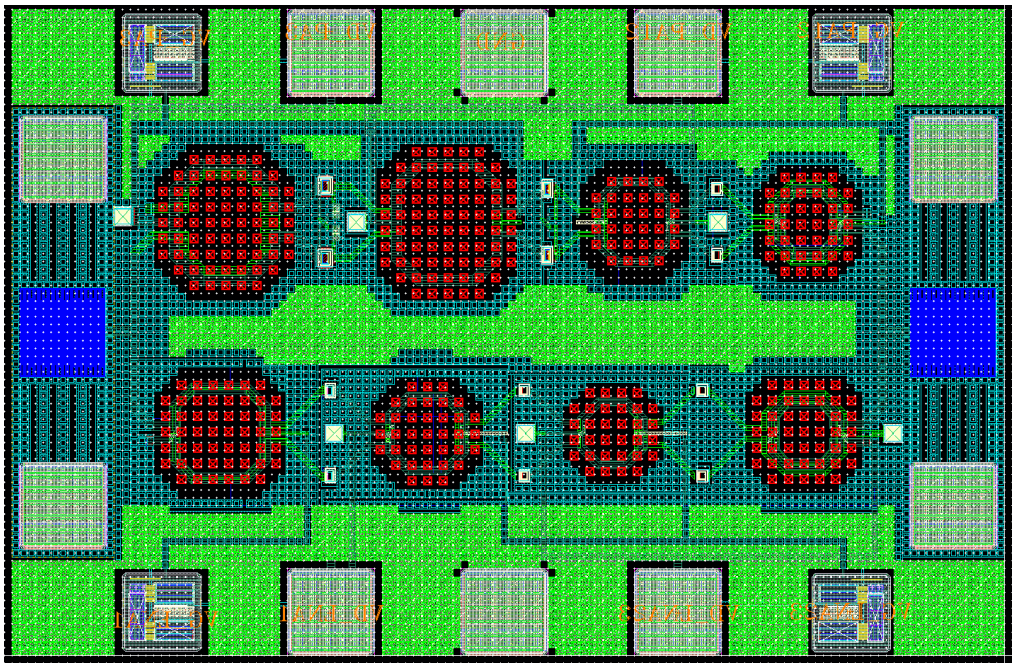


Fig. 3.26. Chip layout of the BDA.

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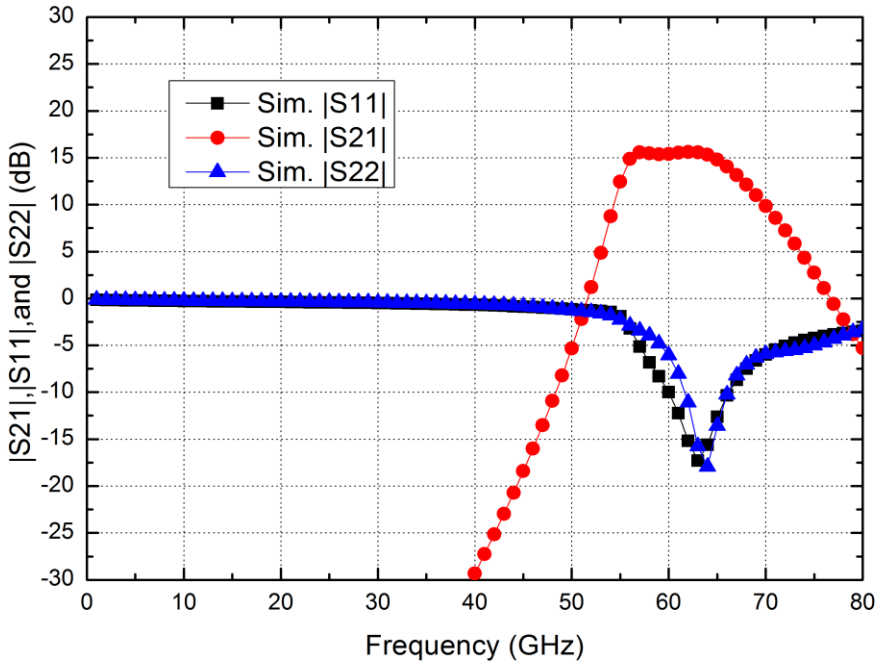

Fig. 3.27. Simulated S-parameters in Rx mode.

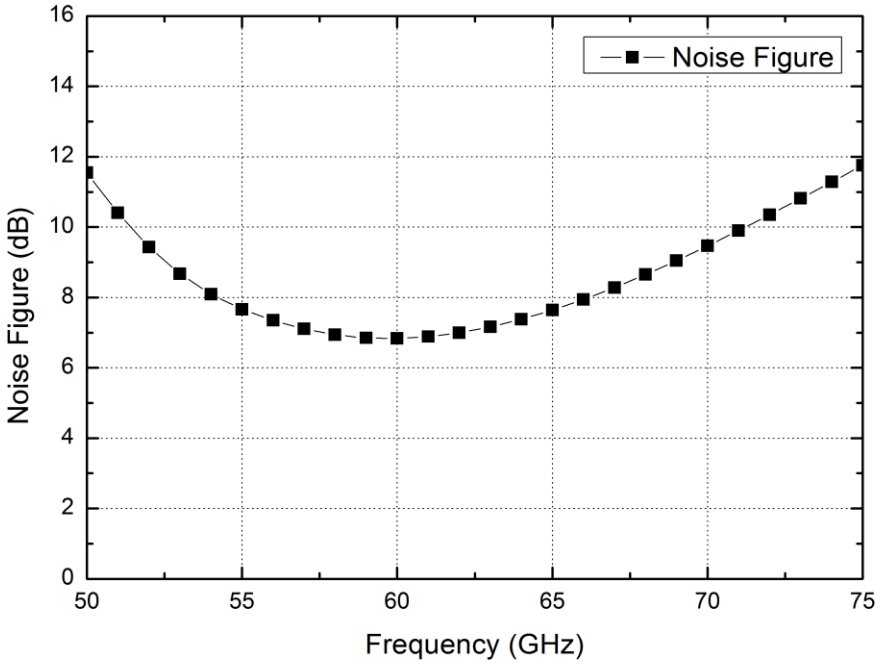

Fig. 3.28. Simulated noise figure in Rx mode.

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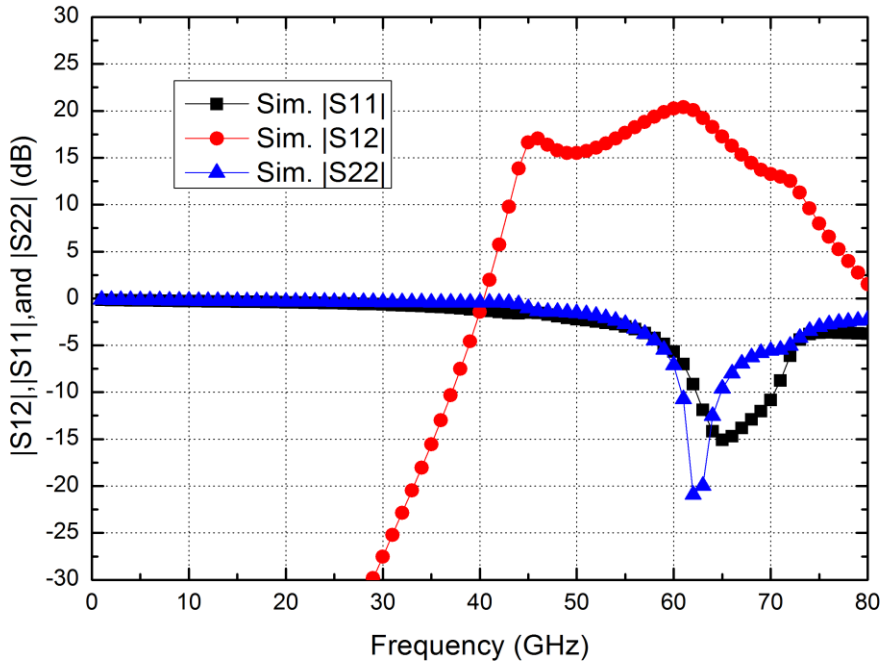

Fig. 3.29. Simulated S-parameters in Tx mode.

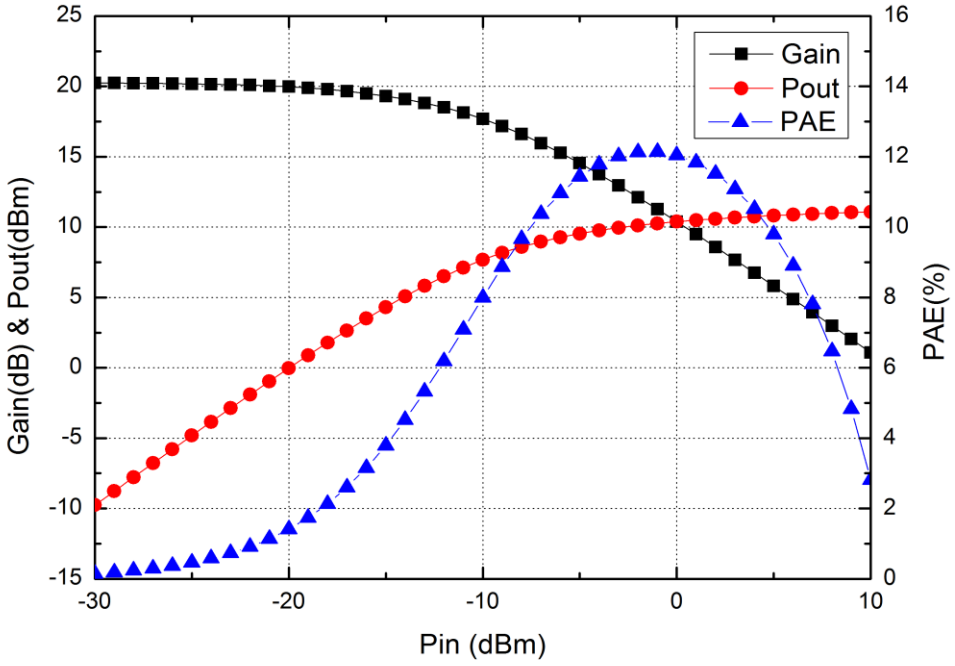

Fig. 3.30. Simulated large-signal performance in Tx mode at 60 GHz.

doi:10.6342/NTU201603106

Table 3.8. Bias condition of the simulation.

	$V_{G,\,LNA}$ (V)	$V_{D,\,LNA}$ (V)	$I_{D,\,LNA}$ (mA)	$V_{G,\,PA}$ (V)	$V_{D,\,PA}$ (V)	$I_{D,\,PA}$ (mA)	P_{dc} (mW)
Rx Mode	0.93	1.1	22	0	1.1	0	24.2
Tx Mode	0	1.1	0	0.65	1.1	63.4	69.7

3.5 Stability Analysis

The stability check is simulated by Agilent Advance Design System (ADS) with build-in tool “S-Probe”. Figs. 3.31 to 3.33 show the check results among the 3-stage of LNA in Rx mode. Figs. 3.34 to 3.36 show the check results among the 3-stage of PA in Tx mode. All the stability indices are smaller than 1 in magnitude; the BDA is stable in each mode.

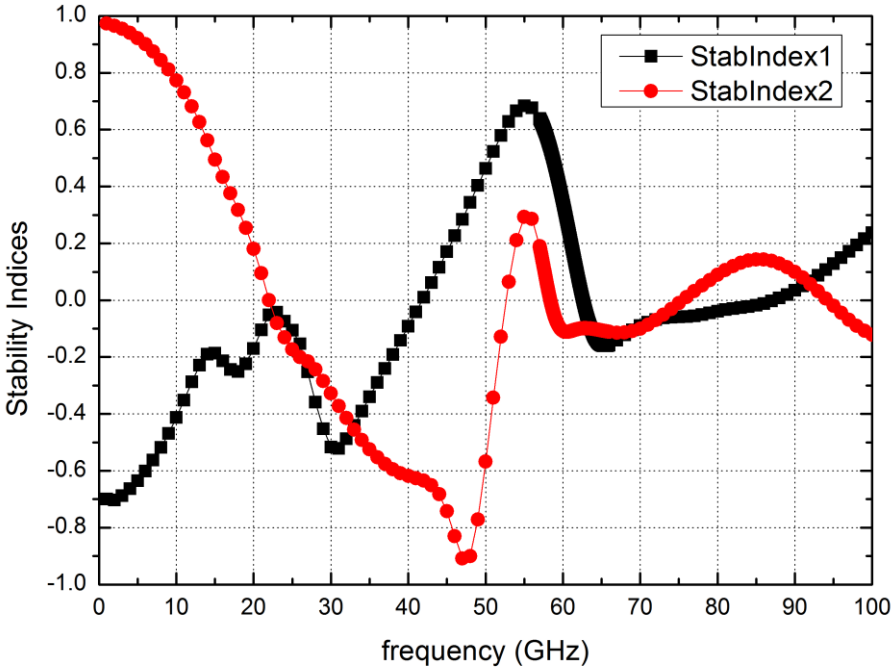

Fig. 3.31. Stability indices of LNA 1st stage.

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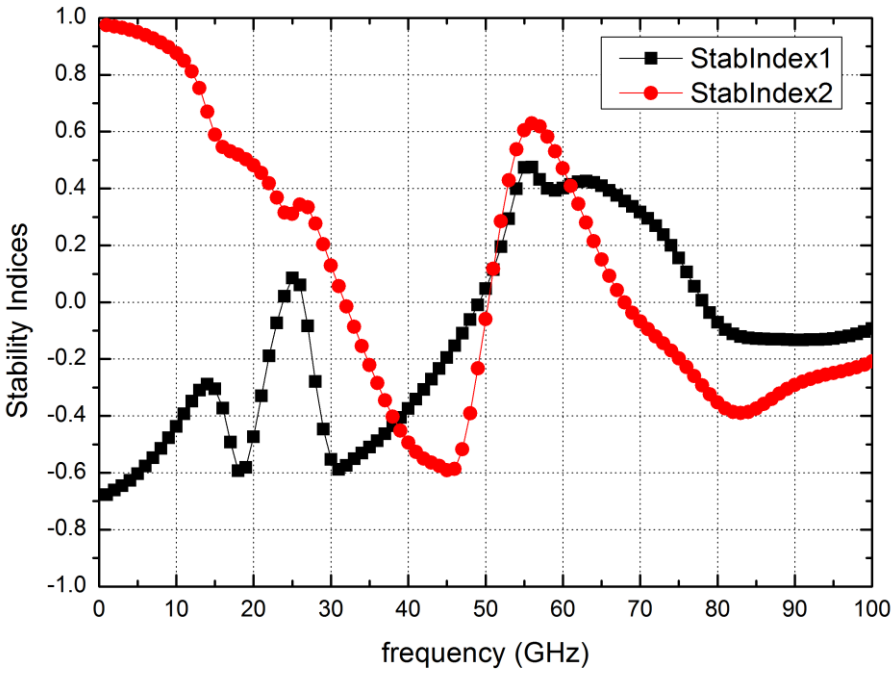

Fig. 3.32. Stability indices of LNA 2nd stage.

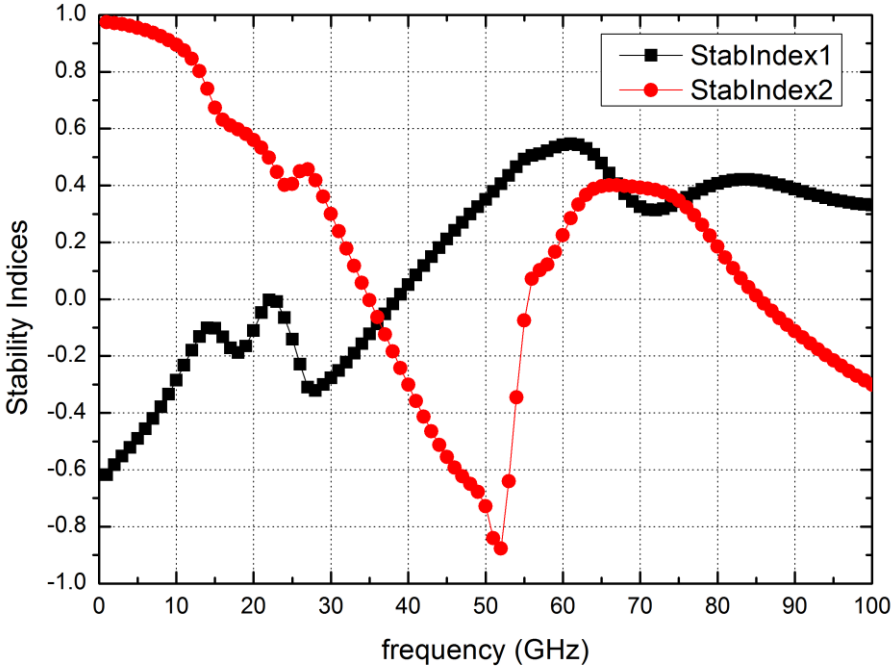

Fig. 3.33. Stability indices of LNA 3rd stage.

doi:10.6342/NTU201603106

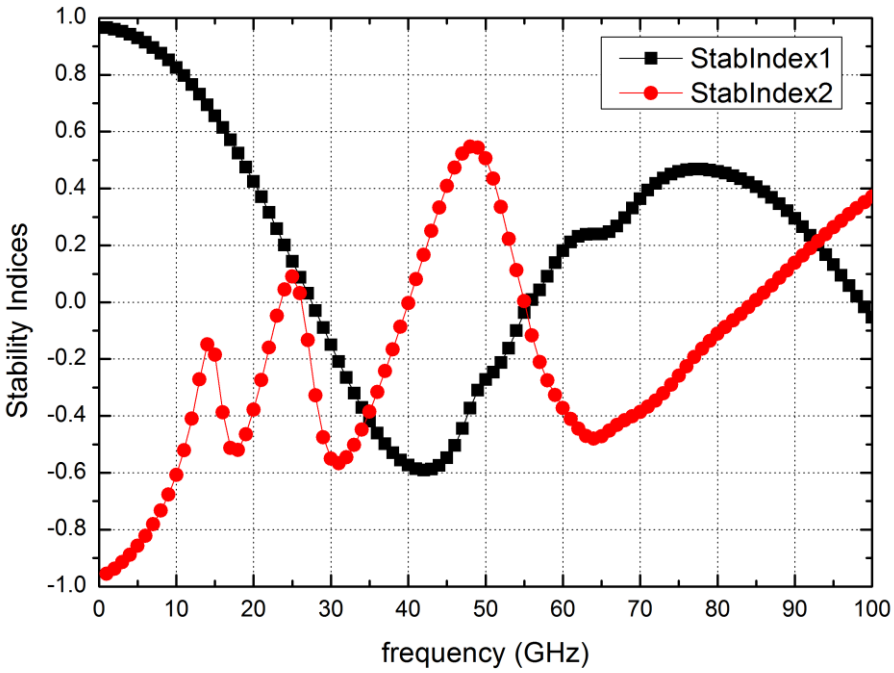

Fig. 3.34. Stability indices of PA 1st stage.

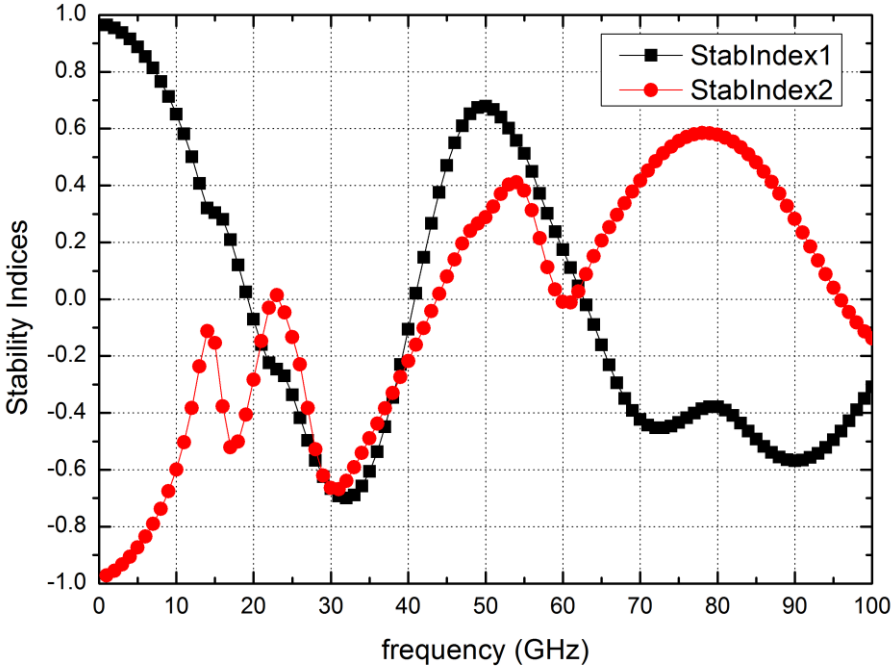

Fig. 3.35. Stability indices of PA 2nd stage.

doi:10.6342/NTU201603106

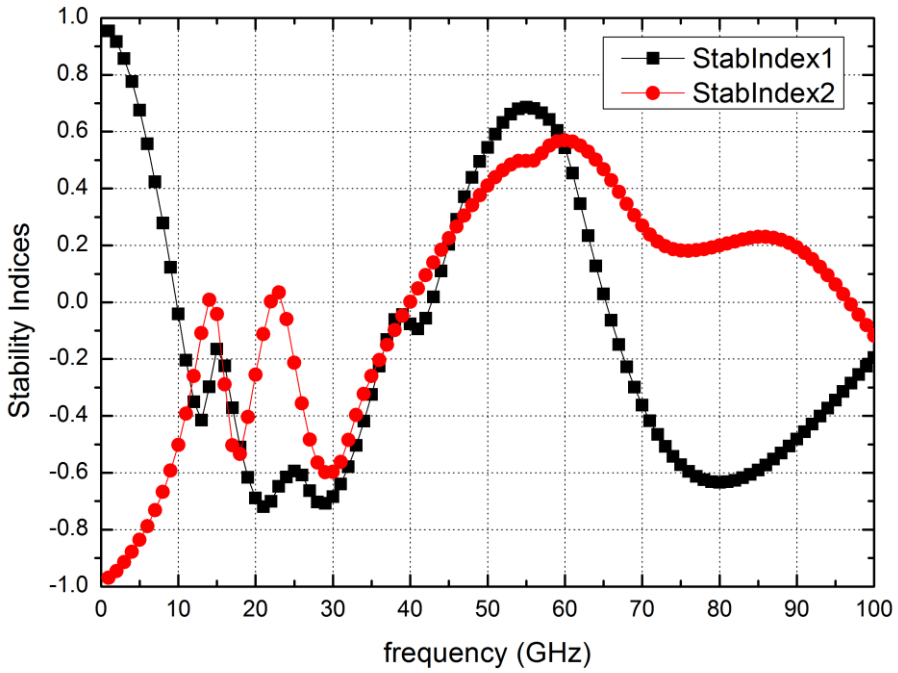

Fig. 3.36. Stability indices of PA 3rd stage.

3.6 Experiment Results

The BDA is fabricated in TSMC 40-nm Low power (LP) CMOS process. The chip photo is shown in Fig. 3.37. The chip size is 0.21 mm^2 including all pads, and the core size is 0.12 mm^2.

The chip measurement is taken via on-wafer probing. The S-parameter is measured by Agilent E8361C vector network analyzer. The noise figure is measured by Agilent N8975A noise figure analyzer with N8975AZ-K63 and N8975AZ-K75 downconverters. The large-signal measurement is taken by Agilent E8257D vector signal generator and Agilent E4419B power meter with Agilent V8486A V-band power sensor.

The measured gain in Rx mode is above 4.5 dB from 57 to 66 GHz, as shown in Fig.

doi:10.6342/NTU201603106

3.38. The measured noise figure is below 10 dB from 57 to 66 GHz, and below 8 dB from 53 to 63 GHz, as shown in Fig. 3.39. The measured gain in Tx mode is above 10.1 dB from 57 to 66 GHz, as shown in Fig. 3.40. The measured large-signal performance at 50, 55, and 60 GHz are shown in Figs. 3.40 to 3.42, respectively. At 50 GHz, the measured OP_{1dB} is 2.2 dBm, and saturated output power is 8.9 dBm with peak PAE of 5.9 %. At 55 GHz, the measured OP_{1dB} is 2.7 dBm, and saturated output power is 9.7 dBm with peak PAE of 8.5 %. At 60 GHz, the measured OP_{1dB} is 1.6 dBm, and saturated output power is 8.6 dBm with peak PAE of 6.2 %. The quiescent power consumption in Rx mode and Tx mode are 22.3 mW and 49.5 mW, respectively. The bias condition of the measurement as shown in Table 3.9.

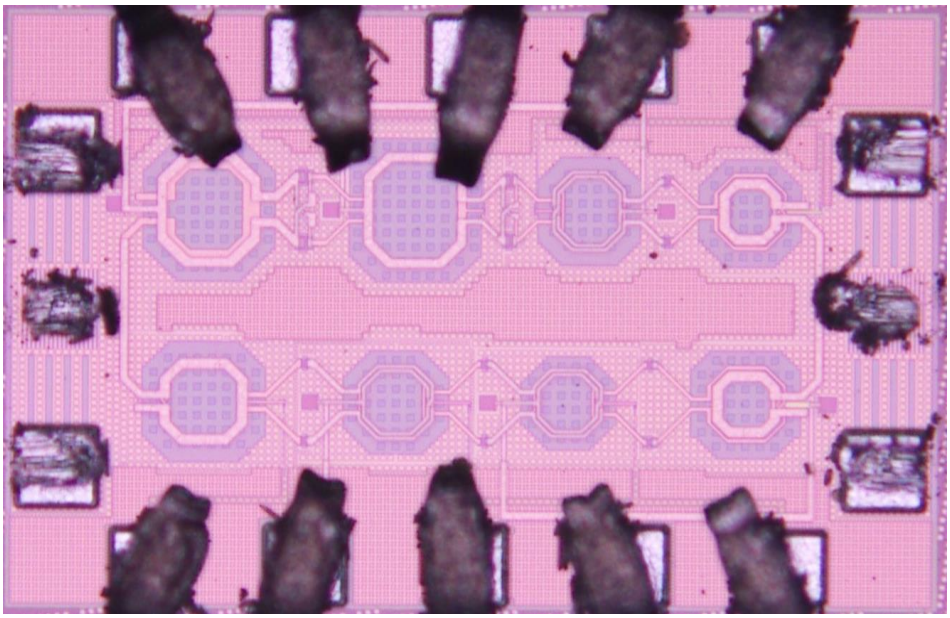

Fig. 3.37. Chip photo of the BDA.

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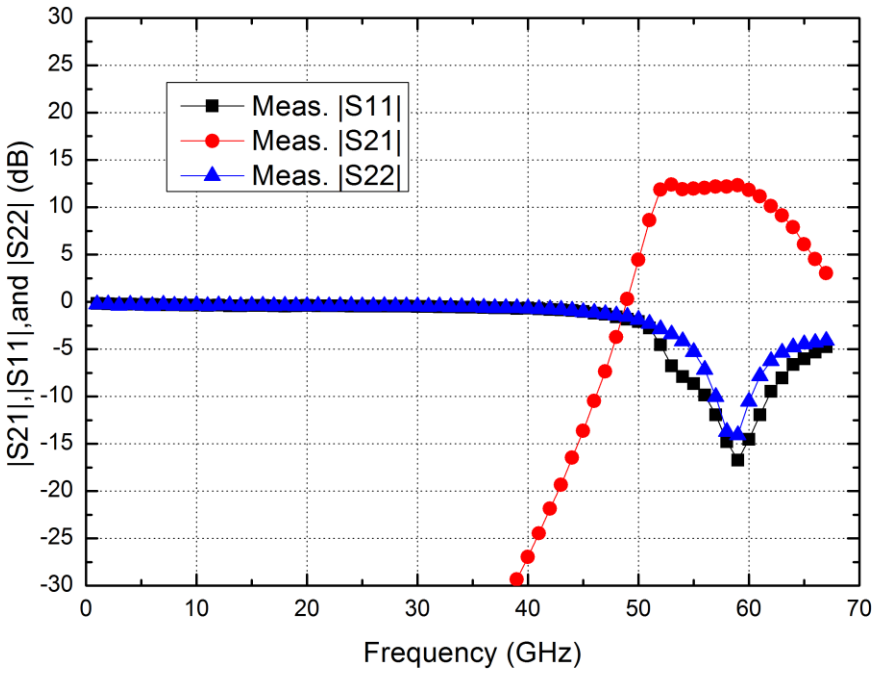

Fig. 3.38. Measured S-parameters in Rx mode.

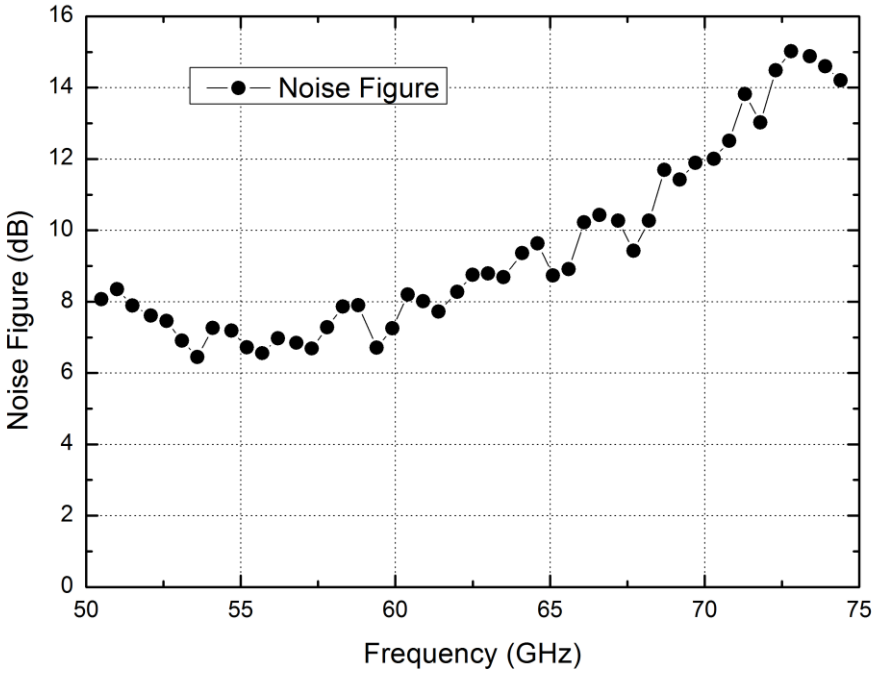

Fig. 3.39. Measured noise figure in Rx mode.

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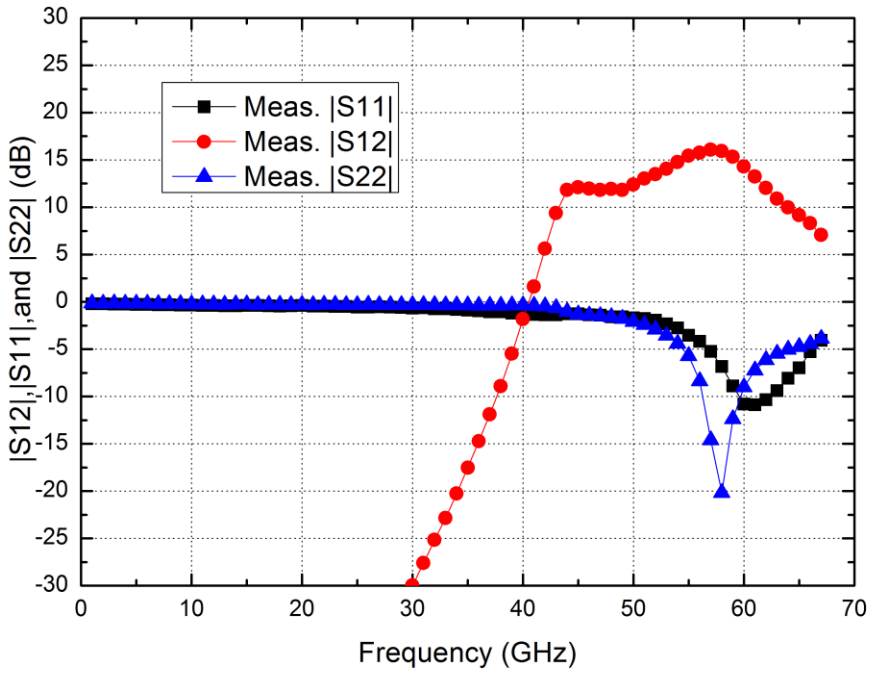

Fig. 3.40. Measured S-parameters in Tx mode.

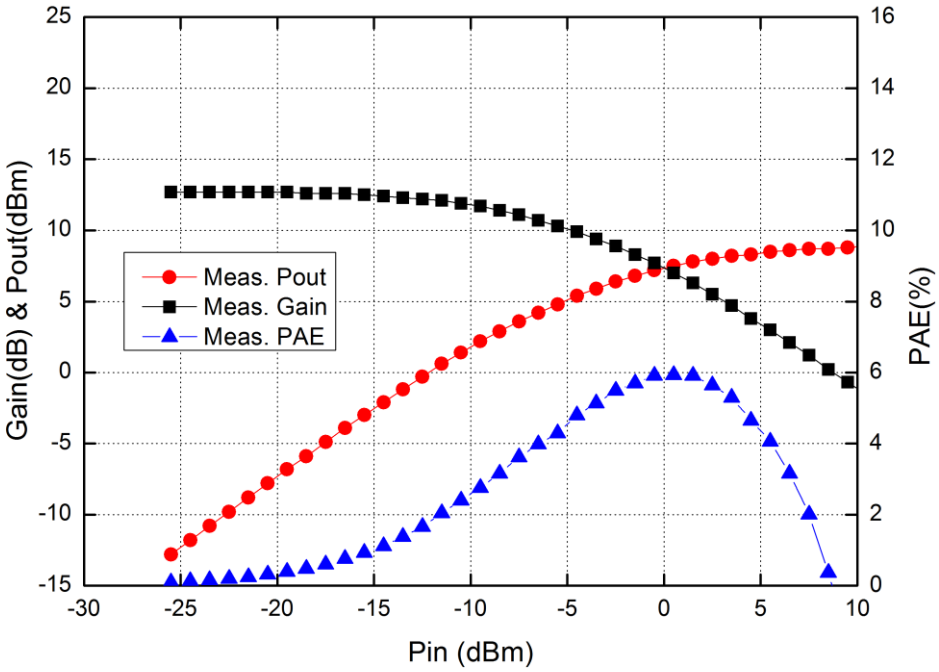

Fig. 3.41. Measured large-signal performance at 50 GHz.

doi:10.6342/NTU201603106

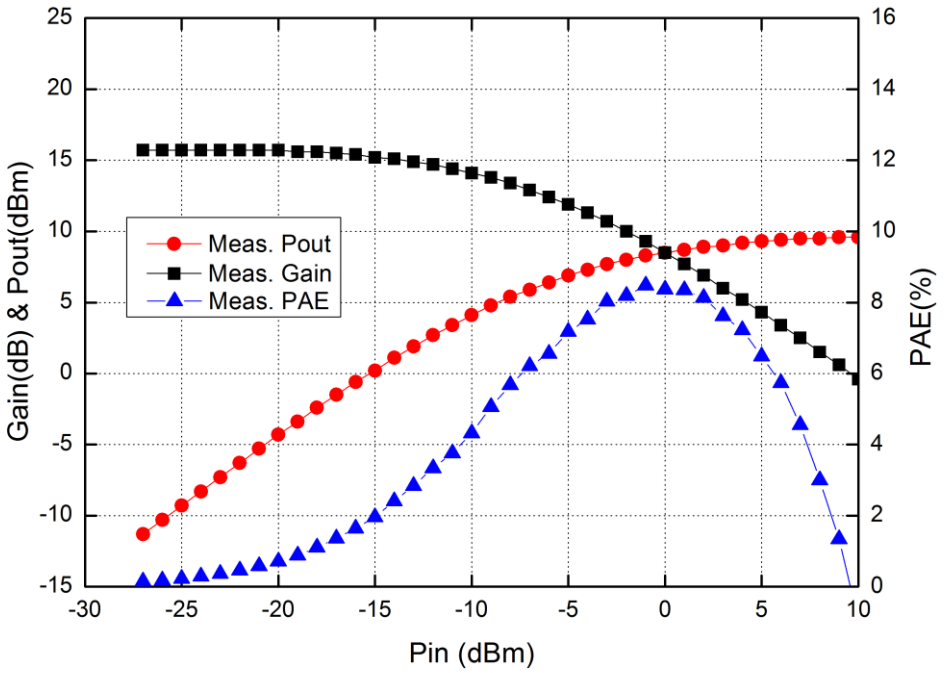

Fig. 3.42. Measured large-signal performance at 55 GHz.

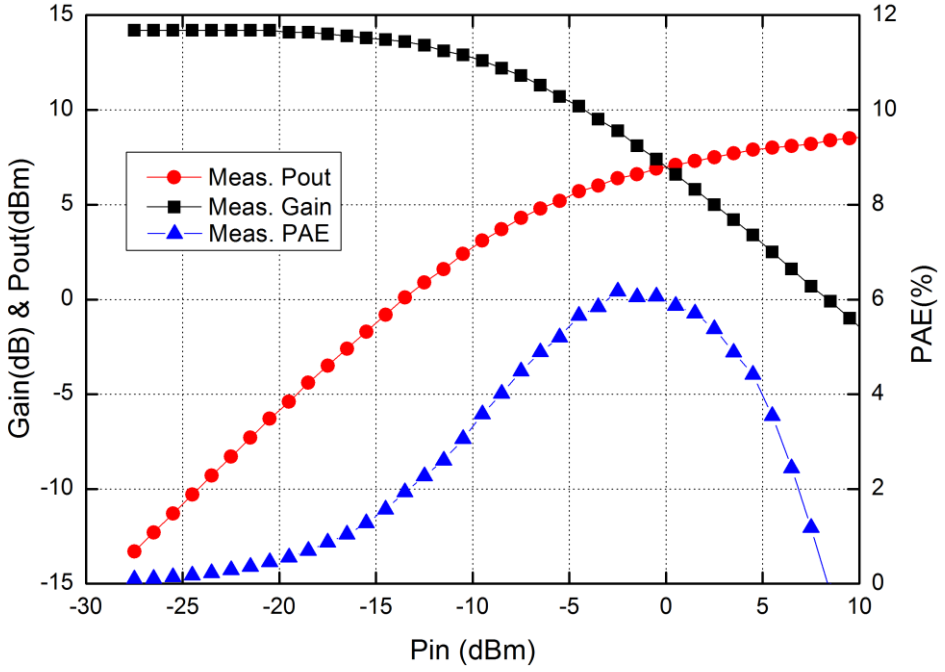

Fig. 3.43. Measured large-signal performance at 60 GHz.

doi:10.6342/NTU201603106

Table 3.9. Bias condition of the measurement.

	$V_{G, LNA}$ (V)	$V_{D, LNA}$ (V)	$I_{D, LNA}$ (mA)	$V_{G, PA}$ (V)	$V_{D, PA}$ (V)	$I_{D, PA}$ (mA)	P_{dc} (mW)
Rx Mode	0.93	1.1	20.3	0	1.1	0	22.3
Tx Mode	0	1.1	0	0.65	1.1	45	49.5

3.7 Discussion

3.7.1 Performance Comparison

Fig. 3.44 shows the comparison between simulated and measured S-parameters in Rx mode. The measured results show the frequency shifted around 4 GHz toward the lower band, and the gain falls around 3 dB that lower than simulation. Besides, the measured noise figure in Fig. 3.45 shows the same shifting phenomenon. Same as the Rx mode, the comparison results in Tx mode show the same frequency shift and gain drop, as shown in Fig. 3.46. Owing to the difference, the large-signal performance at 50, 55, and 60 GHz are quite worse than simulation, as shown in Figs. 3.47 to 3.49, respectively.

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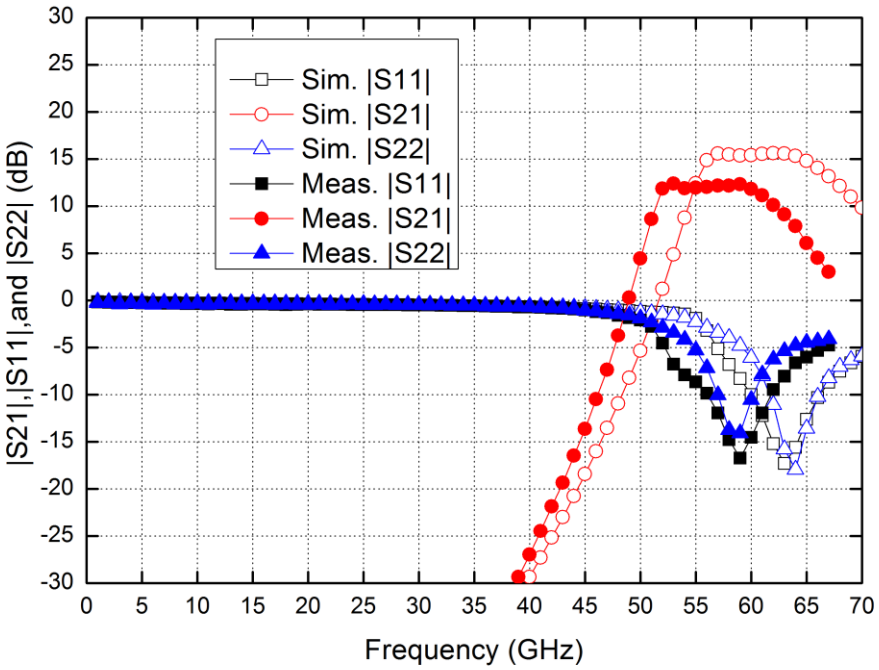

Fig. 3.44. Comparison of S-parameters in Rx mode.

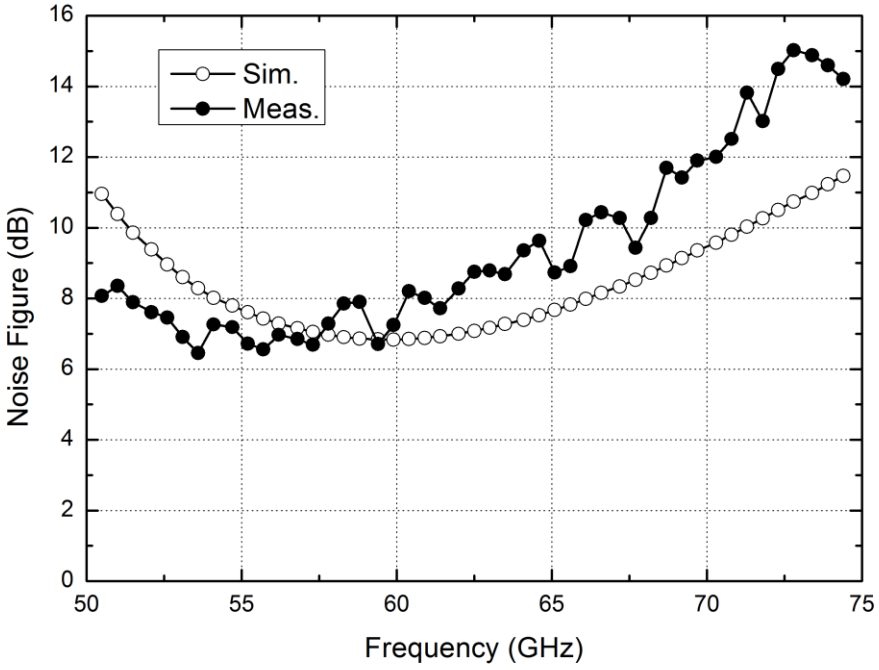

Fig. 3.45. Comparison of noise figure in Rx mode.

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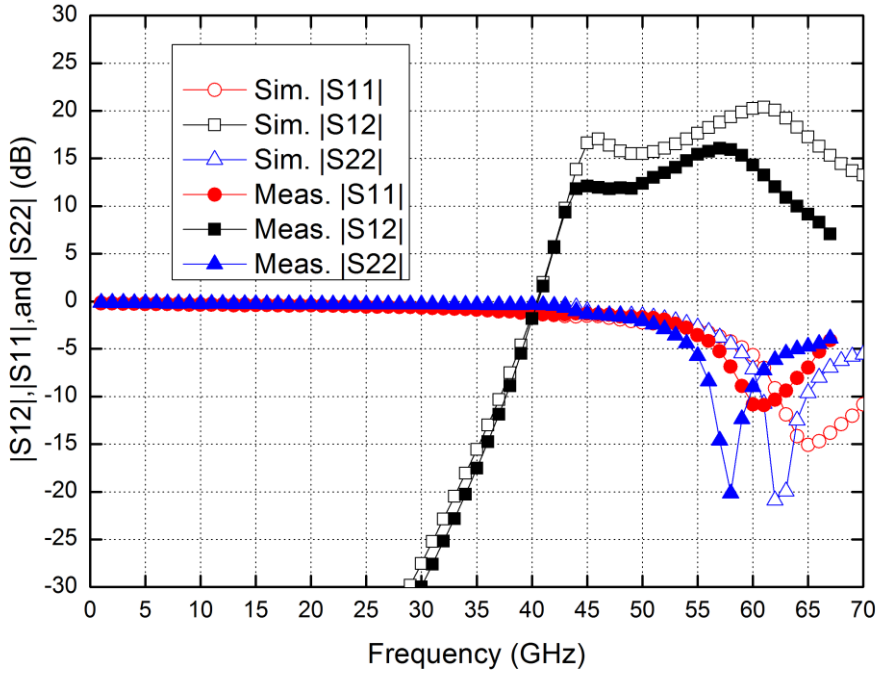

Fig. 3.46. Comparison of S-parameters in Tx mode.

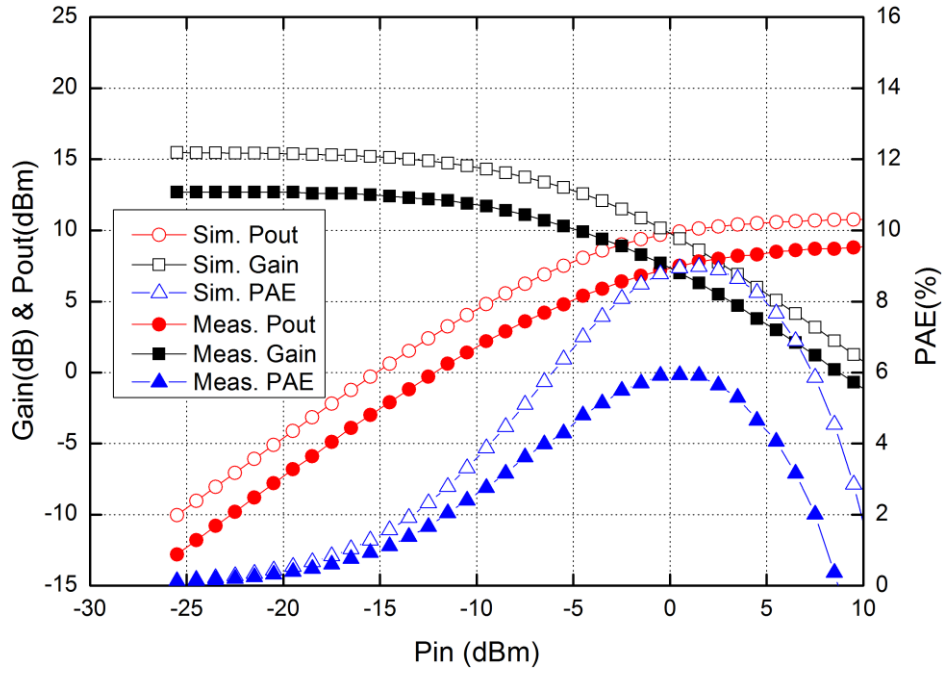

Fig. 3.47. Comparison of large-signal performance at 50 GHz.

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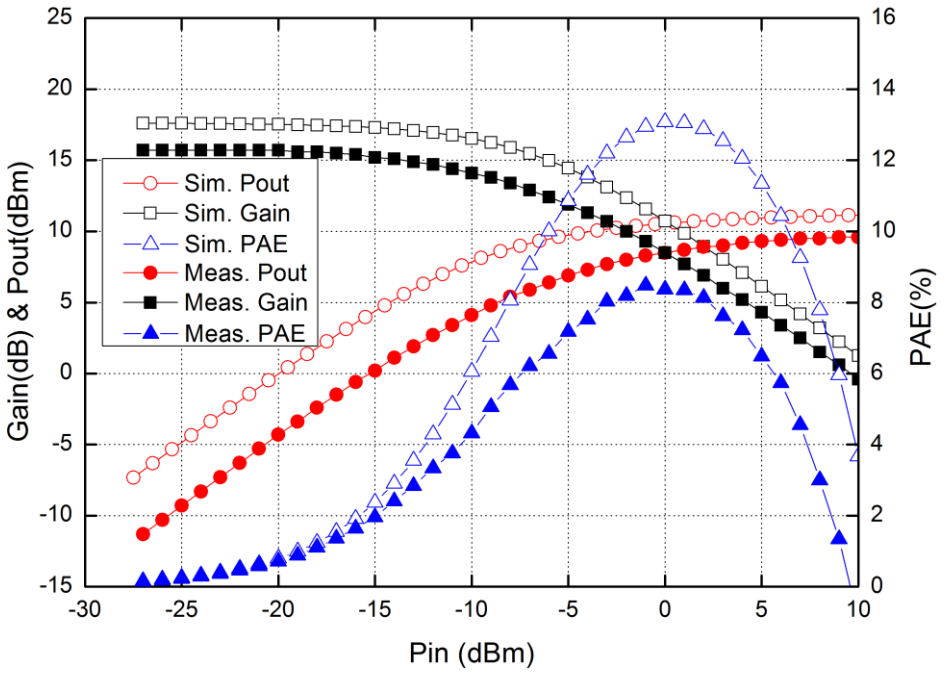

Fig. 3.48. Comparison of large-signal performance at 55 GHz.

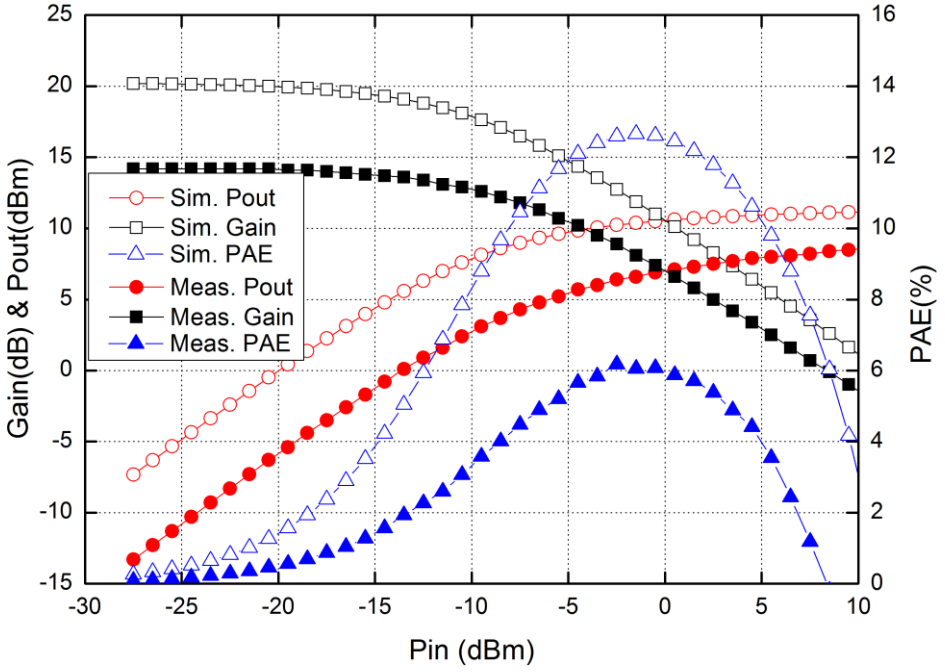

Fig. 3.49. Comparison of large-signal performance at 60 GHz.

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3.7.2 Measurement of test devices

In order to find the reason of the difference in performance comparison, the test devices on the same wafer have measured for this debugging. Figs. 3.50 to 3.52 show the drain current (I_D) versus gate voltage (V_G) of HVT, SVT, and LVT device, respectively. Figs. 3.53 to 3.55 show the derived transconductance (gm) from the above dc testing results.

In the HVT device testing results, it can be observed that the I_D and gm is almost agree with the Process Design Kit (PDK) model while V_G is below 0.95 V. In the SVT device testing results, the measured I_D and gm show around 10 % difference by comparing with the PDK model. In the LVT device testing results, the measured I_D and gm show 20~30 % difference by comparing with the PDK model.

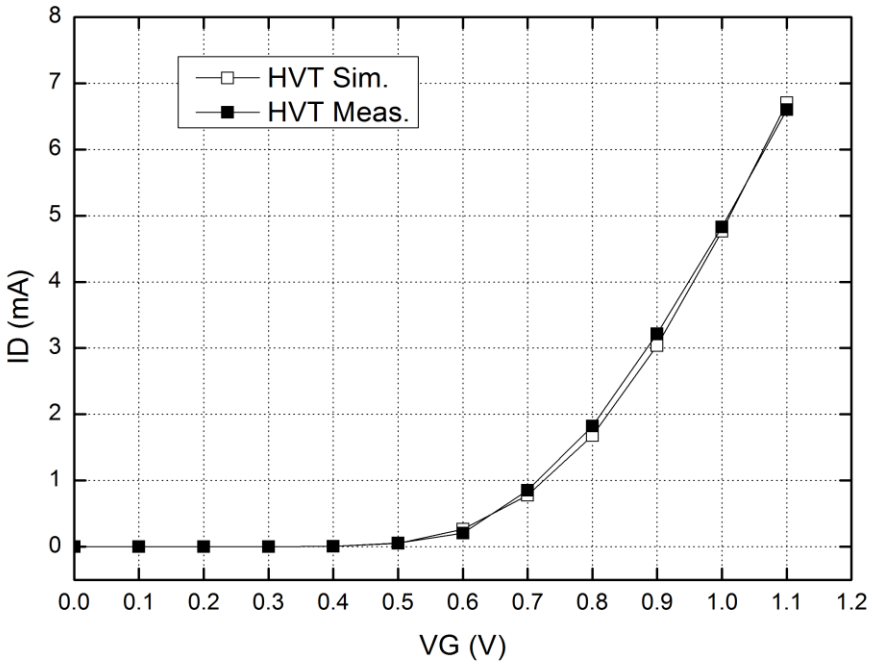

Fig. 3.50. Comparison of I_D versus V_G of HVT device.

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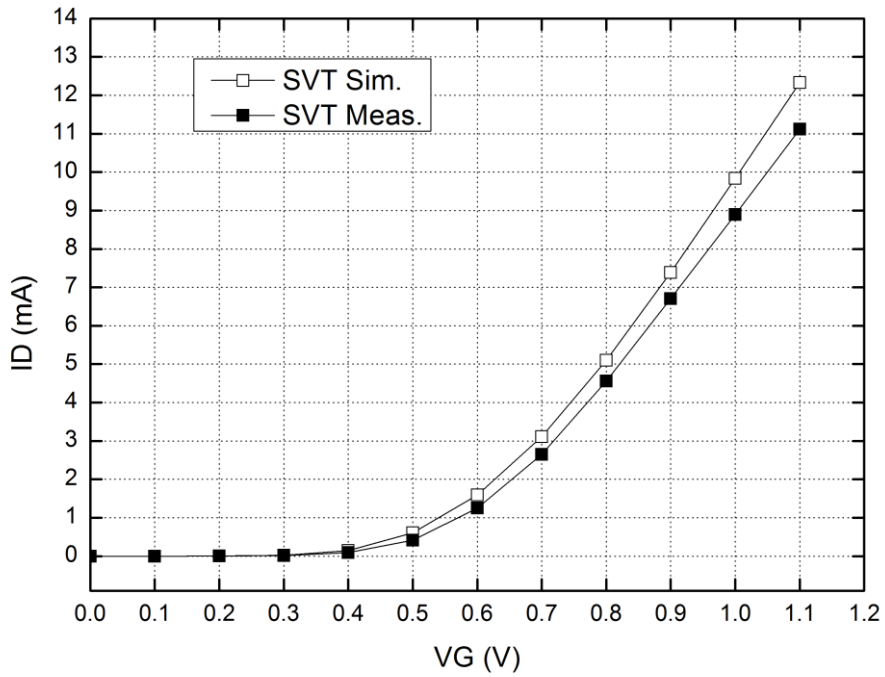

Fig. 3.51. Comparison of I_D versus V_G of SVT device.

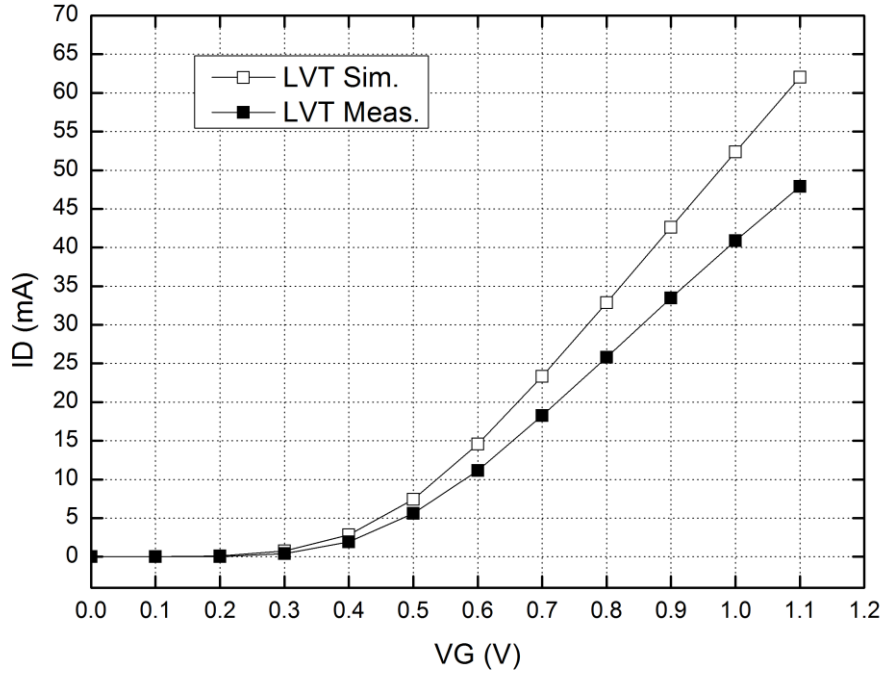

Fig. 3.52. Comparison of I_D versus V_G of LVT device.

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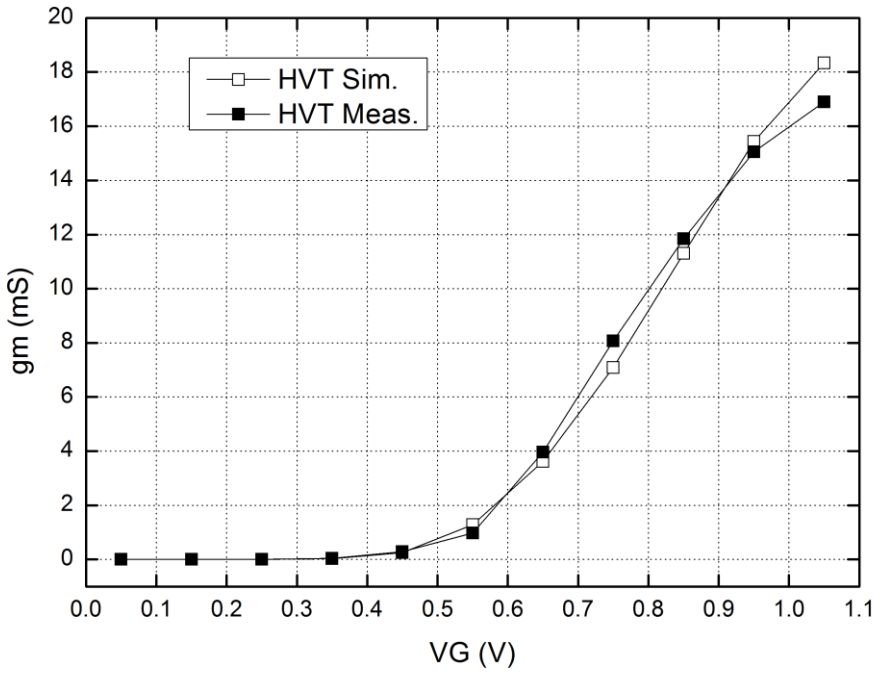

Fig. 3.53. Comparison of transconductance of HVT device.

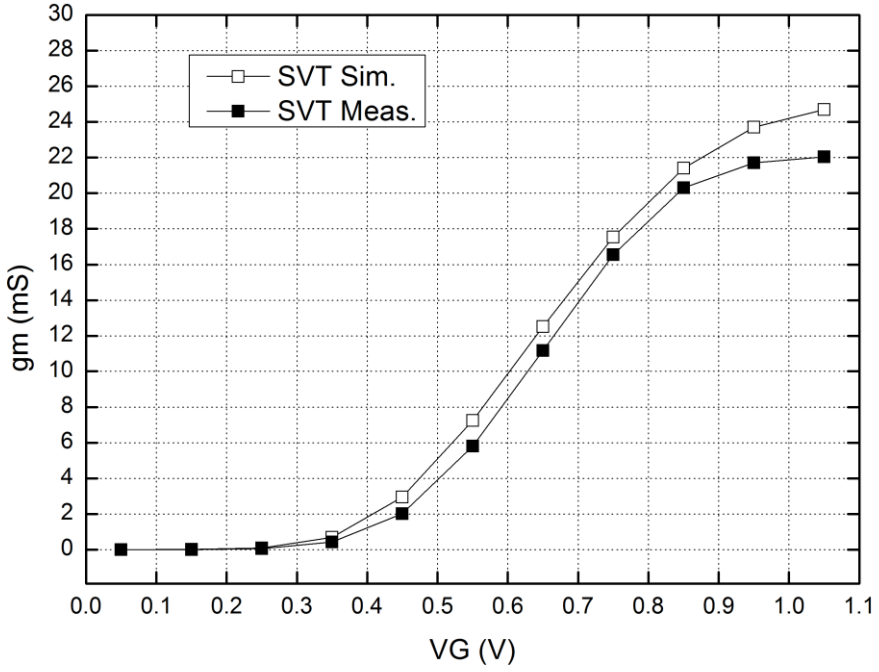

Fig. 3.54. Comparison of transconductance of SVT device.

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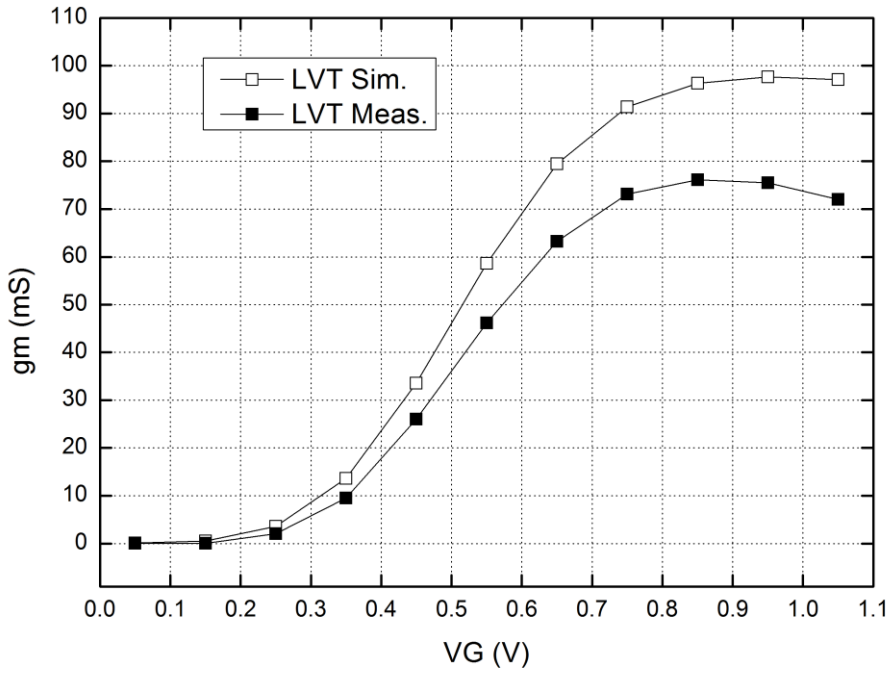

Fig. 3.55. Comparison of transconductance of LVT device.

3.7.3 Revised Model

In this BDA design, the PA part uses 3-stage LVT devices. The LNA part uses 1-stage HVT device and 2-stage SVT devices. Based on the results of test devices, the PDK model can be modified to fit the measured results, the negative transconductance is used to revise the gm in the PDK model, and the shunt capacitor is used to revise the frequency shift. The proposed revised model is shown in Fig. 3.56.

In theory, the gm is proportional to the total width of transistor, the fitting values are derived by the width ratio of the devices used in the amplifiers to the test devices. The g_m fitting value can be derived by:

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$$\left(g_{m_{meas.}} - g_{m_{sim.}}\right) \times \frac{Width\ of\ used\ device}{Width\ of\ test\ device} \tag{3.6}$$

In PA part, all the LVT devices are biased at V_G=0.65 V, and the devices size are 1×16 μm, 1.5×32 μm, and 3×32 μm, the derived fitting gm are:

$$(63.25-79.5)\times\frac{3\times32}{3\times32}=-16.25(\text{mS}) \tag{3.7}$$

$$(63.25-79.5)\times\frac{1.5\times32}{3\times32}=-8.125(\text{mS}) \tag{3.8}$$

$$(63.25-79.5)\times\frac{1\times16}{3\times32}=-4.063(\text{mS}) \tag{3.9}$$

In LNA part, all the HVT and SVT devices are biased at V_G=0.93 V. There is no need to revise the HVT device since the derived g_m agrees with that in the PDK model while V_G is below 0.95 V. The used SVT devices size are 1×12 μm and 1×10 μm, the derived fitting g_m are:

$$(23.7-21.7)\times\frac{1\times12}{2\times12}=-1(\text{mS}) \tag{3.10}$$

$$(23.7-21.7)\times\frac{1\times10}{2\times12}=-0.833(\text{mS}) \tag{3.11}$$

The frequency shift between the simulation and the measurement is a common phenomenon in the first tape-out on the advanced process, because the first design only relies on the PDK model. The PDK model of this process is confirmed up to 30 GHz based on the measurement by the foundry. However, in this design, the operated frequency is up to 66 GHz, which is twice higher than the confirmed frequency, the parasitic effect maybe underestimated that affect the response at high frequency. For this

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reason, the model fitting is necessary for accurate device behavior in the future design.

The 6-fF additional capacitances are shunt at gate and drain terminals to fit the measured results of other 60-GHz circuits (PA, LNA, buffer amplifier, and switches) that fabricated on the same wafer. The proposed model compensates the difference between the simulated and measured results for all these circuits.

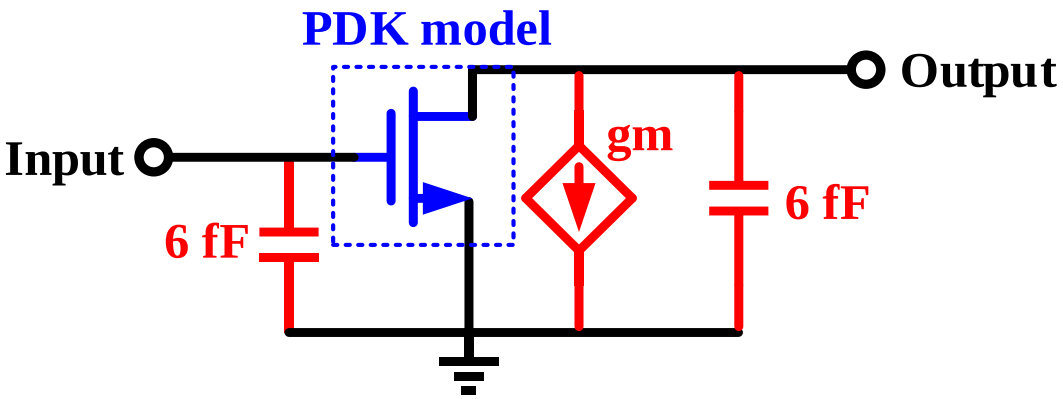

Fig. 3.56. Proposed revised model.

3.7.4 Revised Simulation

Base on the revised model, the circuit is re-simulated. Figs. 3.57 and 3.58 show the re-simulated gain and the noise figure in Rx mode, respectively. Fig. 3.59. shows the re-simulated linear gain in Tx mode. Figs. 3.60 to 3.62 show the re-simulated large-signal performance at 50, 55, 60 GHz. By comparing with the original simulation, the results are much closer to the measurement.

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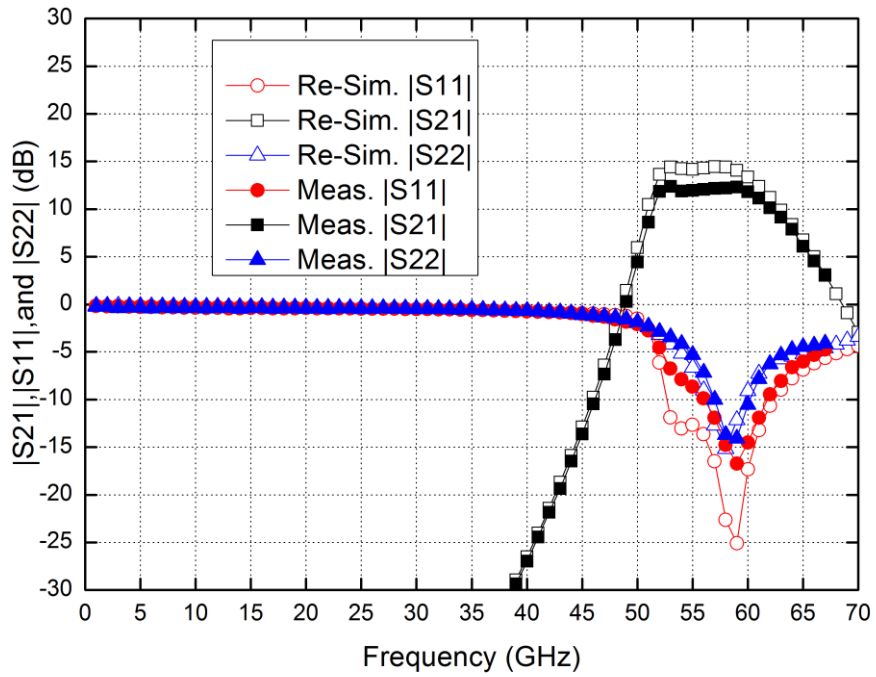

Fig. 3.57. Comparison of S-parameters in Rx mode.

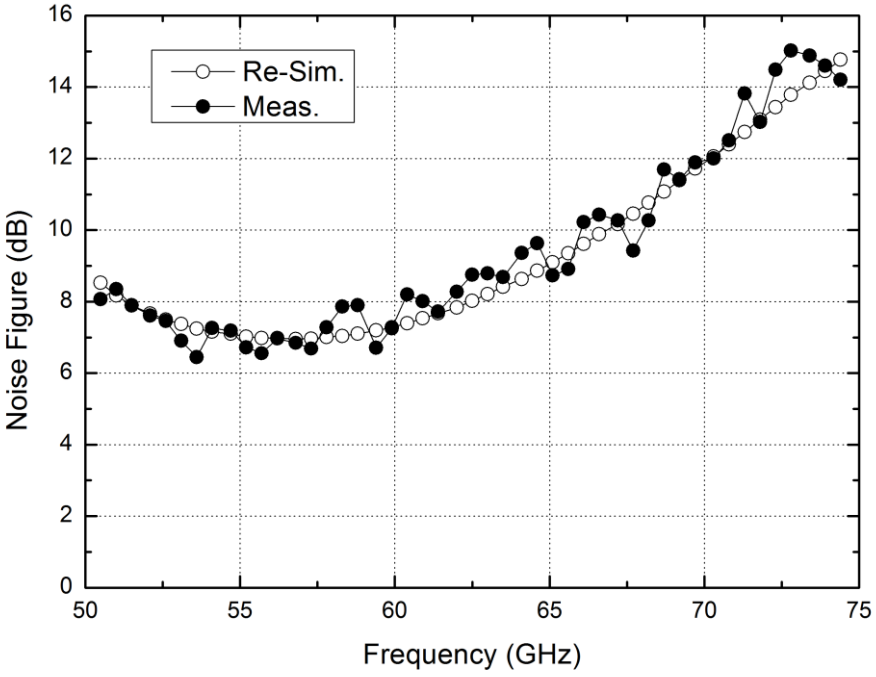

Fig. 3.58. Comparison of noise figure in Rx mode.

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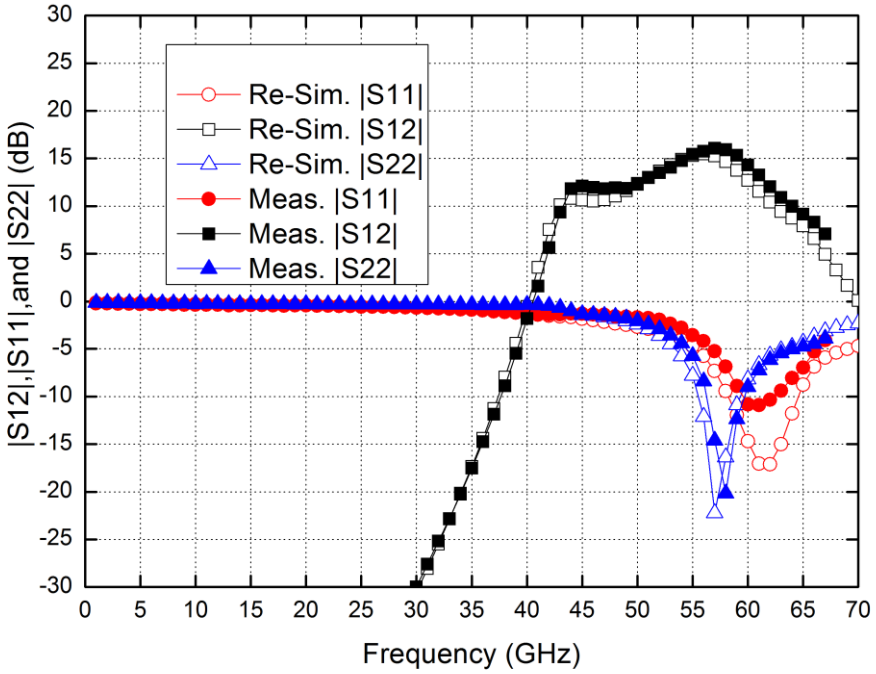

Fig. 3.59. Comparison of S-parameters in Tx mode.

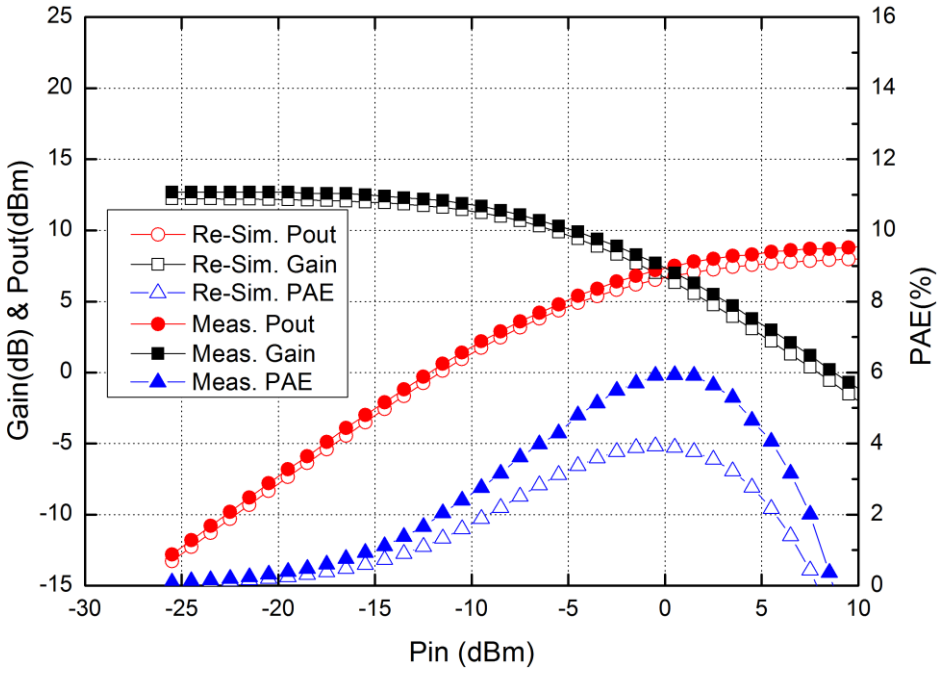

Fig. 3.60. Comparison of large-signal performance at 50 GHz.

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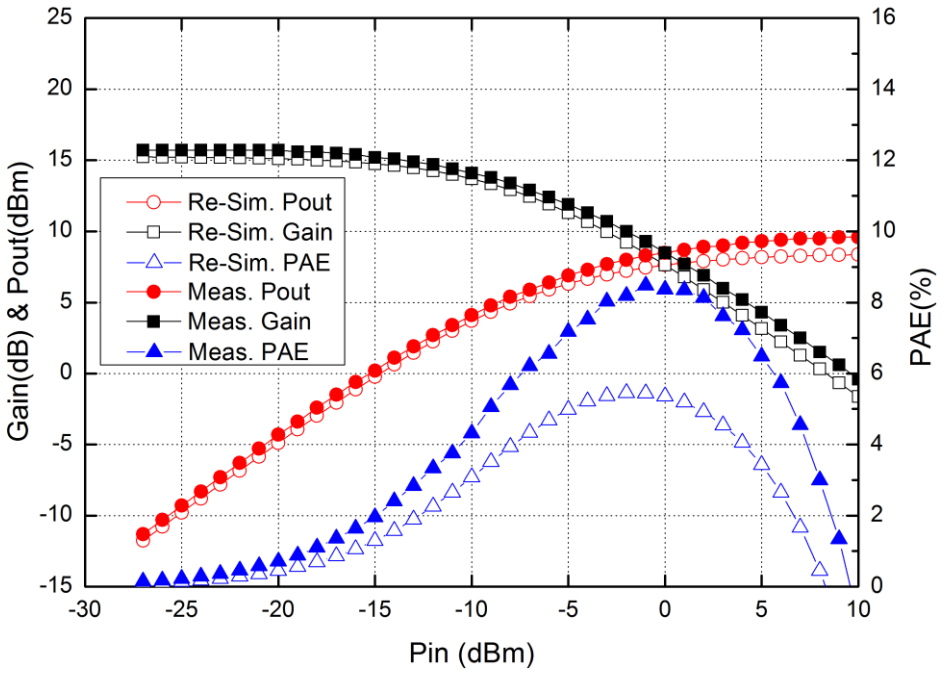

Fig. 3.61. Comparison of large-signal performance at 55 GHz.

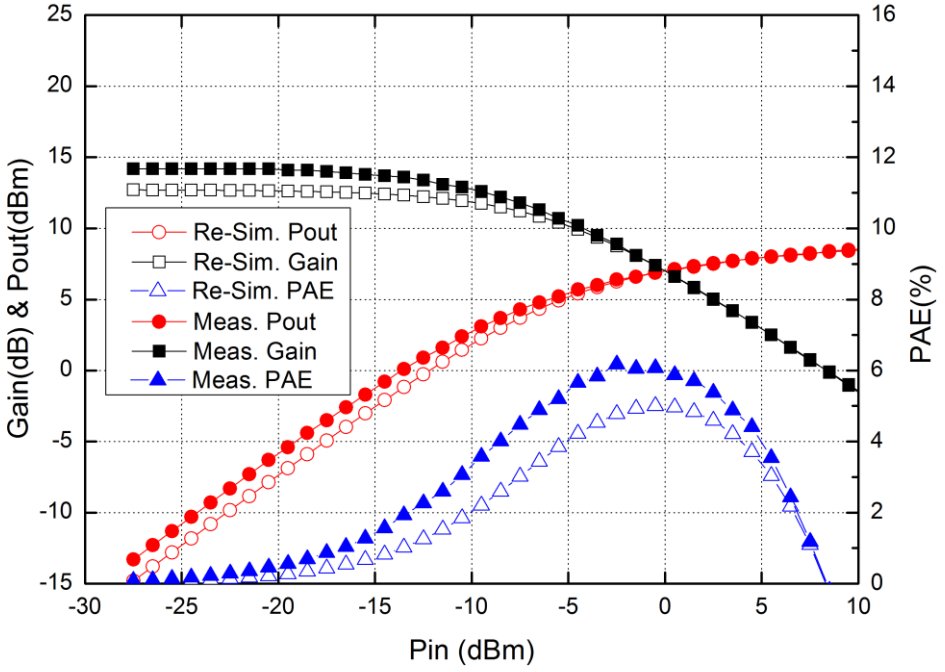

Fig. 3.62. Comparison of large-signal performance at 60 GHz.

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3.8 Summary

In this chapter, a 60-GHz switchless bidirectional amplifier based on differential topology, transformer-coupled and neutralization technique is presented. It consists a power amplifier, a low noise amplifier, and the input/output junction networks. All the inter-stage matching networks and the I/O junction networks are realized by transformers. By using the impedance difference in the on/off state of amplifiers, the junction transformers are designed to transform the impedance into matched/isolated condition.

By using the differential design, the bypass capacitors is reduced to half size. By using the all-transformer design, the dc-block capacitor is removed. The chip size is 0.21 mm^2, and the core size is 0.12 mm^2, the compact size improves the area efficiency while applied in large-scale phased array.

Table 3.10 shows the comparison with the 90-nm bidirectional amplifier in previous chapter and the published switchless bidirectional amplifiers. Comparing with the 90-nm BDA, the differential topology with the transformer-coupled method enhances the power performance and reduces the chip size. Although the 40-nm BDA has the higher dc consumption due to its differential circuits, it demonstrates higher output power in Tx mode. The similar noise performance is obtained for both BDAs which is better than 8 dB in the band.

Although the performance is drop due to the inaccurate PDK model, the 40-nm bidirectional amplifier still demonstrates a comparable performance. It shows 8 dB noise figure and a useful gain of 10.1 dB in receiving mode. On the other hand, it demonstrate the highest output power above 50 GHz, the maximum 9.7-dBm output power beats all other circuits that above 50 GHz and in high-cost (InP, GaAs, SiGe, and CMOS SOI) process. To the author's knowledge, this 40-nm CMOS switchless bidirectional amplifier

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has the highest maximum output power with the most compact chip size in V-band.

Table 3.10. Performance comparison of the reported MMW switchless BDAs.

Ref.	Process	Topology	Frequency (GHz)	Rx Mode Gain (dB)	NF (dB)	Tx Mode Gain (dB)	OP_{1dB} (dBm)	P_{sat} (dBm)	P_{dc} (mW)	Chip Size (mm^2)
[20]	GaAs	CG	32-37	13	4.7	13	N/A	10	N/A	2.6
[21]	75-nm InP	CG	90-140	12	5	9	1*	5	15	0.46
[4]	0.12-μm SiGe	CE	41.7-45.8	34**	4.7	35**	8.5	9.5	26(R) 91(T)	1.28***
[23]	90-nm SiGe	CE	66-73	9.6	8.6	14.5	N/A	7.2	21/85	0.65
[25]	0.13-μm SiGe	CE	94	5.7	9.5	5.7	-2.8*	N/A	9.9	0.31
[20]	GaAs	CS	26-43	17	4	13	N/A	17	N/A	1.3
[22]	65-nm CMOS	CS	77.3	42**	9	42**	N/A	9.2	20.2(R) 71.5(T)	0.69***
[26]	0.13-μm CMOS	DA	3-20	10	6.5	10	8	16	68	0.81
[28]	0.18-μm CMOS	DA	21.6-31	6.4	9.1	6.4	4.3	12	46.8	0.28
[29]	0.12-μm SiGe	BCWA	77-90	16	N/A	16	N/A	N/A	65.8	0.47
[30]	45-nm CMOS SOI	BCWA	40/85	4.6	N/A	4.5	-2.9	3.9	N/A	0.48
This work	**90-nm CMOS**	**CS**	**57-66**	**18.2**	**8**	**13.5**	**3.6**	**6.5**	**15.3(R) 46(T)**	**0.44**
This work	**40-nm CMOS**	**CS**	**52-62**	**10.1**	**8**	**13.4**	**2.7**	**9.7**	**22.3(R) 49.5(T)**	**0.21**

*Inferenced by IP_{1dB} with Gain in Tx Mode.
**Including the IF amplifiers.
***Total transceiver.

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Chapter 4 Design of 60-GHz Bidirectional Beamformer in 40-nm CMOS Process

In the previous chapters, we have described the advantages of bidirectional system (chapter 1) and presented two switchless BDAs (Chapters 2 and 3). In this chapter, a 60-GHz bidirectional beamformer built by the BDAs and realized in the 40-nm CMOS process is demonstrated.

4.1 System plan

4.1.1 Application

The 60 GHz, or IEEE 802.11ad standard [42], is evolved from 802.11b/g/n and 802.11a/ac, which are in 2.4-GHz and 5-GHz carrier frequency, respectively. Due to the higher carrier frequency, the bandwidth is enlarged proportionally. The wider bandwidth results in higher throughput that is up to 7 gigabit per second (Gbps), which is more than 10 times of currently popular 802.11n standard. Besides, the 60-GHz microwave has the property of high attenuation in the oxygen environment. Although it seems a disadvantage of propagation, but it is suitable for short-range private communication. In commercial application, it is aimed in the high speed indoor communication, such as wireless uncompressed video transmission, wireless docking station, and rapid file transfer [43].

The 60 GHz is an unlicensed band, the applied frequency is 57 to 64 GHz in US and 57 to 66 GHz in EU [43], as shown in Fig. 4.1. The 60 GHz offers a much higher throughput and is compatible with the current 802.11 WLAN standard [44]. In the

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specification of 802.11ad [42], the beamforming technique is formulated for tracking the position of object, and concentrating the main beam of multi-antenna to the object. By using the beamforming technique, the high throughput and the high directivity can be reached at the same time. This chapter presents a beamformer which can be applied in the high speed communication module of mobile devices.

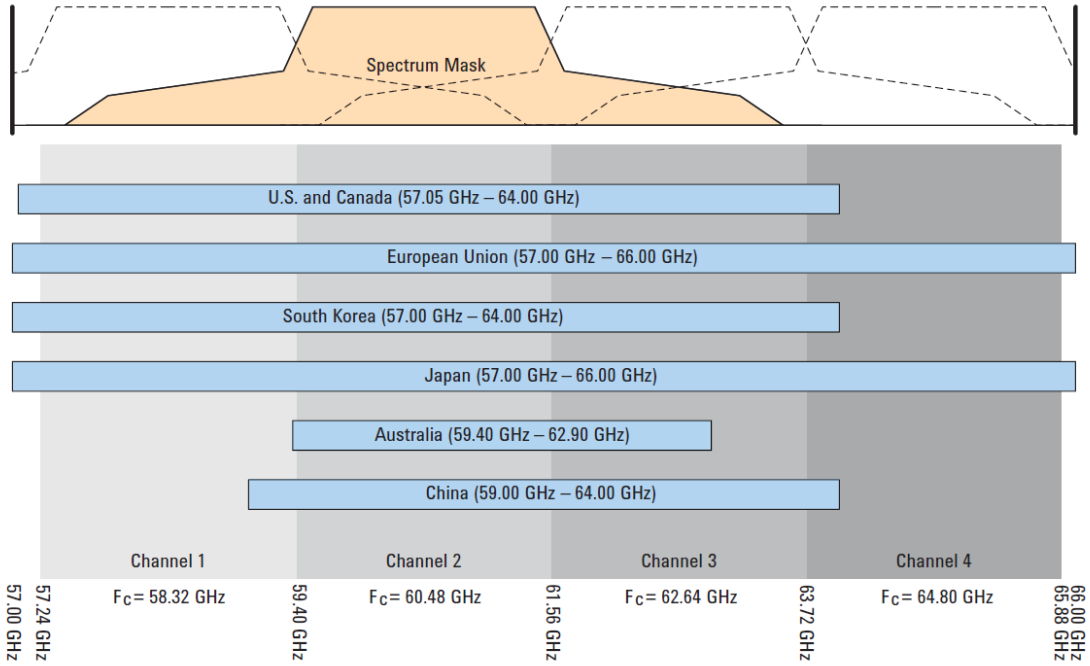

Fig. 4.1. Unlicensed spectrum allocation in the 60 GHz region [43].

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4.1.2 Approach

Owing to the rapid growth of mobile devices in recent years, the demand of high speed communication among the mobile devices is growing simultaneously. The 60 GHz is a practical solution due to its wide bandwidth. However, the propagation loss increased proportionally with the carrier frequency, to resolve this problem, the beamforming technique is proposed. The multiple antennas are designed for combining the beams into a specified direction in spatially. Thus it provides a higher directivity, improves the equivalent isotropically radiated power (EIRP) in Tx and required signal-to-noise ratio (SNR) in Rx. The concept of beamforming is that, the antenna array is excited by proper phase, thus the radiation pattern is interfered combined in specific direction. By controlling the excited phases, the radiated beam can be controlled to the desired direction.

The wavelength of 60-GHz microwave in air is 5 mm. For a 4-element linear antenna array in dipole form with half-wavelength spacing results in around 10 mm of dimension, which is a suitable size be integrated in the mobile devices. For the practical application, the communication between the mobile devices can be in any direction, thus the omnidirectional beamforming is necessary. For a mobile device module, there are possibly six faces to place the antenna array, the four in sidewall edge (with linear form), and the other two in front board and back board (with planar form). However, for efficient radiation, the clearance zone for antennas is necessary. Considering the integration, the antenna module has at least two sidewall edge connected with other circuit or power supplied path in the mobile device, thus the two edges are not suitable to place the antennas. As a results, the 4 main directions with 4 beamforming resolution in each direction (4×4) are designed to cover the omnidirectional communication. The proposed module used in mobile devices and its beam-steering plan as shown in Fig. 4.2. The 3-D

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diagram of the proposed module as shown in Fig. 4.3.

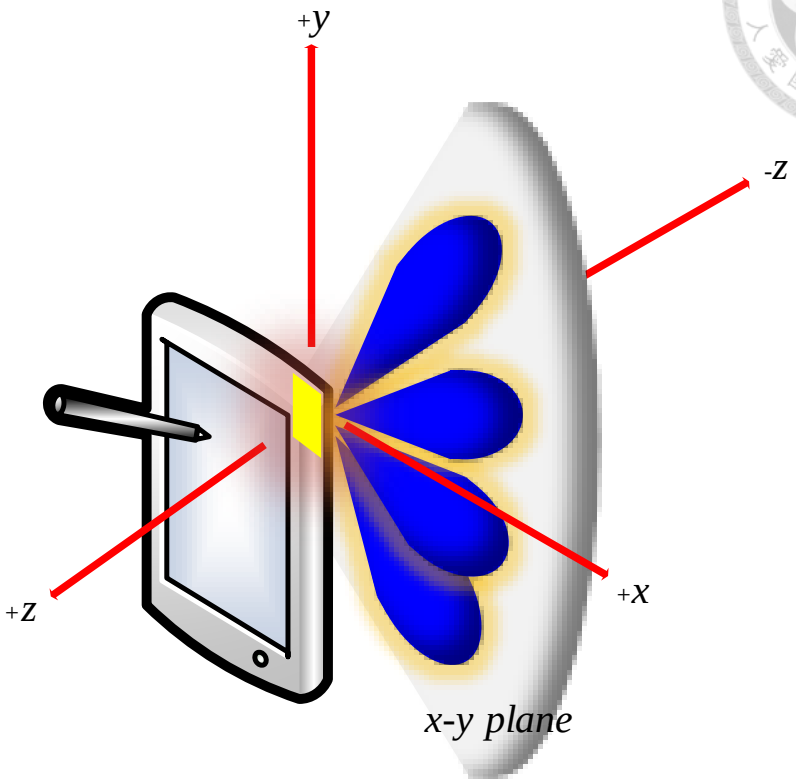

Fig. 4.2. Beam-steering diagram of the proposed module.

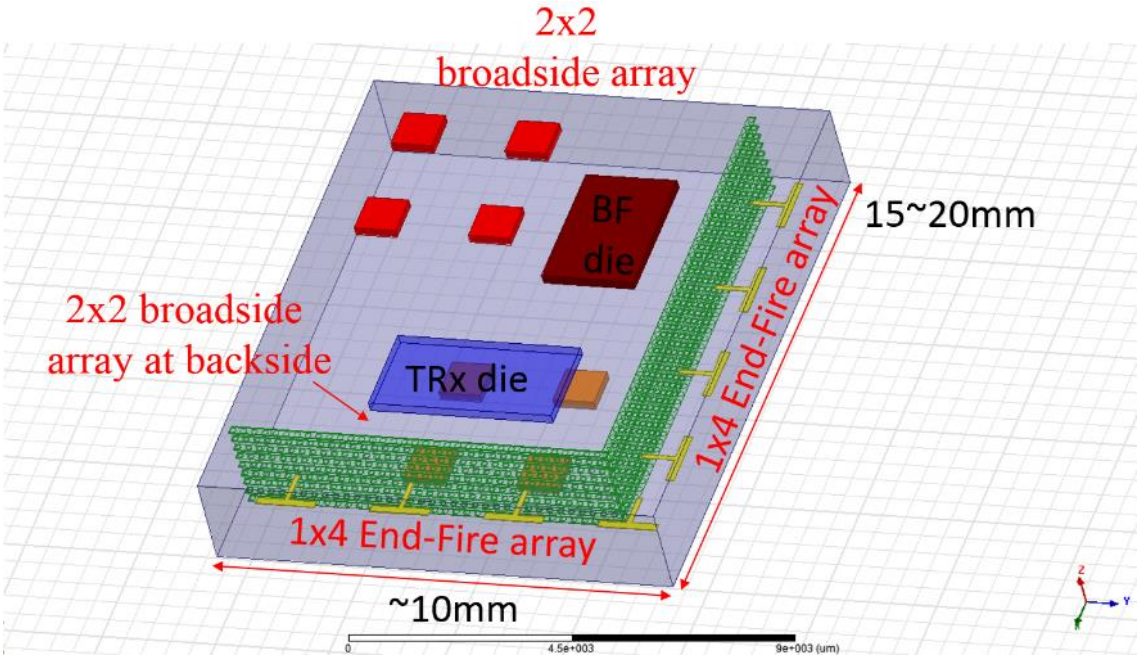

Fig. 4.3. 3-D diagram of the proposed module.

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4.1.3 System architecture

For point-to-point connection between the mobile devices, both of transmitter (Tx) and receiver (Rx) are necessary for data interchange. However, the conventional architecture using separated Tx and Rx, even the individual T/R antennas can be shared by adding a T/R switch, extra loss and chip size make it be non-practical. To place the individual Tx/Rx antenna in a limited space of the mobile devices, the quantity of antenna array will need to be reduced. Therefore, the space coverage of beam-steering will be limited, and the omnidirectional feature will be sacrificed. To resolve the problem, we use the bidirectional architecture [3]-[5] in the system, as shown in Fig. 4.4. By sharing all the passive components including the antennas, the system uses only half components to achieve the function of Tx and Rx. Moreover, when the number of I/O quantity is reduced, it not only enhances the reliability of assembly, but also minimizes the chip area.

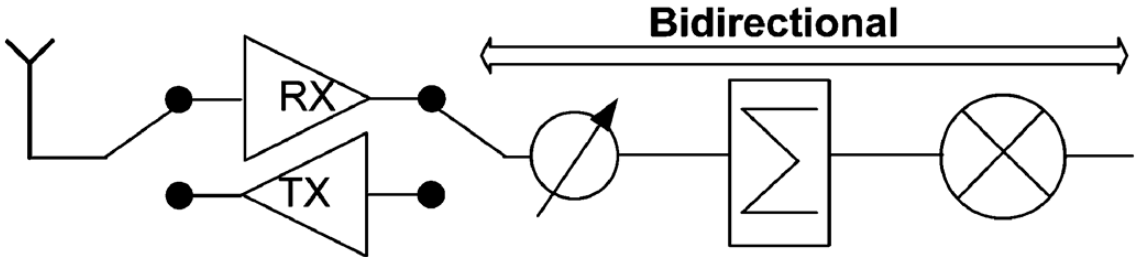

Fig. 4.4. Bidirectional transceiver [3].

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4.1.4 Beamforming control

The beam direction is controlled by the excited phase to the antenna array. To generate the specific exited phase, the phase control circuits are designed.

The phase shifter, which is commonly used in conventional phased array that realized in each element. In the bidirectional system, all the components must be reciprocal and passive. Thus the vector-sum phase shifter [45], or other topologies that using the transmission from gate to drain terminals in transistor cannot be used. On the other hand, using the nearly symmetrical characteristic between the source and drain terminals is a possible solution. For example, switch-type phase shifter (STPS) [46]. The shifting phase can be controlled by switching the gate voltage and by cascading the multiple cell of the switches with different size and impedance of lump components. The phase control resolution can be improved by adding the cascade stages. However, the topology suffers the high insertion loss due to the use of switches and large quantity of cascading stages. The STPS suffers a loss around 3 dB in each cascading cell [46]. It can be estimated that the loss will be 9 dB for 45^{o} phase control resolution.

Butler matrix [47] is proposed to generate the specific phase of linear placed input/output ports, as shown in Fig. 4.5. It is built by 90^{o} couplers and 45^{o} delay lines, and has the property of reciprocal due to symmetric structure of the matrix and the reciprocal couplers. Specific phases can be produced among all the output ports while exciting one of input ports. Butler matrix has the advantages of no transistors and predictable behavior is by using the EM simulator. Although the drawback is large size due to the multiple quarter-wave components in the matrix, fortunately, the quarter-wave components are relatively small at 60 GHz, and thus it becomes a practical solution.

For this application, each antenna array is with 4-beam states. Thus a 4-input and 4-

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output (4×4) Butler matrix is sufficient for this purpose. Besides, the insertion loss of the 4×4 Butler matrix is around 3 dB. It is lower than 9 dB of STPS in the same 45º phase control resolution. As the result, Butler matrix is used in this design as phase control circuit and for the beam-steering function.

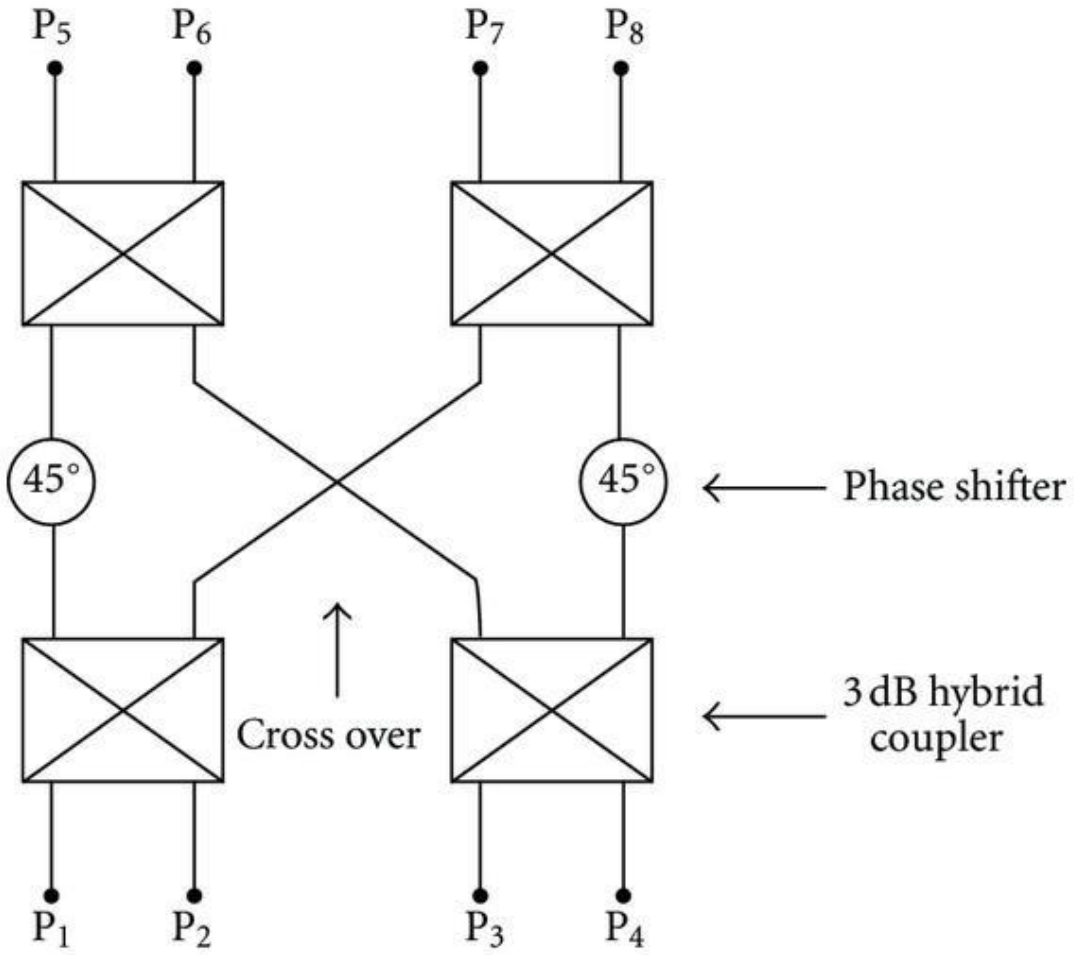

Fig. 4.5. Basic schematic of the 4×4 Butler Matrix [48].

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4.1.5 System Link budget

The gain budget of the beamformer is formulated by the link budget of the whole module which the beamformer be involved. For the whole module, the link budget can be planned into three parts: receiving path, transmitting path, and air channel.

A. Receiving path

The receiver required sensitivity is depended on the modulation and coding scheme (MCS) of signal, which affect the required signal-to-noise ratio (SNR) for demodulation in baseband circuit. In this system, the design target is 4.6-Gbps throughput over 3-meter distance point-to-point transmission. The data rate is supported by using π/2-16QAM modulation with 3/4 coding rate of single-carrier physical layer (SC PHY) [42]. The practical throughput depends on the packet error ratio (PER) of the demodulated signal [49]:

$$\text{Throughput} = (1 - PER) \times \text{bit rate} \tag{4.1}$$

The relation between packet error ratio (PER) and symbol error rate (SER) [49]:

$$PER = 1 - (1 - SER)^n, \text{ where n is the symbols in a packet} \tag{4.2}$$

Thus,

$$\text{Throughput} = (1 - SER)^n \times \text{bit rate} \tag{4.3}$$

Note that the 16QAM have 16 symbols in its constellation and carries 4 bits in a symbol, and there are 448 symbols in a packet that defined in the 802.11ad specification [42].

The throughput can be confirmed to exceed 89.4% of bit rate while the SER is below

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5×10^{-3}. The SER versus SNR among modulation scheme in additive white Gaussian noise (AWGN) channel as shown in Fig. 4.6. It shows that the SER is below 5×10^{-3} while the SNR is higher than 12 dB. Thus we use 12 dB of SNR for the receiving path link budget calculation.

The link budget of receiver path can be calculated from the sensitivity. Behind the baseband, the noise figure is determined by the BDA with its front-end circuits due to the 16-dB gain is adequate to isolate its back-end loss in the noise figure calculation. The BDAs have a noise figure of 7 dB, the front-end SPDT switch has 2-dB insertion loss, and the transition and routing loss between the chip and antenna is estimated as 2 dB. As the results, the 11-dB noise figure is estimated for each antenna path. In the principle of phased array [50], an *N*-element array can improve the SNR by *N* times. In other words, the SNR is improved by 6 dB for the 4-element array.

The sensitivity $(S_{\min})$ can be derived from noise floor (kT_0), channel bandwidth (*B*), noise figure of front-end circuit (*NF*), and minimal required SNR of baseband $\left(SNR_{\min}\right)$ [51]:

$$\begin{aligned} S_{\min} &= kT_0B\left(NF\right)\left(SNR_{\min}\right) \\ &= \text{-}174\text{dBm} + 10\log\left(B\right) + NF\left(\text{dB}\right) - 10\log(N) + SNR_{\min}\left(\text{dB}\right) \\ &= \text{-}81.6\text{dBm} + 11\left(\text{dB}\right) - 6(\text{dB}) + 12\left(\text{dB}\right) \\ &= \text{-}64.6\text{dBm} \end{aligned} \tag{4.4}$$

Note that the bandwidth is 1.76 GHz for each channel of 802.11ad band.

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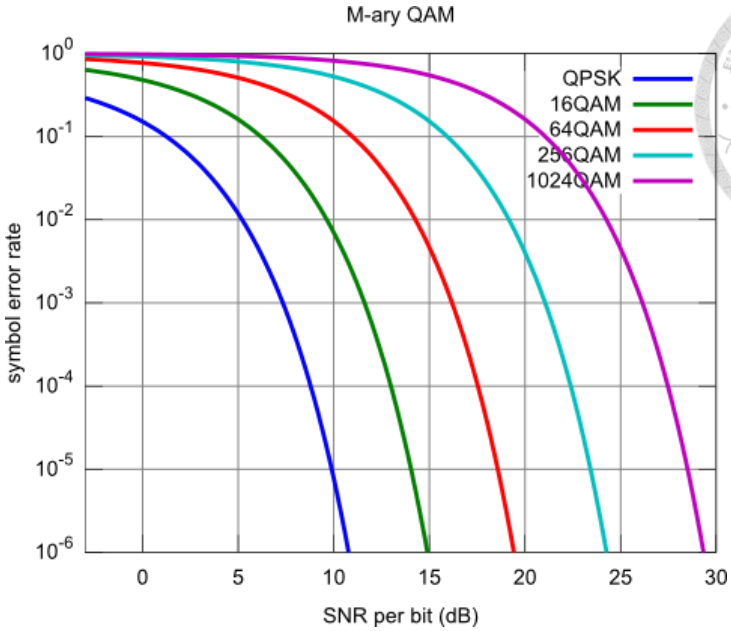

Fig. 4.6. SER versus SNR [52].

B. Antenna and air channel

The antennas do not offer real power gain, but focus the main beam of radiation pattern to a specific direction. In fact, the high antenna gain can avoid the power dissipation in the unwanted radiation direction. At 60 GHz, the 4-element antenna array demonstrates above 10-dBi gain [53]. In order to cover bigger beamwidth and achieve the tolerance of excited phase error, a conservative 8-dBi gain for each 4-element antenna array is expected. Note that the small-range excited phase error will cause the degradation of the directivity, but the wider beam width can cover a larger radiation angle.

The propagation loss of microwave can be estimated by Friis free space equation [54]:

$$P_r = \frac{g_r g_t \lambda_0^{\,2}}{(4\pi r)^2} P_t \tag{4.5}$$

The channel loss is depended on the operated frequency and path distance. The proposed

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module is designed for application of 3-meter distance with 60-GHz carrier frequency. From the Friis equation, the path loss (PL) is 77.6 dB.

C. Transmitting path

The transmitter budget planning is the last step because the EIRP of transmitter is determined by the receiver sensitivity and the path loss. The *N*-element phased-array improves the EIRP by *N* times [55], thus the 4-element array can offer extra 6-dB gain. The maximum signal amplitude is 3 times of the minimum signal amplitude in the 16QAM modulation. In other words, there are up to around 5-dB variation of power while transmit the 16QAM signal. The link budget must confirm that the lowest Tx power is adequate to cover the sensitivity of Rx through the air channel. Thus a back-off 5 dB from Tx $OP_{1\text{dB}}$ is considered in the calculation.

The BDA have 6-dBm $OP_{1\text{dB}}$, thus the operated output power is 1-dBm after a 5-dB back-off. By adding the 4-dB loss produced by front-end SPDT switch and transition, the operating power is -3 dBm for each Tx antenna. Thus the received power of each Rx antenna is:

$$\begin{aligned} \text{Pr} &= Pt + 10\log(N) + Gt(\text{dB}) - PL(\text{dB}) + Gr(\text{dB})\text{-}AF(\text{dB}) \\ &= -3\text{dBm}+6(\text{dB}) + 8(\text{dB}) - 77.6(\text{dB}) + 8(\text{dB})\text{-}6(\text{dB}) \\ &= -64.6\text{dBm} \end{aligned} \tag{4.6}$$

which is equal to the Rx sensitivity. From the above calculation, the link budget of the whole module as shown in Fig. 4.7.

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In the whole module, the beamformer is placed between antenna arrays and transceiver. We suppose that the transceiver have the same noise figure and OP_{1dB} as the BDA, it is a conservative assumption due to the separated PA and LNA usually have the better performance. From the budget of front-end and back-end sides, the gain budget of the beamformer is estimated. The Butler matrix have the loss of 3 dB, the switches for T/R port selection with array group selection have the loss of 5 dB, the front-end switch used for selecting the antenna array have the 2-dB loss. For the packaging concern, the flip-chip and routing loss for the I/O of the beamformer is estimated as 2 dB for each transition. Finally, as the only active components, the BDAs are expected to offer a bidirectional 16-dB gain to compensate the loss of passive components. As the results, the gain budget of the beamformer is shown in Fig. 4.8.

Note that the beamformer is operating in Rx mode in the receiving path, and operating in Tx mode in the transmitting path. The design of the functional blocks and the whole beamformer are presented in the sections 4.2 and 4.3, respectively.

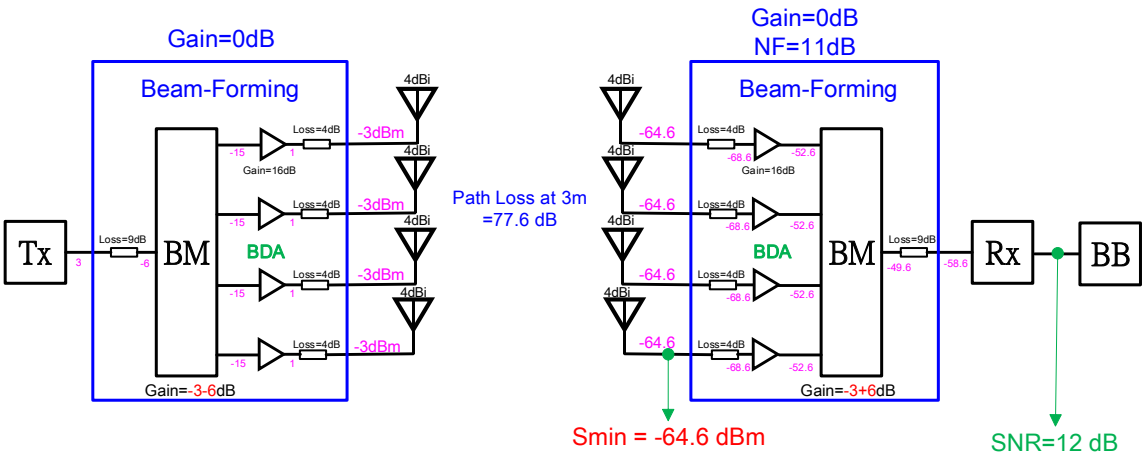

Fig. 4.7. Link budget of the whole module.

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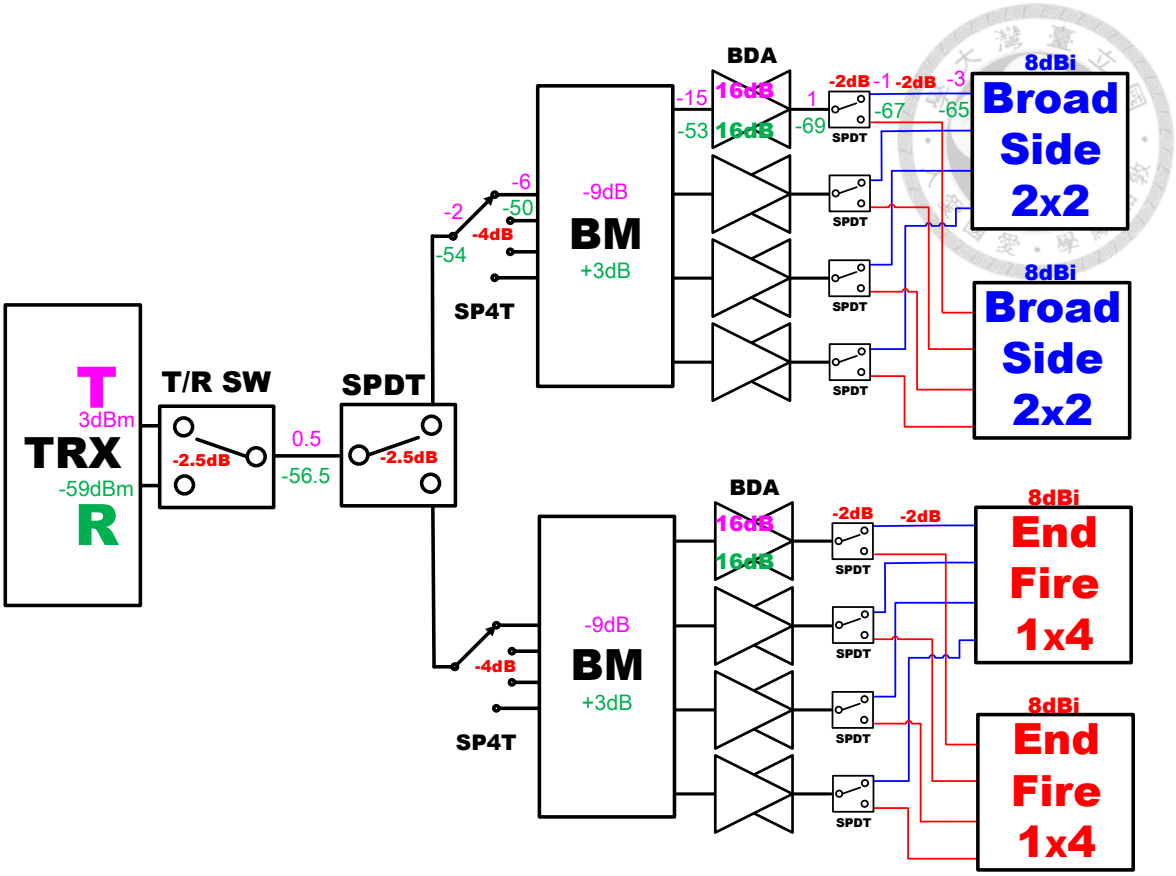

Fig. 4.8. Gain budget of the beamformer.

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4.1.6 Digital Control

To control the operation of the phase-array module, the digital circuit is used to reduce the physical I/O in the system. The 3-bit SET [2:0] are used to determine the control mode. In each control mode, the 4-bit PAR [3:0] are the control parameters. The digital control plan are shown in Table 4.1.

The plan offers 8 control modes, the [001] and [010] are used for local control of beamformer. The [000] is defined as idle state used for the connection have established. The [100] and [111] are used for the local control of transceiver. The [101] and [110] are the global control of gain change. The [011] is the global control for turning off the whole phased array module. Besides, the 8-bit parameters PAR [7:0] are defined to control the RFICs, the beamformer uses the first 4-bit PAR [3:0], the other 4-bit PAR [7:4] are used in the transceiver for simultaneously controlled in the whole phased array module.

Table 4.1. Digital control plan of the beamformer.

SET[2:0]	Control Mode	PAR[3:0]	Description
011	Power down	[xxxx]	Turn off all RF circuits
001/010	Beam Selection	[0000]-[1111]	16-beam state selection
101/110	Gain Change (Power Saving)	[xx00]-[xx11]	4 gain state selection

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4.2 Implementation of Functional Blocks

The system plan has been presented in section 4.1, and the physical design will be illustrated in next section (section 4.3). This section will present the functional blocks which are used in the system design.

4.2.1 Butler Matrix

The Butler matrix is contributed by Professor Huei Wang and his student Yi-Ching Wu and Po-Yu Chen of National Taiwan University. The 4×4 Butler matrix is designed for phase control. It is built by four 90º couplers, a cross-over, and two 45º phase shifters. The 90º couplers are built by broadside-coupled lines for stronger coupling. However, the broadside couplers are imbalanced between through arm and coupled arm because the top two metal layers are non-identical in this CMOS process. To resolve this problem, the metal layers are interchanged in the middle of the coupled lines. Although the extra loss will be produced by the additional via, the imbalance can be minimized. The EM structure of the couplers is shown in Fig. 4.9. The cross-over and 45º phase shifters are built by the TFMS lines with 420-μm and 750-μm length, respectively. The 45º phase shift is produced by the 330-μm length difference. Besides, a quarter-wave short stub is placed in the middle of the cross-over line for bandwidth improvement [56].

The block diagram and layout of the Butler matrix as shown in Figs. 4.10 and 4.11, respectively. The layout size is 0.54×0.4 mm^2. The overall simulated results of the 4×4 Butler matrix is shown in Figs. 4.12 to 4.16 which present the frequency response of gain and phase. Note that the response of port1 is identical of port4 due to the symmetric structure, and so are in port2 and port3. For more details, the designed frequency response of phase between all the 16 ports as shown in Table 4.2. From the simulated results, the

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gain and phase error among the 4 excited states from 57 to 66 GHz are below 1.8 dB and 3.3º, respectively.

Table 4.2. Phase relation among the I/O of the proposed Butler matrix.

	Port 5	Port 6	Port 7	Port 8
Port1	-45º	-135º	-90º	-180º
Port2	-135º	-225º	0º	-90º
Port3	-90º	0º	-225º	-135º
Port4	-180º	-90º	-135º	-45º

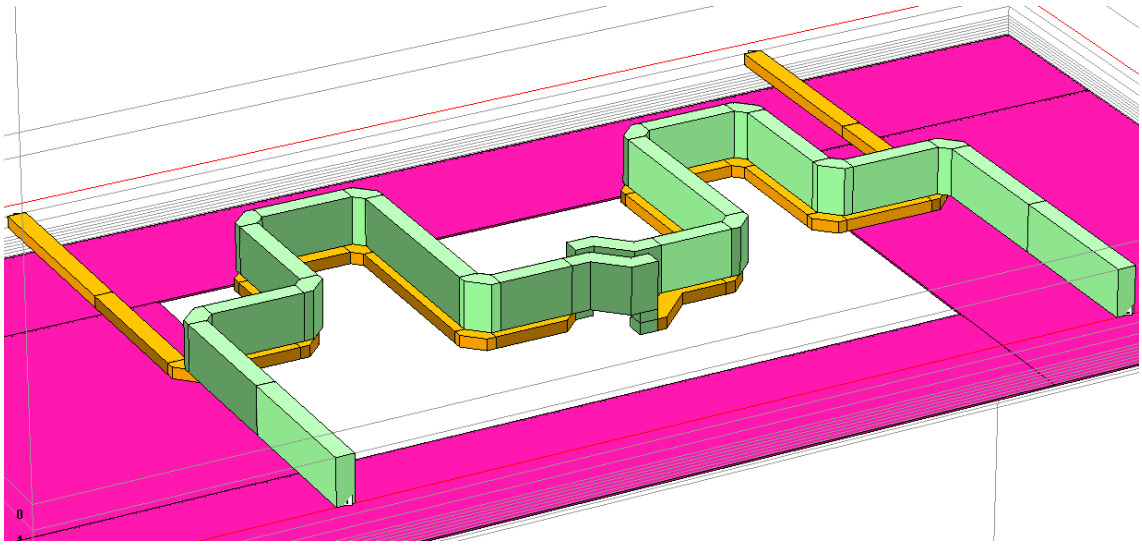

Fig. 4.9. EM structure of the symmetric 90º coupler.

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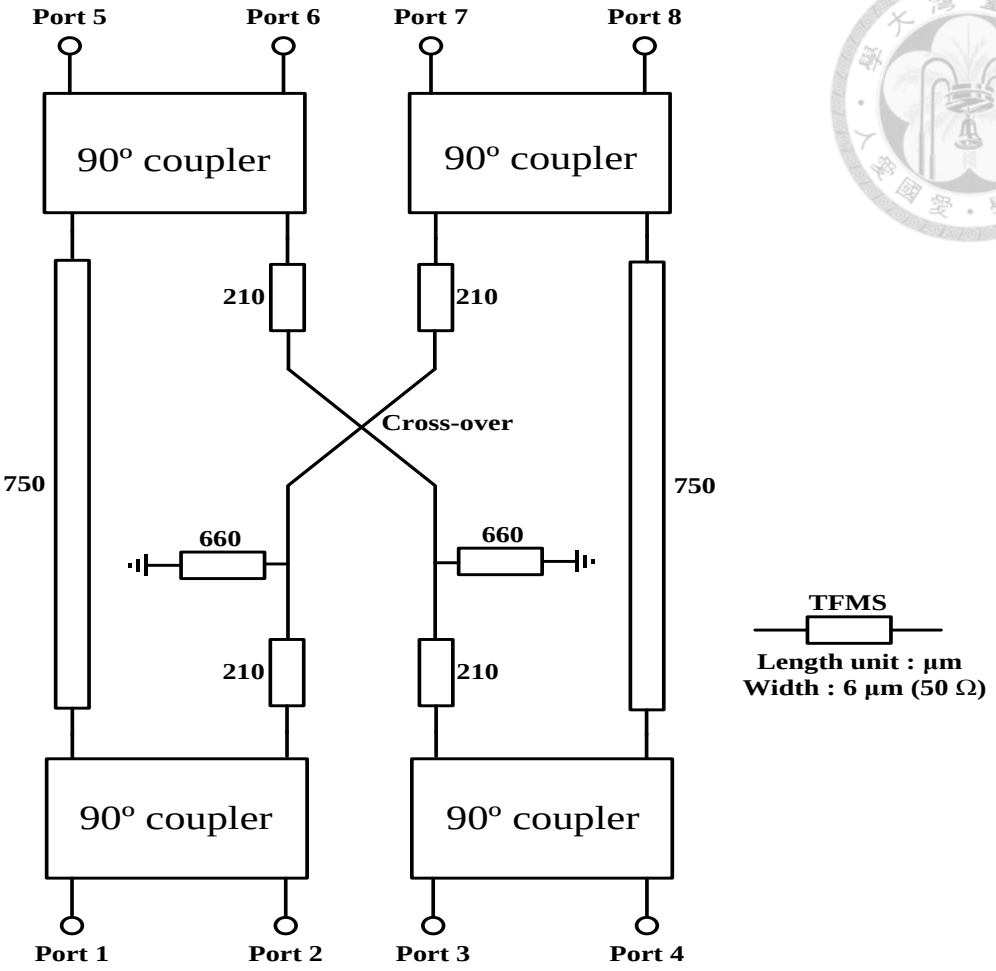

Fig. 4.10. Block diagram of the proposed 4×4 Butler matrix.

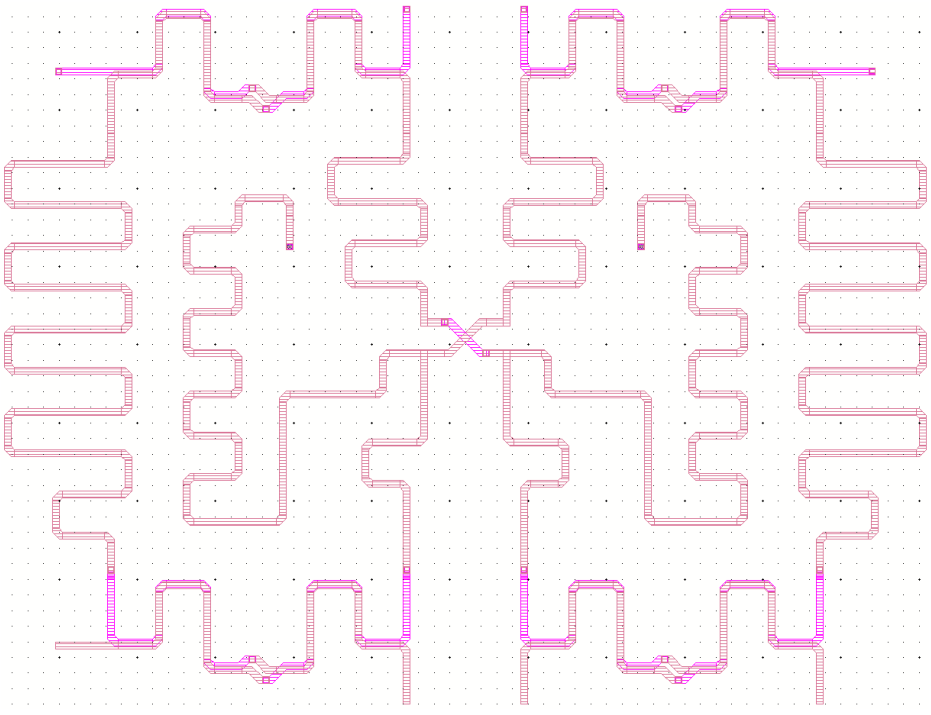

Fig. 4.11. Layout of the proposed Butler matrix.

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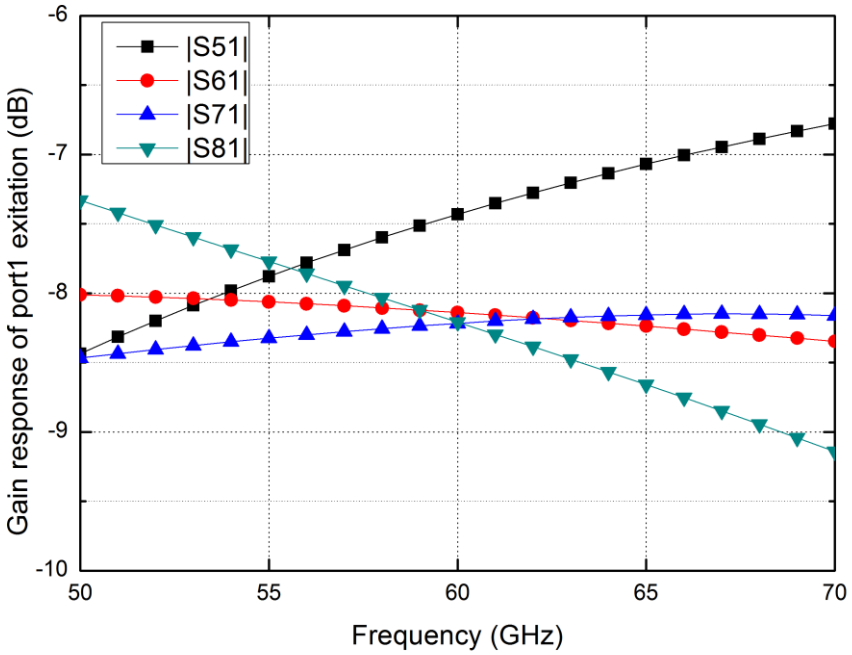

Fig. 4.12. Simulated gain of port1 excitation.

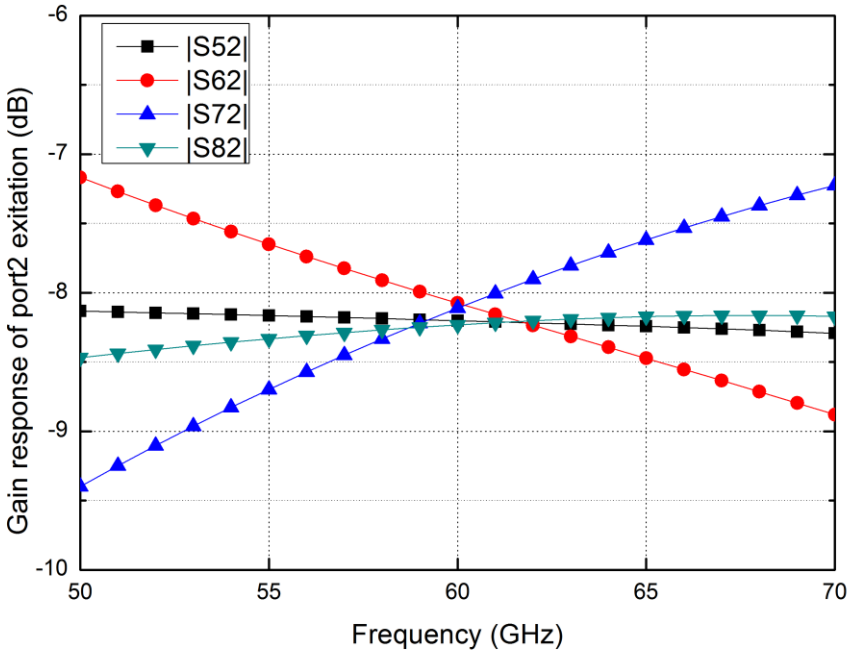

Fig. 4.13. Simulated gain of port2 excitation.

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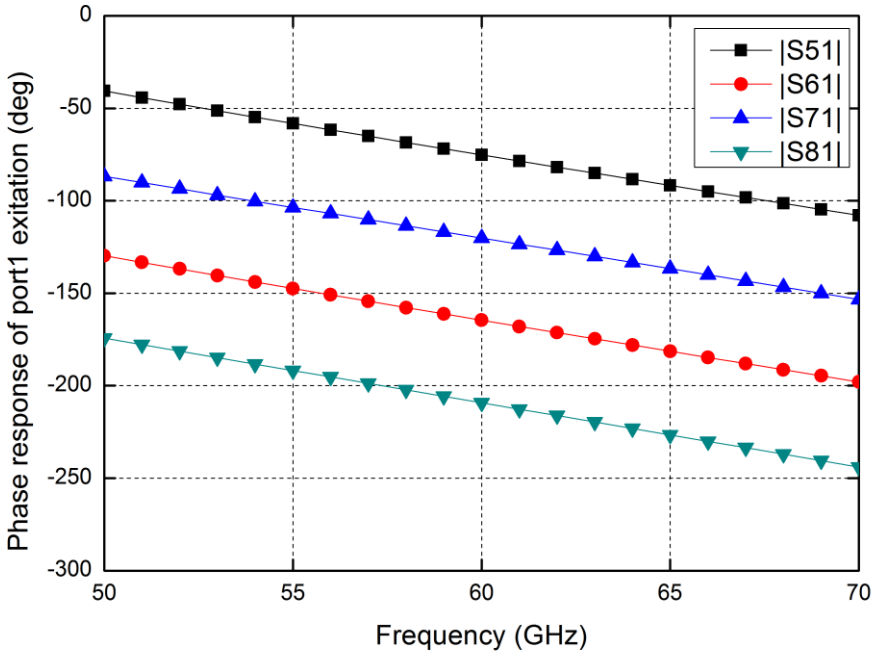

Fig. 4.14. Simulated phase of port1 excitation.

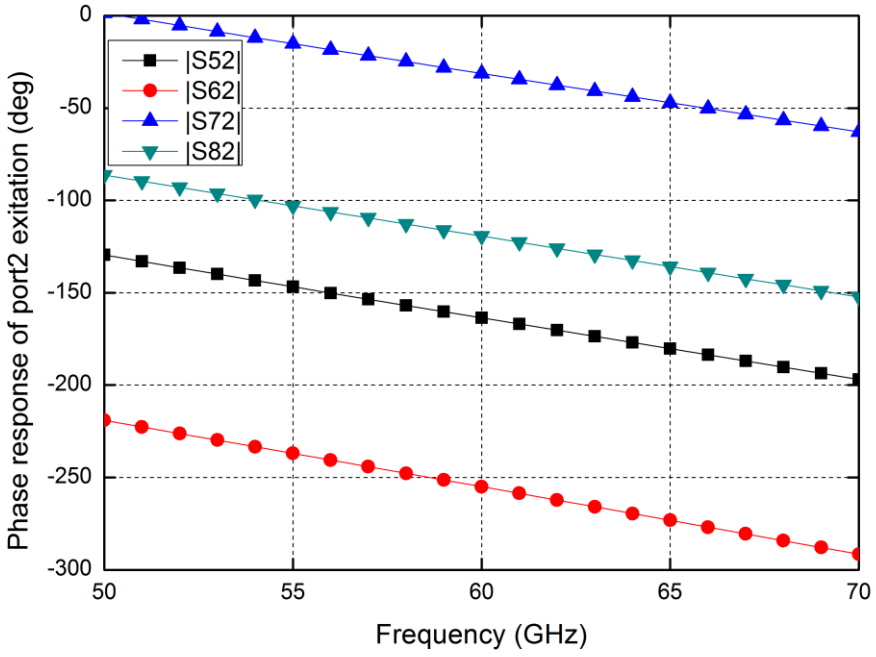

Fig. 4.15. Simulated phase of port2 excitation.

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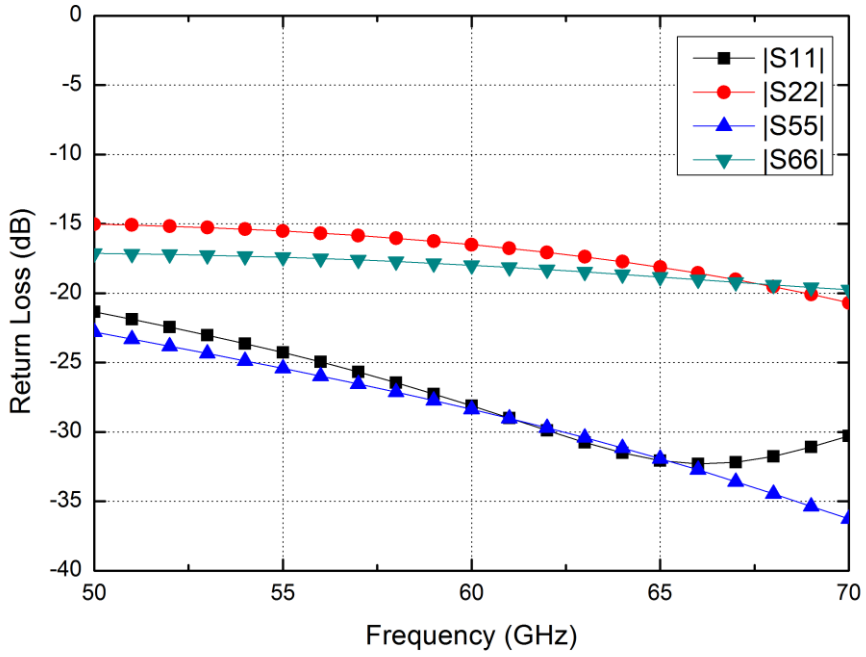

Fig. 4.16. Simulated return loss among the I/Os of the proposed Butler matrix.

4.2.2 Absorptive SPQT switch

The absorptive SPQT switch is contributed by Professor Kun-You Lin and his student Dong-Ru Lin of National Taiwan University. To drive the 4×4 Butler matrix, the port-selected excitation is required. Moreover, due to the built-in couplers in the Butler matrix, the terminations are necessary to avoid the reflection of unwanted signal. For these reasons, an absorptive SPQT switch is designed for these purposes. The absorptive switches have the property of well matching condition at all the I/O ports regardless which arm is tuned on.

Fig. 4.17 shows the schematic of the SPQT switch. The series-shunt structure is used in each output arm. The series-switch and shunt-switch are built by 3×30-μm and 2×8-μm NMOS device, respectively. When the series switch is turned-on, and shunt switch is

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turned-off, the through condition is achieved. On the other hand, when the series switch is turned-off, and shunt switch is turned-on, the isolation condition is achieved.

In order to reach the matching condition of each port, a spiral inductor is parallel connected with the series switch. The inductance is designed to reach the LC resonance at 60 GHz that forms the high impedance in the isolation arm. Thus the input port will only see the through arm, and each output port will see a near 50 Ω produced by the turned-on shunt switch. Fig. 4.18 shows the test circuit layout of the SPQT switch, for which we only use the circuit core in the system, and the core size is 0.29×0.23 mm^2.

The simulated and measured results of S-parameter in through arm and isolated arm are shown in Figs. 4.19 and 4.20, respectively. The SPQT switch performs an insertion loss of lower than 4.3 dB, return losses better than 9.3 dB (through port) and 18 dB (absorptive port), and isolations better than 18.2 dB in each port from 57 to 66 GHz.

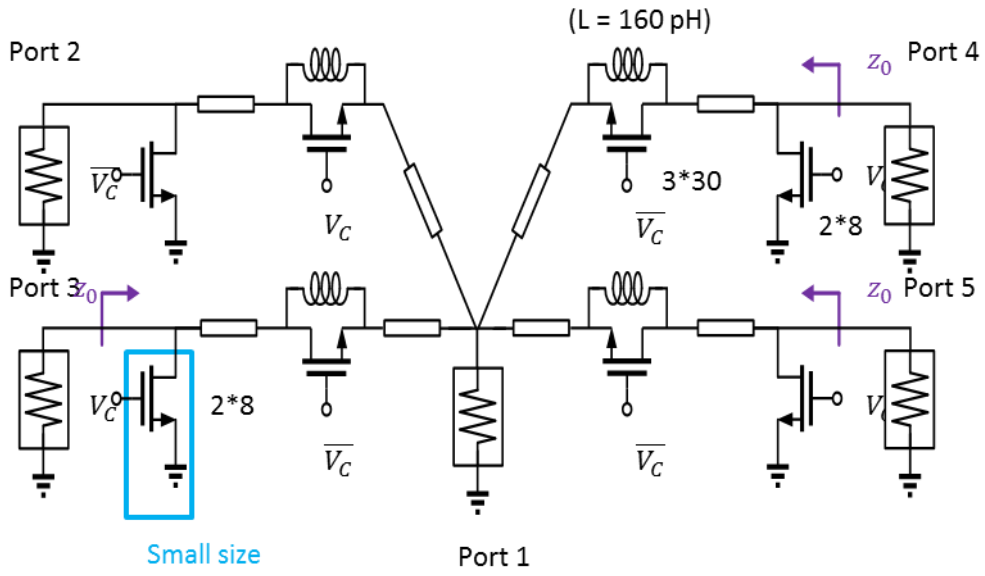

Fig. 4.17. Schematic of the absorptive SPQT switch.

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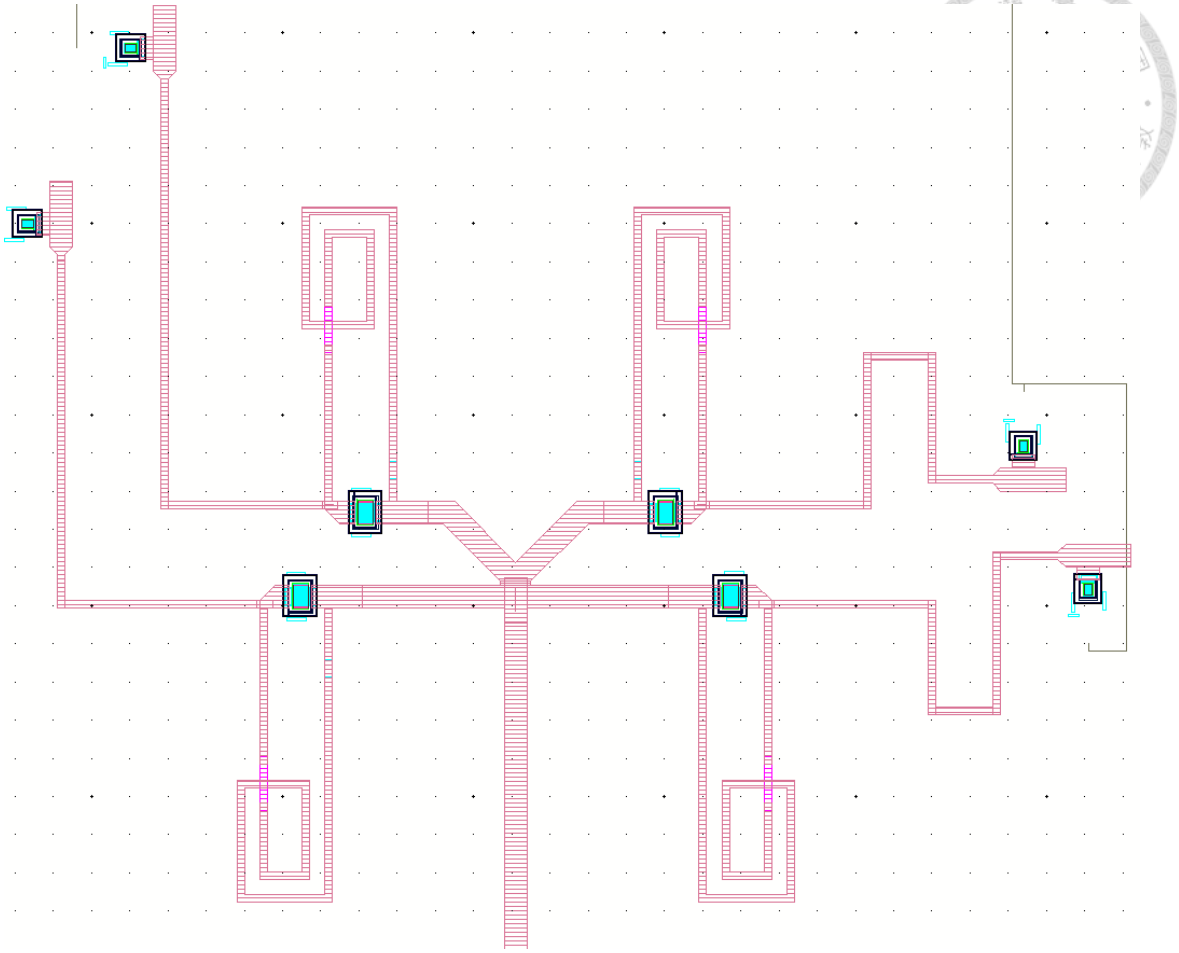

Fig. 4.18. Layout of the absorptive SPQT switch.

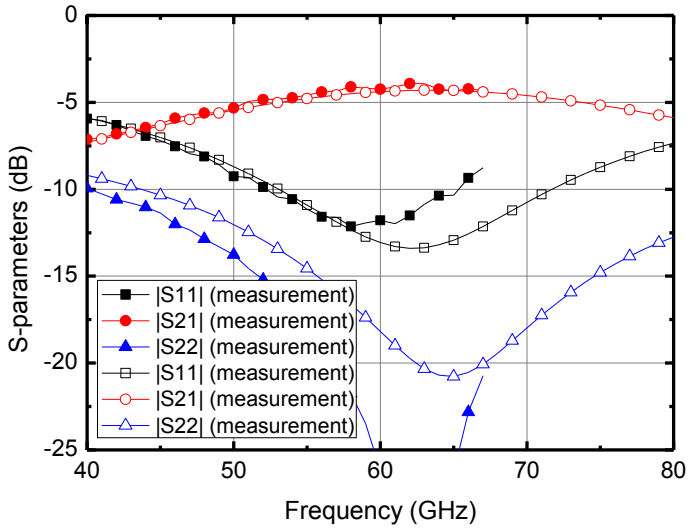

Fig. 4.19. Results of return loss and insertion loss in the thru arm.

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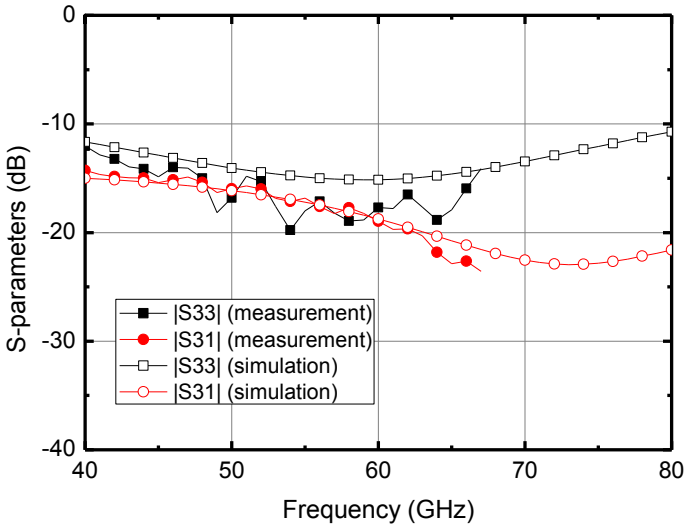

Fig. 4.20. Results of return loss and isolation in the isolated arm.

4.2.3 SPDT switch

The SPDT switch is contributed by Professor Kun-You Lin and his student Dong-Ru Lin of National Taiwan University. The SPDT switches are placed in the front-end of the system, and the insertion loss is the most important parameter. In order to reduce the insertion loss, the single-shunt topology is used in this design. Although the lack of series components results in worse isolation, it is not critical due to the leakage signal will radiate to other direction and will not affect the main radiation pattern.

Fig. 4.21 shows the schematic of designed SPDT switch. The shunt 2×22-μm LVT NMOS with series 470-μm TFMS line are designed for a low insertion loss matching network in the through arm, and also offer adequate isolation in the isolation arm. Figs. 4.22 and 4.23 shows the layout of the two versions of SPDT switches which used in the front-end of the system, the chip areas are 0.27×0.2 mm^2 and 0.48×0.15 mm^2, respectively. The non-symmetry of the TFMS lines in two arms are caused by the routing

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between I/O pads and BDAs in the system chip. The simulated and measured results of the test circuit of version1 SPDT switch are presented. The insertion loss, isolation and return loss are shown in Figs. 4.24 and 4.25.

In the back-end of the system, a DPDT switch consisted of two SPDT switches is used. One SPDT is for selecting the connection of Tx/Rx port, and another is for selecting group of endfire/broadside antenna array. Based on the same architecture of front-end SPDT switches, the insertion loss can be minimize. Figs. 4.26 and 4.27 show the simulation and layout of the DPDT switches, respectively. The same as the front-end switches, the two arms are non-equal in the single SPDT switches due to the system integration.

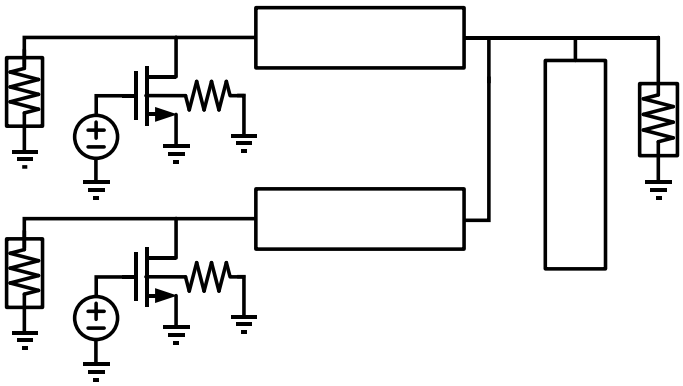

Fig. 4.21. Schematic of the SPDT switch.

doi:10.6342/NTU201603106

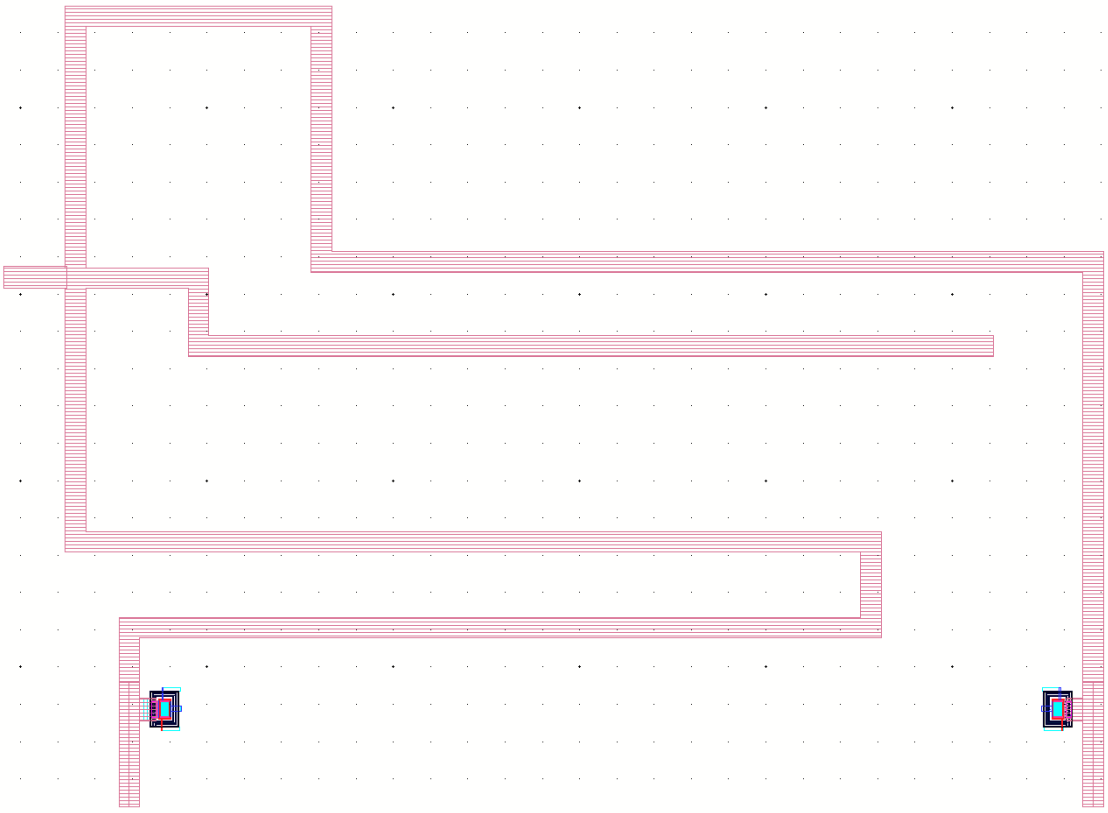

Fig. 4.22. Layout of the SPDT switch (version1).

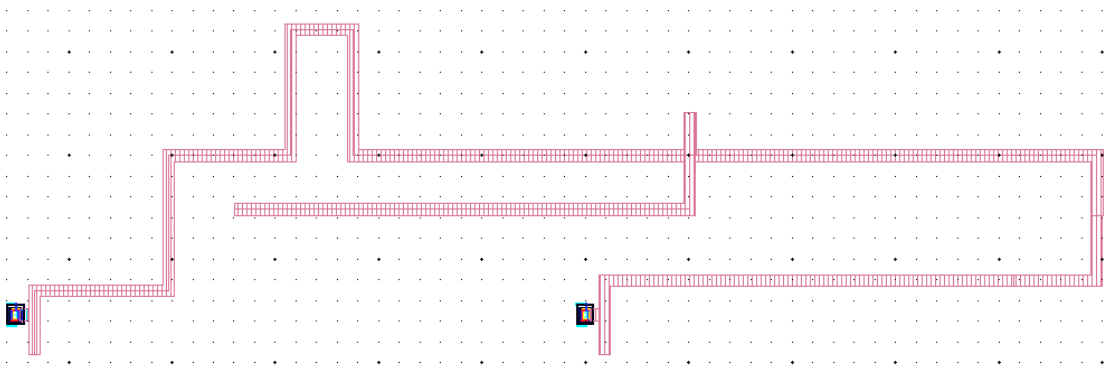

Fig. 4.23. Layout of the SPDT switch (version2).

doi:10.6342/NTU201603106

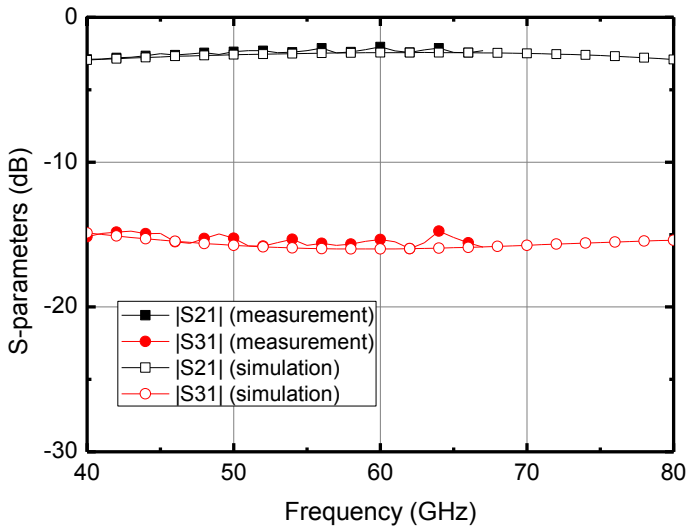

Fig. 4.24. Experiment results of the insertion loss and isolation.

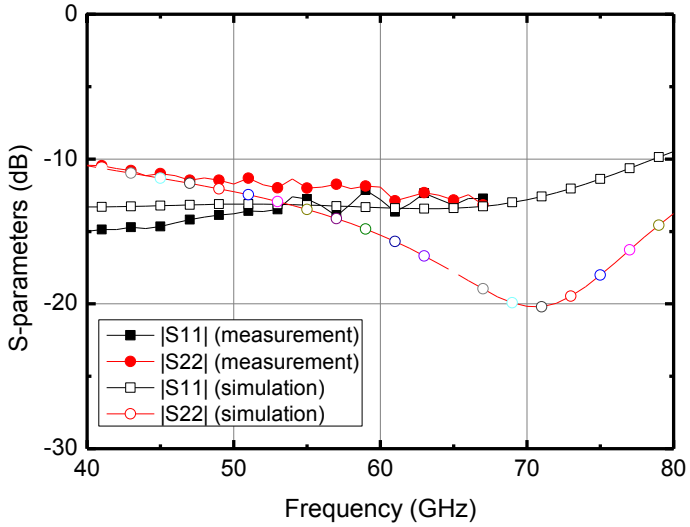

Fig. 4.25. Experiment results of the return loss.

doi:10.6342/NTU201603106

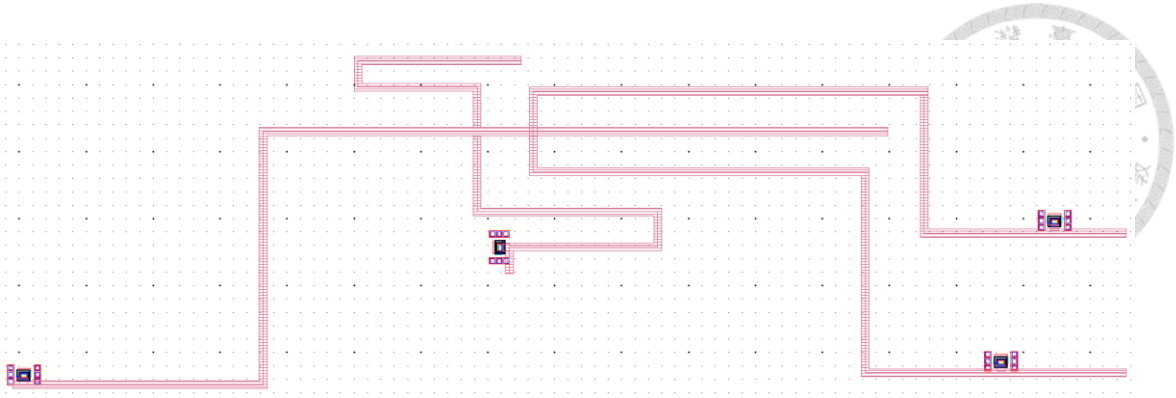

Fig. 4.26. Layout of the back-end DPDT switch.

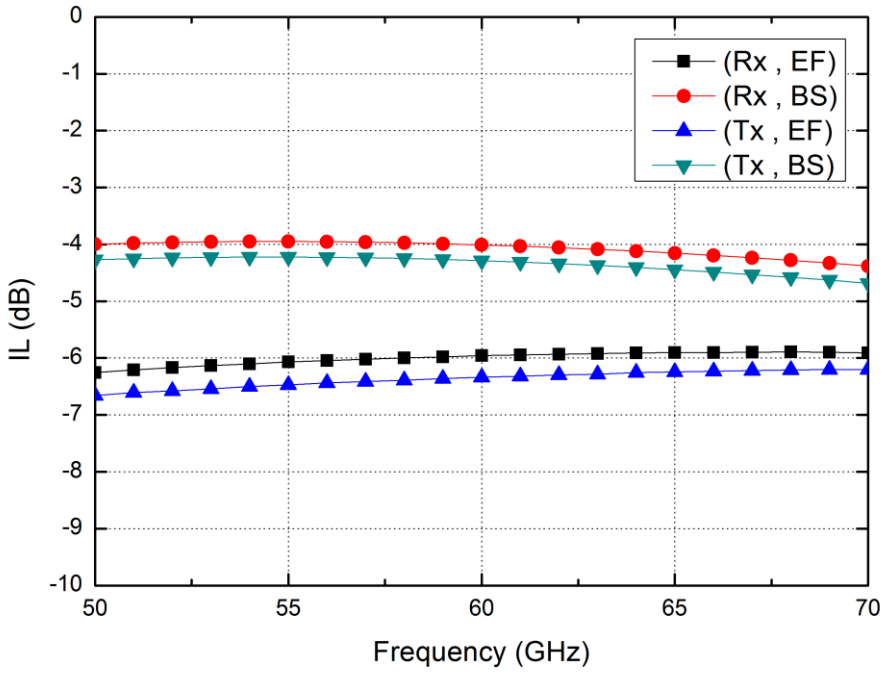

Fig. 4.27. Simulated results of the DPDT switch.

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4.2.4 Bidirectional Amplifier

The BDAs is the most critical component in the system, it functions a LNA and avoids the SNR degrade in Rx mode, and functions a PA for offering an adequate power to antennas in Tx mode.

Fig. 4.28 shows the schematic of the BDA. The BDA is consisted of a PA and a LNA, which are in anti-parallel placement and connected by the junction networks. The direction of amplification is controlled by gate bias in each amplifier. By using the difference of I/O impedance between on/off states, the junction networks perform act as the matching network in the turned-on path, and as an isolating network in the turned-off path. Both the PA and LNA utilize differential common-source stages with transformer-coupled matching network. Besides, the neutralized capacitors are used in the last two stages of PA for better performance of gain and bandwidth. From the measured results of test circuit, it exhibits a gain of higher than 10-dB in each mode, 8-dB noise figure in Rx mode, and near 10-dBm maximum output power in Tx mode. More design details have been presented in chapter 3.

Fig. 4.29 shows the layout of the BDA. Because the circuiut of BDAs dominates the total size of the beamforming system, the transformer-coupled and differential topology help to minimized the size of BDAs. We use the circuit core with a compact size of 0.12 mm^2. By reducing the size of the repeated components, the total chip size can be minimized.

doi:10.6342/NTU201603106

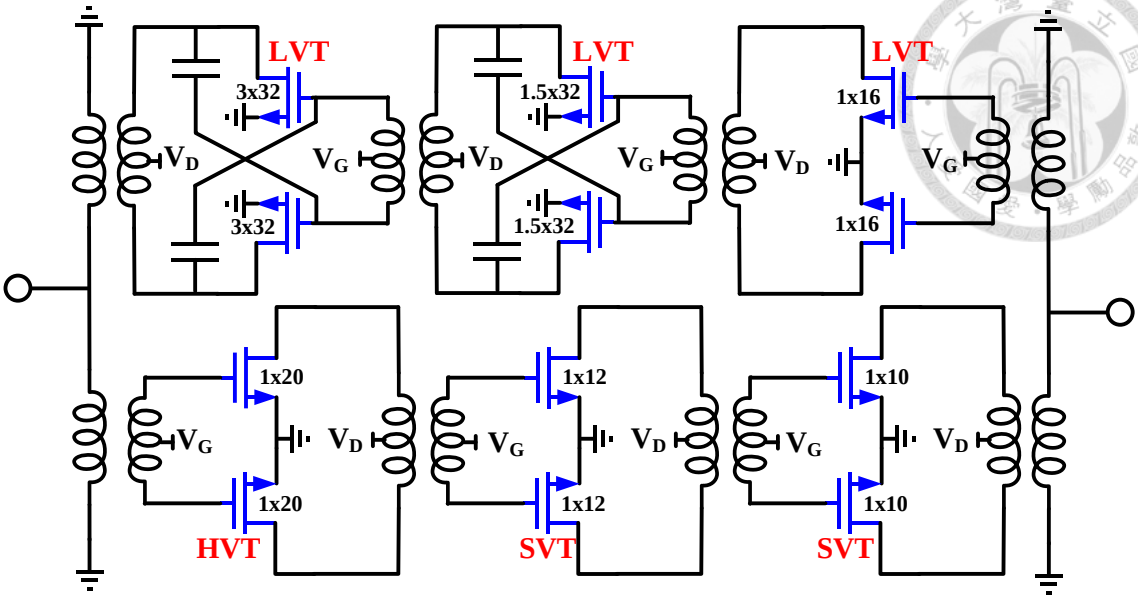

Fig. 4.28. Schematic of the BDA.

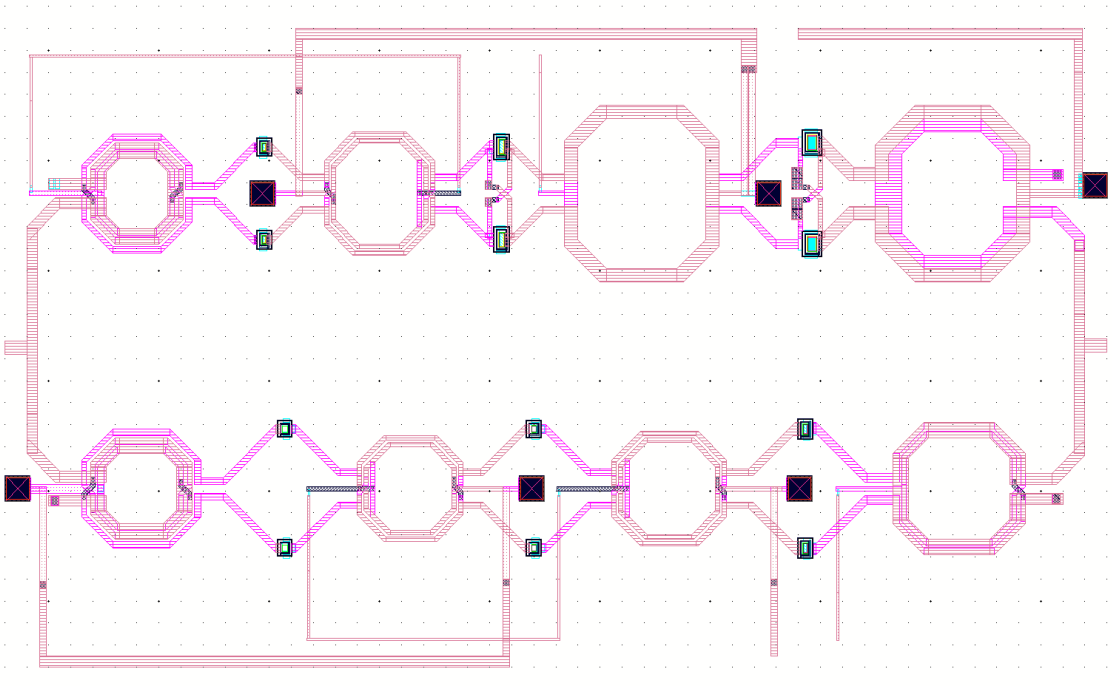

Fig. 4.29. Layout of the circuit core of BDA.

doi:10.6342/NTU201603106

4.2.5 Bias circuit

The global bias circuit is contributed by Dr. Kun-Yao Kao. In order to provide the temperature independent bias for the RF circuits, the bias circuits are designed. Fig. 4.30 show the schematic of the global bias circuit. The global bias circuit include a bandgap reference generator which offers the temperature invariant reference voltage (V_{ref}) of 1.25 V in the silicon process. Thus a near-ideal reference current (I_{ref}) is generated by an operational amplifier (OPA) and an accuracy external resistor (R_{ext}) The I_{ref} produces the 15 replicas that each one offers the current from 75 to 150 μA in 25 μA steps, the value is controlled by the PMOS switches that cascoded on the current mirrors. The operated voltage of VDD is 2.5 V for the global bias circuit.

The local bias circuit is designed for translating the global bias current to the gate voltage of the local BDAs. The 0.6 μm/0.24 μm NMOS is used for mapping the 100 μA I_{ref} to 0.93 V for the LNAs, and 2.4 μm/0.24 μm NMOS is used for mapping the 100 μA I_{ref} to 0.65 V for the PAs. Besides, the shunt 12 μm/0.04 μm switch functions as a grounded path while the bias is turned off.

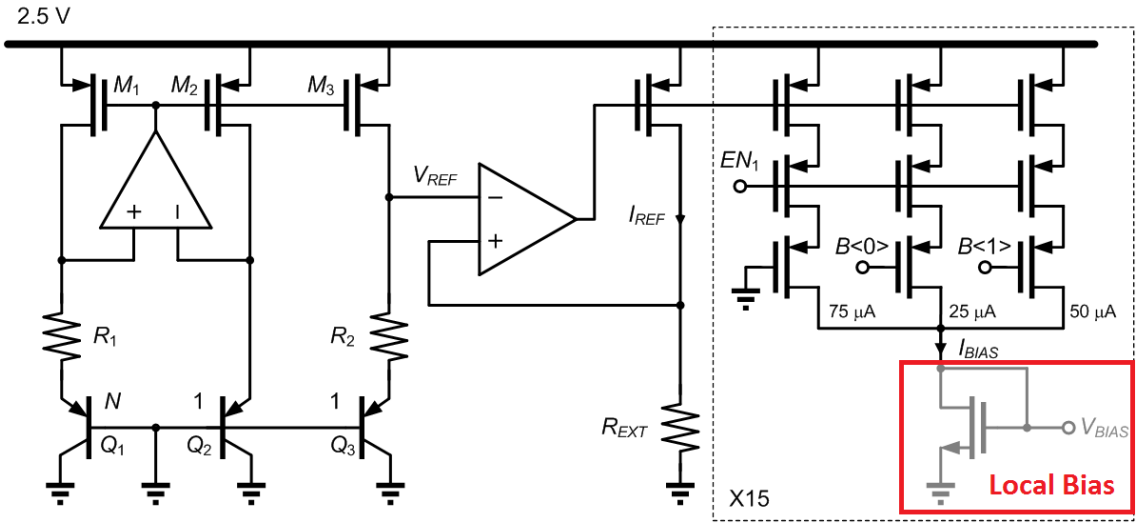

Fig. 4.30. Schematic of the global bias circuit.

doi:10.6342/NTU201603106

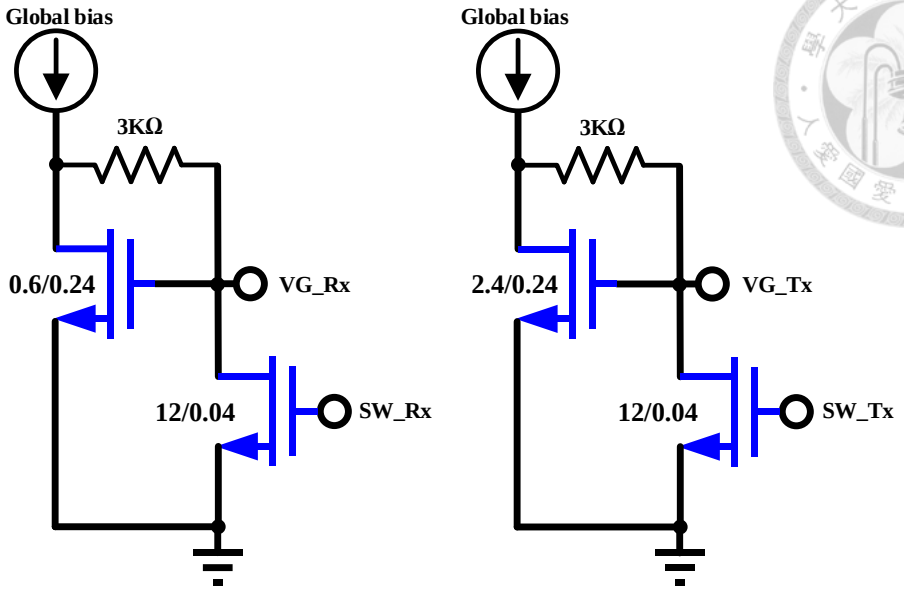

Fig. 4.31. Schematic of the local bias circuit.

4.2.6 Digital circuit

The digital circuit is contributed by Professor Yi-Chang Lu and his student Hao-Wei Liu of National Taiwan University. Based on the control plan, the digital circuit is realized in register transfer level (RTL) code at first, then compiled to the transistor level circuit by using the automatic place and route (APR) tools. The digital control is realized by two digital blocks, which are named as block1 and block2, respectively. The block1 is realized by the original control plan (section 4.1.6). The power-down function is originally planned to control the power switch of global bias circuit by 1-bit in the block1. However, there is no such a switch in the global bias circuit. In order to reduce the effort of re-design, the block2 is designed to resolve this issue. It offers 4-bit to control the grounded switches in the local bias that can turn off all the BDAs, and thus reach the power-down function. In other words, the block2 is a patch to fix the digital connection problem of the block1. The gate level schematic and layout of the two digital blocks as shown in Figs. 4.32 to 4.35. And the physical connections of the two blocks as shown in Fig. 4.36.

doi:10.6342/NTU201603106

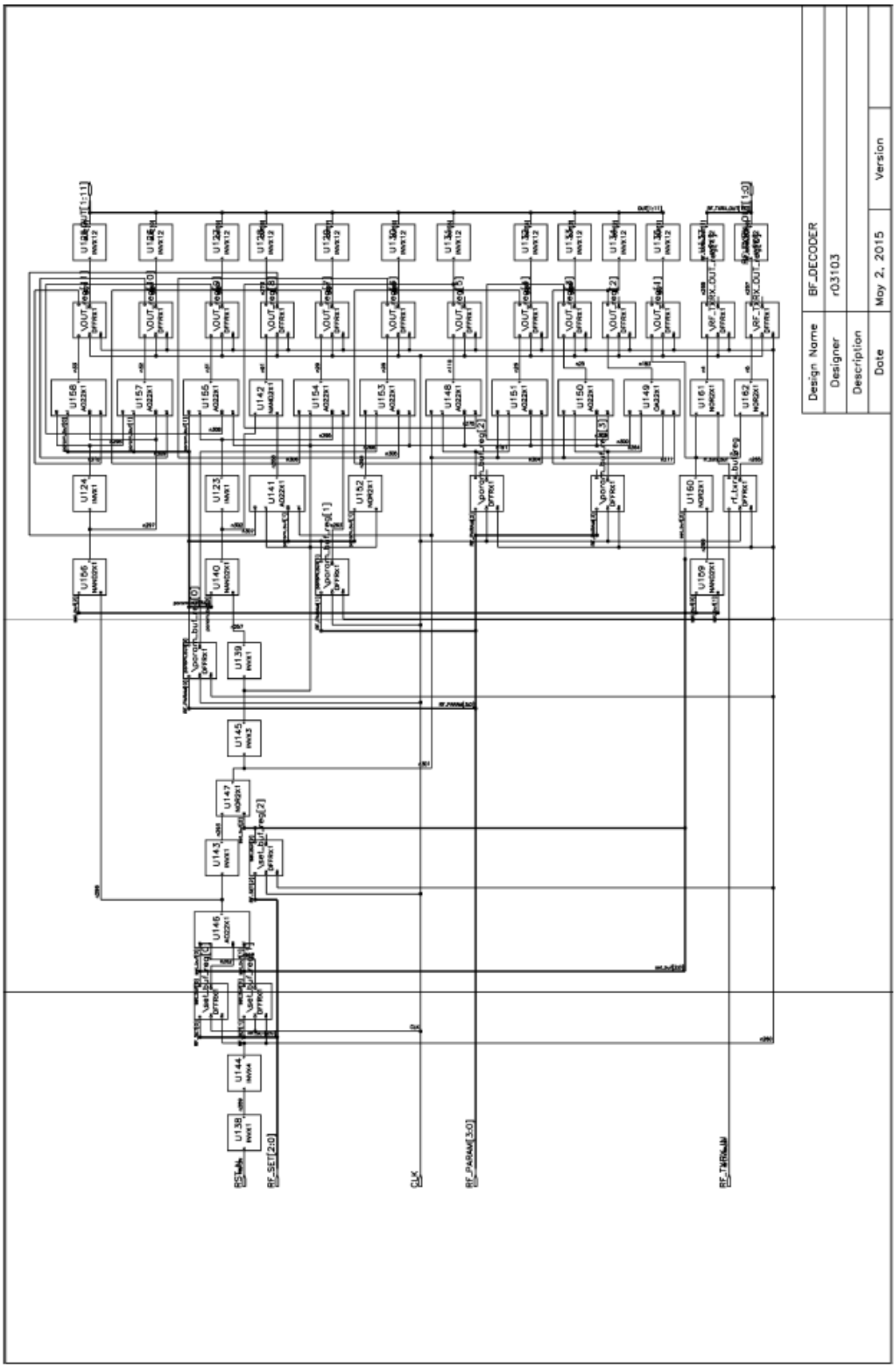

Fig. 4.32. Gate level schematic of the digital block1.

doi:10.6342/NTU201603106

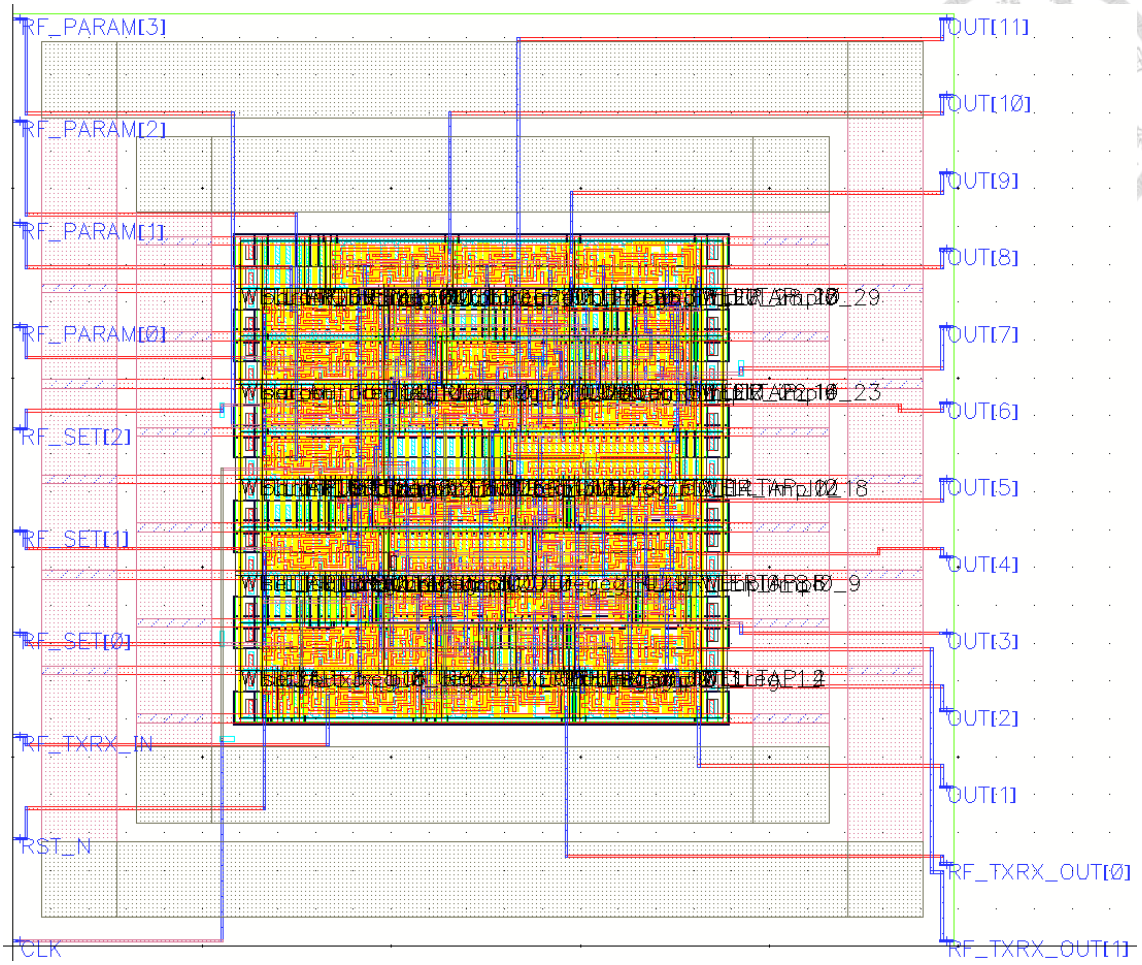

Fig. 4.33. Physical layout of the digital block1.

doi:10.6342/NTU201603106

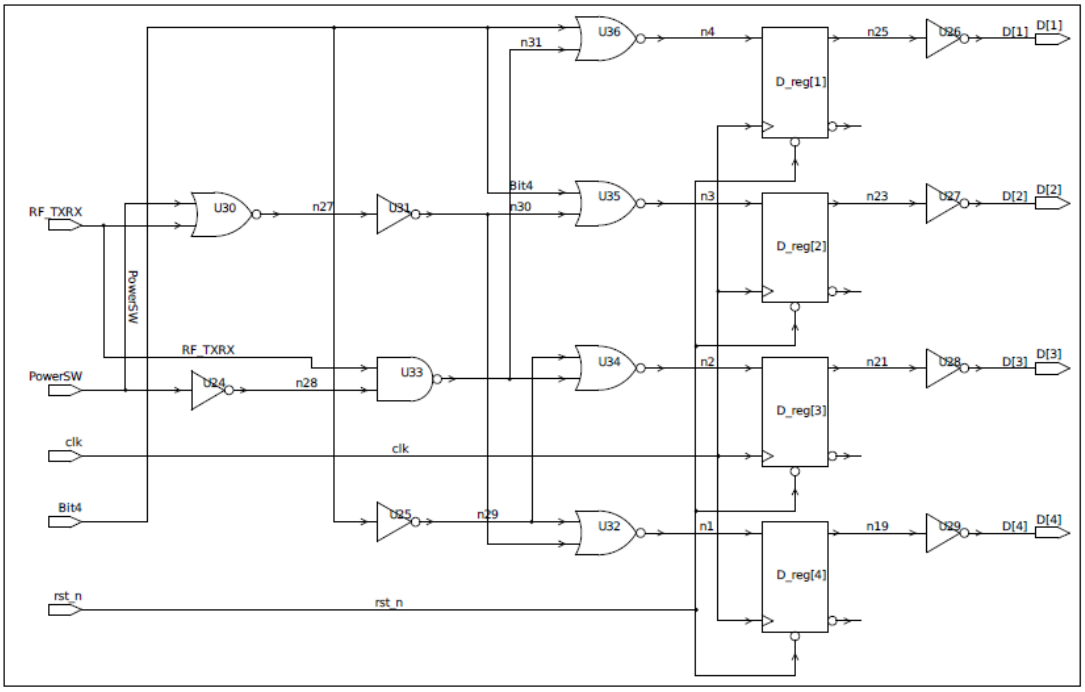

Fig. 4.34. Gate level schematic of the digital block2.

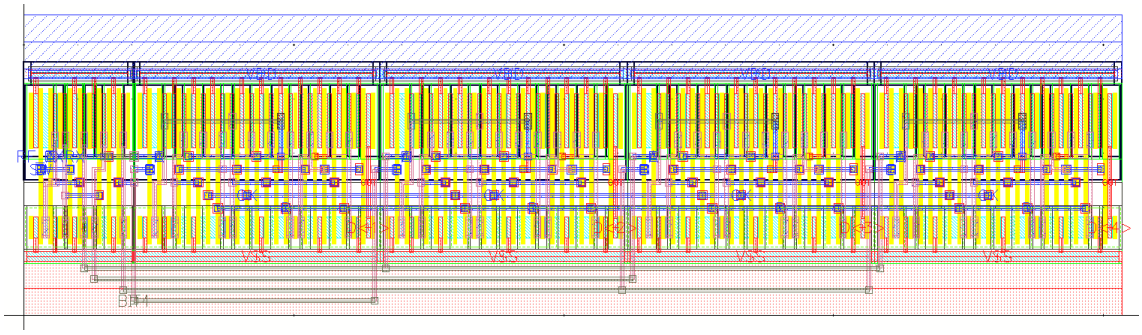

Fig. 4.35. Physical layout of the digital block2.

doi:10.6342/NTU201603106

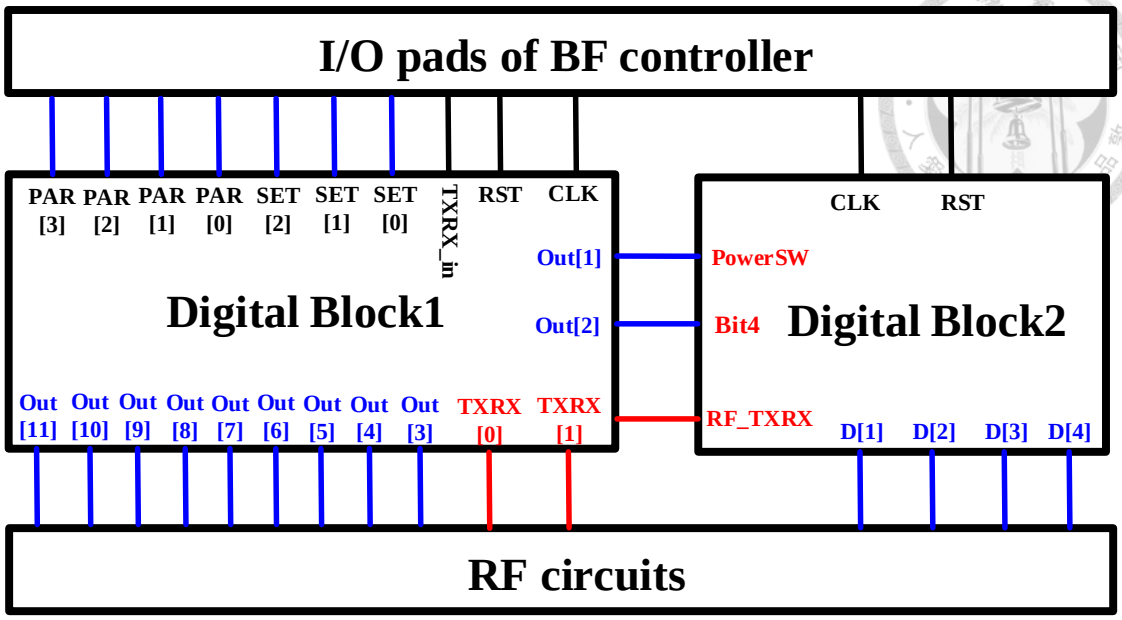

Fig. 4.36. Pin connection between the digital blocks.

doi:10.6342/NTU201603106

4.3 Beam forming system

4.3.1 System design

By compositing the functional blocks as mentioned in section 4.2, the beamforming system is shown in Fig. 4.37. The system is designed to incorporate with a transceiver and 4 individual antenna array in 2 groups. One group includes 2 endfire arrays and the other one includes 2 broadside arrays. Each group is driven by a gain/phase control network which includes a SPQT switch, a Butler matrix, 4 BDAs, and 4 front-end SPDT switches. The phase control is realized by using the SPQT switch to select the excited port of the Butler matrix, and thus the Butler matrix produce the designed phase relation at the 4 output ports. After the Butler matrix, the BDA offers the signal amplification. Finally, the front-end SPDT switches are used to select the one of two array in the array group.

All the front-end SPDT switches are controlled by a synchronous digital bit. Although the other switches which are in the unused array group will be operated simultaneously, it is not critical because only one array is used at the same time. From system viewpoint, the switches offer the port expansion form 8 to 16. At the back-end side, the other two SPDT switches are placed. One is for selecting the array group (endfire/broadside), while another is T/R switch used to guide the signal from Tx port or to Rx port of transceiver.

doi:10.6342/NTU201603106

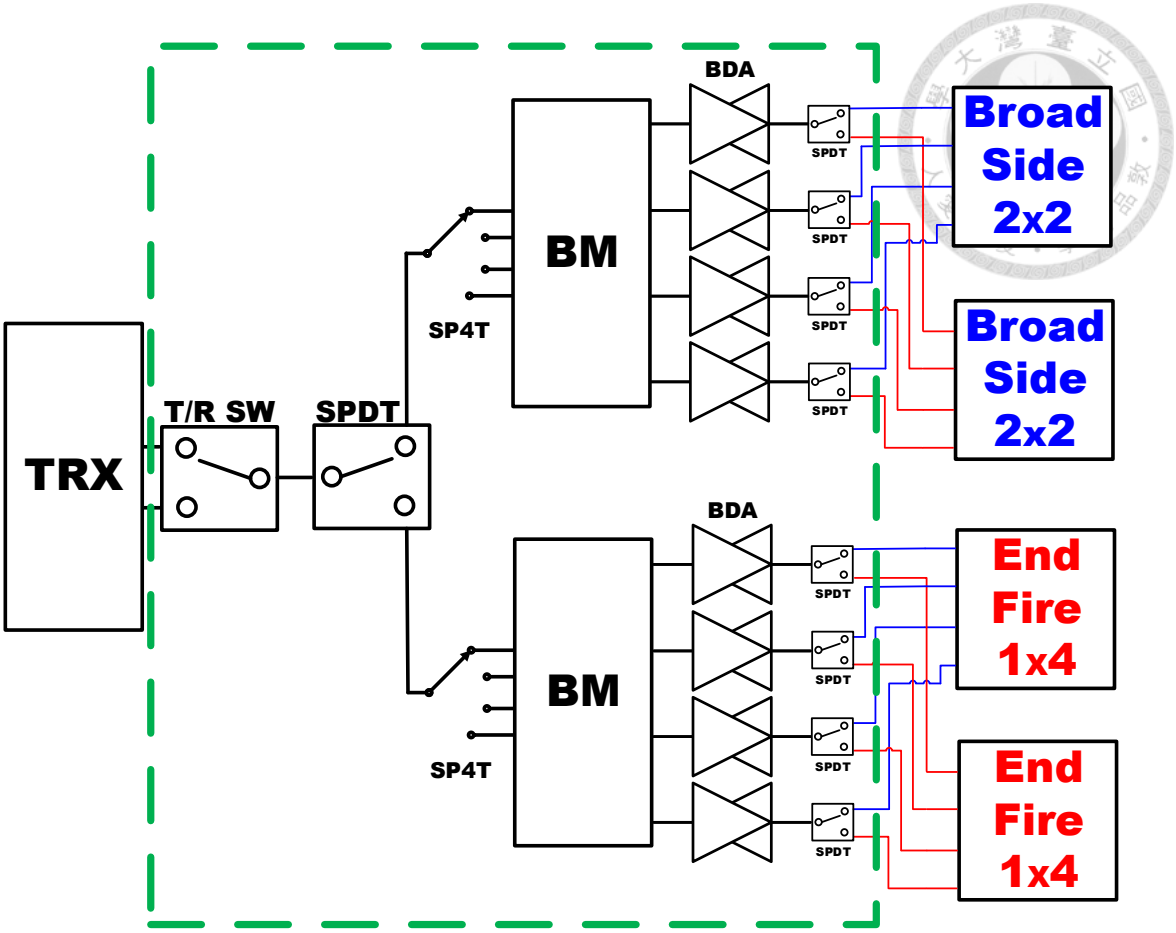

Fig. 4.37. Block diagram of the beamformer.

doi:10.6342/NTU201603106

4.3.2 Layout and I/O arrangement

The layout of the system as shown in Fig. 4.38. The chip size is 1.84×1.58 mm^2, or 2.9 mm^2. The I/O pad size is 63×63 μm^2. The pads are designed for bumping process, with which it helps the system can be flip-chip assembled on the substrate that include the transceiver chip, baseband chip, and antennas module. The connections between RF signal and substrate are realized by the bumping GSG pads with 126-μm pitch. In order to save the chip area, the ground pads are reused with the nearby ports. As the results, the GSGSG pads are arranged on two corners of each side. The total 16 antenna ports are evenly distributed on the outer ring of the chip.

The pin definition and blocks placement are shown in Fig. 4.39. The arrangement of the I/O pads is shown as follows, 16 for antennas, 10 for digital, 2 for individual T/R ports of transceiver, 1 for RF VDD with digital VDD, 1 for analog VDD, 1 for external resistor of global bias circuit, and other 21 are ground pads; total 52 pads.

doi:10.6342/NTU201603106

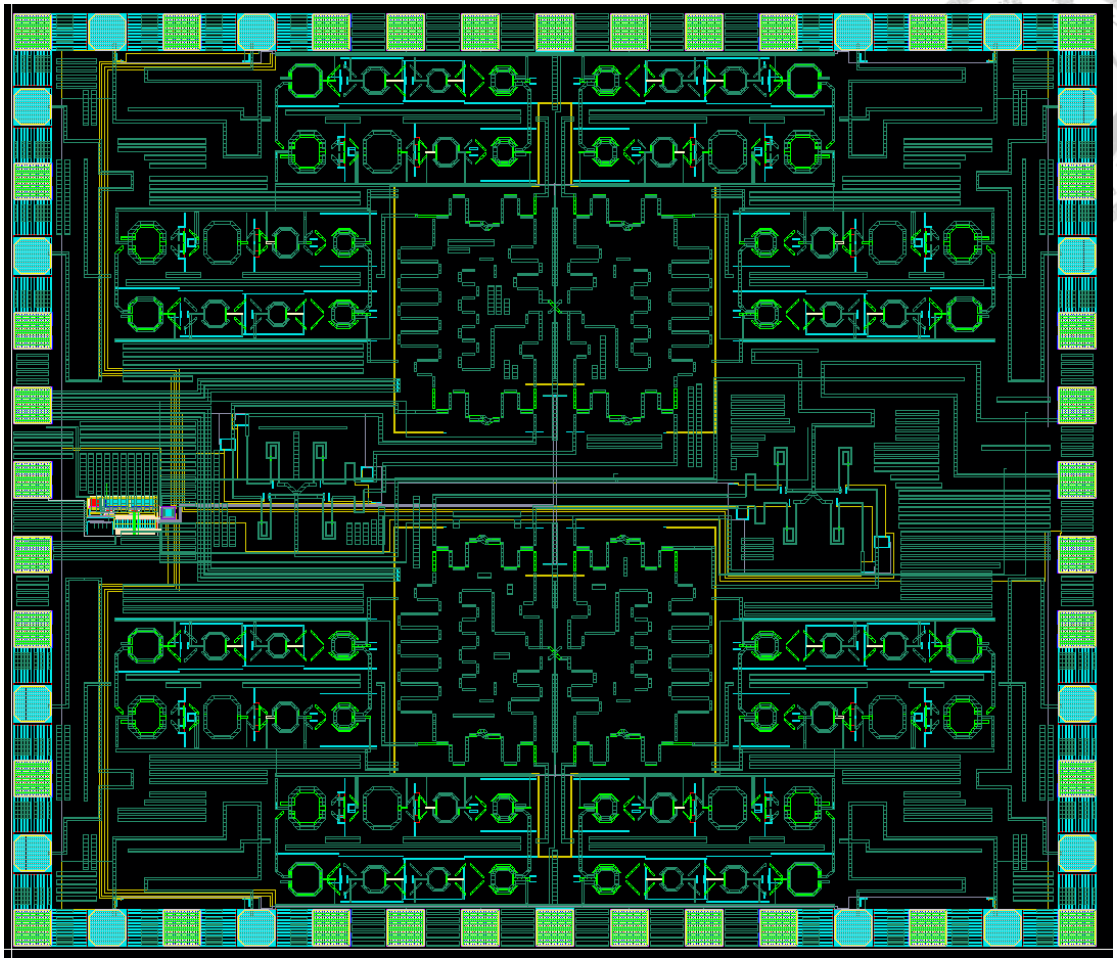

Fig. 4.38. Layout of the beamformer.

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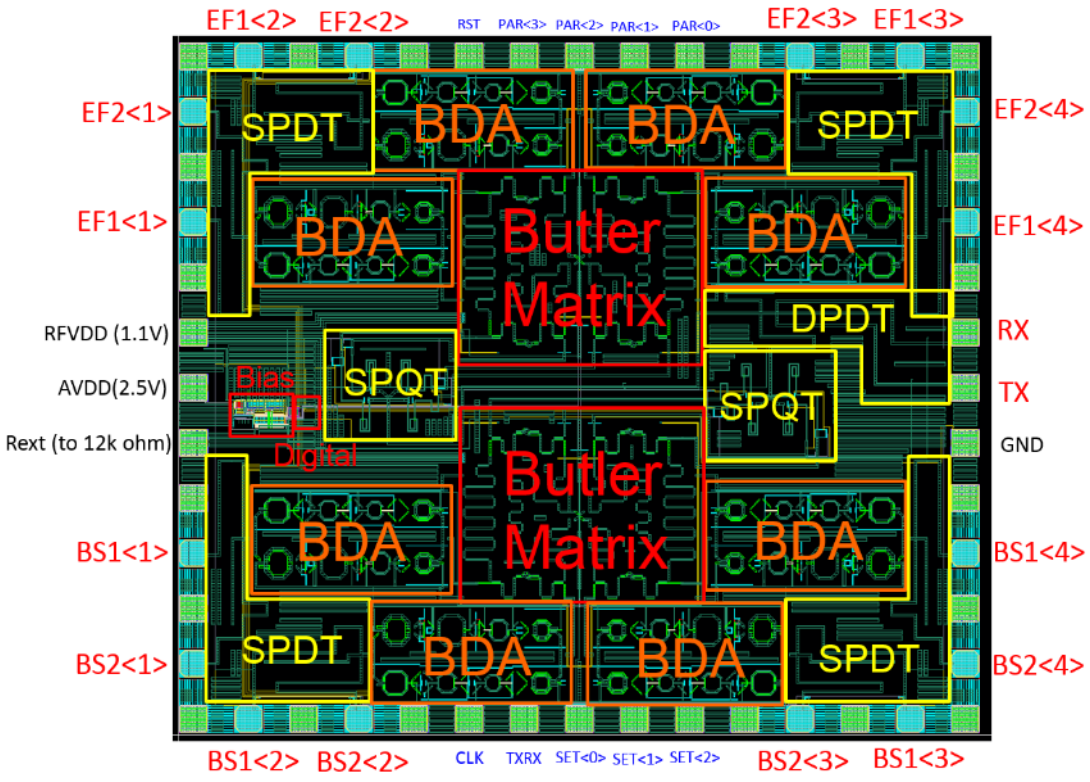

Fig. 4.39. Pad definition of the beamformer.

4.3.3 Control Plan

The beamforming system is controlled by 10 digital pins, the physical location of the pads are labeled in Fig. 4.39 (section 4.3.2). The functions and description of digital pins are list in Table 4.3. The power-down function is planned as SET[2:0] = 011. In this mode, all the PMOS switches in bias circuit will be turned to logic high, thus the switches turn off all the bias currents.

The Tx/Rx mode selection is controlled by TXRX, the system functions Rx while TXRX = 0, and functions Tx while TXRX = 1. The beam control function is defined while SET[2:0] = 001 or 010. In this condition, PAR[0] control the selection of the array group, PAR[1] control the array selection in each group, PAR[3:2] control the 4 beam states. The beam control table of endfire and broadside array as listed in Tables 4.4 and

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4.5, respectively.

Besides, the gain control function is defined while SET[2:0] = 101 or 110. In this condition, PAR[0] and PAR[1] control the switch of 25 μA and 50 μA reference current, respectively. By adding the 75 μA fixed reference current, the total reference current can be controlled from 75 to 150 μA in 25 μA steps. The gain and linearity of BDAs can be improved by adding the bias current, or system can remain in the power saving mode by minimal 75 μA bias current. The gain/power control table as listed in Table 4.6.

Table 4.3. Functions and description of the digital pins

Digital Pin	**Description**
RST	Reset of digital circuit (1 : no action, falling edge triggered)
CLK	Clock signal up to 110 MHz
TXRX	Tx/Rx Mode switching (0 : Rx, 1 : Tx)
SET[2:0]	Control Mode : 011 : power down 001=010 : beam control 101=110 : gain/power control Otherwise : no action
PAR[3:0]	Control parameters of each control mode

doi:10.6342/NTU201603106

Table 4.4. Phase control truth table of endfire array.

SET[2:0]= 001 or 010	State1	State2	State3	State4
PAR[3:0]	[0X00]	[0X10]	[0X01]	[0X11]
Bit[6:9] of BF Decoder	[1000]	[0010]	[0100]	[0001]
Excitation seq. in EF Ant.	[1000]	[0001]	[0100]	[0010]
EF<1>	-45º	-180º	-135º	-90º
EF<2>	-135º	-90º	-225º	0º
EF<3>	-90º	-135º	0º	-225º
EF<4>	-180º	-45º	-90º	-135º

Table 4.5. Phase control truth table of broadside array.

SET[2:0]= 001 or 010	State1	State2	State3	State4
PAR[3:0]	[1X00]	[1X10]	[1X01]	[1X11]
Bit[6:9] of BF Decoder	[1000]	[0010]	[0100]	[0001]
Excitation seq. in BS Ant.	[0100]	[0001]	[1000]	[0010]
BS<1>	-90º	-45º	-180º	-135º
BS<2>	0º	-135º	-90º	-225º
BS<3>	-225º	-90º	-135º	0º
BS<4>	-135º	-180º	-45º	-90º

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Table 4.6. Gain/power control truth table.

PAR[3:0]	[XX00]	[XX10]	[XX01]	[XX11]
Iref (mA)	150	125	100	75
Idc (mA) at Rx Mode	139	113	88	64
Mapping voltage for Rx (V)	1.08	1	0.93	0.85
Idc (mA) at Tx Mode	326	291	254	213
Mapping voltage for Tx (V)	0.71	0.68	0.65	0.62

doi:10.6342/NTU201603106

4.4 Simulated results

4.4.1 Introduction

Based on the BDA test circuit which is presented in chapter 3, the measured results show the frequency drift and gain drop since the operated frequency is 66 GHz, which is out of the frequency range confirmed by PDK model. Although the system is originally designed for the 802.11ad band which is from 57 to 66 GHz, we expect the frequency drift and gain drop will occur due to the system is on the same wafer with the BDA test circuit. For this reason, the revised model is used to generate the re-simulated results in the following sections. Besides, the bias condition of simulation is fixed to I_{ref} equal to 150 μA for the identical bias condition of measurement.

The RF circuits is designed with Agilent Advance Design System (ADS), and all the passive components are simulated by Sonnet EM solver. The following simulated results are presented by 4-ports of each antenna array in Rx/Tx mode and among the 4 beam-state control, respectively. For brief description, the endfire array1 is expressed as EF1, the broadside array1 is expressed as BS1, and so on EF2 and BS2.

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4.4.2 Beam control simulation at Rx mode

This section presents the Rx mode simulation. Figs. 4.40 to 4.47 show the frequency response of gain and phase error of EF1 array among the 4 beam states. Figs. 4.48 to 4.55 show the frequency response of gain and phase error of EF2 array among the 4 beam states. Figs. 4.56 to 4.63 show the frequency response of gain and phase error of BS1 array among the 4 beam states. Figs. 4.64 to 4.71 show the frequency response of gain and phase error of BS2 array among the 4 beam states.

The simulated results of phase error are referenced from the beam control plan (section 4.3.3), and presented as the relative phase to port1 in each array. The simulated results show the phase errors at 60 GHz all are smaller than 30º, and most of them are smaller than 15º. Note that the phase error is independent of relative port, which is defined as the maximum offset phase between the 4 ports with the ideal response. In the following results of phase error, port1 is chosen for the sequence phase.

doi:10.6342/NTU201603106

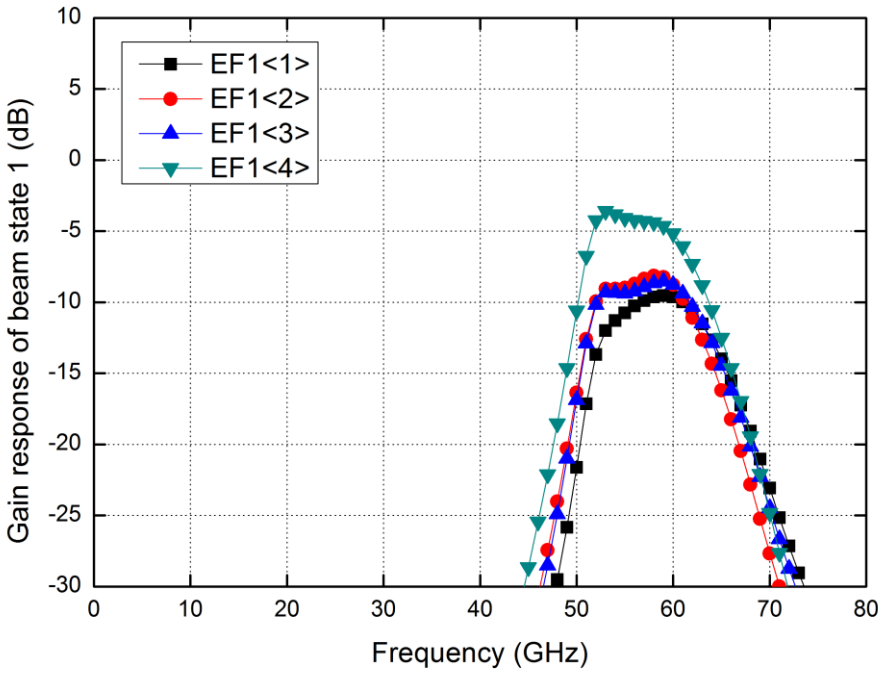

Fig. 4.40. Frequency response of gain of EF1 array at beam state1 at Rx mode.

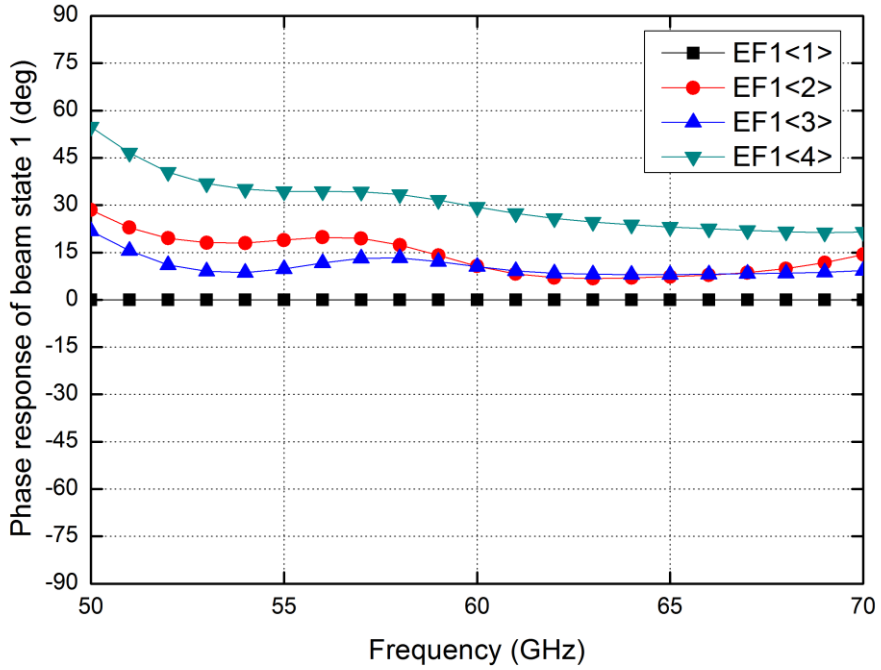

Fig. 4.41. Phase error of EF1 array at beam state1 at Rx mode.

doi:10.6342/NTU201603106

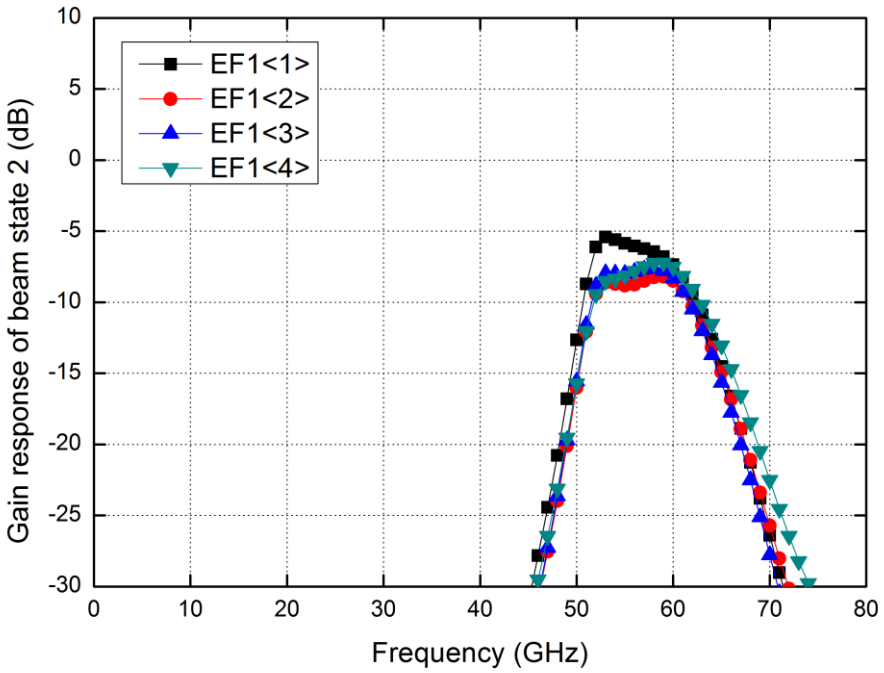

Fig. 4.42. Frequency response of gain of EF1 array at beam state2 at Rx mode.

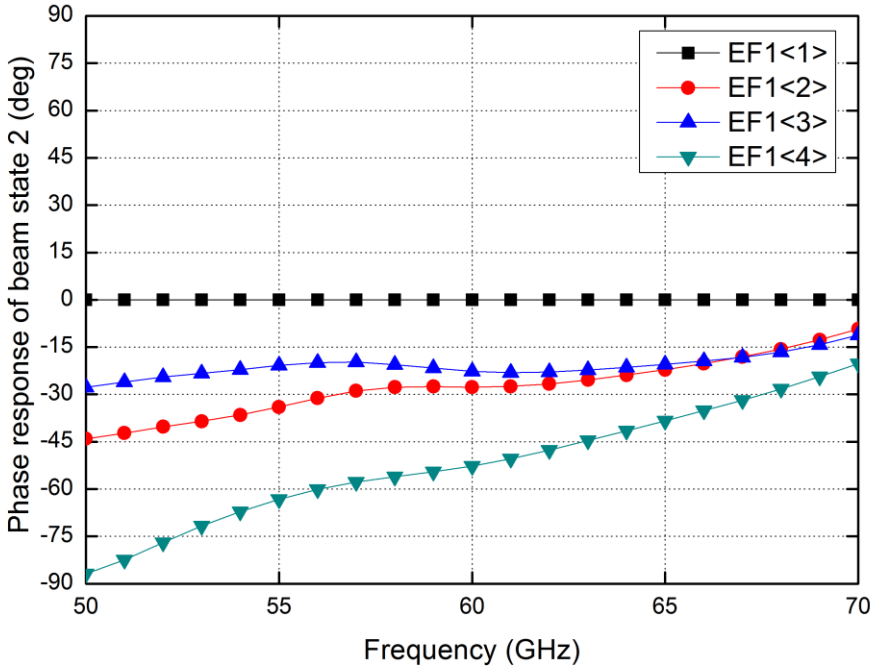

Fig. 4.43. Phase error of EF1 array at beam state2 at Rx mode.

doi:10.6342/NTU201603106

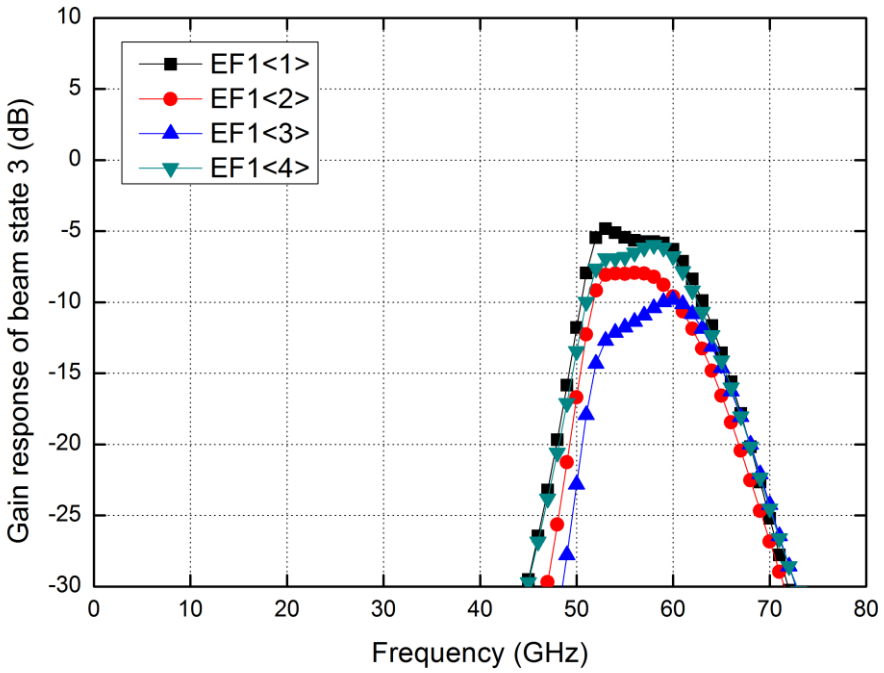

Fig. 4.44. Frequency response of gain of EF1 array at beam state3 at Rx mode.

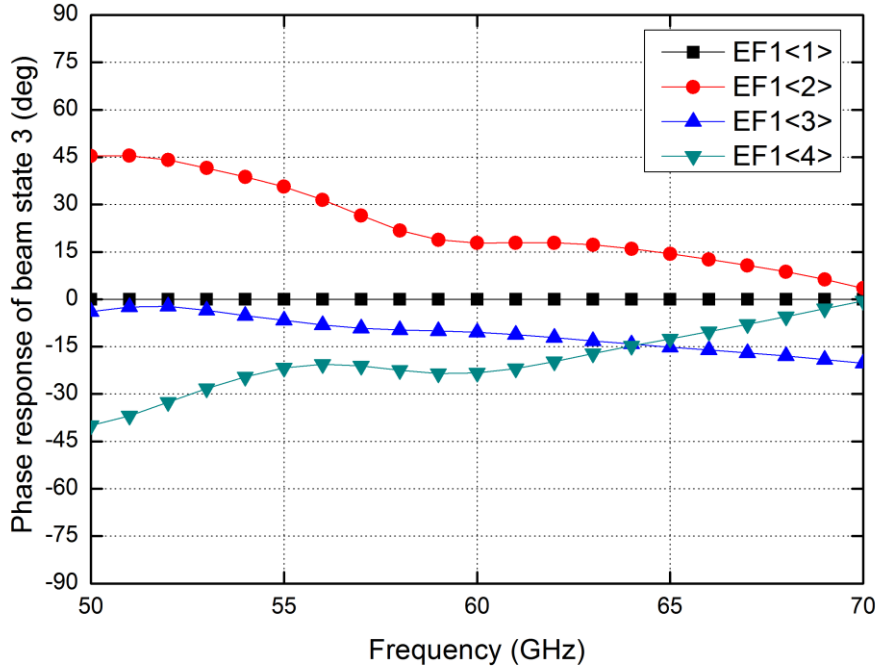

Fig. 4.45. Phase error of EF1 array at beam state3 at Rx mode.

doi:10.6342/NTU201603106

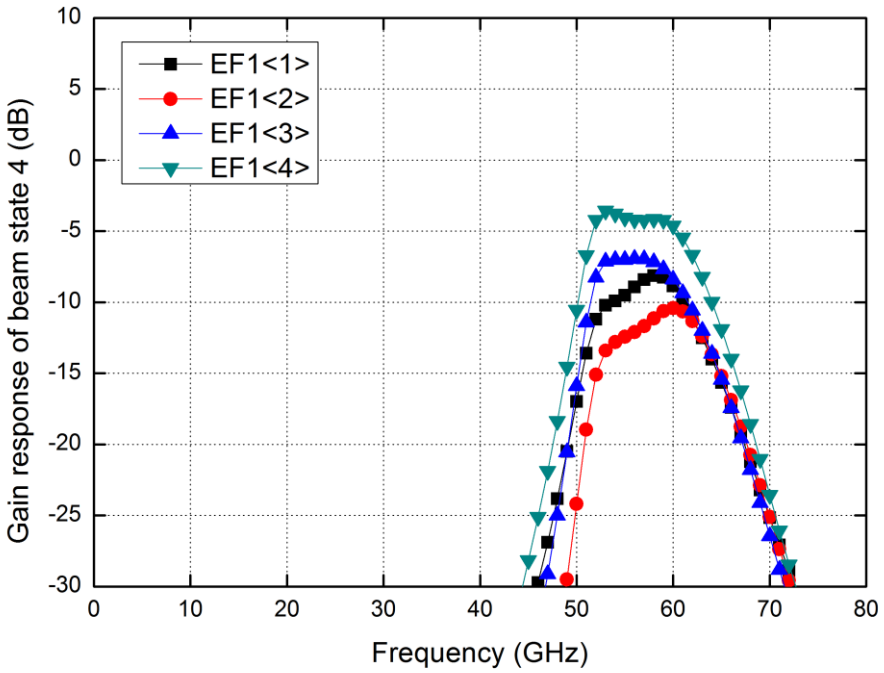

Fig. 4.46. Frequency response of gain of EF1 array at beam state4 at Rx mode.

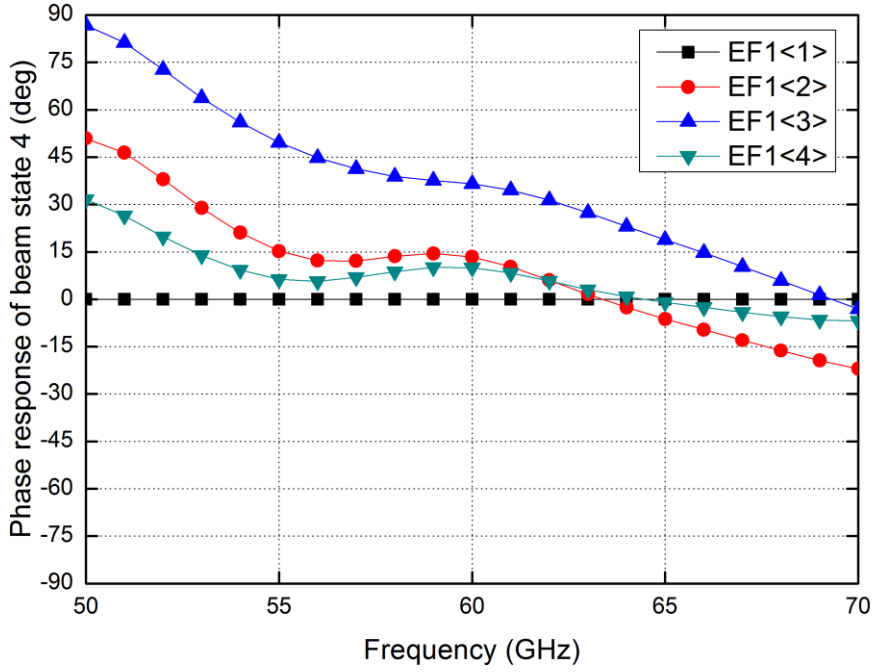

Fig. 4.47. Phase error of EF1 array at beam state4 at Rx mode.

doi:10.6342/NTU201603106

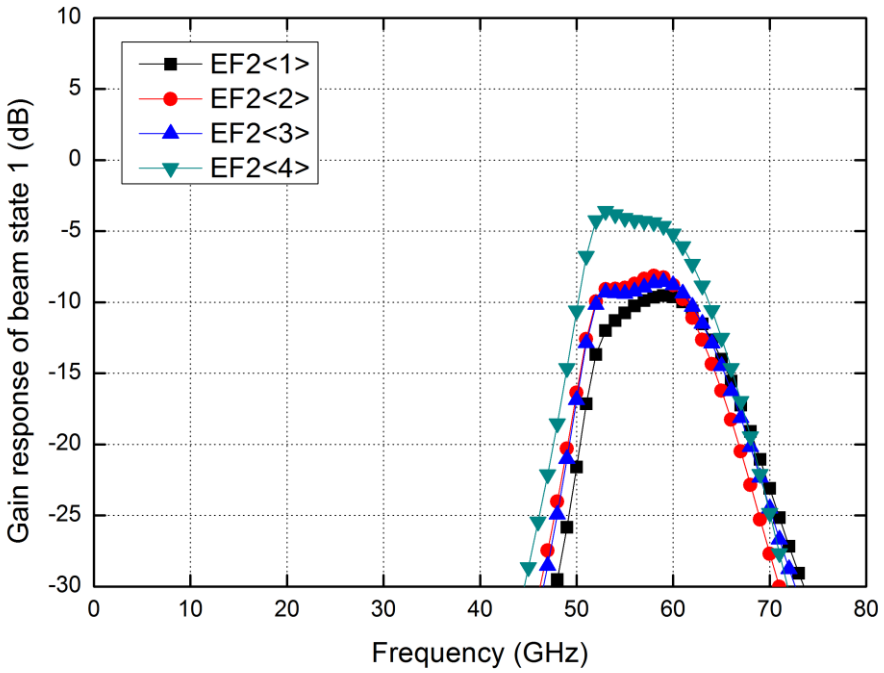

Fig. 4.48. Frequency response of gain of EF2 array at beam state1 at Rx mode.

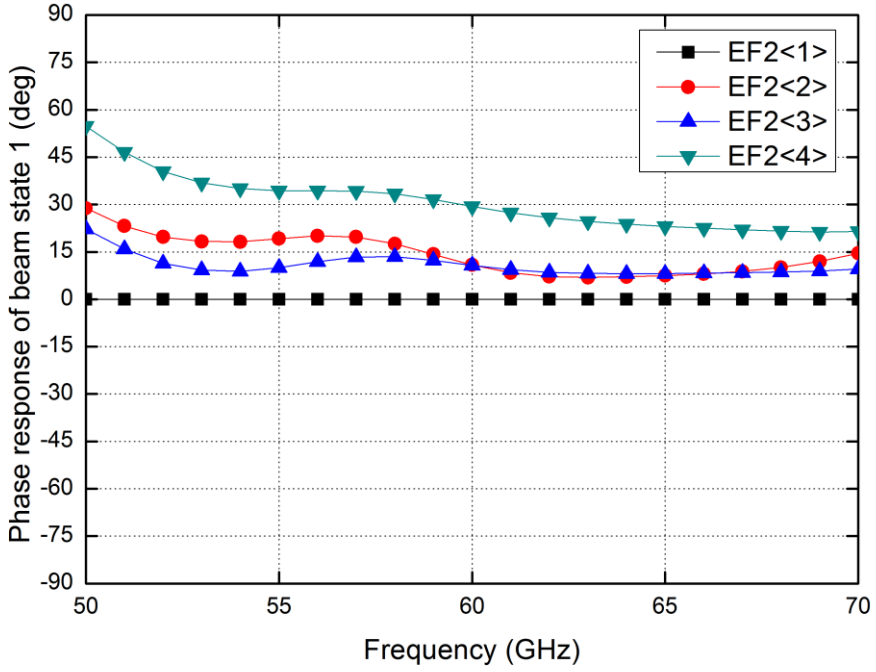

Fig. 4.49. Phase error of EF2 array at beam state1 at Rx mode.

doi:10.6342/NTU201603106

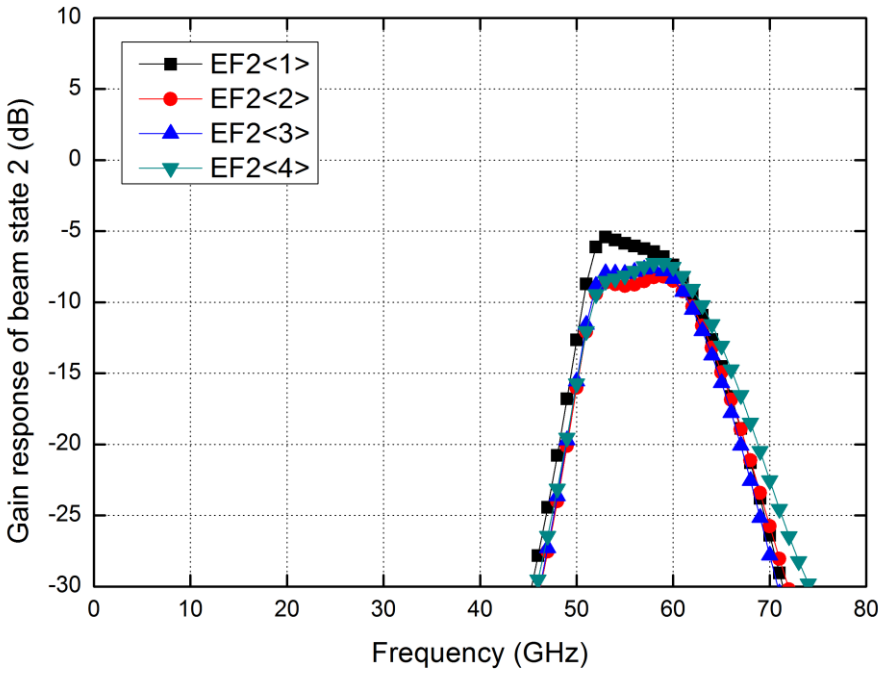

Fig. 4.50. Frequency response of gain of EF2 array at beam state2 at Rx mode.

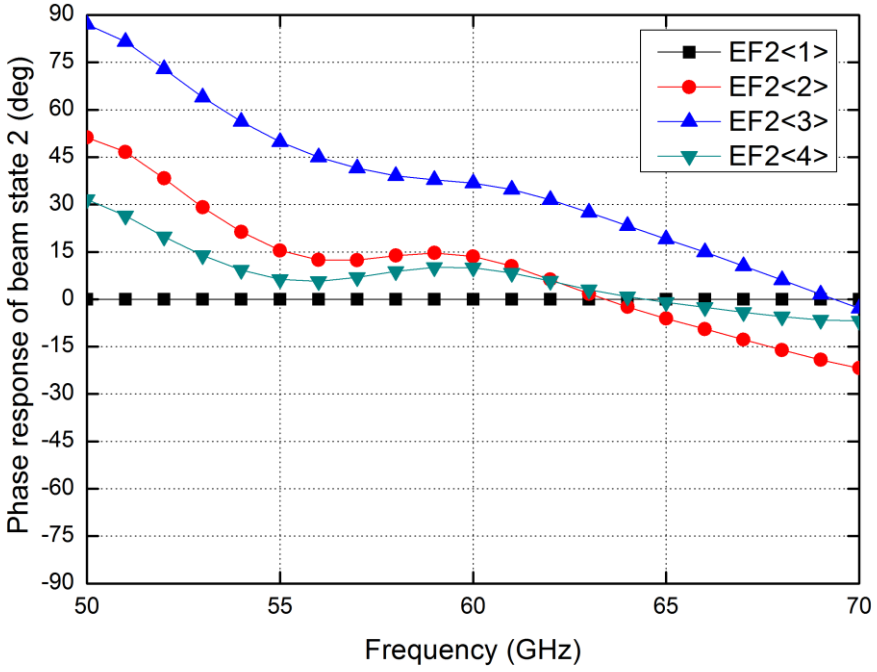

Fig. 4.51. Phase error of EF2 array at beam state2 at Rx mode.

doi:10.6342/NTU201603106

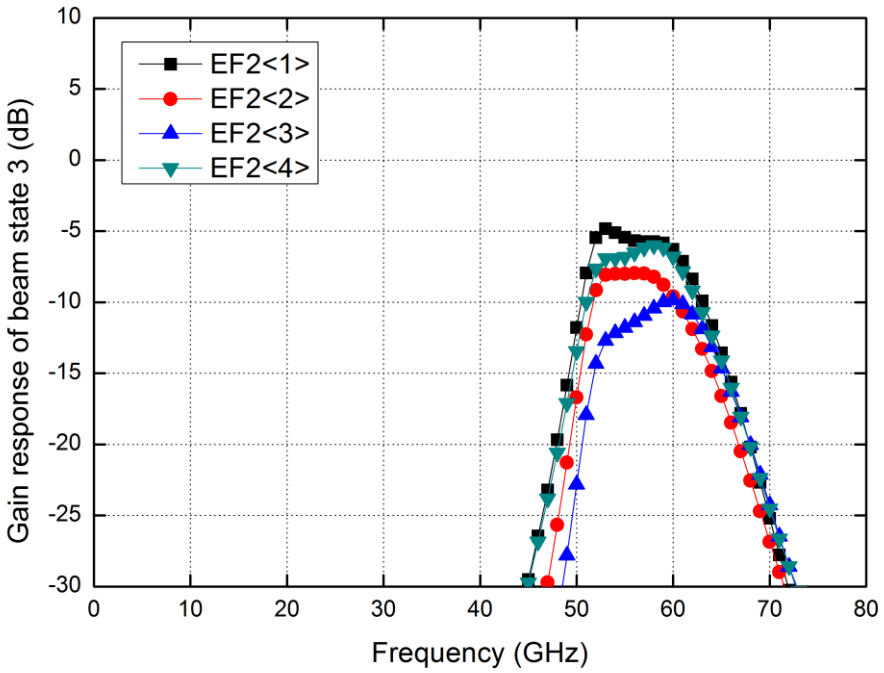

Fig. 4.52. Frequency response of gain of EF2 array at beam state3 at Rx mode.

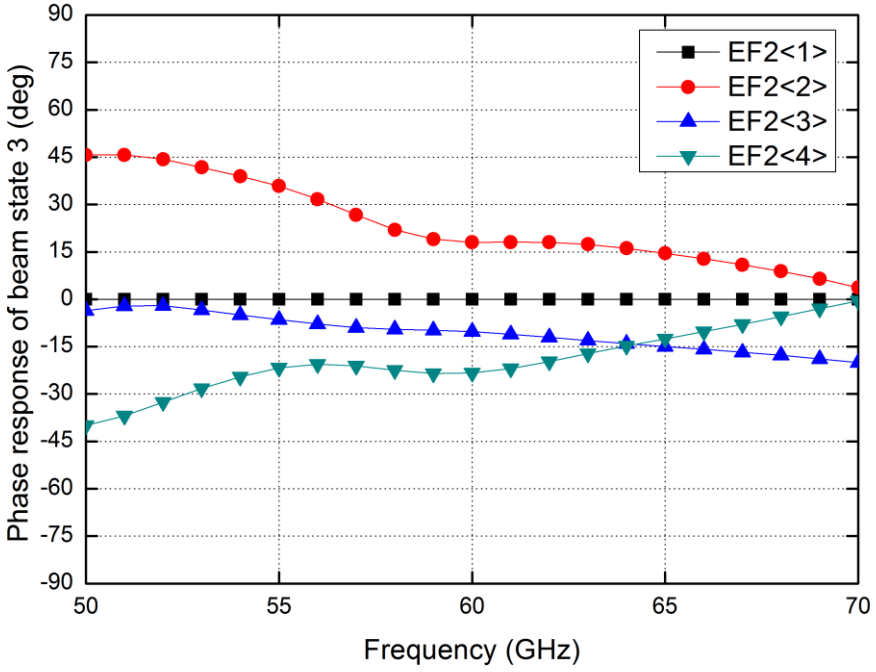

Fig. 4.53. Phase error of EF2 array at beam state3 at Rx mode.

doi:10.6342/NTU201603106

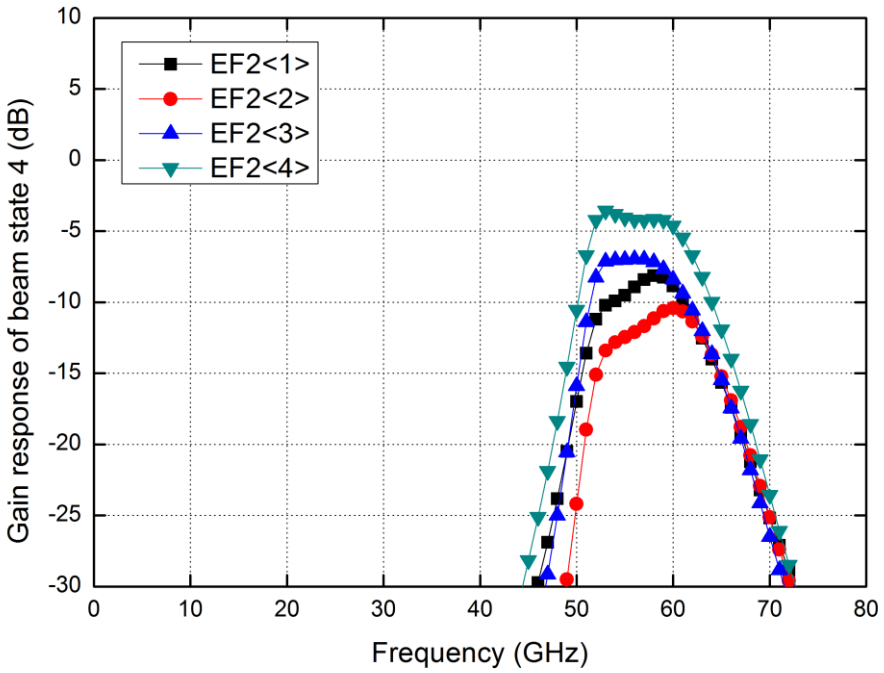

Fig. 4.54. Frequency response of gain of EF2 array at beam state4 at Rx mode.

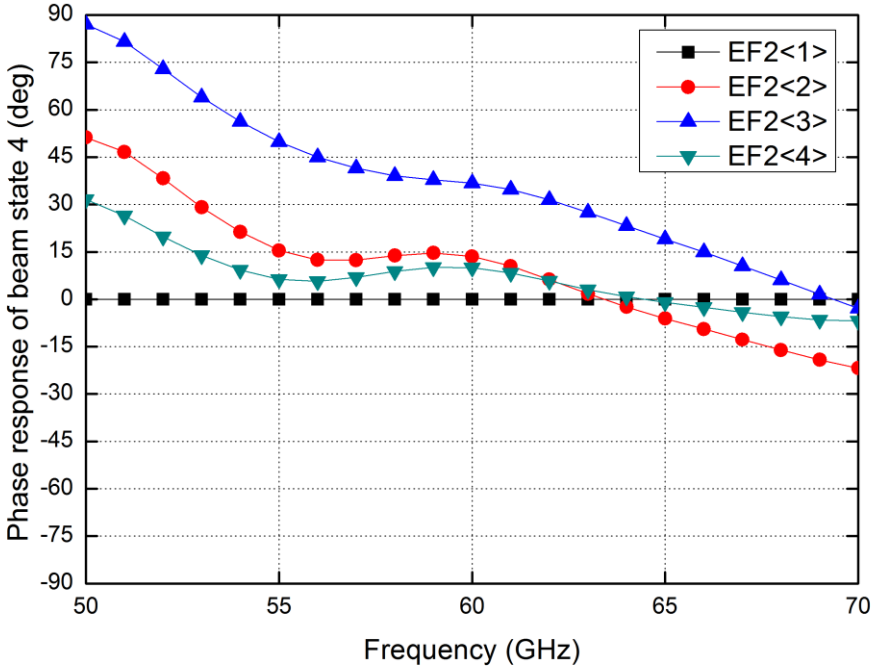

Fig. 4.55. Phase error of EF2 array at beam state4 at Rx mode.

doi:10.6342/NTU201603106

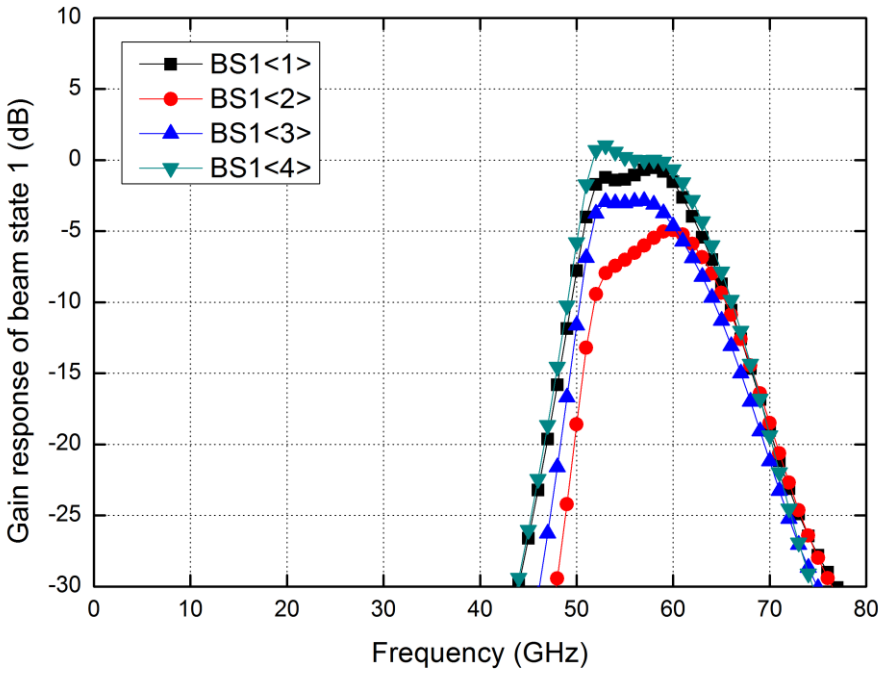

Fig. 4.56. Frequency response of gain of BS1 array at beam state1 at Rx mode.

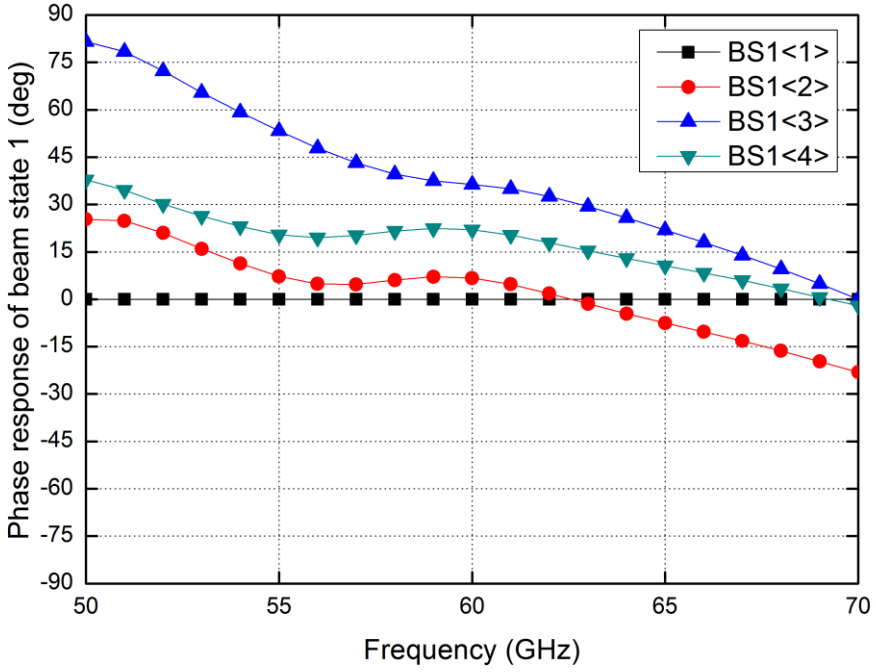

Fig. 4.57. Phase error of BS1 array at beam state1 at Rx mode.

doi:10.6342/NTU201603106

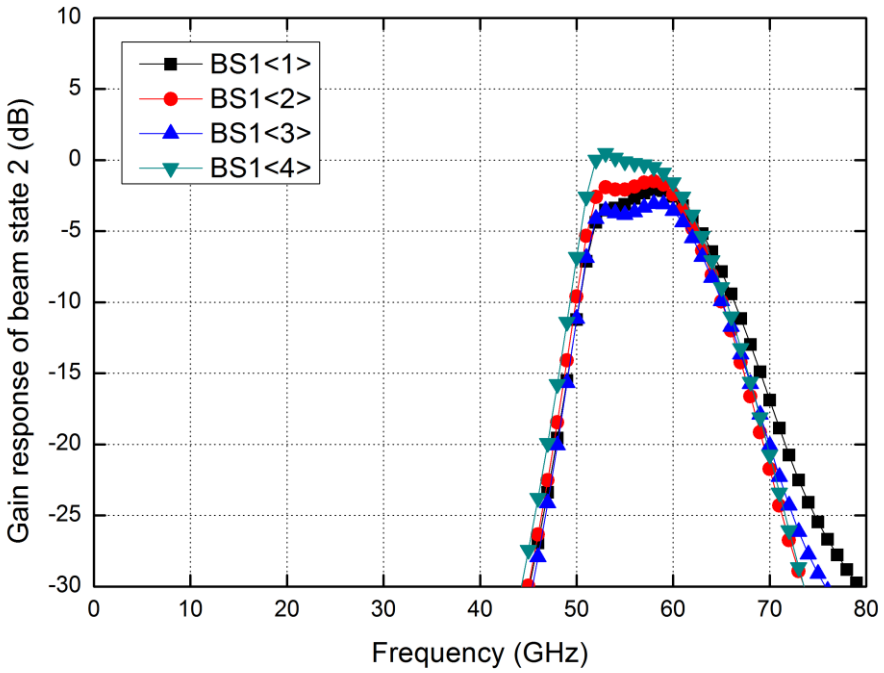

Fig. 4.58. Frequency response of gain of BS1 array at beam state2 at Rx mode.

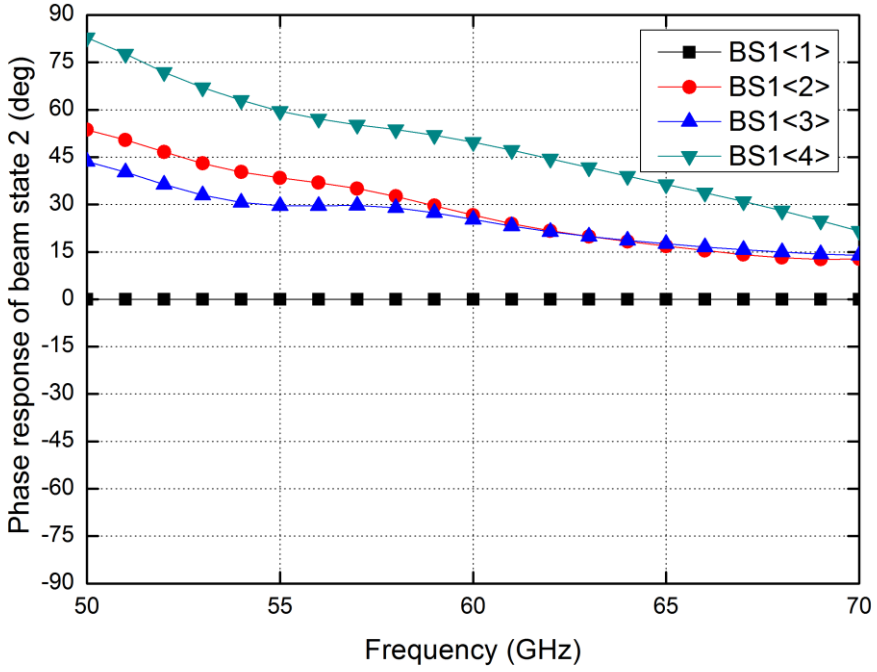

Fig. 4.59. Phase error of BS1 array at beam state2 at Rx mode.

doi:10.6342/NTU201603106

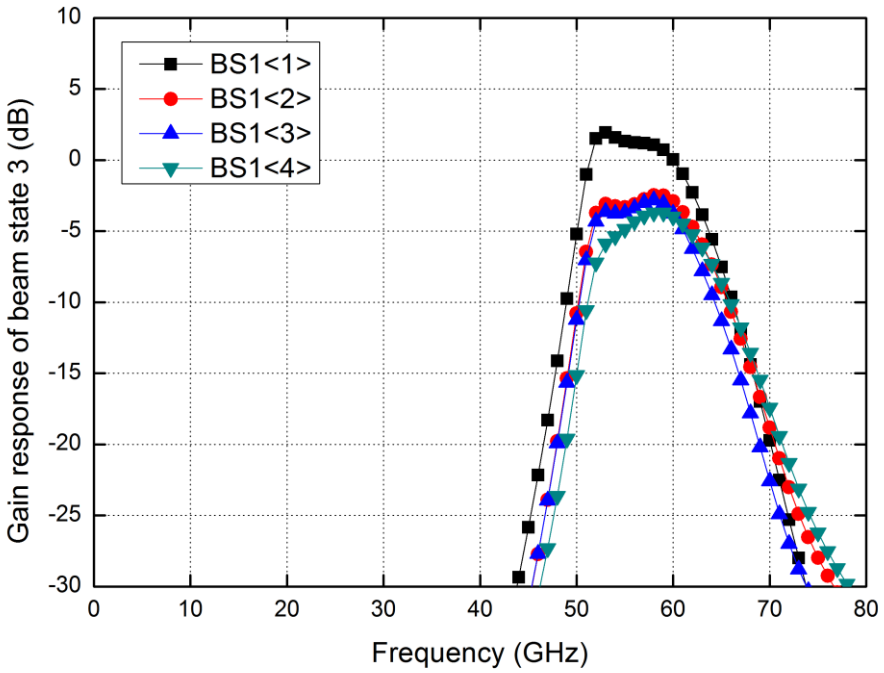

Fig. 4.60. Frequency response of gain of BS1 array at beam state3 at Rx mode.

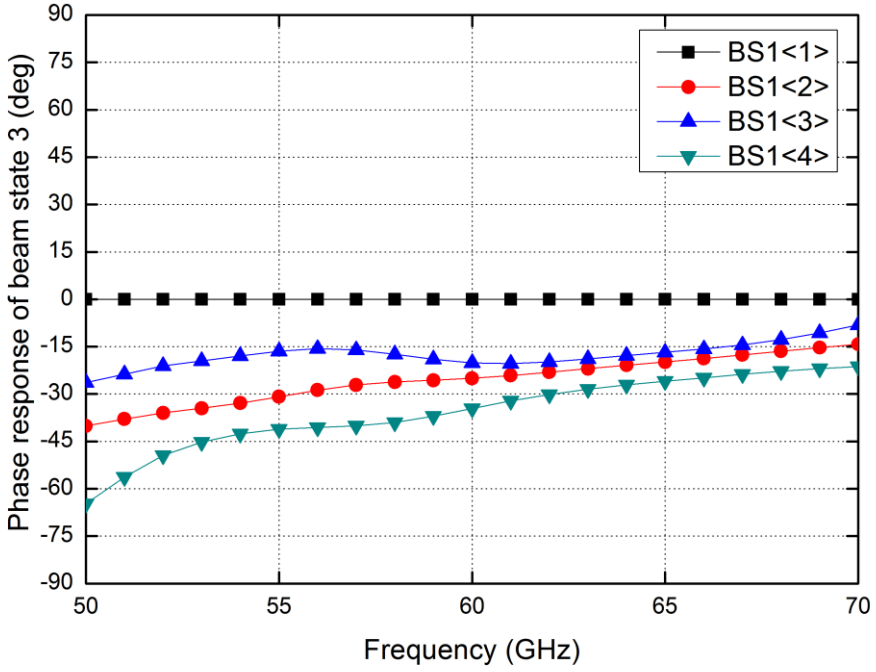

Fig. 4.61. Phase error of BS1 array at beam state3 at Rx mode.

doi:10.6342/NTU201603106

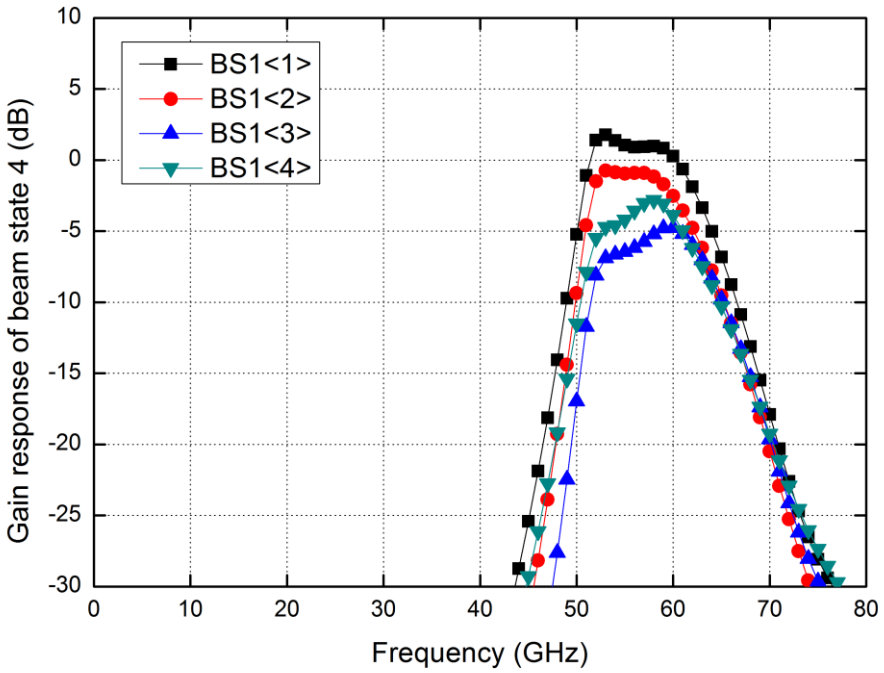

Fig. 4.62. Frequency response of gain of BS1 array at beam state4 at Rx mode.

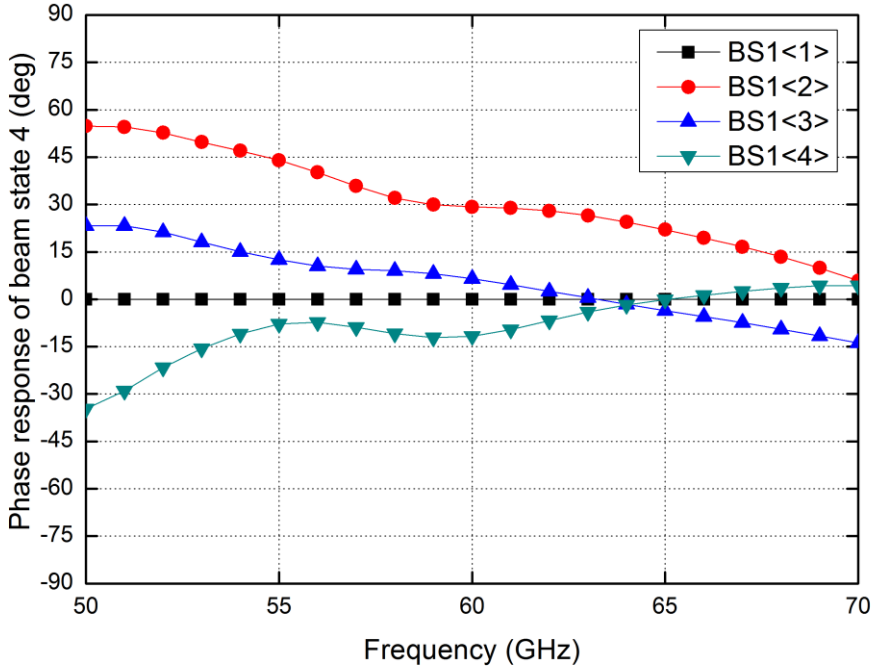

Fig. 4.63. Phase error of BS1 array at beam state4 at Rx mode.

doi:10.6342/NTU201603106

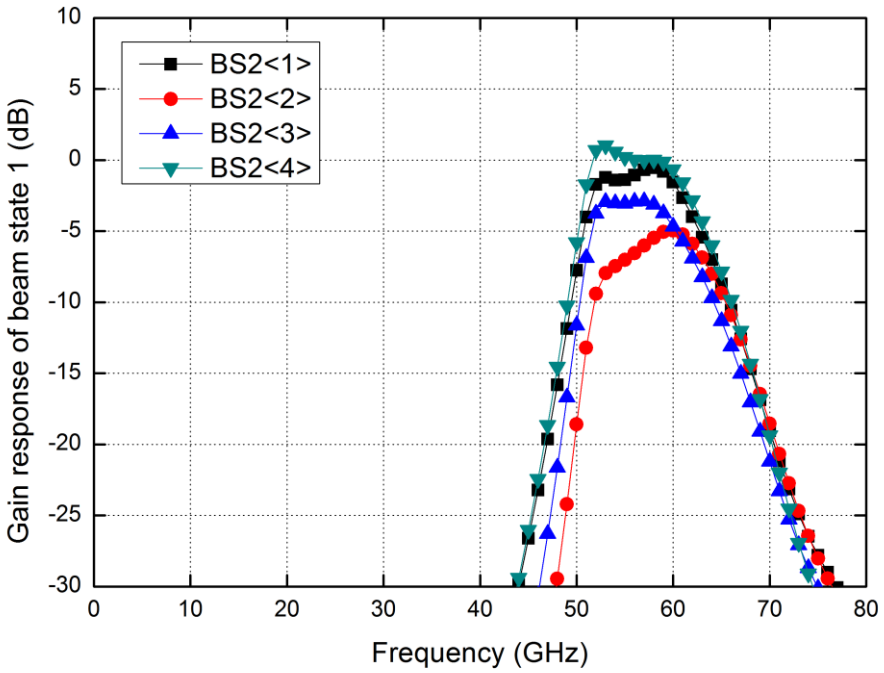

Fig. 4.64. Frequency response of gain of BS2 array at beam state1 at Rx mode.

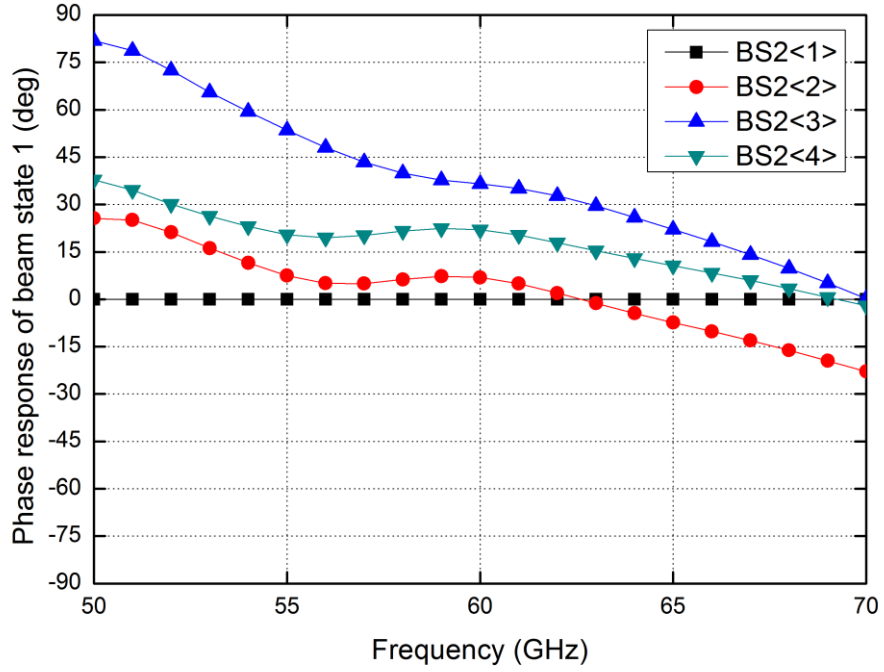

Fig. 4.65. Phase error of BS2 array at beam state1 at Rx mode.

doi:10.6342/NTU201603106

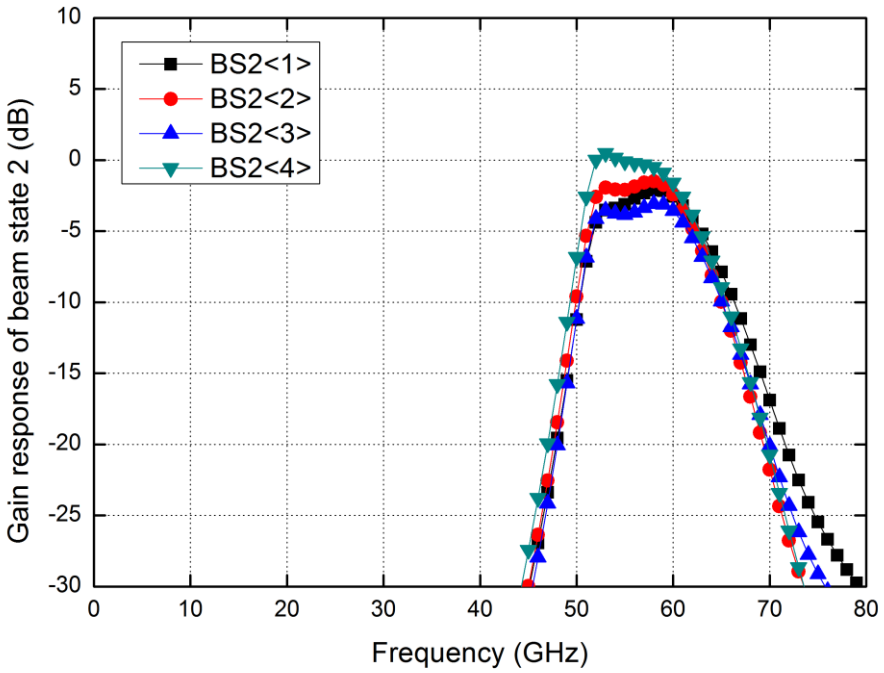

Fig. 4.66. Frequency response of gain of BS2 array at beam state2 at Rx mode.

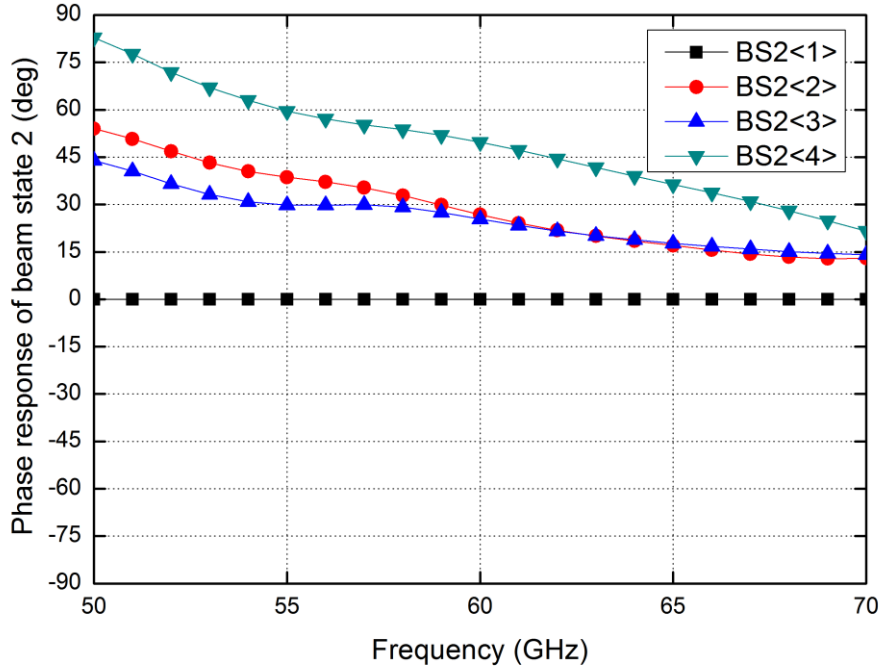

Fig. 4.67. Phase error of BS2 array at beam state2 at Rx mode.

doi:10.6342/NTU201603106

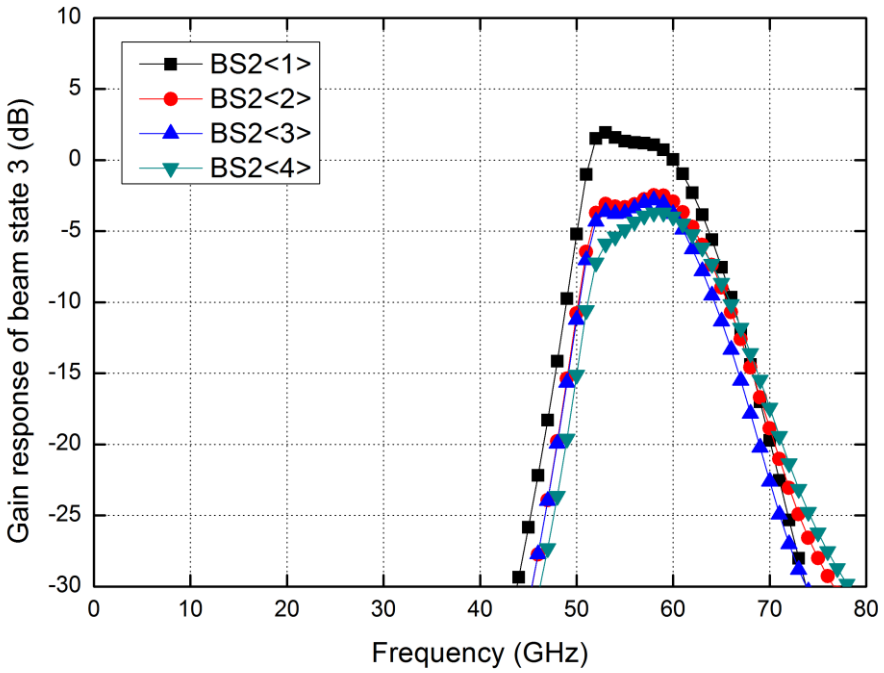

Fig. 4.68. Frequency response of gain of BS2 array at beam state3 at Rx mode.

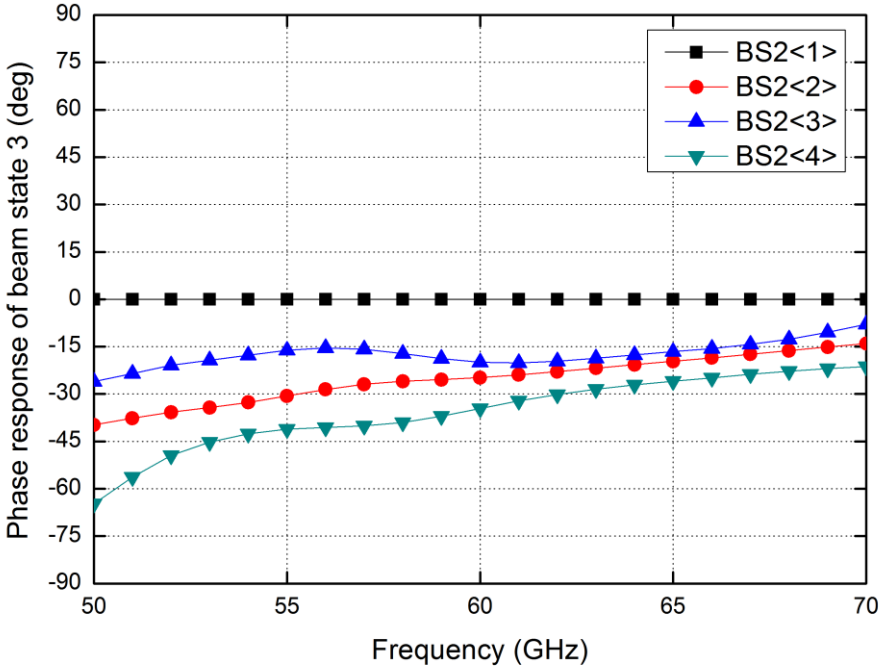

Fig. 4.69. Phase error of BS2 array at beam state3 at Rx mode.

doi:10.6342/NTU201603106

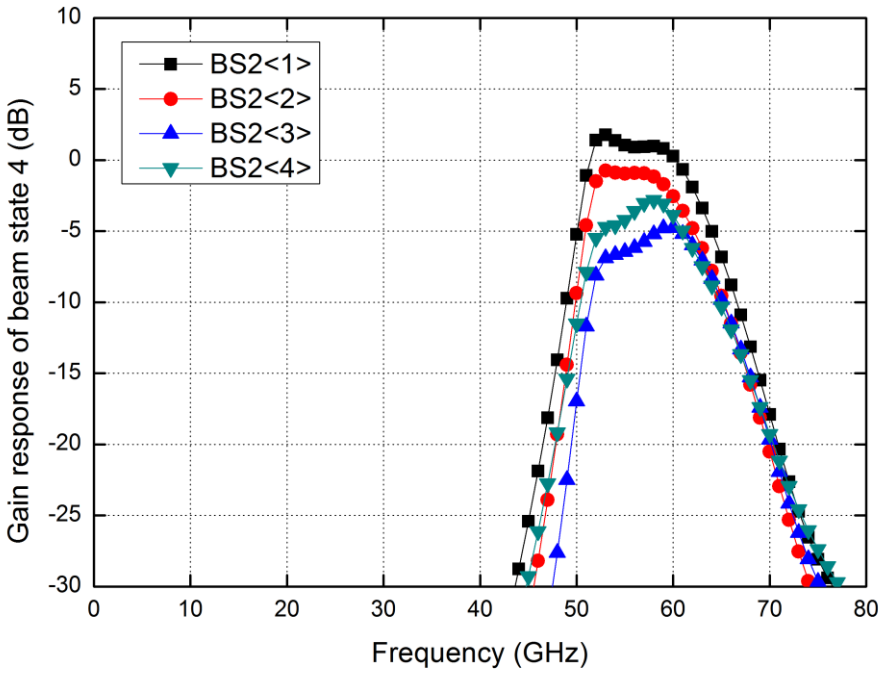

Fig. 4.70. Frequency response of gain of BS2 array at beam state4 at Rx mode.

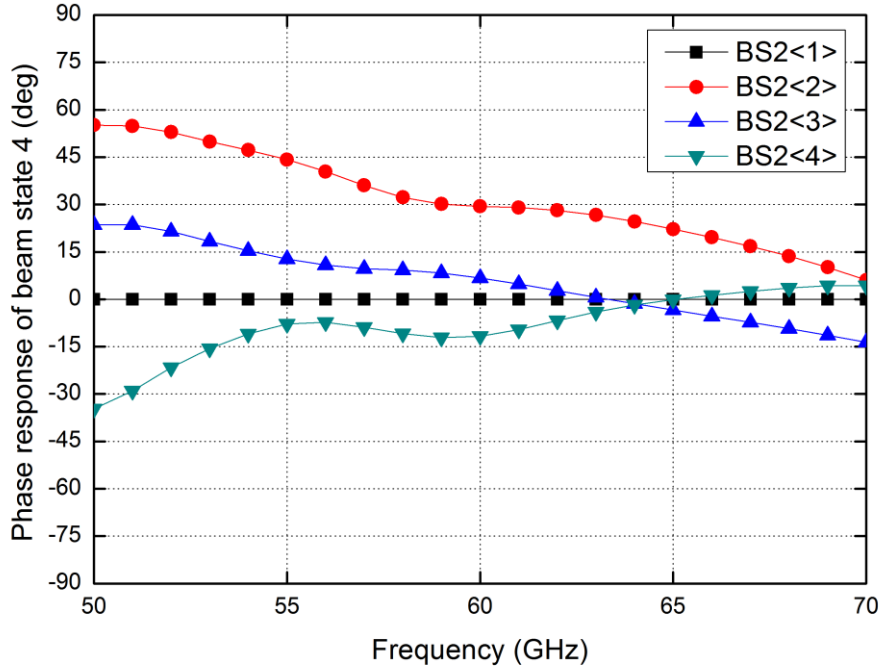

Fig. 4.71. Phase error of BS2 array at beam state4 at Rx mode.

doi:10.6342/NTU201603106

4.4.3 Beam control simulation at Tx mode

This section presents the Tx mode simulation. Figs. 4.72 to 4.79 show the frequency response of gain and phase error of EF1 array among the 4 beam states. Figs. 4.80 to 4.87 show the frequency response of gain and phase error of EF2 array among the 4 beam states. Figs. 4.88 to 4.95 show the frequency response of gain and phase error of BS1 array among the 4 beam states. Figs. 4.96 to 4.103 show the frequency response of gain and phase error of BS2 array among the 4 beam states.

The responses of the relative phase is the same as in Rx mode due to the system is bidirectional and symmetric. The simulated results show the phase errors at 60 GHz all are smaller than 30º, and most of them are smaller than 15º.

doi:10.6342/NTU201603106

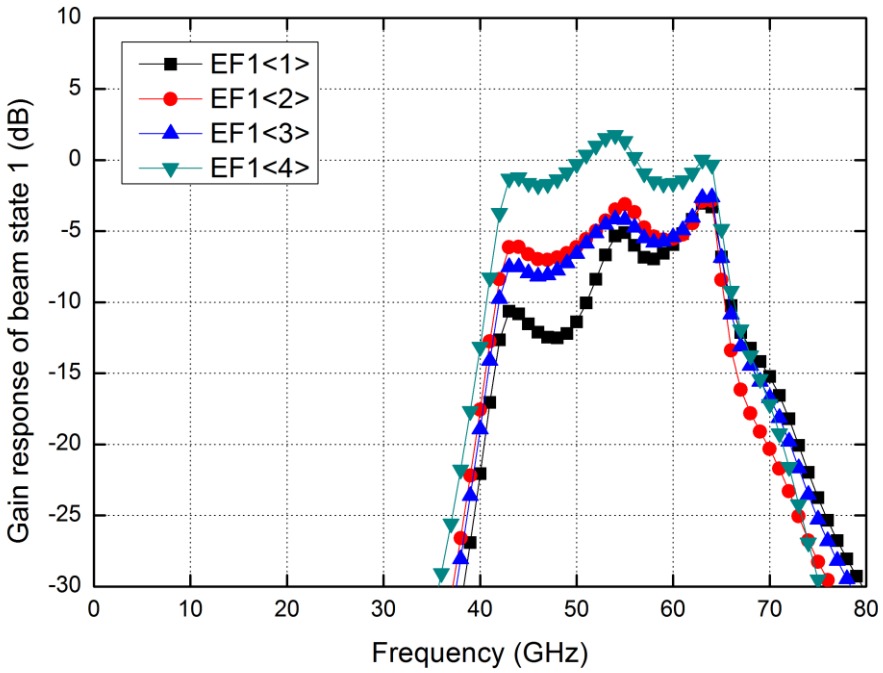

Fig. 4.72. Frequency response of gain of EF1 array at beam state1 at Tx mode.

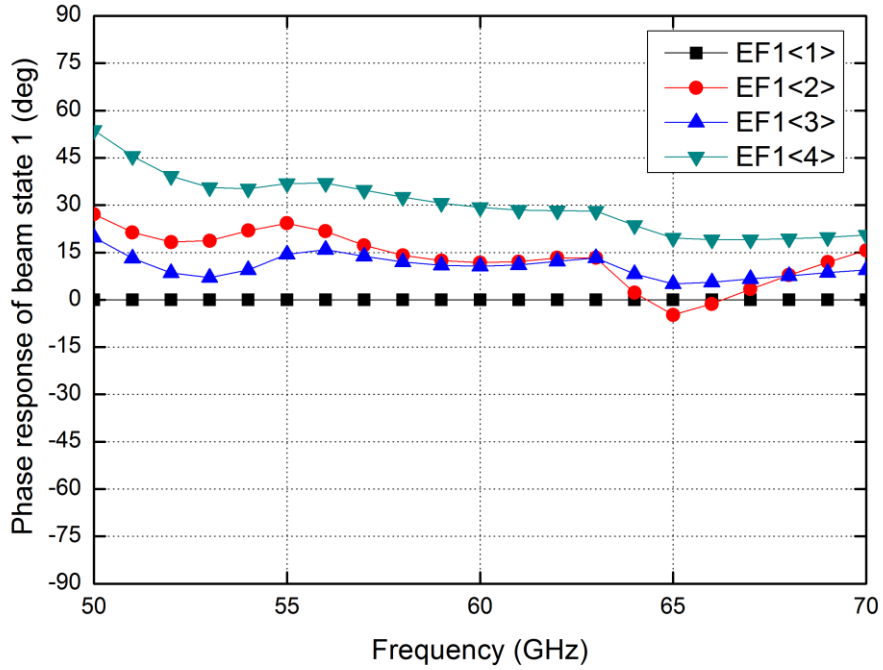

Fig. 4.73. Phase error of EF1 array at beam state1 at Tx mode.

doi:10.6342/NTU201603106

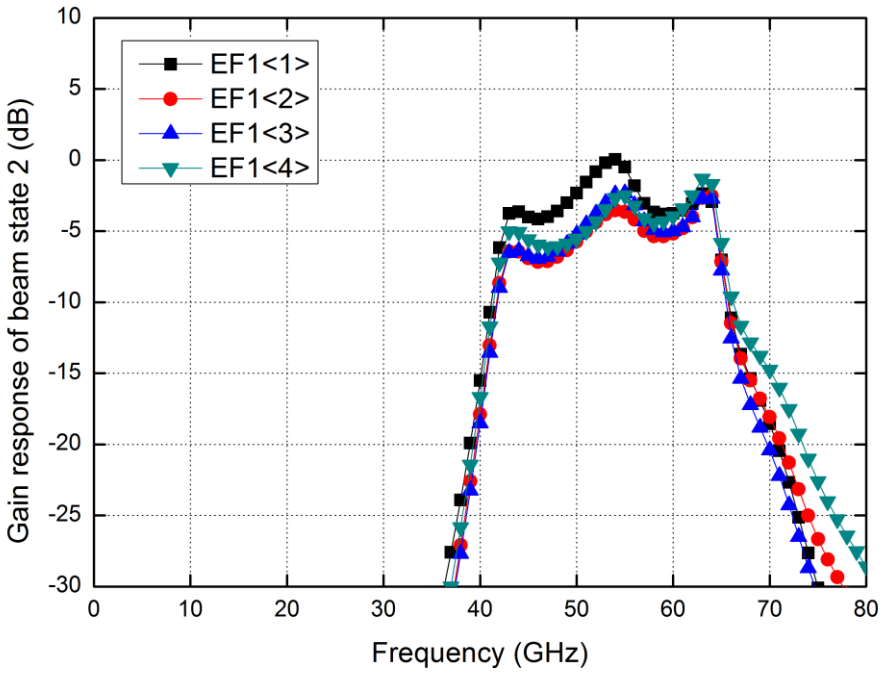

Fig. 4.74. Frequency response of gain of EF1 array at beam state2 at Tx mode.

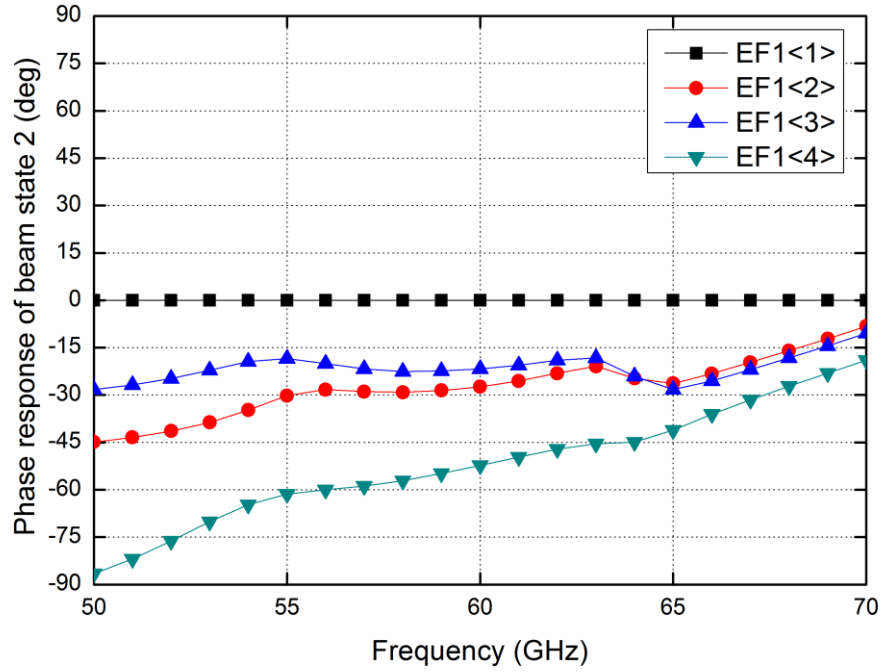

Fig. 4.75. Phase error of EF1 array at beam state2 at Tx mode.

doi:10.6342/NTU201603106

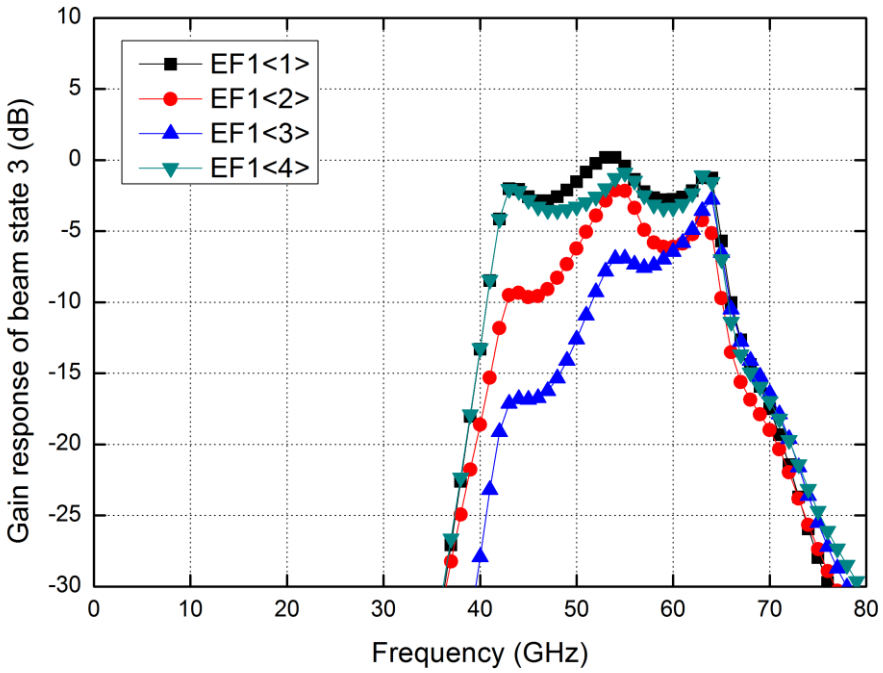

Fig. 4.76. Frequency response of gain of EF1 array at beam state3 at Tx mode.

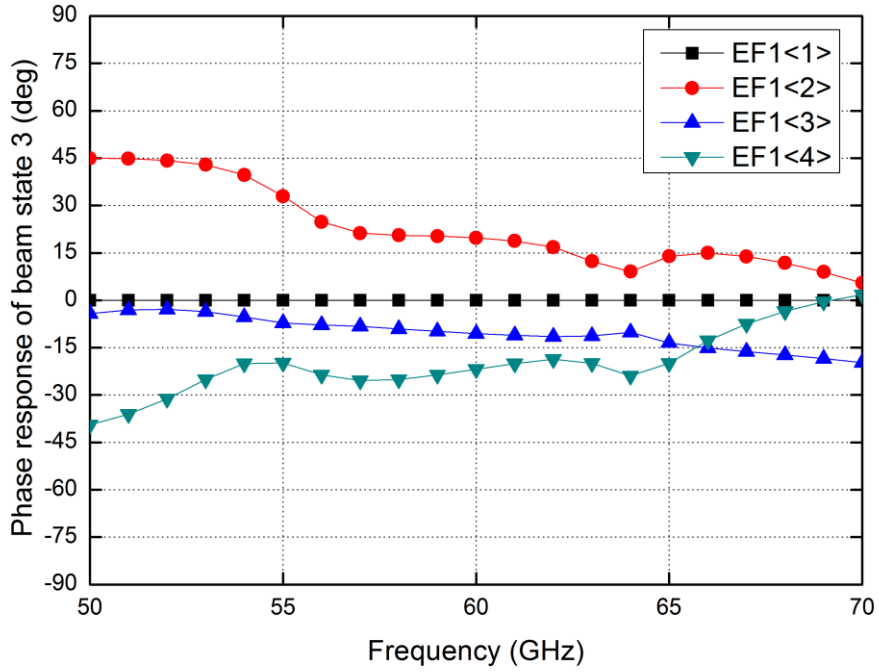

Fig. 4.77. Phase error of EF1 array at beam state3 at Tx mode.

doi:10.6342/NTU201603106

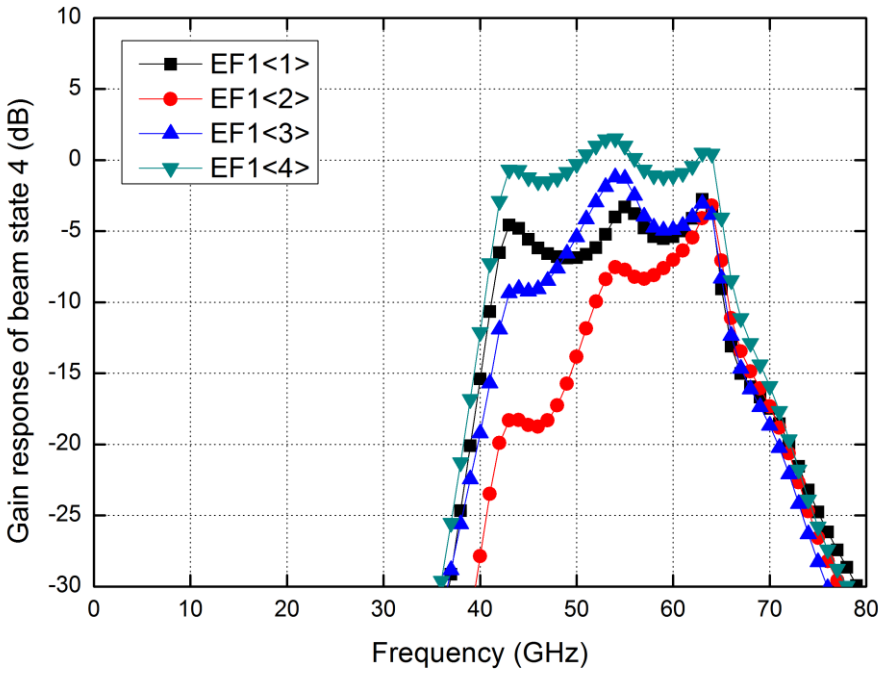

Fig. 4.78. Frequency response of gain of EF1 array at beam state4 at Tx mode.

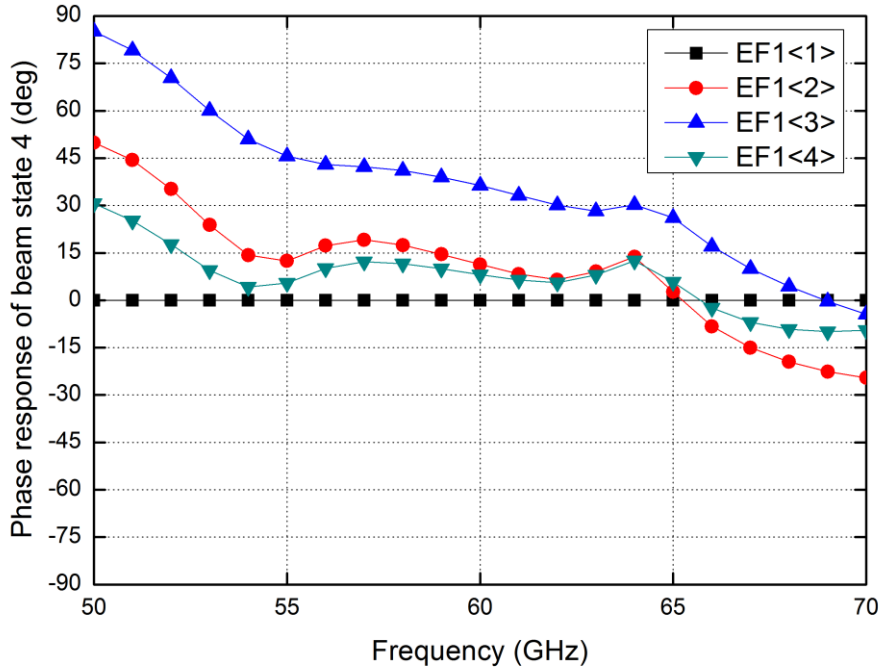

Fig. 4.79. Phase error of EF1 array at beam state4 at Tx mode.

doi:10.6342/NTU201603106

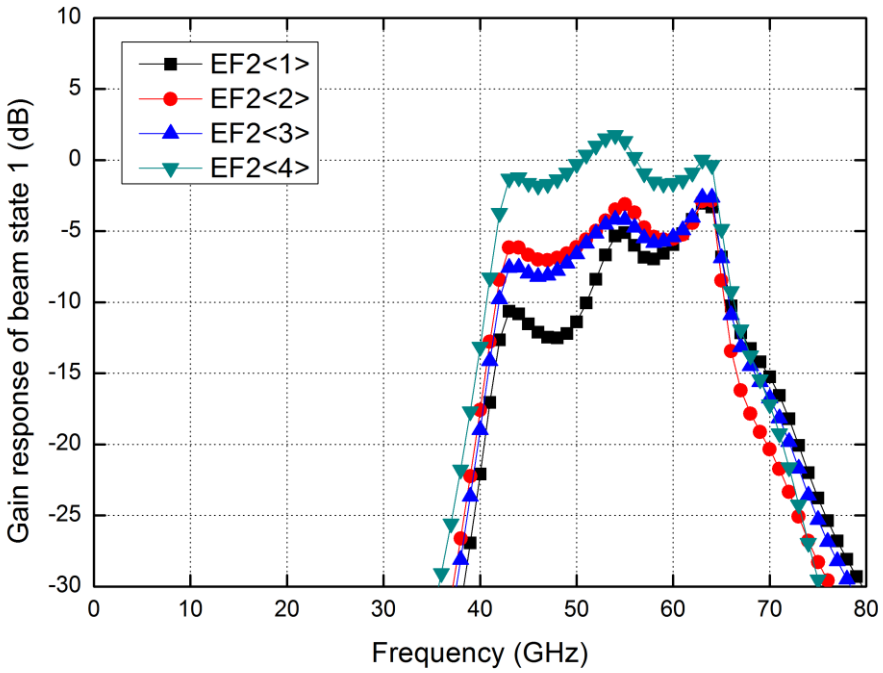

Fig. 4.80. Frequency response of gain of EF2 array at beam state1 at Tx mode.

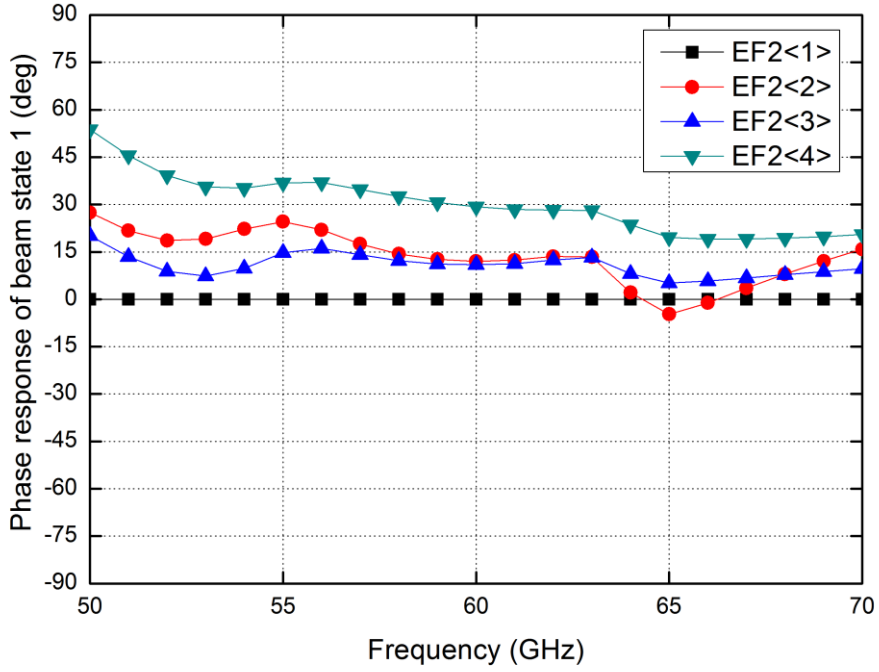

Fig. 4.81. Phase error of EF2 array at beam state1 at Tx mode.

doi:10.6342/NTU201603106

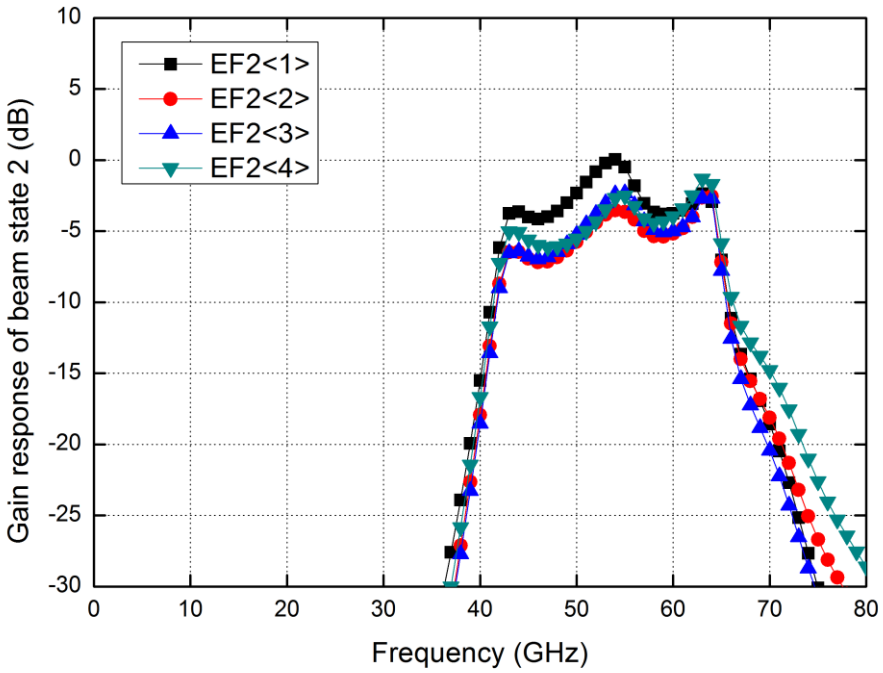

Fig. 4.82. Frequency response of gain of EF2 array at beam state2 at Tx mode.

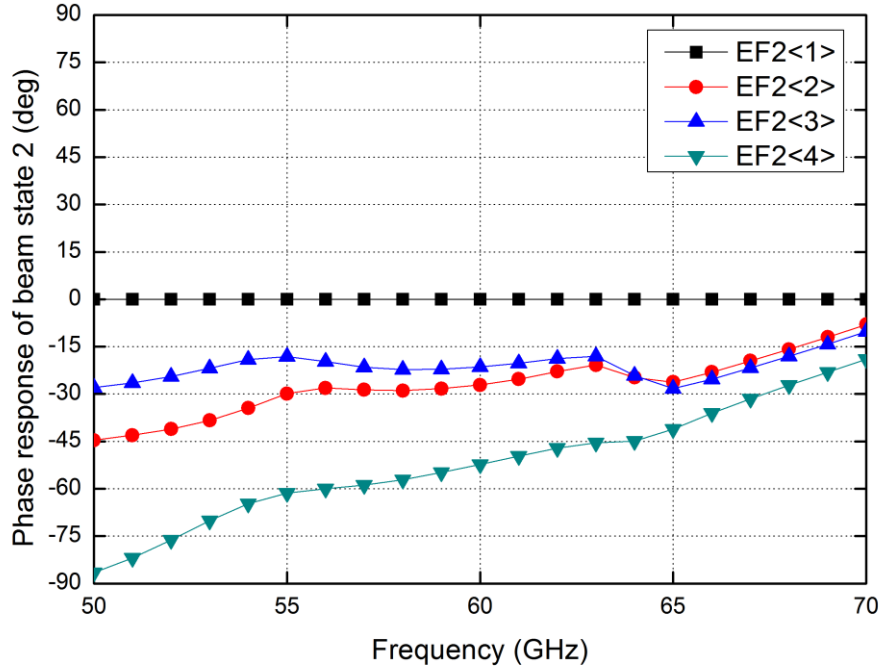

Fig. 4.83. Phase error of EF2 array at beam state2 at Tx mode.

doi:10.6342/NTU201603106

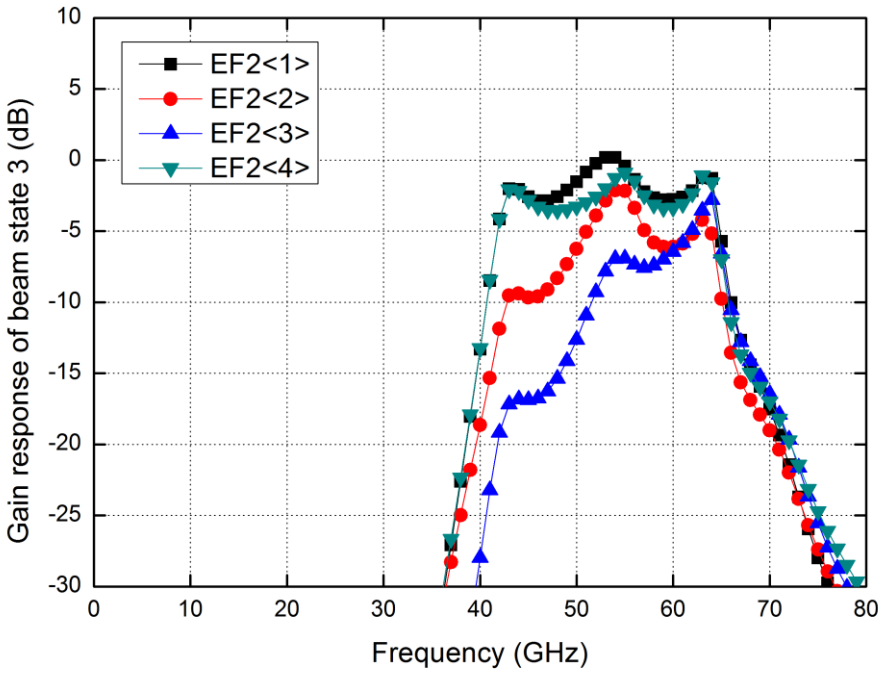

Fig. 4.84. Frequency response of gain of EF2 array at beam state3 at Tx mode.

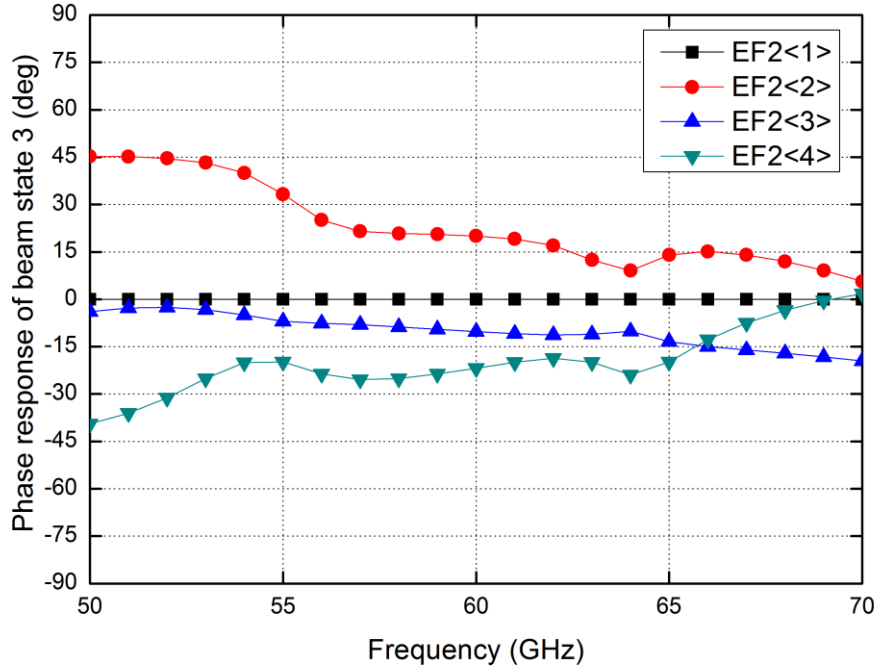

Fig. 4.85. Phase error of EF2 array at beam state3 at Tx mode.

doi:10.6342/NTU201603106

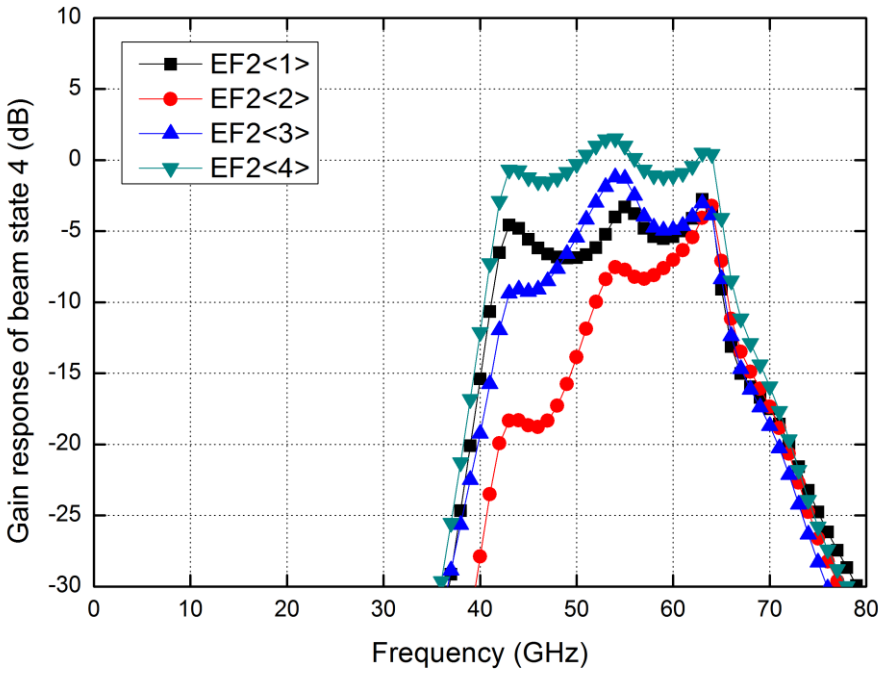

Fig. 4.86. Frequency response of gain of EF2 array at beam state4 at Tx mode.

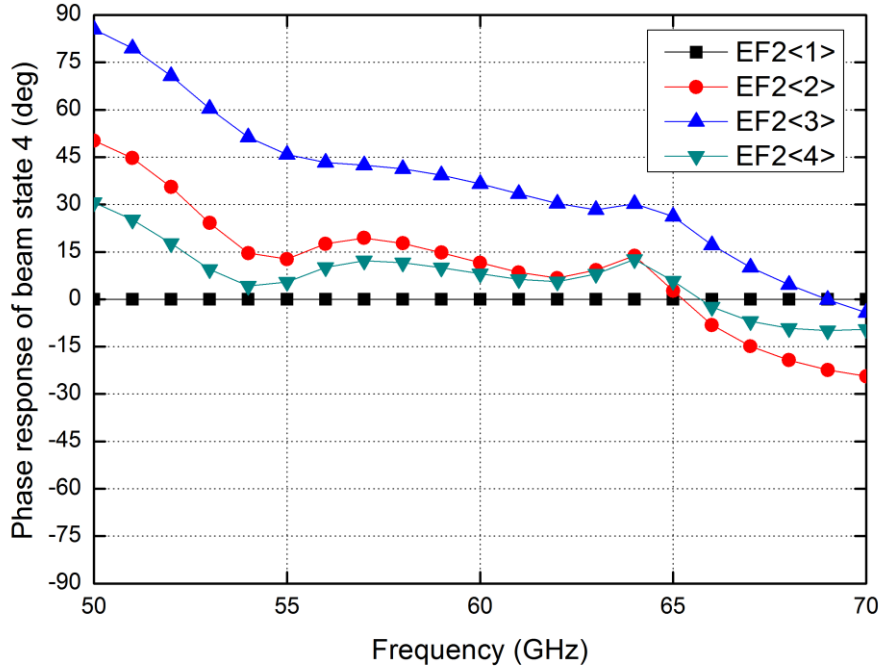

Fig. 4.87. Phase error of EF2 array at beam state4 at Tx mode.

doi:10.6342/NTU201603106

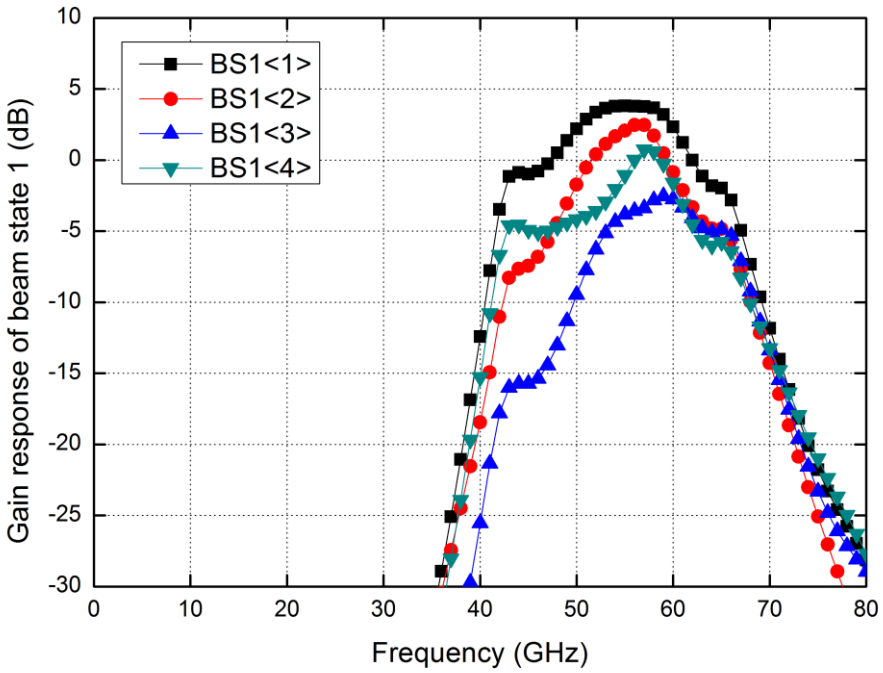

Fig. 4.88. Frequency response of gain of BS1 array at beam state1 at Tx mode.

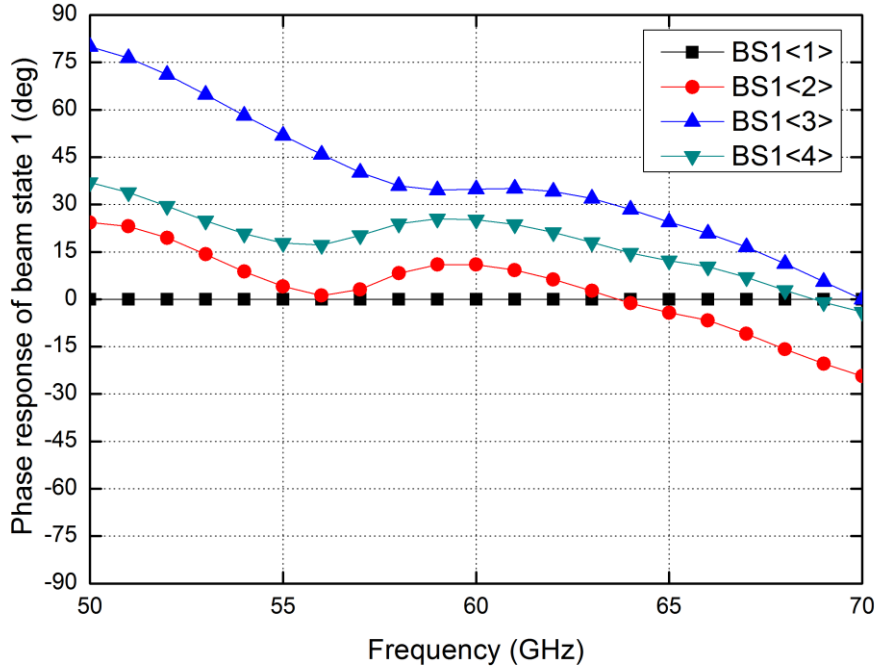

Fig. 4.89. Phase error of BS1 array at beam state1 at Tx mode.

doi:10.6342/NTU201603106

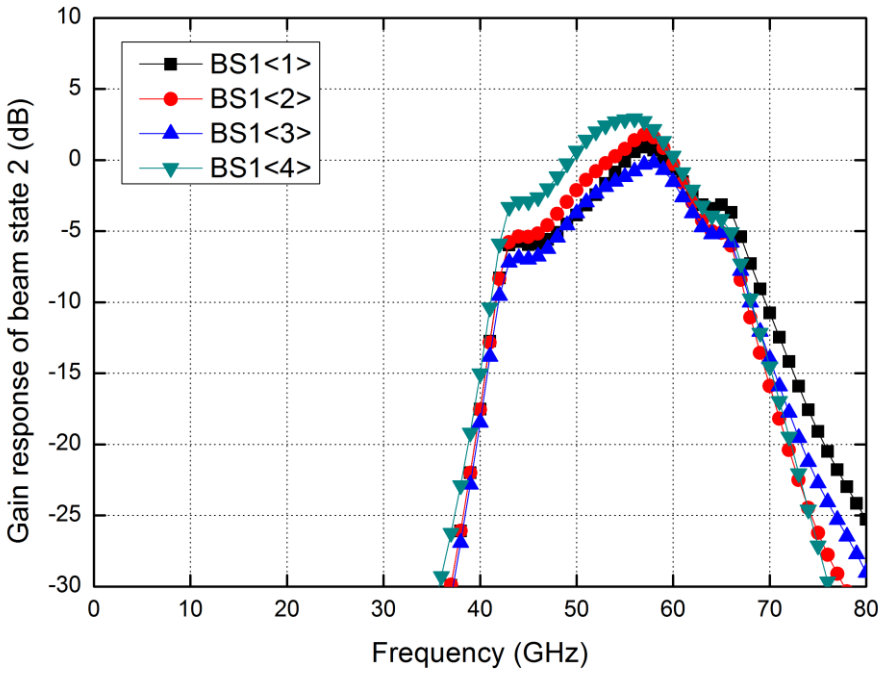

Fig. 4.90. Frequency response of gain of BS1 array at beam state2 at Tx mode.

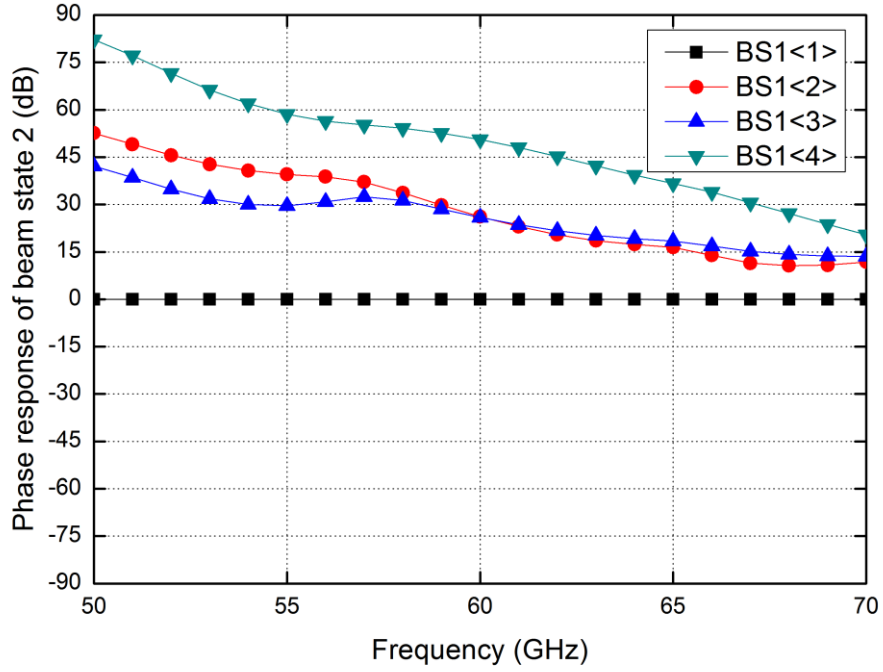

Fig. 4.91. Phase error of BS1 array at beam state2 at Tx mode.

doi:10.6342/NTU201603106

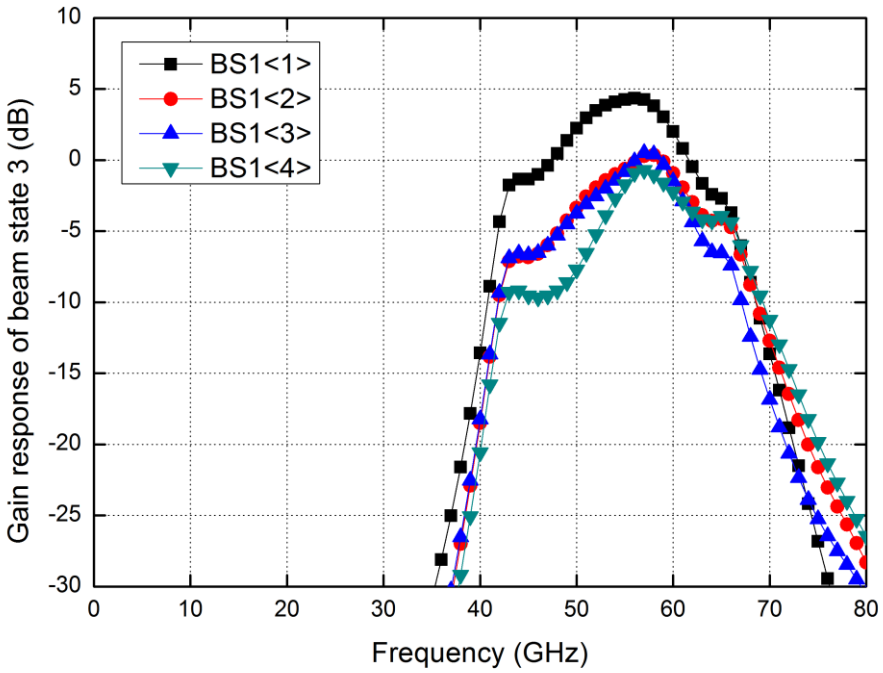

Fig. 4.92. Frequency response of gain of BS1 array at beam state3 at Tx mode.

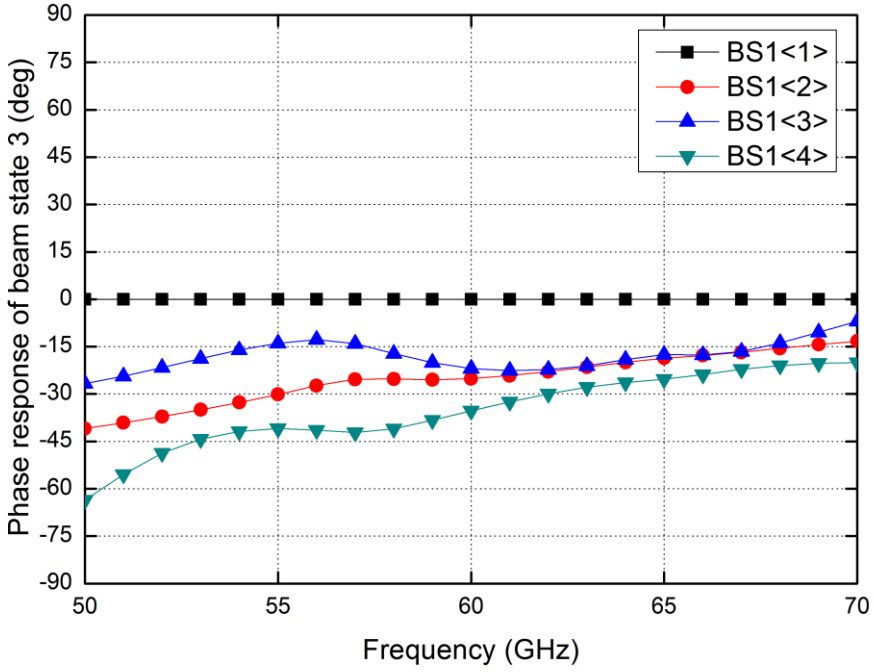

Fig. 4.93. Phase error of BS1 array at beam state3 at Tx mode.

doi:10.6342/NTU201603106

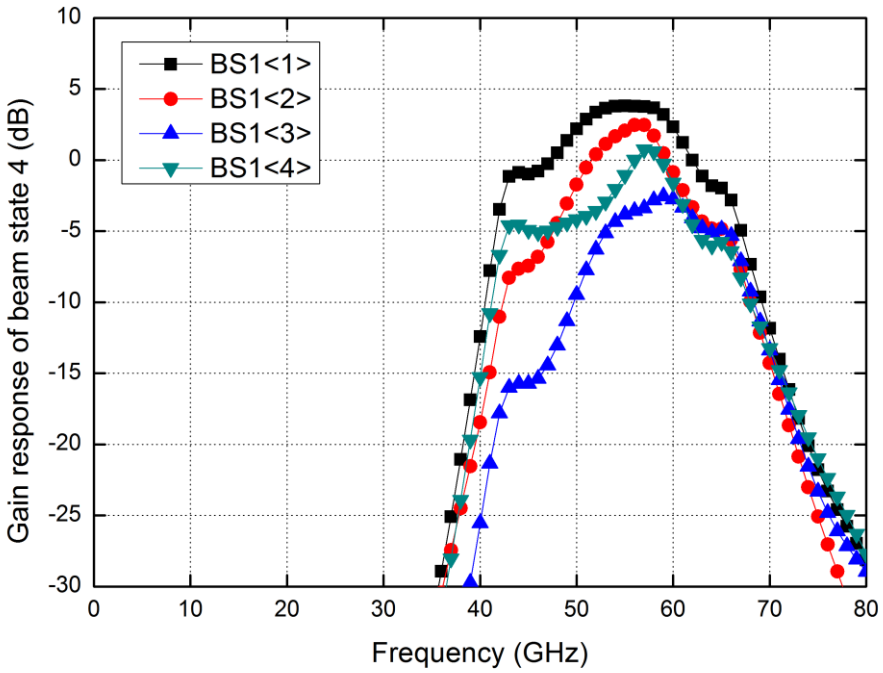

Fig. 4.94. Frequency response of gain of BS1 array at beam state4 at Tx mode.

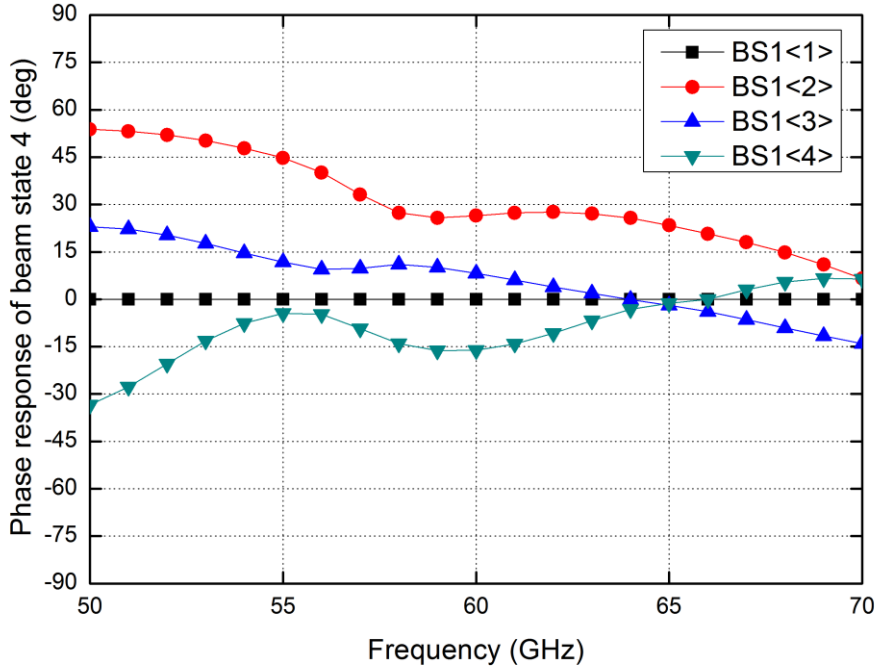

Fig. 4.95. Phase error of BS1 array at beam state4 at Tx mode.

doi:10.6342/NTU201603106

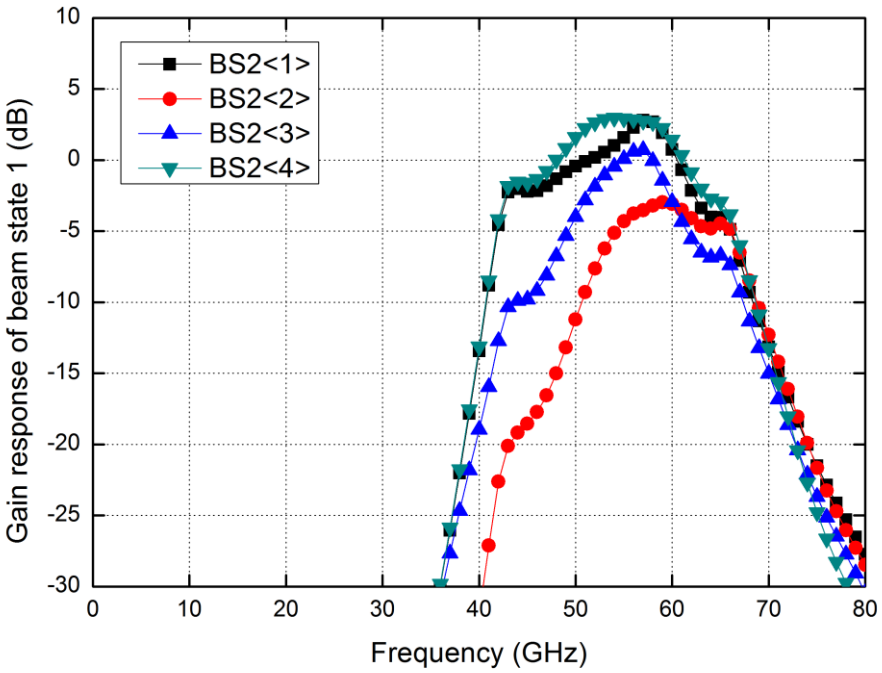

Fig. 4.96. Frequency response of gain of BS2 array at beam state1 at Tx mode.

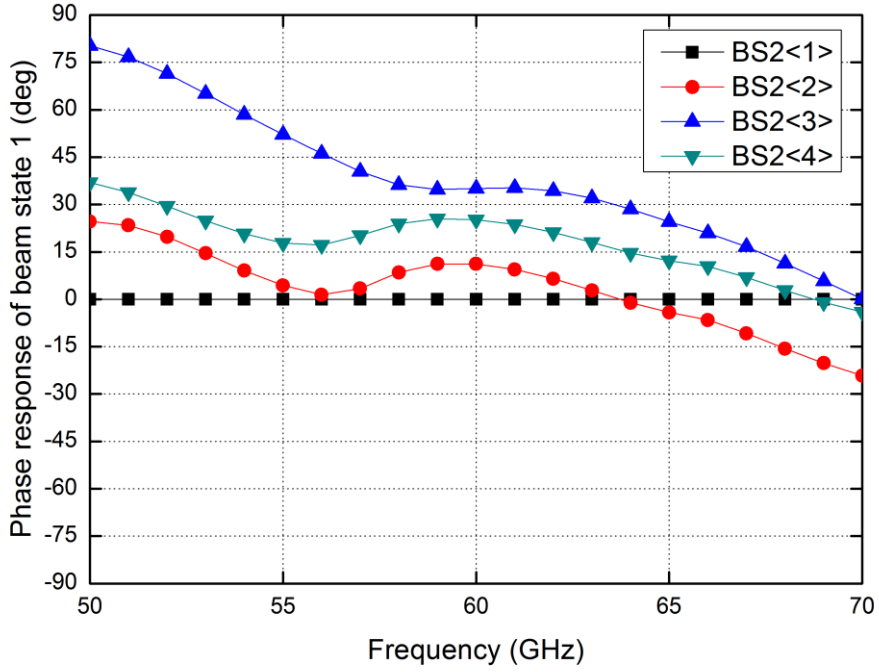

Fig. 4.97. Phase error of BS2 array at beam state1 at Tx mode.

doi:10.6342/NTU201603106

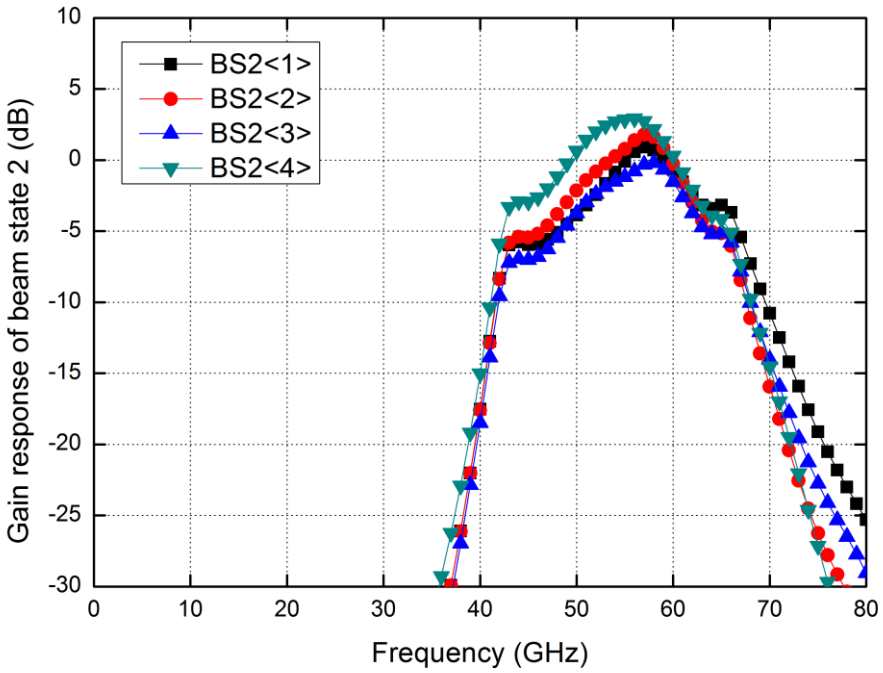

Fig. 4.98. Frequency response of gain of BS2 array at beam state2 at Tx mode.

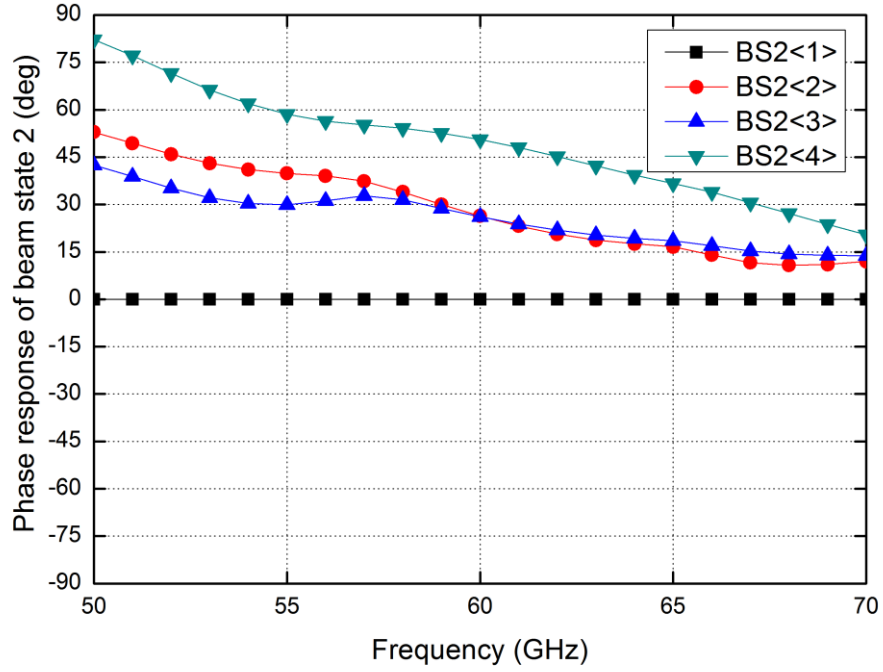

Fig. 4.99. Phase error of BS2 array at beam state2 at Tx mode.

doi:10.6342/NTU201603106

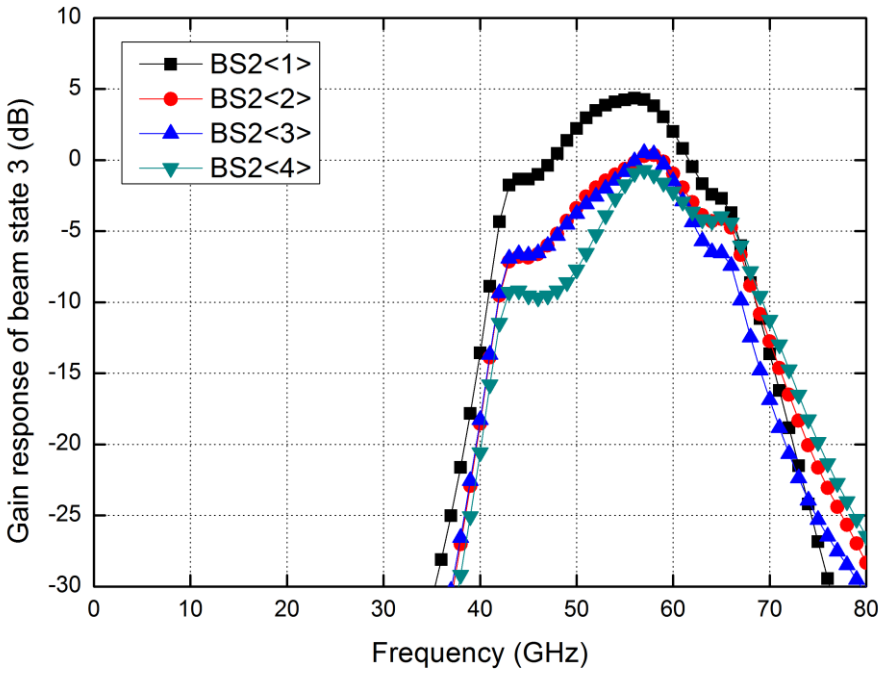

Fig. 4.100. Frequency response of gain of BS2 array at beam state3 at Tx mode.

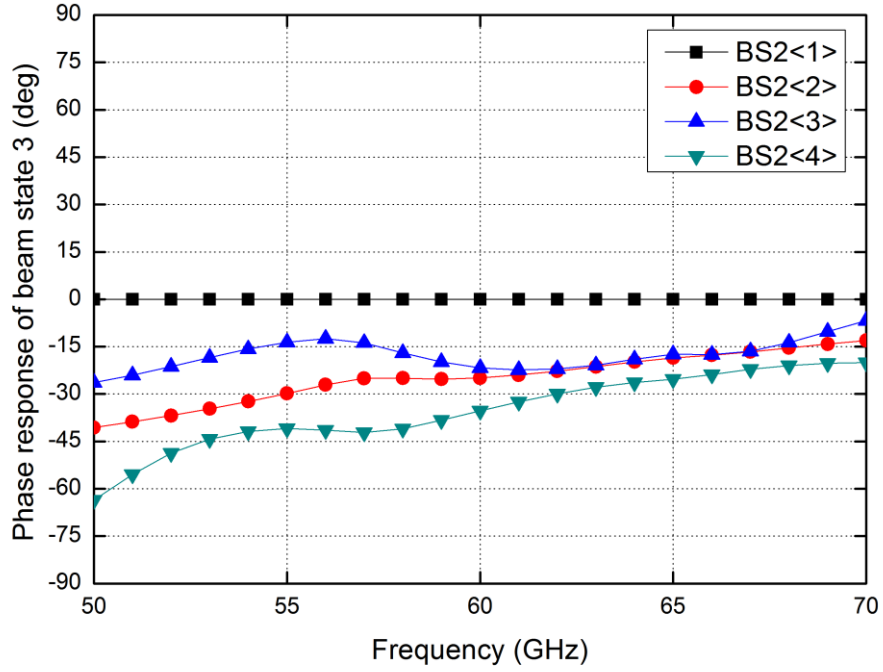

Fig. 4.101. Phase error of BS2 array at beam state3 at Tx mode.

doi:10.6342/NTU201603106

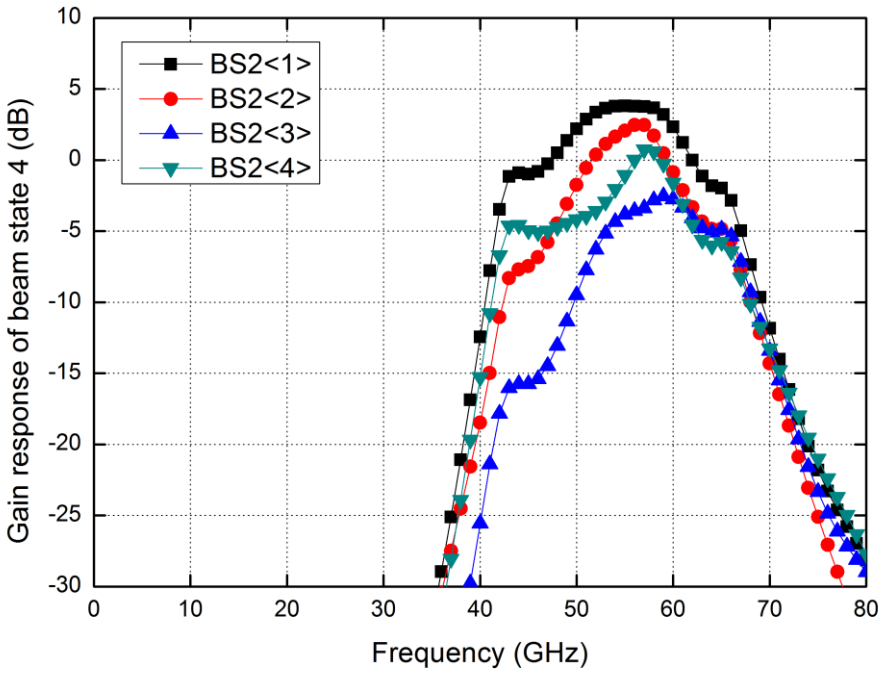

Fig. 4.102. Frequency response of gain of BS2 array at beam state4 at Tx mode.

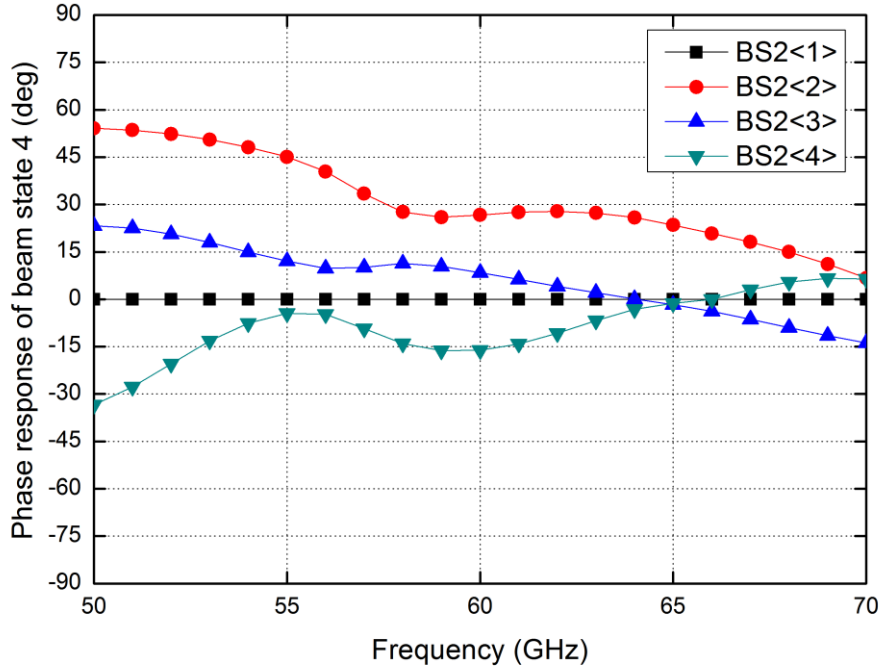

Fig. 4.103. Phase error of BS2 array at beam state4 at Tx mode.

doi:10.6342/NTU201603106

4.4.4 Discussion

Tables 4.7 and 4.8 list the gain imbalance and phase error among the 4 antenna arrays in each mode. The gain imbalance and phase error are up to 5.8 dB and 26.4º, respectively. From the simulated results with the revised model, it can be observed that the frequency response of gain is similar to that of the BDA (section 3.6), but there are some gain imbalance among the 4 beam states.

By using the revised model, the simulated frequency response of the BDA gain indicates the frequency shift (to lower frequency), and the gain is lower than compare with the original gain budget (section 4.1.5). Besides, the Butler matrix operated in the lower band that produce more gain and phase imbalance.

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Table 4.7. Simulated gain imbalance and phase error in Rx mode.

BS1 array in Rx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.3	2	4	5
Phase error (°)	18.2	24.9	17.3	20.5
BS2 array in Rx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.3	2	4	5
Phase error (°)	18.3	24.9	17.3	20.6
EF1 array in Rx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.5	1.1	3.6	5.8
Phase error (°)	14.7	26.4	20.6	18.3
EF2 array in Rx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.5	1.1	3.6	5.8
Phase error (°)	14.7	26.4	20.7	18.4

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Table 4.8. Simulated gain imbalance and phase error in Tx mode.

BS1 array in Tx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.5	1.8	4.2	5.1
Phase error (º)	17.4	25.3	17.7	21.3
BS2 array in Tx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.5	1.8	4.2	5.1
Phase error (º)	17.5	15.3	17.7	21.4
EF1 array in Tx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.3	1.4	3.7	5.9
Phase error (º)	14.6	26.2	20.8	18.2
EF2 array in Tx Mode at 60 GHz	State1	State2	State3	State4
Gain Imbalance (dB)	4.3	1.4	3.7	5.9
Phase error (º)	14.7	26.2	21	18.3

doi:10.6342/NTU201603106

4.5 Experiment results

4.5.1 Measurement setup

Although the chip is designed for bumping process and flip-chip assembly, partial function can be measured without flip-chip. The measurement is performed via on-wafer probing, while the digital and dc pins are biased via bondwire. The digital pins are controlled by DIP switches on the bread board to control the digital signal to logic high or low.

Although the antenna ports are designed in 126-μm pitch, the 63-μm width of the open window of the pads allows to use the GSG RF probe with 100-μm pitch to contact the signal with one of two ground pad, regardless the window-unopen area will damage the contacted probe. Besides, because the Tx port is near the Rx port, in the Tx mode testing, the probe contacts the Tx signal pad with its nearby ground pad, rather than the Rx signal pad, and so as in Rx mode testing. Fig. 4.104 shows the probing condition of the measurement.

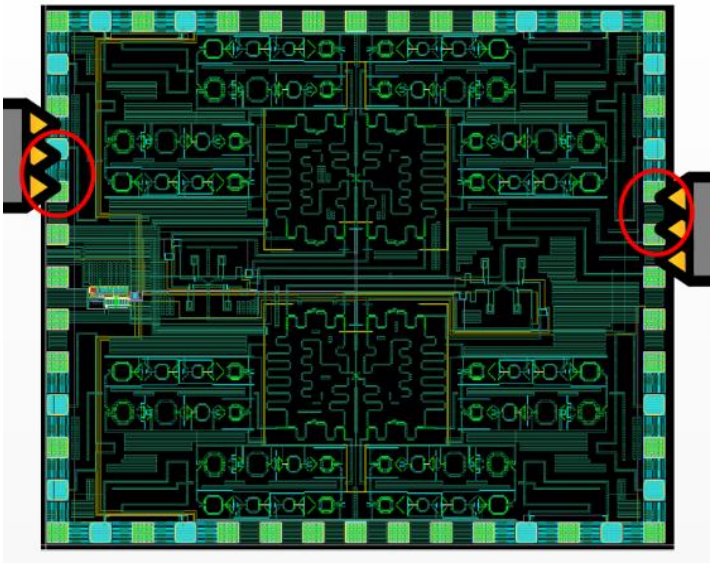

Fig. 4.104. Probing condition of the measurement.

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4.5.2 Digital control testing

To confirm the control function, the non-probing testing is planned. All the ground pads are connected to the common ground by using bondwire, and measured the dc current of RF VDD pin while the system is controlled by the digital pins.

In the tested 6 samples, we found 4 out of 6 samples are out of control but remain in the initial state, it is due to no ESD protection for the digital circuits. Fortunately, the other 2 samples work normally and exhibit consistent results. Table 4.9 shows the results of the digital control testing.

From the results, we found the Tx/Rx control pins have connected reversely, thus the control have the reversed logic that results in the Tx/Rx mode interchanged. Note that the logic connection errors will not affect the system operation, and it only changes the definition of Tx/Rx mode control. Besides, the gain/power control function failed, because the current control is taken by the PMOS switch of global bias circuit, which need the 2.5-V voltage to turn off the 25-μA or 50-μA current, and the digital circuit offers 1.1-V voltage is not adequate to turn off the switches. This results in the system stay in the most high gain mode. Fortunately, we have designed the additional switches to guide the unused current to ground in the local bias circuit, thus the power-down function is still functional. All the above errors have fixed in the revised version of system (section 4.6).

Although we found these mistakes, the beam control testing still can be measured by RF probing. The beam control testing results have presented in the following sections.

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Table 4.9. Dc and digital control testing results.

SET[2:0]	PAR[3:0]	Simulated current (mA)		Measured current of BDA test circuit (multiply by 4)		System Measurement	
		TXRX=0	TXRX=1	TXRX=0	TXRX=1	TXRX=0	TXRX=1
011	[XXXX]	0	0	0	0	0	0
101/110	[00XX]	139	326	125	238	216	123
	[01XX]	113	291	102	210	214	123
	[10XX]	88	254	82	183	214	122
	[11XX]	64	213	60	158	213	120

4.5.3 Beam control testing results at Rx mode

This section presents the Rx mode beam state control measurement. Due to the reversed connection of the digital pins in the Tx/Rx mode selection, the Rx mode testing is configured at TXRX=1. All the RF ports keep in open condition except the probing ports.

The antenna ports are distributed along the outer ring of the system chip, they are placed in the different sides. Measuring all the 4 relative ports of array at the same time is hard to achieve because the probes must be rearranged to another direction and need to re-calibrated. Besides, the 4 antenna ports, EF1<1>, EF2<1>, BS1<1>, and BS2<1> , are placed at the same side of the Tx and Rx ports (see Fig. 4.39), thus they cannot be measured due to it is not possible to place two probes at the same side in our measurement environment. For these reasons, the following results only include the 3 ports in the same

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array (simulation includes all 4 ports). As a results, only 12 of the 16 antenna ports can be measured. Besides, the following results are measured by probing on the fixed I/O port, and change the 4 beam states, thus the results of 3 ports in the same array are combined by two individual measurements and calibration. All the results are measured by Agilent E8361C vector network analyzer, with GGB CS5-100 calibration substrate, which offers the opposite and vertical direction of calibration kits.

Figs. 4.105 to 4.112 show the gain and phase error of EF1 array among the 4 beam states. Figs. 4.113 to 4.120 show the gain and phase error of EF2 array among the 4 beam states. Figs. 4.121 to 4.128 show the gain and phase error of BS1 array among the 4 beam states. Figs. 4.129 to 4.136 show the gain and phase error of BS2 array among the 4 beam states. From these results, it can be observed that all the phase errors at 60 GHz are smaller than 25º.

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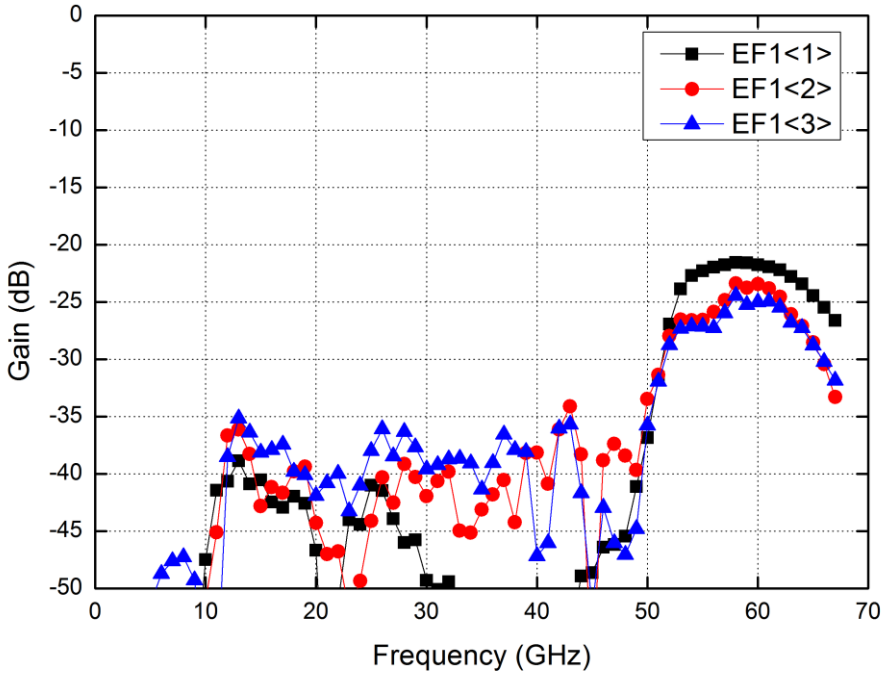

Fig. 4.105. Measured gain of EF1 array at beam state1 in Rx mode.

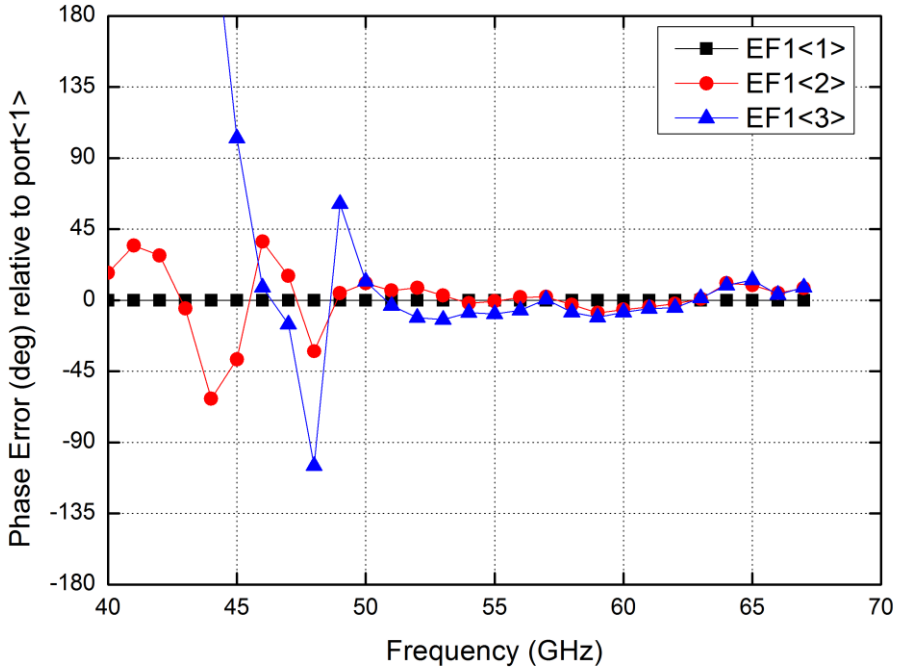

Fig. 4.106. Measured phase error of EF1 array at beam state1 in Rx mode.

doi:10.6342/NTU201603106

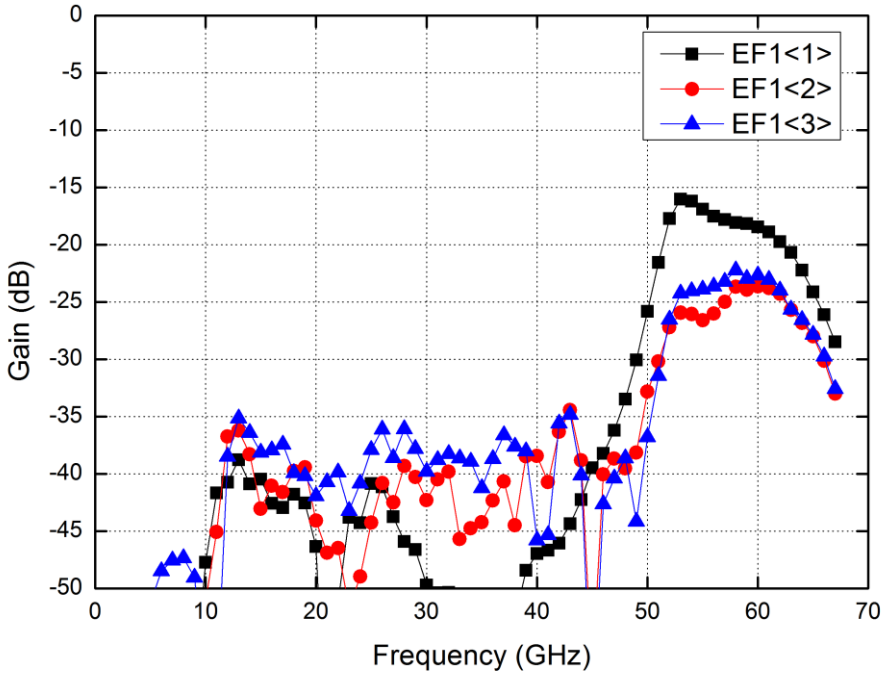

Fig. 4.107. Measured gain of EF1 array at beam state2 in Rx mode.

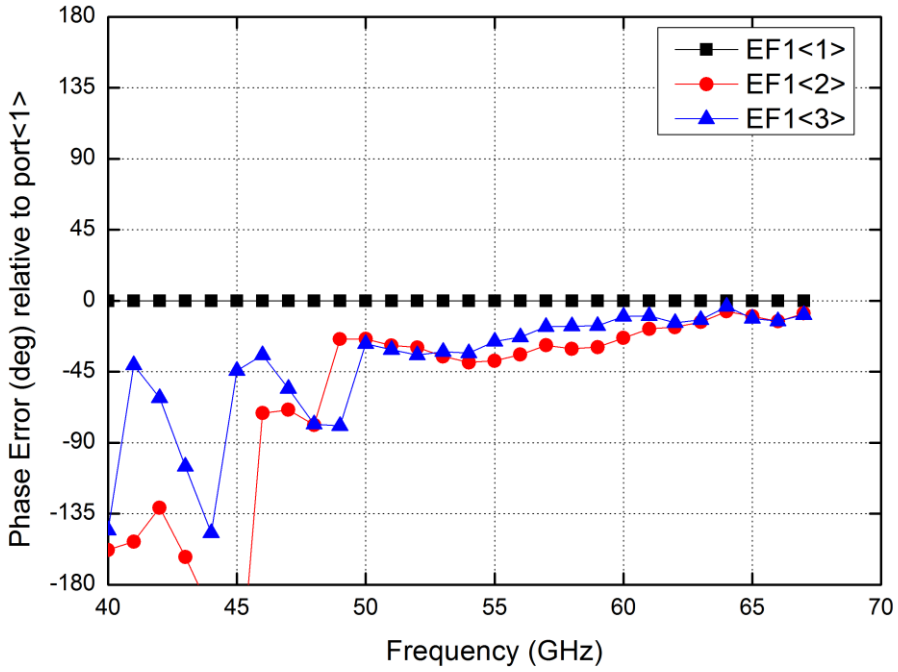

Fig. 4.108. Measured phase error of EF1 array at beam state2 in Rx mode.

doi:10.6342/NTU201603106

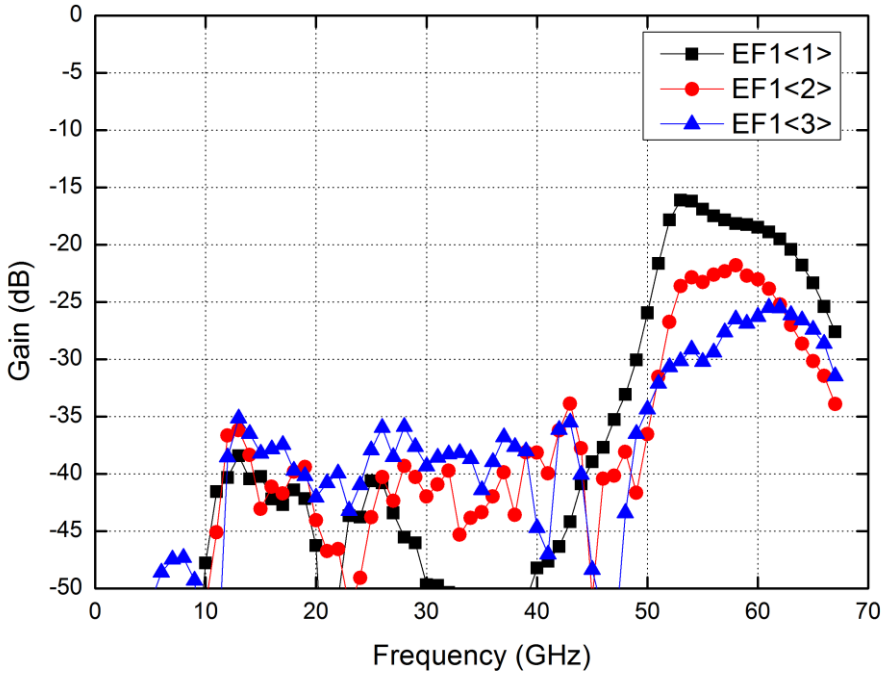

Fig. 4.109. Measured gain of EF1 array at beam state3 in Rx mode

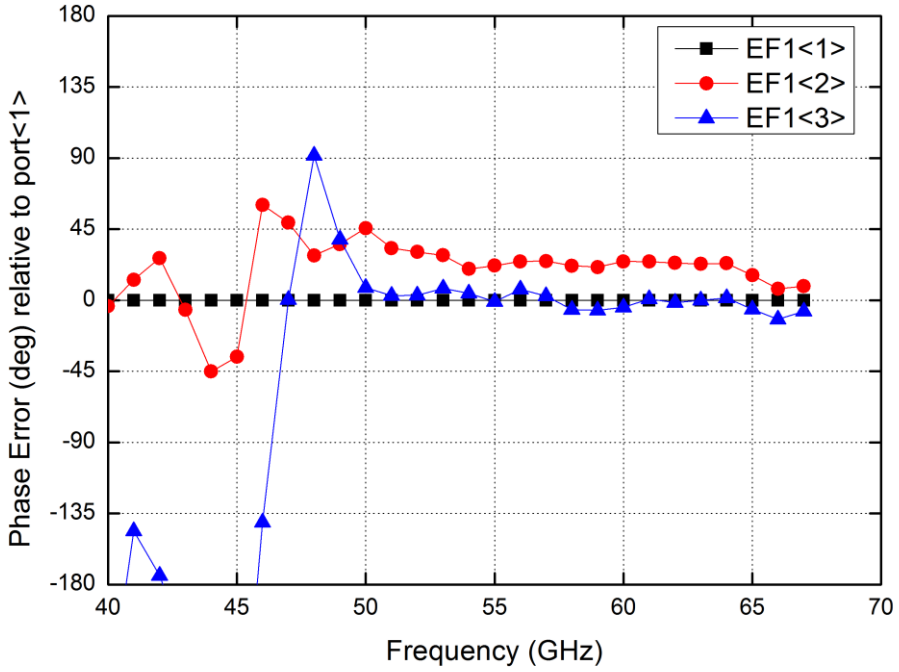

Fig. 4.110. Measured phase error of EF1 array at beam state3 in Rx mode.

doi:10.6342/NTU201603106

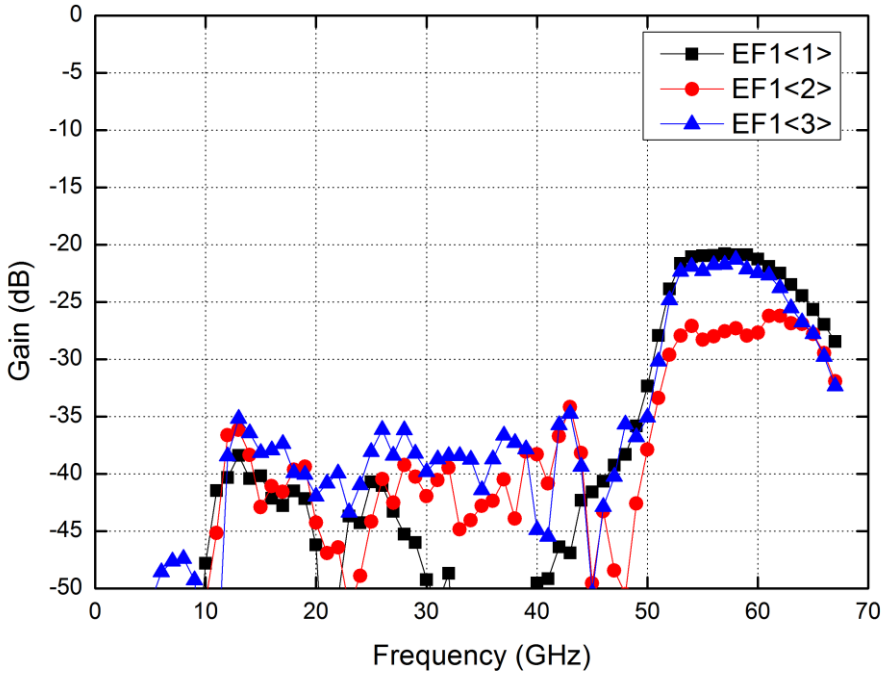

Fig. 4.111. Measured gain of EF1 array at beam state4 in Rx mode.

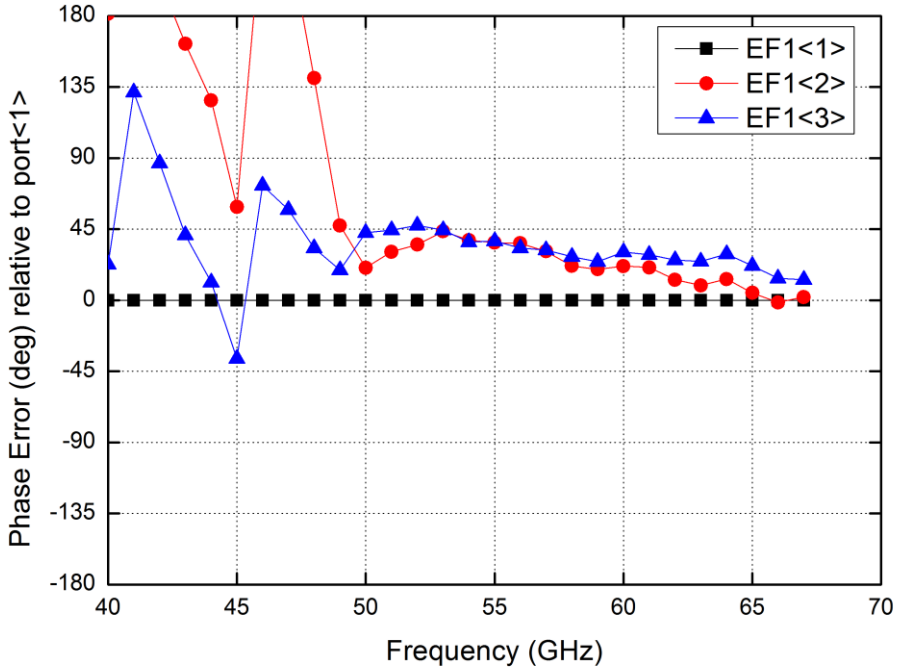

Fig. 4.112. Measured phase error of EF1 array at beam state4 in Rx mode.

doi:10.6342/NTU201603106

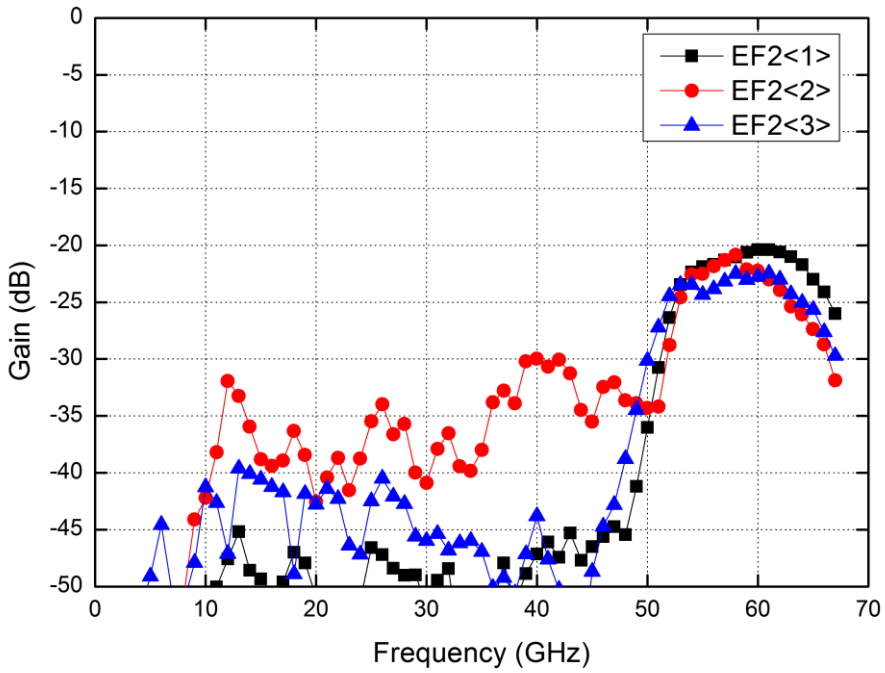

Fig. 4.113. Measured gain of EF2 array at beam state1 in Rx mode.

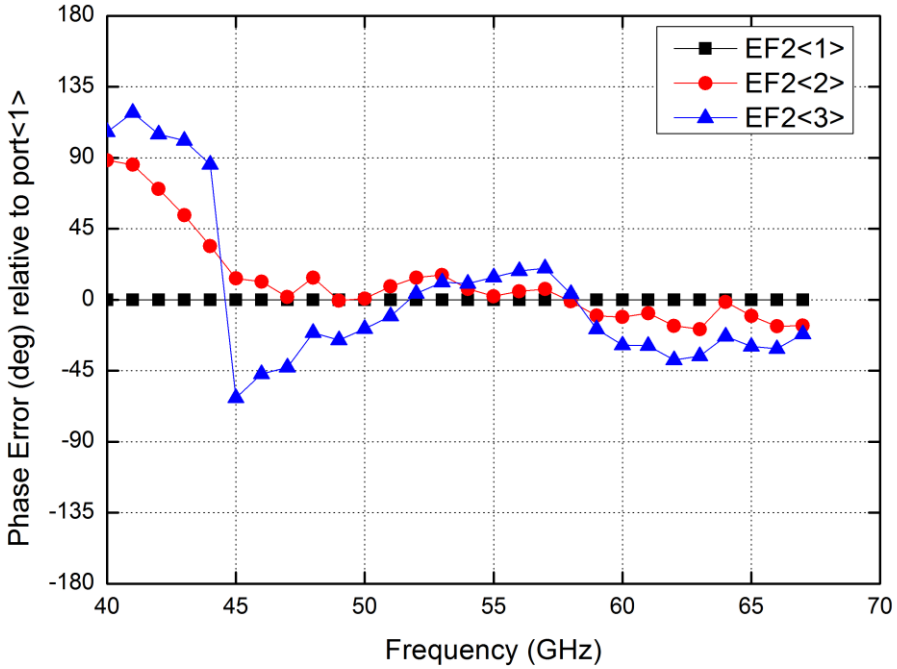

Fig. 4.114. Measured phase error of EF2 array at beam state1 in Rx mode.

doi:10.6342/NTU201603106

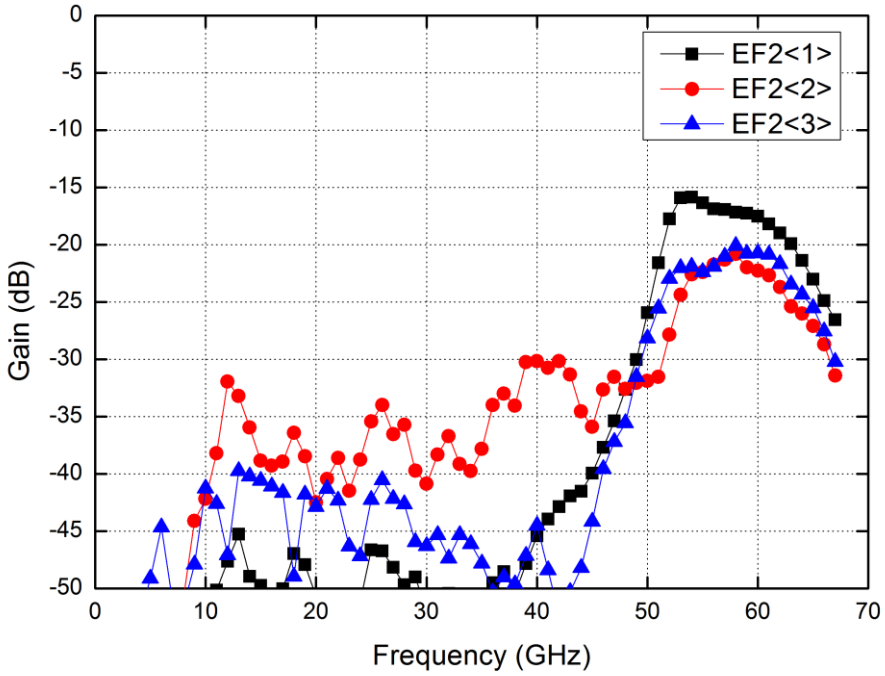

Fig. 4.115. Measured gain of EF2 array at beam state2 in Rx mode.

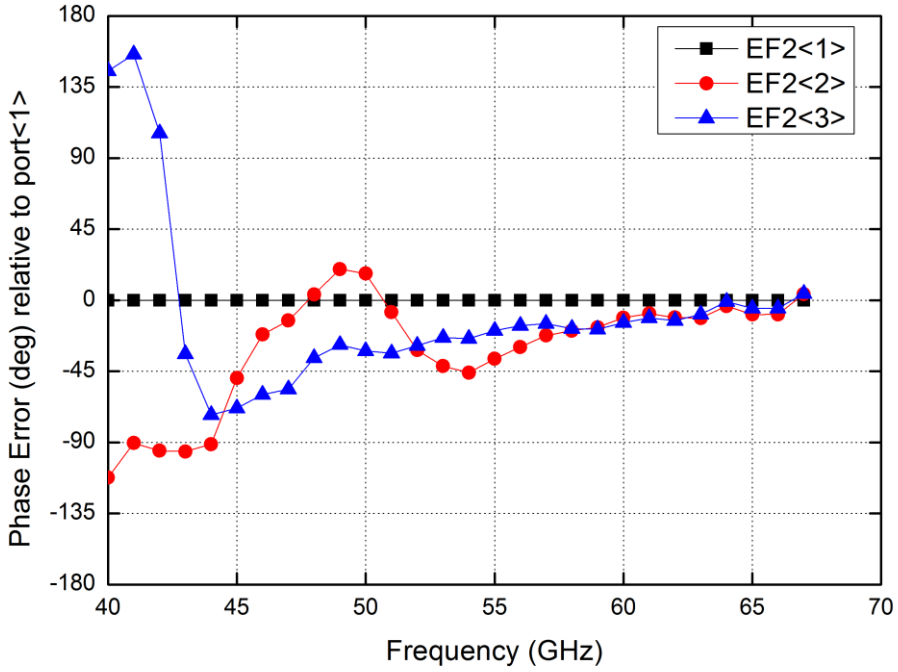

Fig. 4.116. Measured phase error of EF2 array at beam state2 in Rx mode.

doi:10.6342/NTU201603106

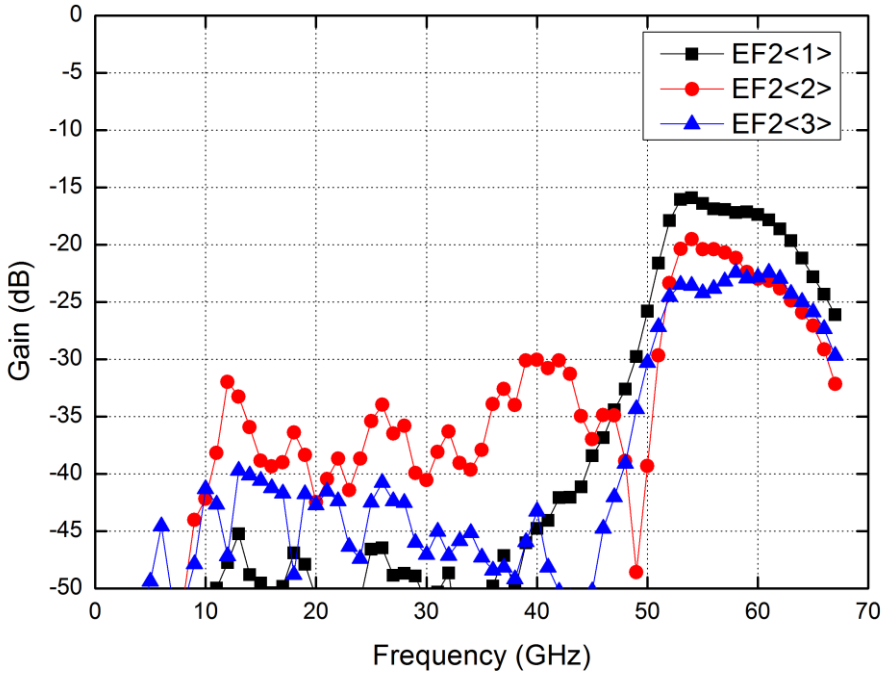

Fig. 4.117. Measured gain of EF2 array at beam state3 in Rx mode.

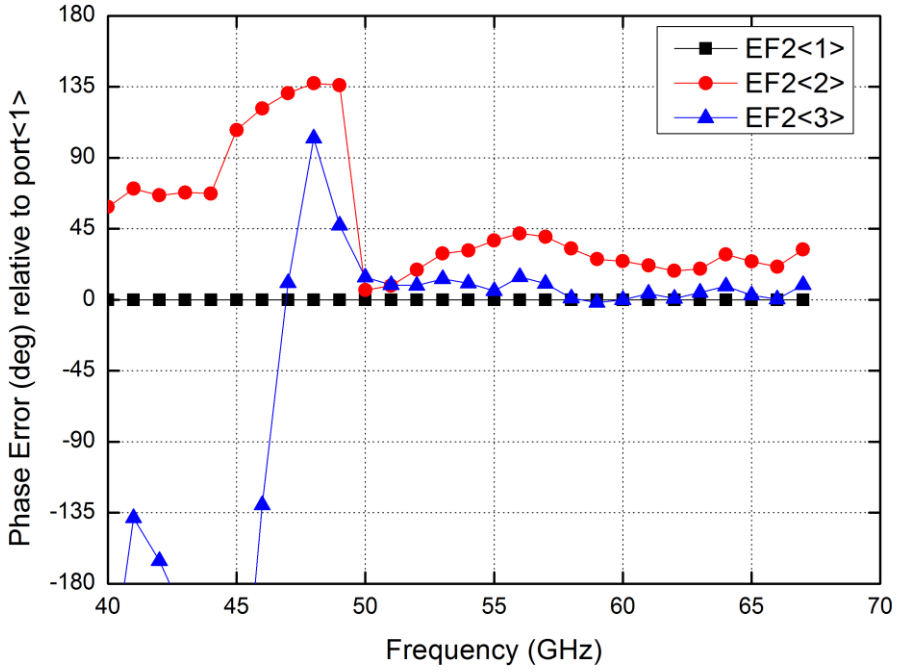

Fig. 4.118. Measured phase error of EF2 array at beam state3 in Rx mode.

doi:10.6342/NTU201603106

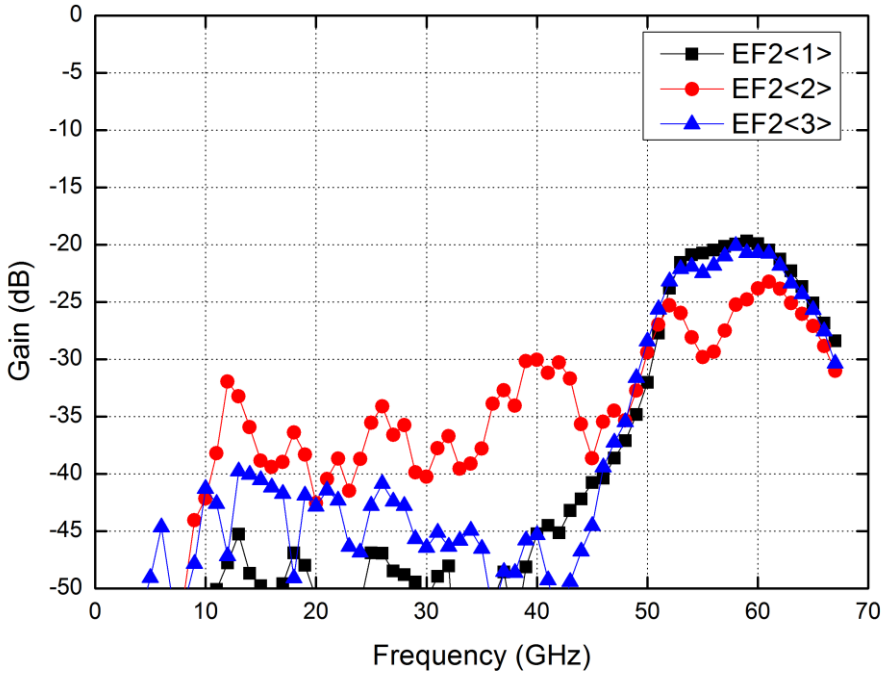

Fig. 4.119. Measured gain of EF2 array at beam state4 in Rx mode.

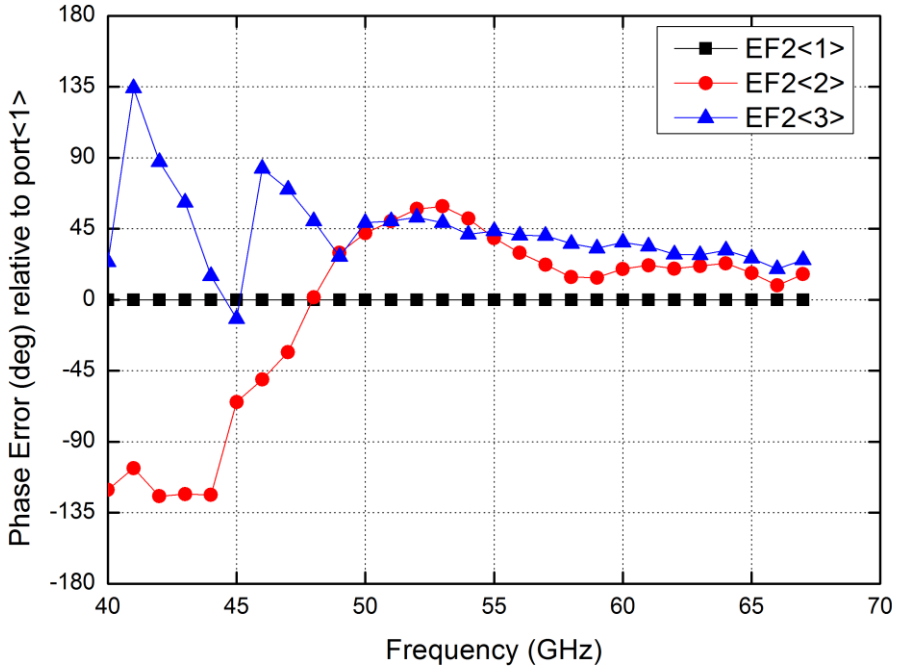

Fig. 4.120. Measured phase error of EF2 array at beam state4 in Rx mode.

doi:10.6342/NTU201603106

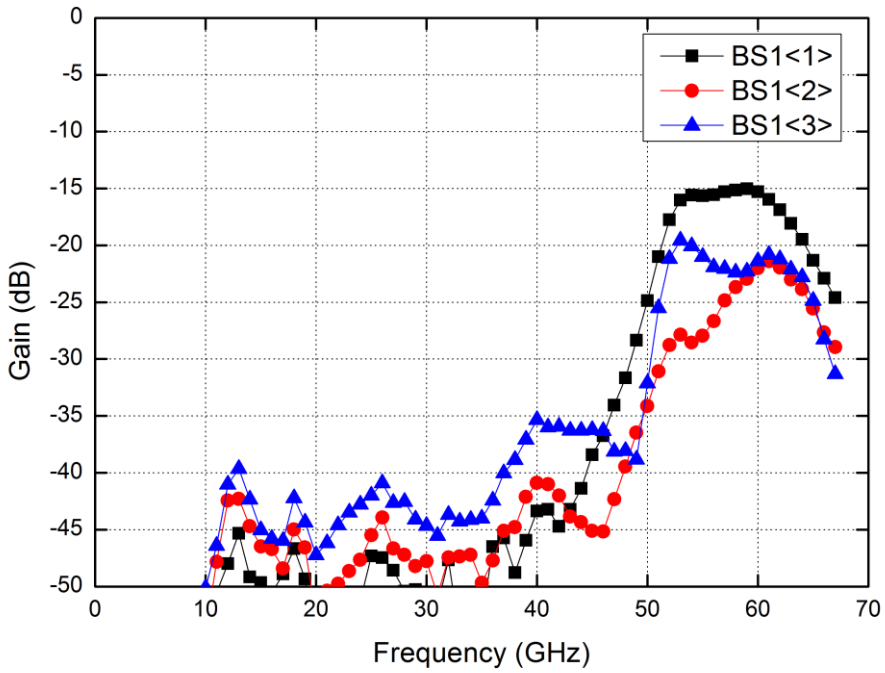

Fig. 4.121. Measured gain of BS1 array at beam state1 in Rx mode.

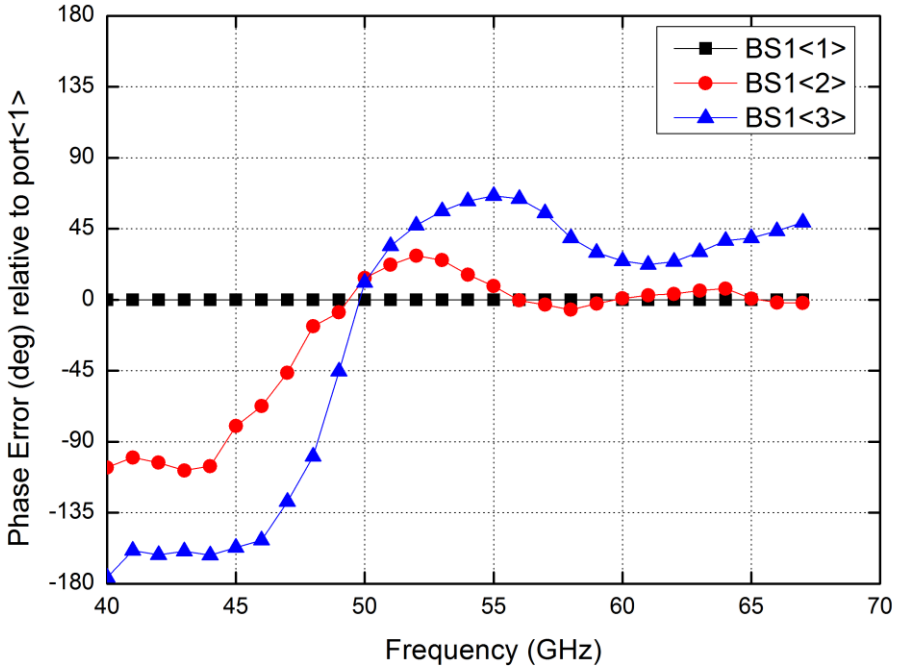

Fig. 4.122. Measured phase error of BS1 array at beam state1 in Rx mode.

doi:10.6342/NTU201603106

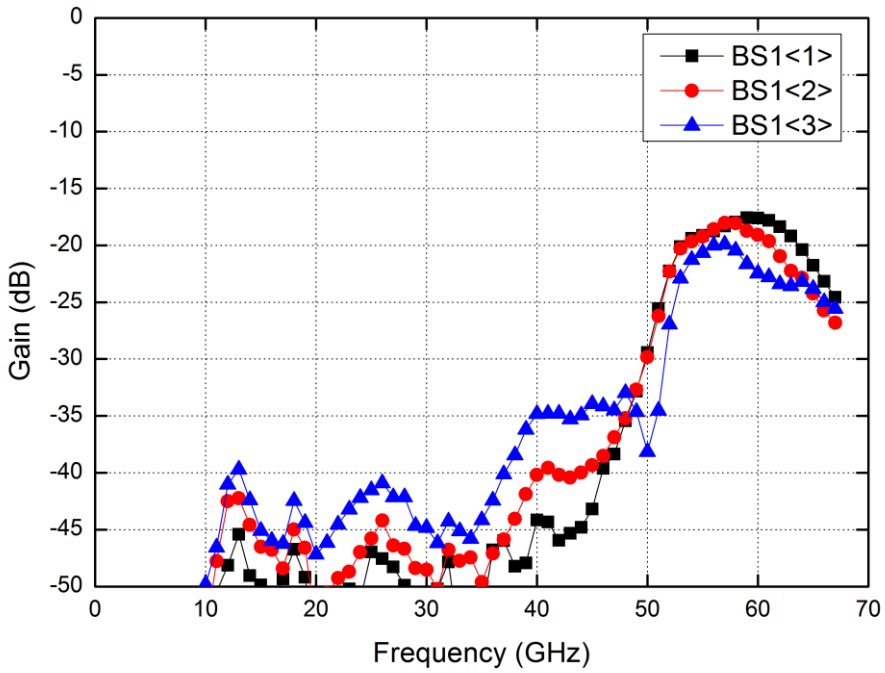

Fig. 4.123. Measured gain of BS1 array at beam state2 in Rx mode.

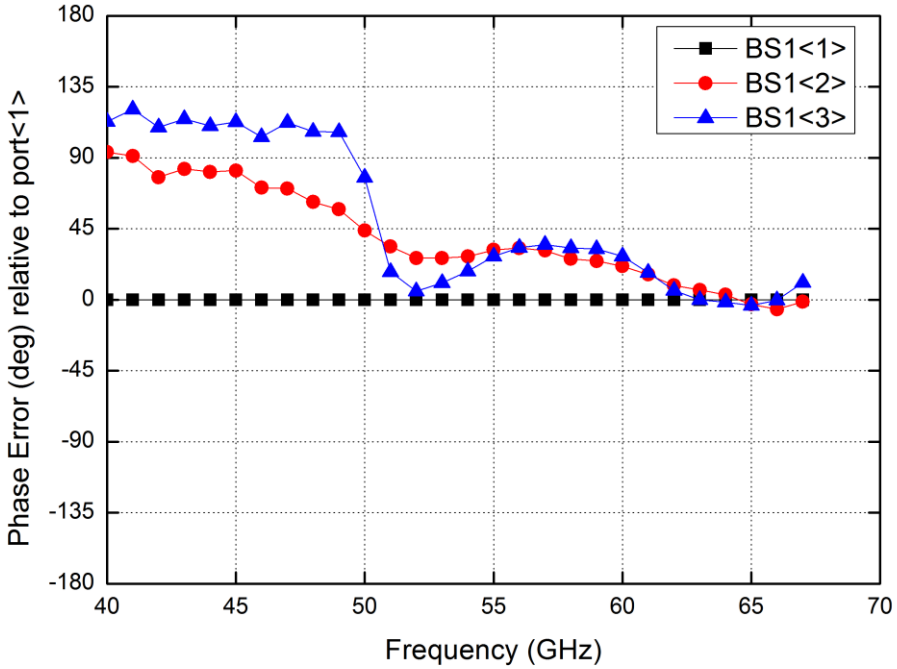

Fig. 4.124. Measured phase error of BS1 array at beam state2 in Rx mode.

doi:10.6342/NTU201603106

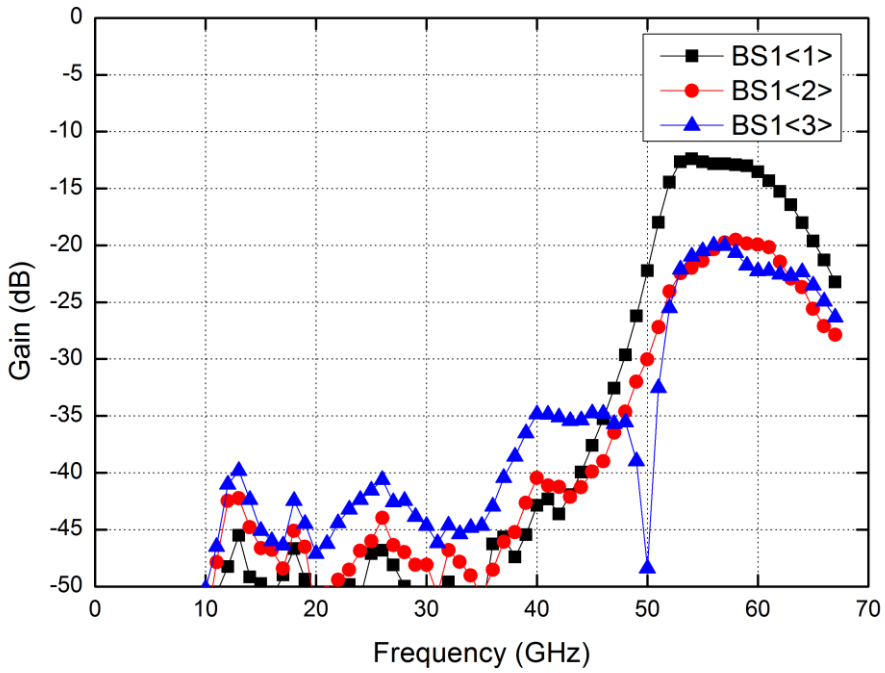

Fig. 4.125. Measured gain of BS1 array at beam state3 in Rx mode.

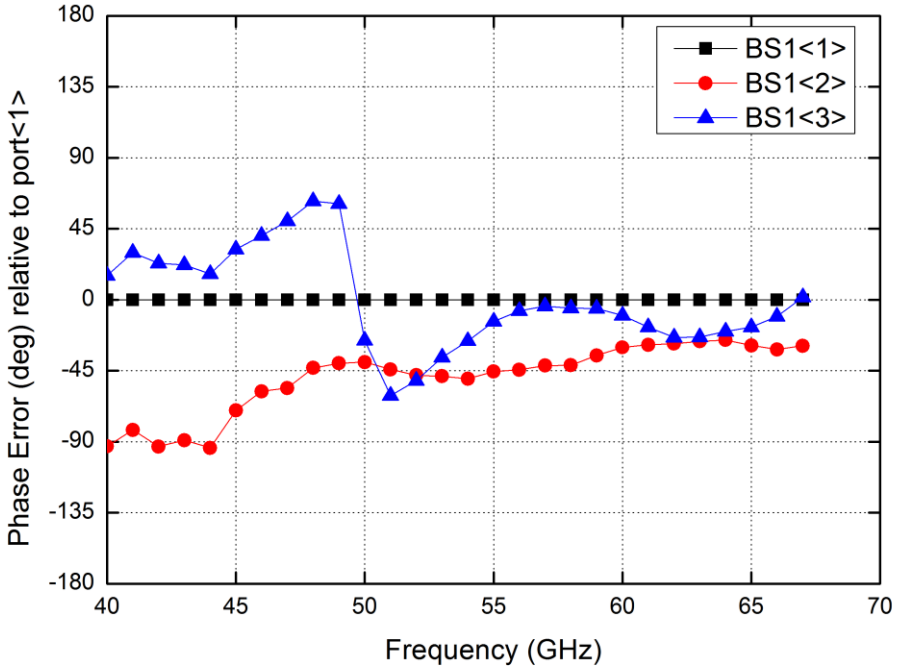

Fig. 4.126. Measured phase error of BS1 array at beam state3 in Rx mode.

doi:10.6342/NTU201603106

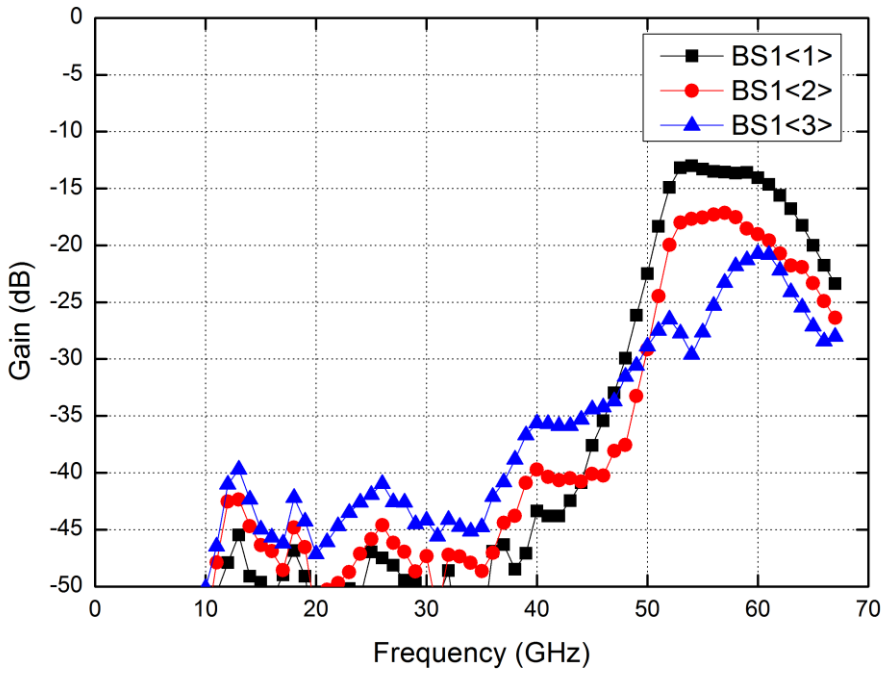

Fig. 4.127. Measured gain of BS1 array at beam state4 in Rx mode.

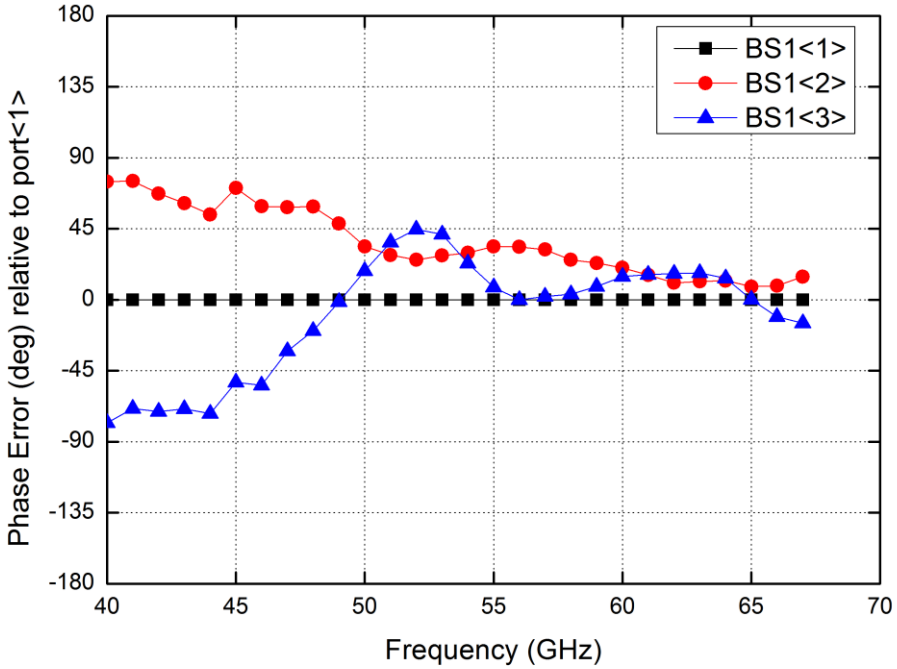

Fig. 4.128. Measured phase error of BS1 array at beam state4 in Rx mode.

doi:10.6342/NTU201603106

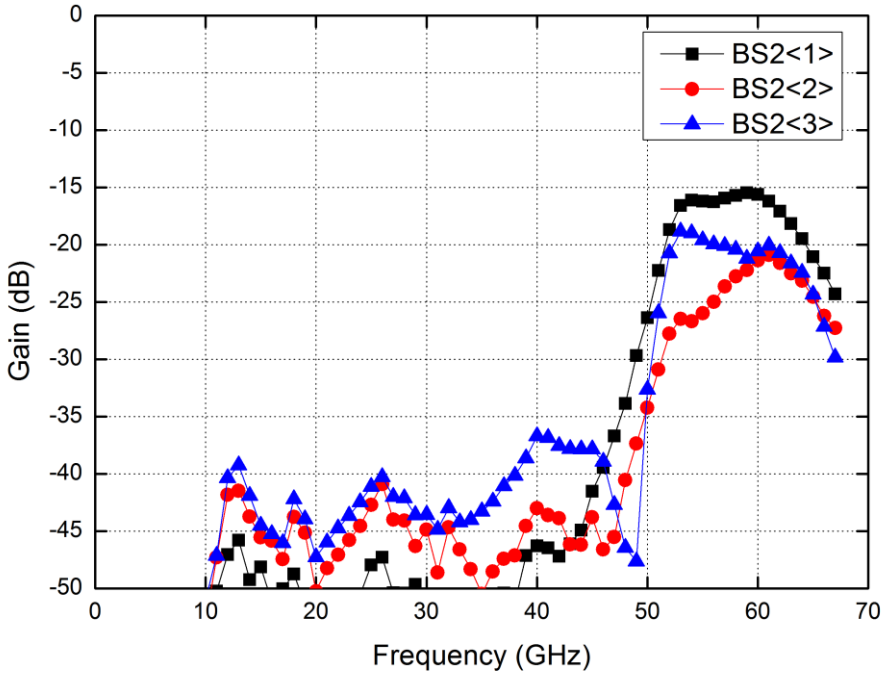

Fig. 4.129. Measured gain of BS2 array at beam state1 in Rx mode.

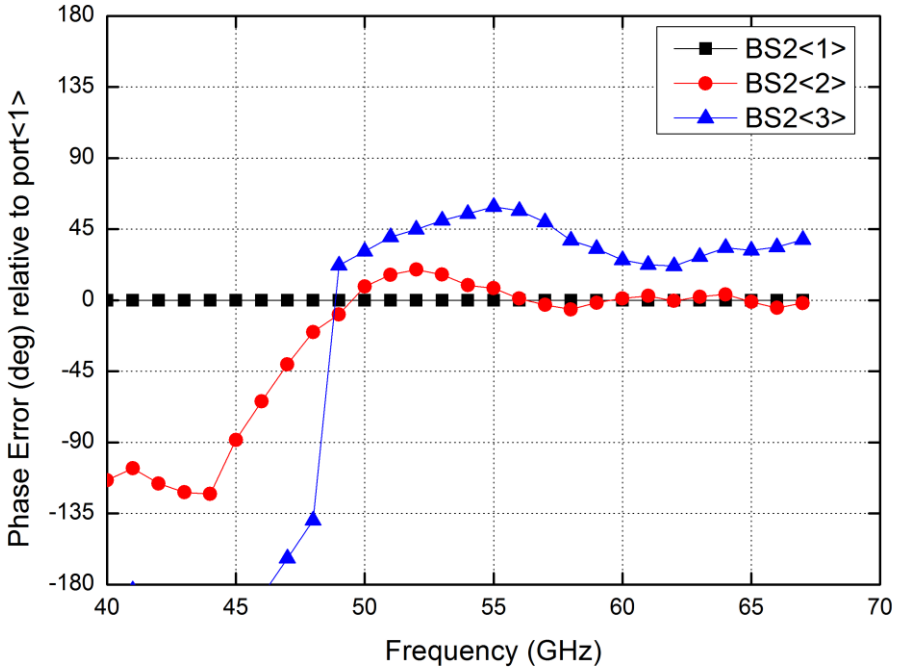

Fig. 4.130. Measured phase error of BS2 array at beam state1 in Rx mode.

doi:10.6342/NTU201603106

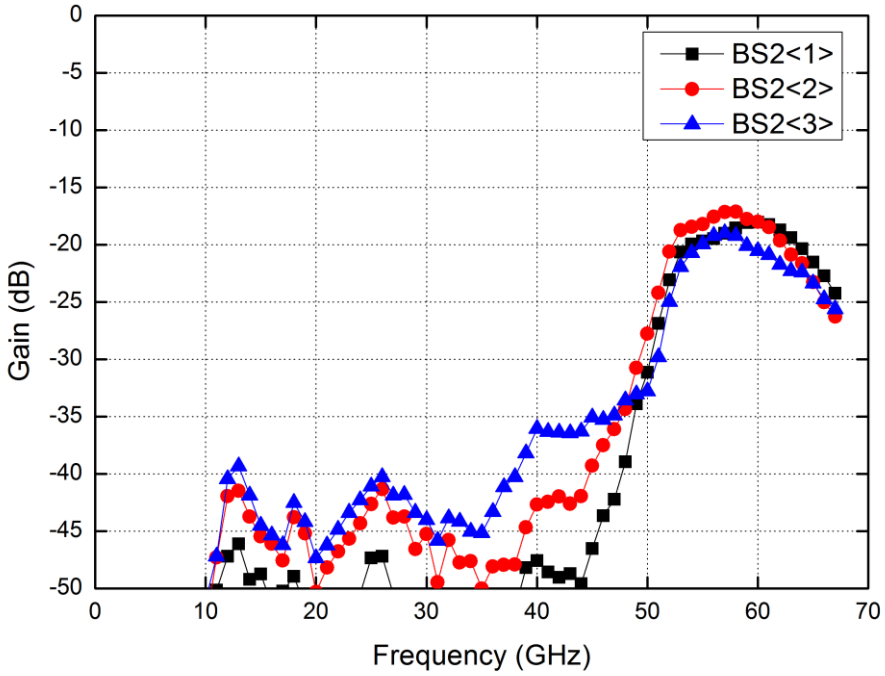

Fig. 4.131. Measured gain of BS2 array at beam state2 in Rx mode.

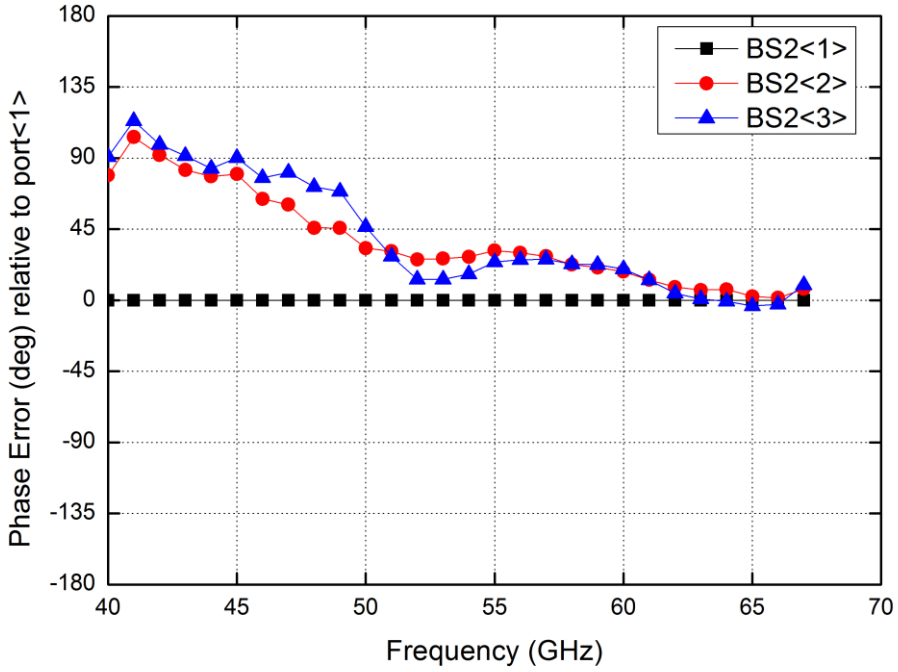

Fig. 4.132. Measured phase error of BS2 array at beam state2 in Rx mode.

doi:10.6342/NTU201603106

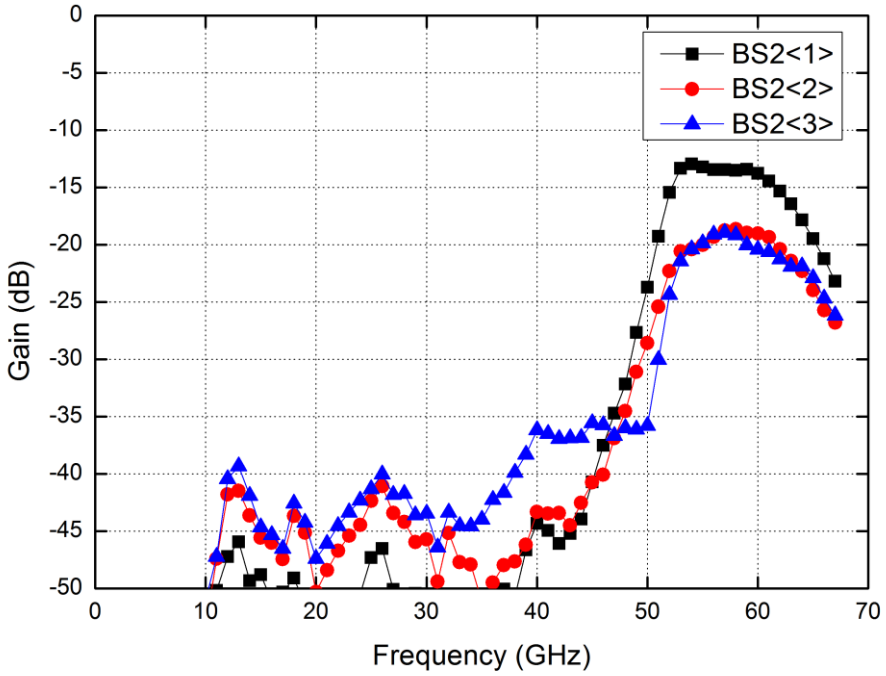

Fig. 4.133. Measured gain of BS2 array at beam state3 in Rx mode.

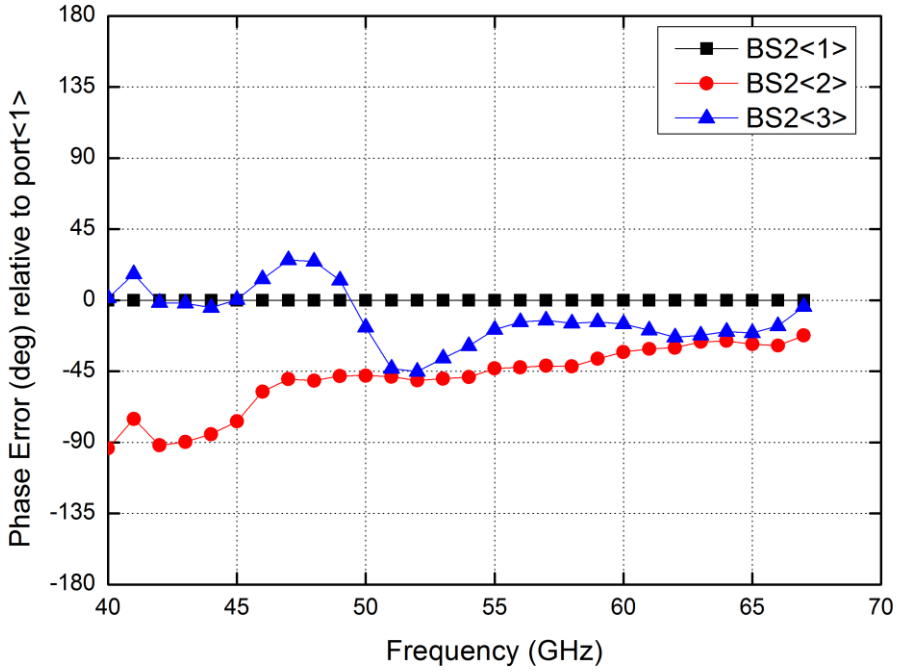

Fig. 4.134. Measured phase error of BS2 array at beam state3 in Rx mode.

doi:10.6342/NTU201603106

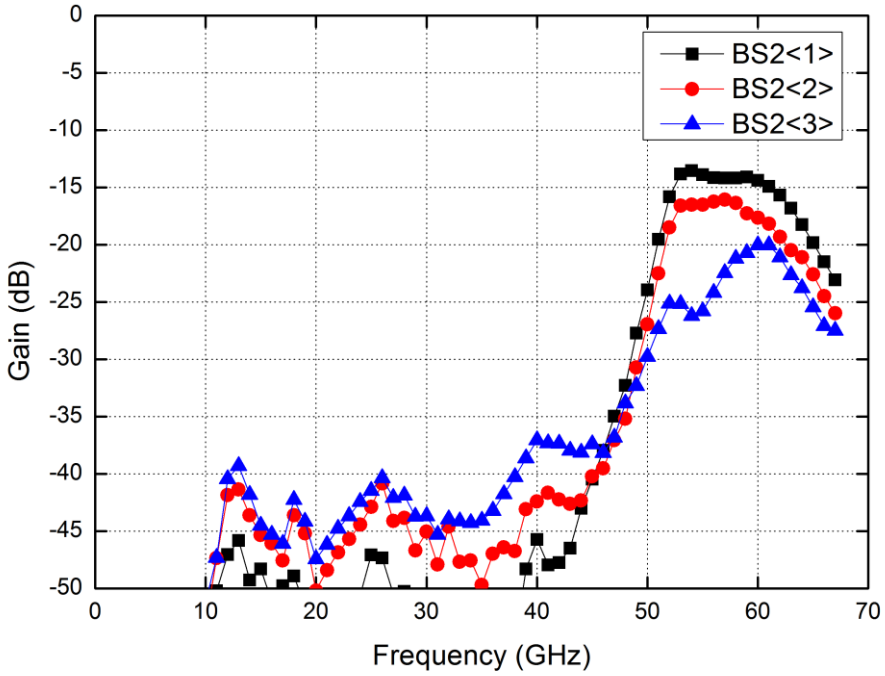

Fig. 4.135. Measured gain of BS2 array at beam state4 in Rx mode.

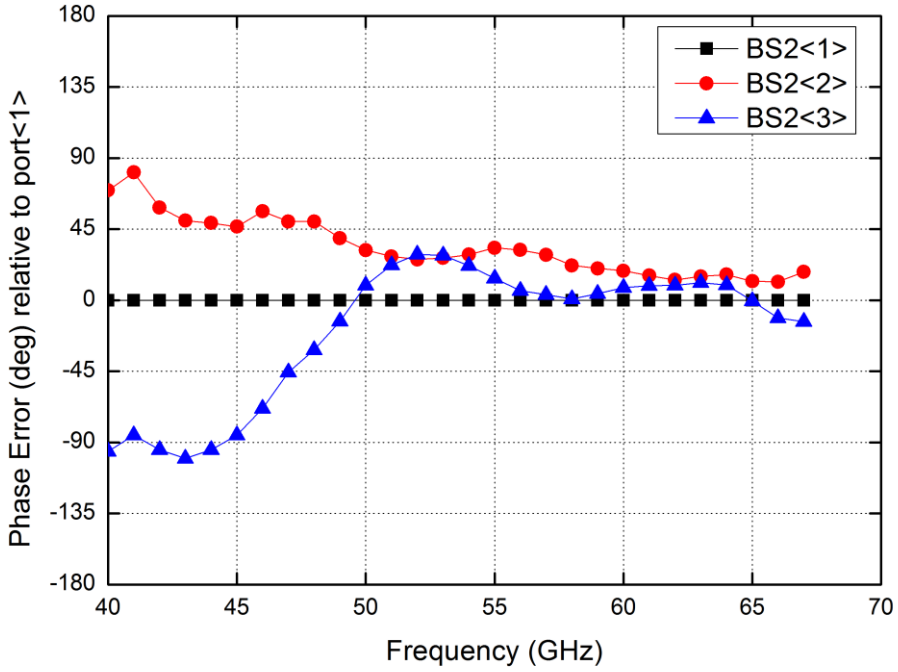

Fig. 4.136. Measured phase error of BS2 array at beam state4 in Rx mode.

doi:10.6342/NTU201603106

4.5.4 Beam control testing results at Tx mode

Due to the reversed connection of the digital pins in the Tx/Rx mode selection, the Tx mode testing is configured at TXRX=0. The other measurement condition is the same as in the Rx mode.

Figs. 4.137 to 4.144 show the gain and phase error of EF1 array among the 4 beam states. Figs. 4.145 to 4.152 show the gain and phase error of EF2 array among the 4 beam states. Figs. 4.153 to 4.160 show the gain and phase error of BS1 array among the 4 beam states. Figs. 4.161 to 4.168 show the gain and phase error of BS2 array among the 4 beam states. From these results, it can be observed that all the phase errors are smaller than 25º, except BS1<1> at state2 (35º) and BS2<1> at state3 (30º).

doi:10.6342/NTU201603106

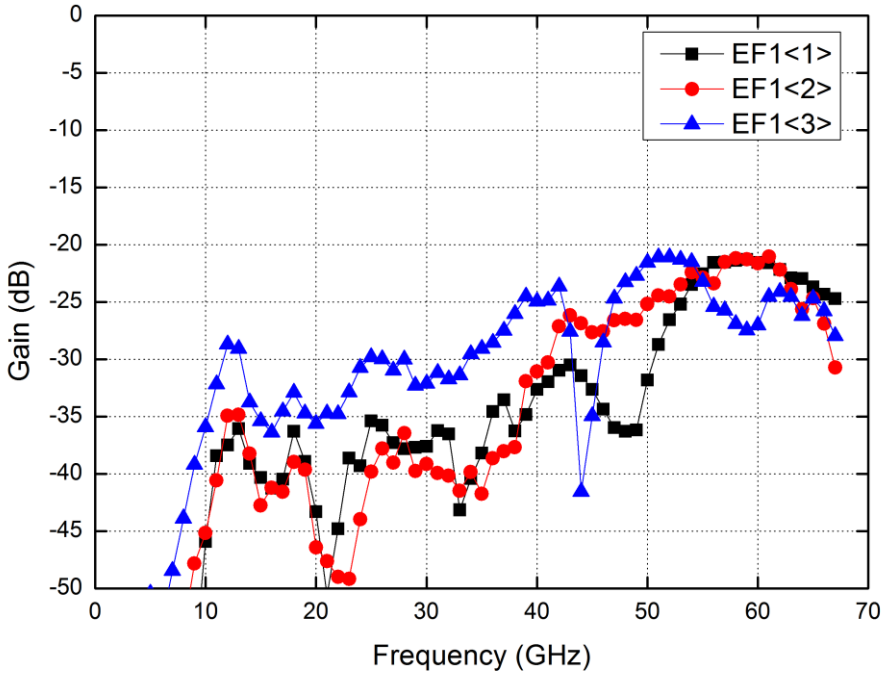

Fig. 4.137. Measured gain of EF1 array at beam state1 in Tx mode.

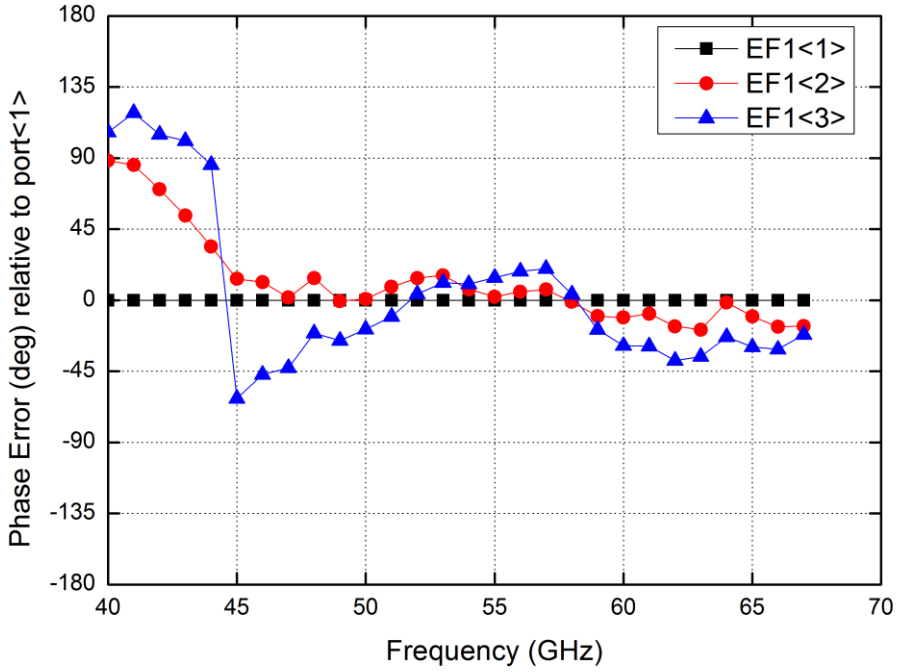

Fig. 4.138. Measured phase error of EF1 array at beam state1 in Tx mode.

doi:10.6342/NTU201603106

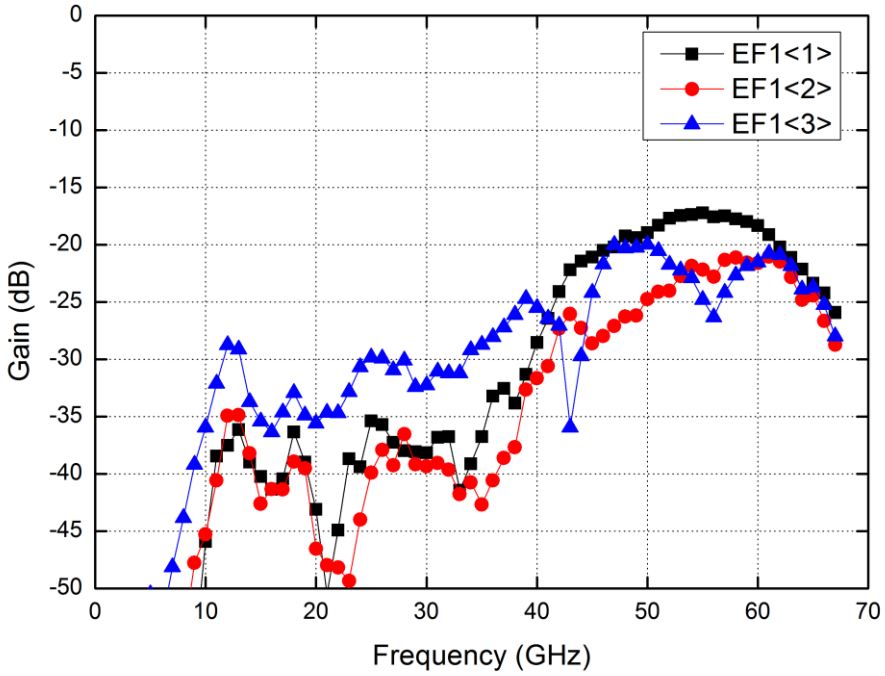

Fig. 4.139. Measured gain of EF1 array at beam state2 in Tx mode.

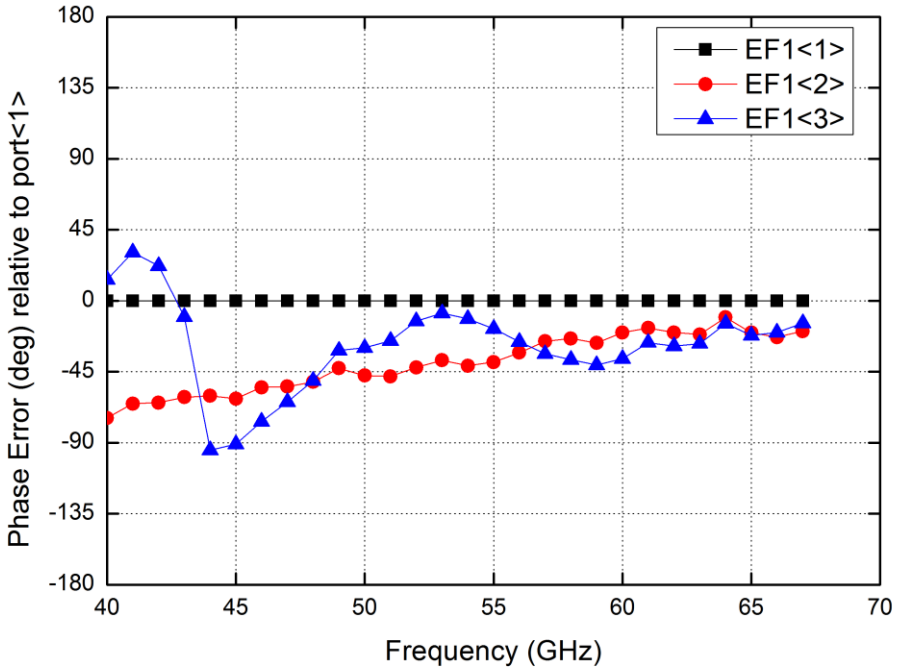

Fig. 4.140. Measured phase error of EF1 array at beam state2 in Tx mode.

doi:10.6342/NTU201603106

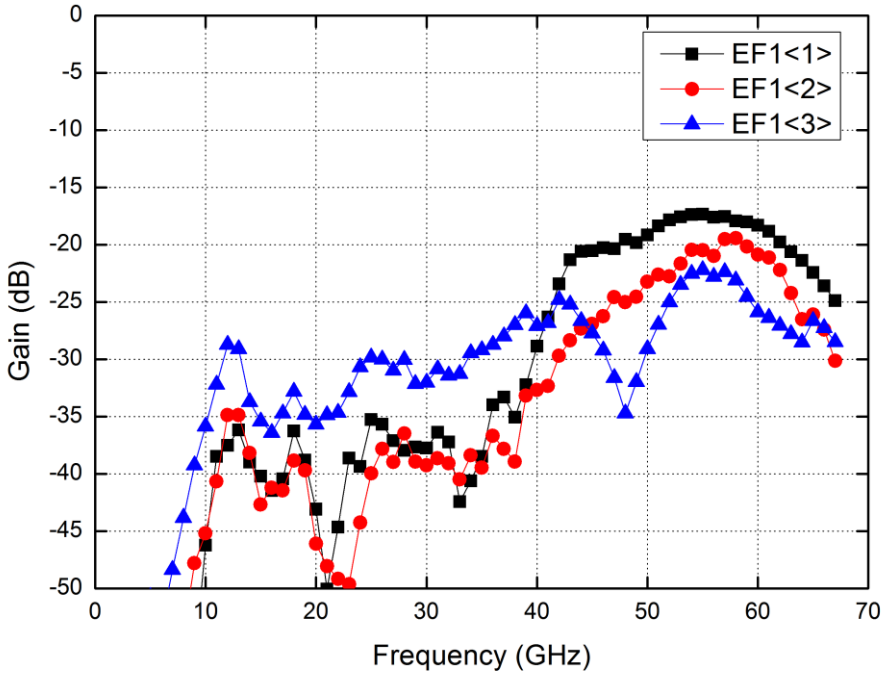

Fig. 4.141. Measured gain of EF1 array at beam state3 in Tx mode.

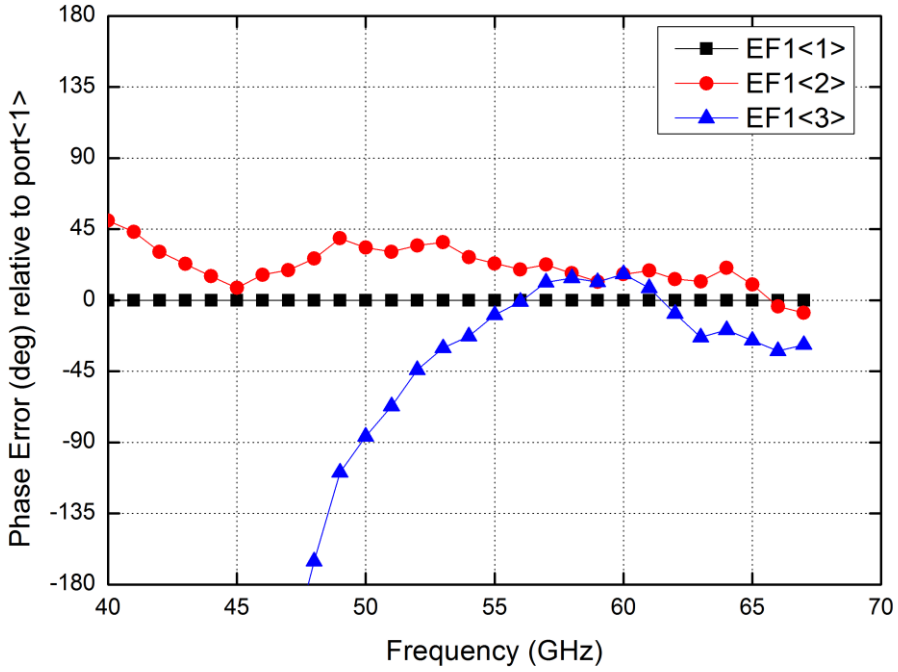

Fig. 4.142. Measured phase error of EF1 array at beam state3 in Tx mode.

doi:10.6342/NTU201603106

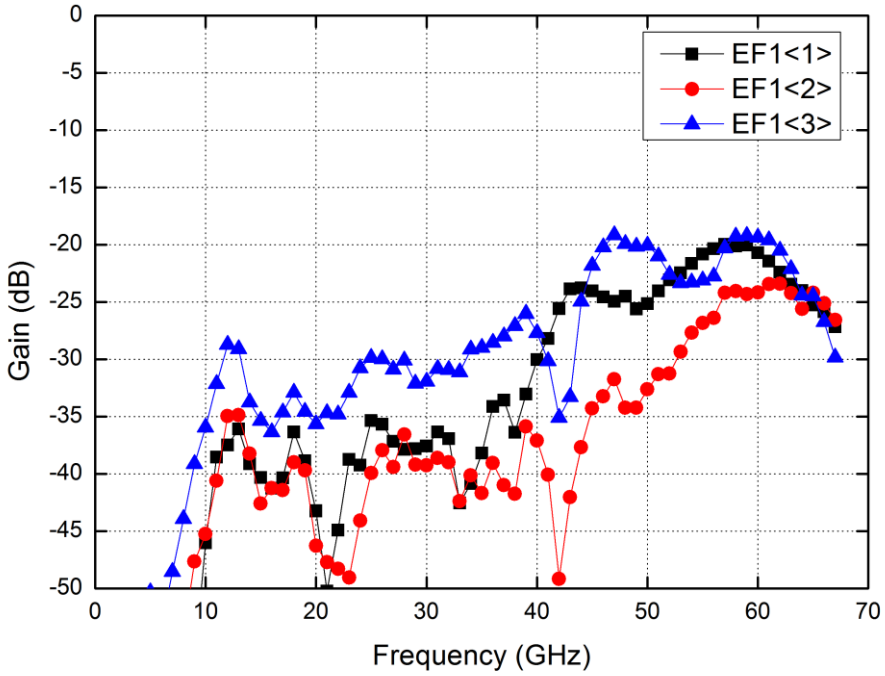

Fig. 4.143. Measured gain of EF1 array at beam state4 in Tx mode.

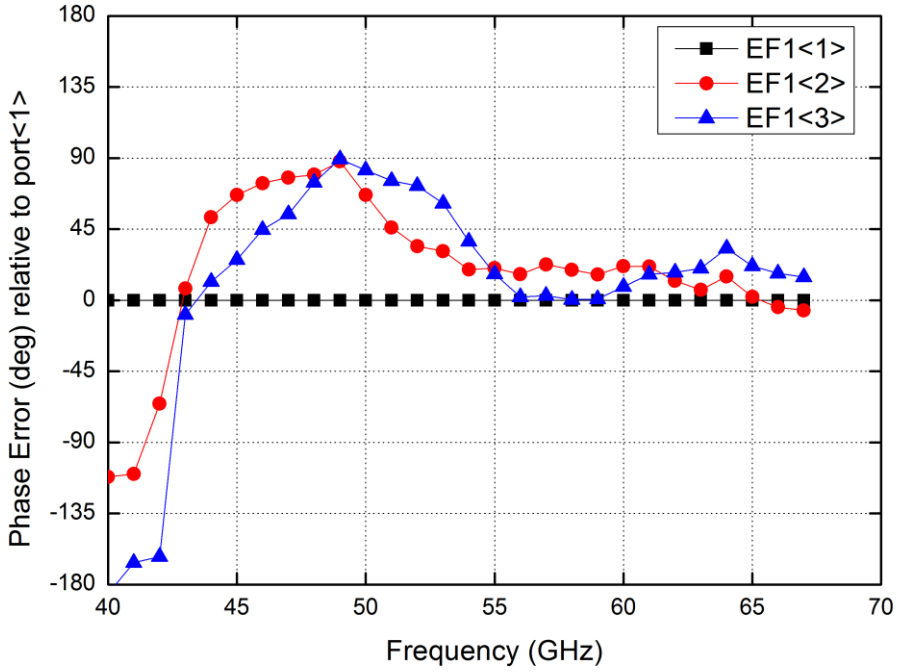

Fig. 4.144. Measured phase error of EF1 array at beam state4 in Tx mode.

doi:10.6342/NTU201603106

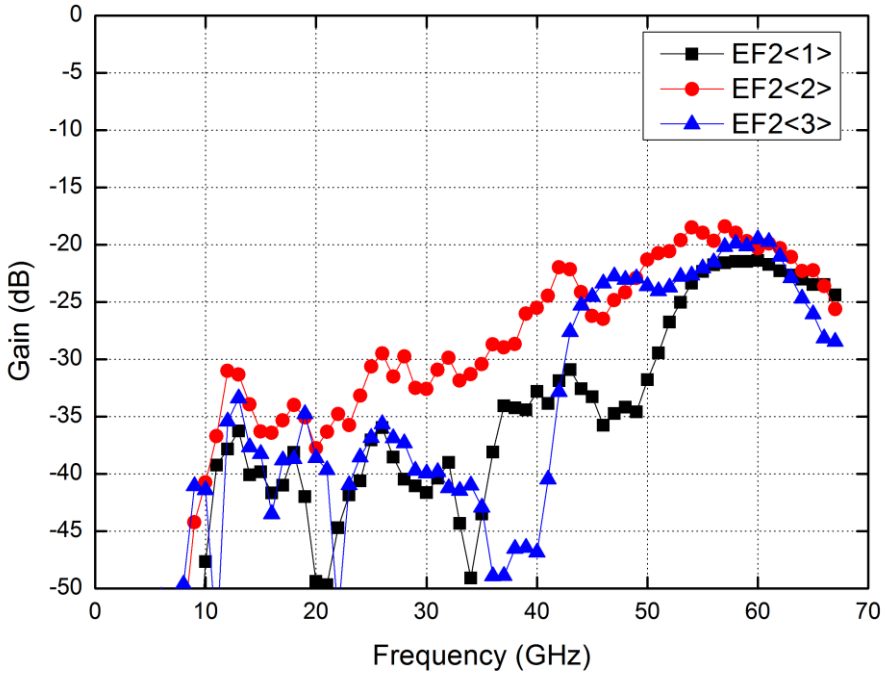

Fig. 4.145. Measured gain of EF2 array at beam state1 in Tx mode.

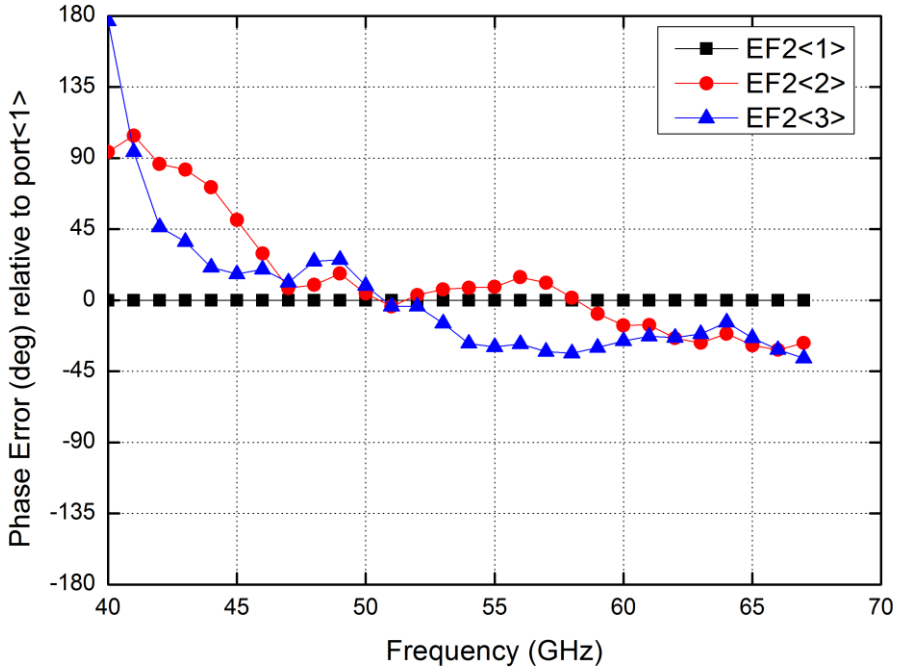

Fig. 4.146. Measured phase error of EF2 array at beam state1 in Tx mode.

doi:10.6342/NTU201603106

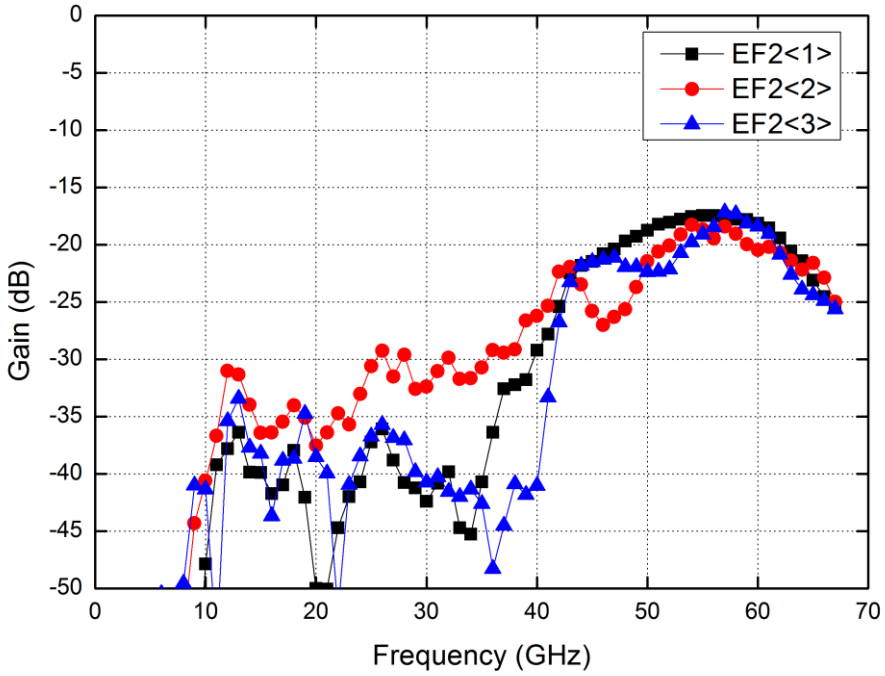

Fig. 4.147. Measured gain of EF2 array at beam state2 in Tx mode.

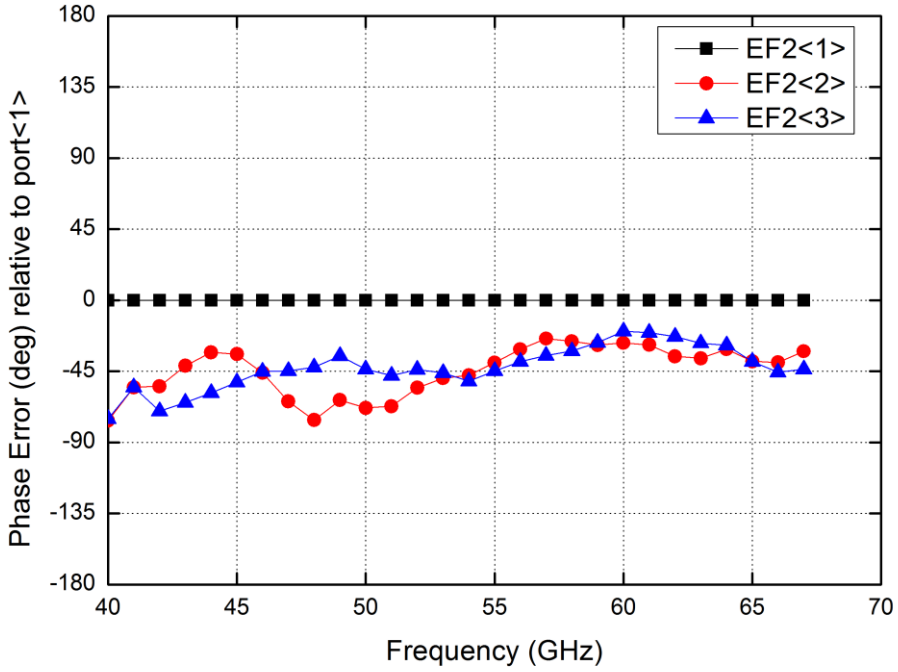

Fig. 4.148. Measured phase error of EF2 array at beam state2 in Tx mode.

doi:10.6342/NTU201603106

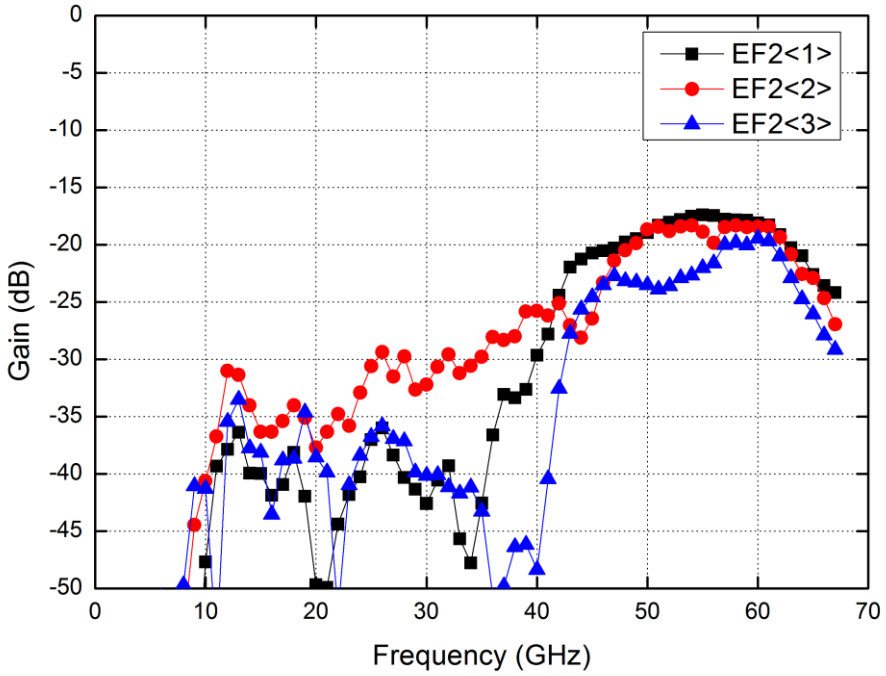

Fig. 4.149. Measured gain of EF2 array at beam state3 in Tx mode.

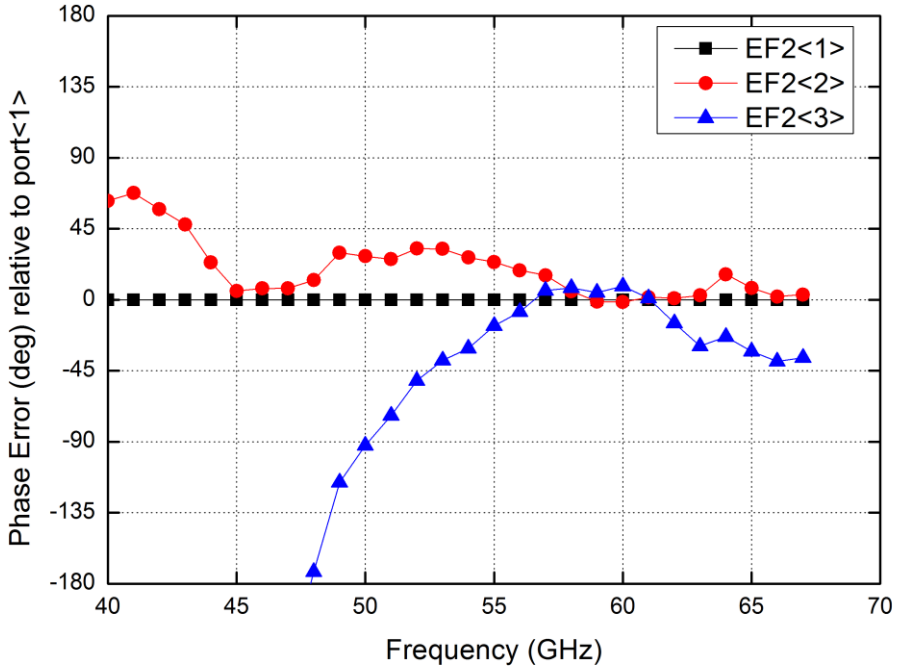

Fig. 4.150. Measured phase error of EF2 array at beam state3 in Tx mode.

doi:10.6342/NTU201603106

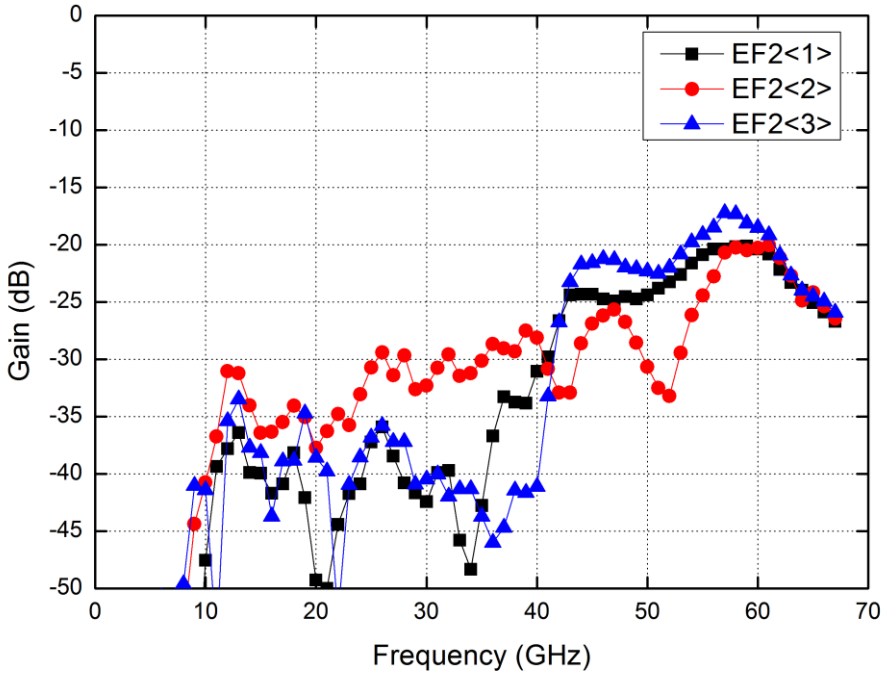

Fig. 4.151. Measured gain of EF2 array at beam state4 in Tx mode.

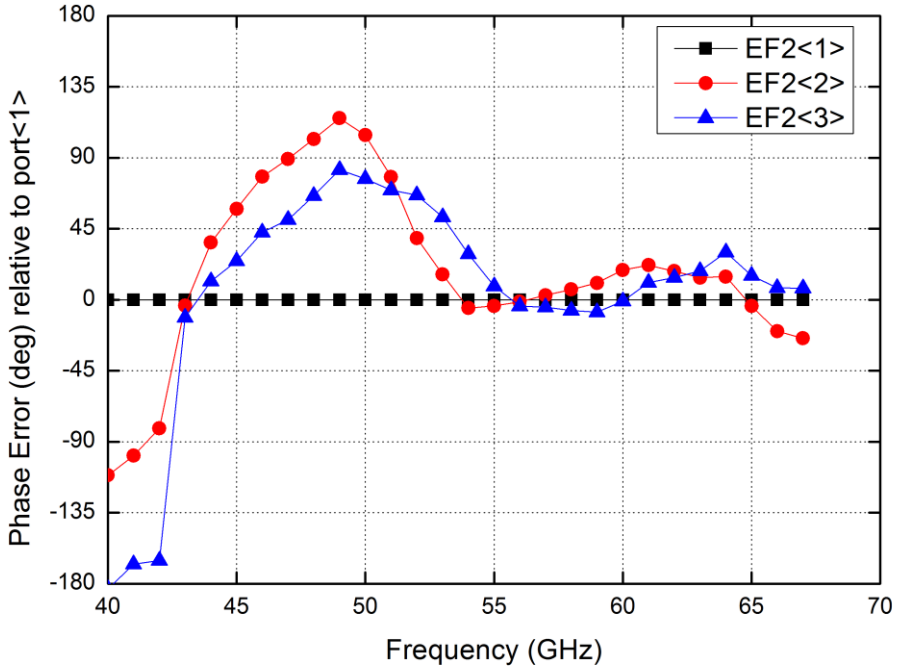

Fig. 4.152. Measured phase error of EF2 array at beam state4 in Tx mode.

doi:10.6342/NTU201603106

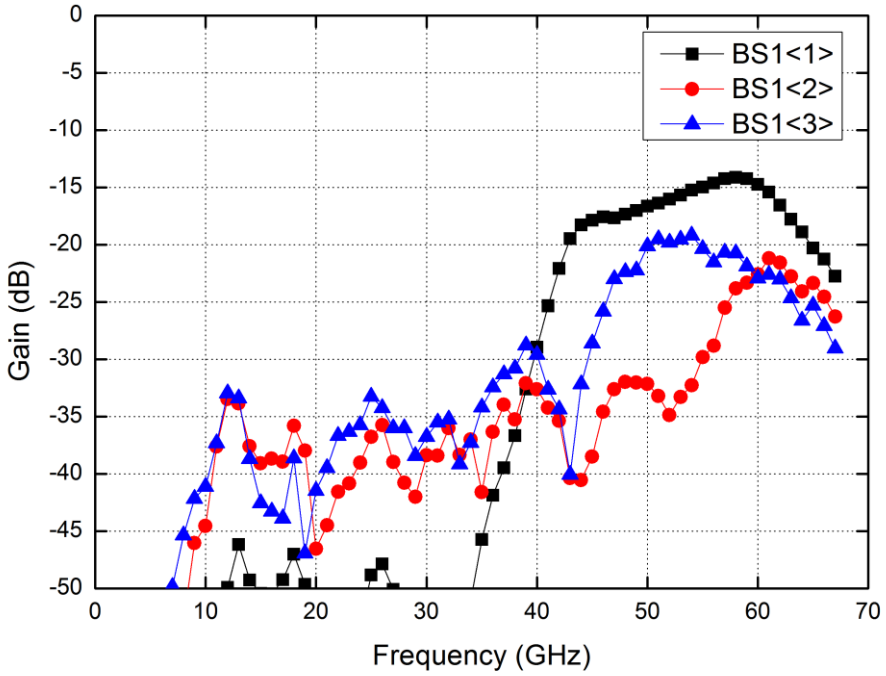

Fig. 4.153. Measured gain of BS1 array at beam state1 in Tx mode.

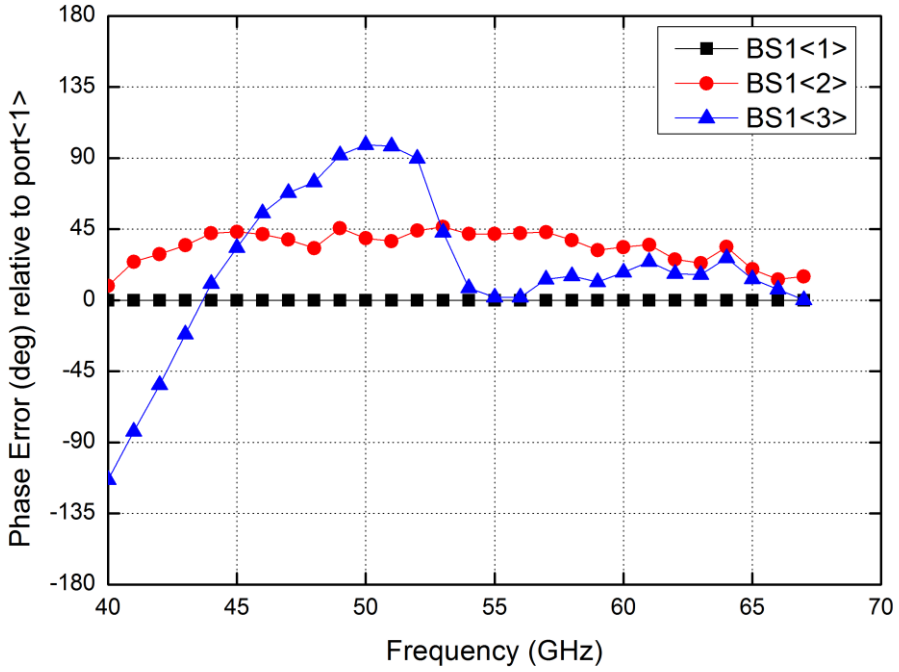

Fig. 4.154. Measured phase error of BS1 array at beam state1 in Tx mode.

doi:10.6342/NTU201603106

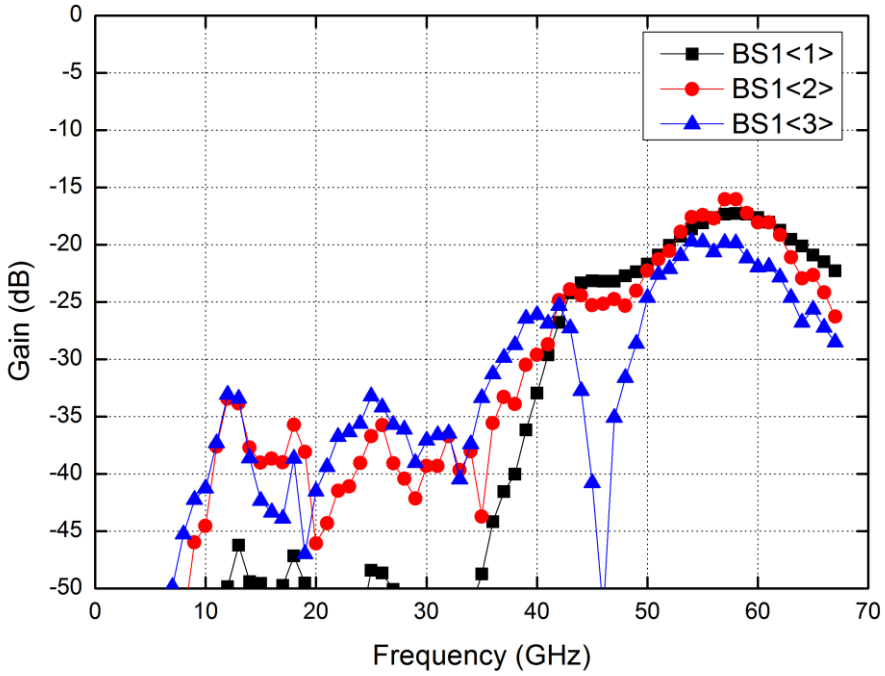

Fig. 4.155. Measured gain of BS1 array at beam state2 in Tx mode.

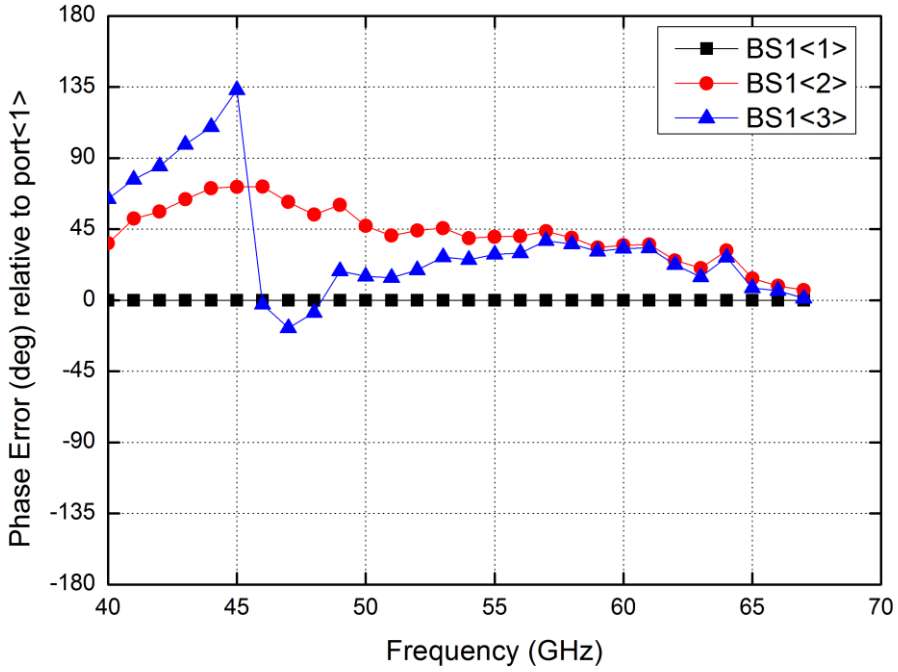

Fig. 4.156. Measured phase error of BS1 array at beam state2 in Tx mode.

doi:10.6342/NTU201603106

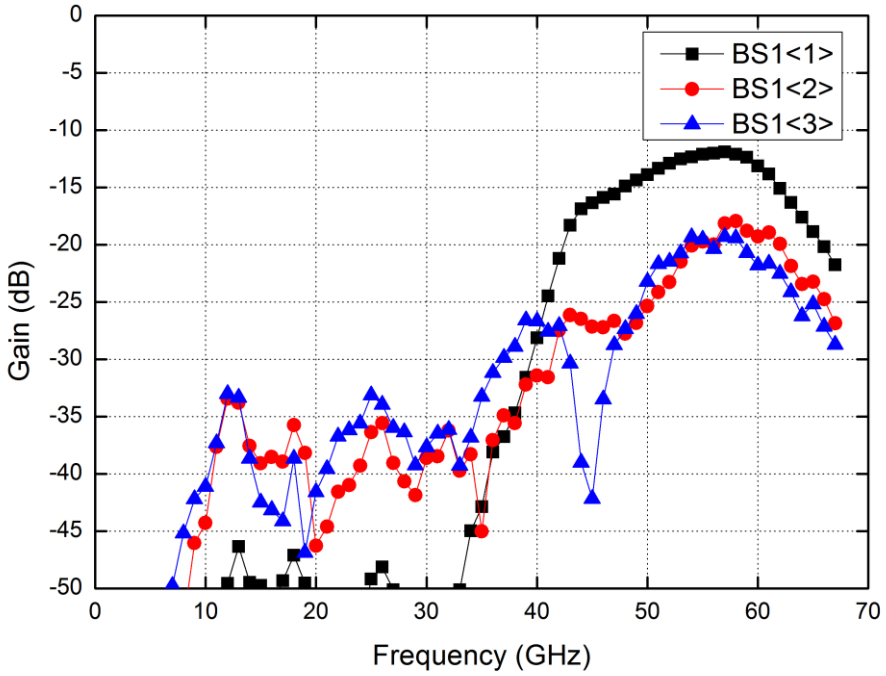

Fig. 4.157. Measured gain of BS1 array at beam state3 in Tx mode.

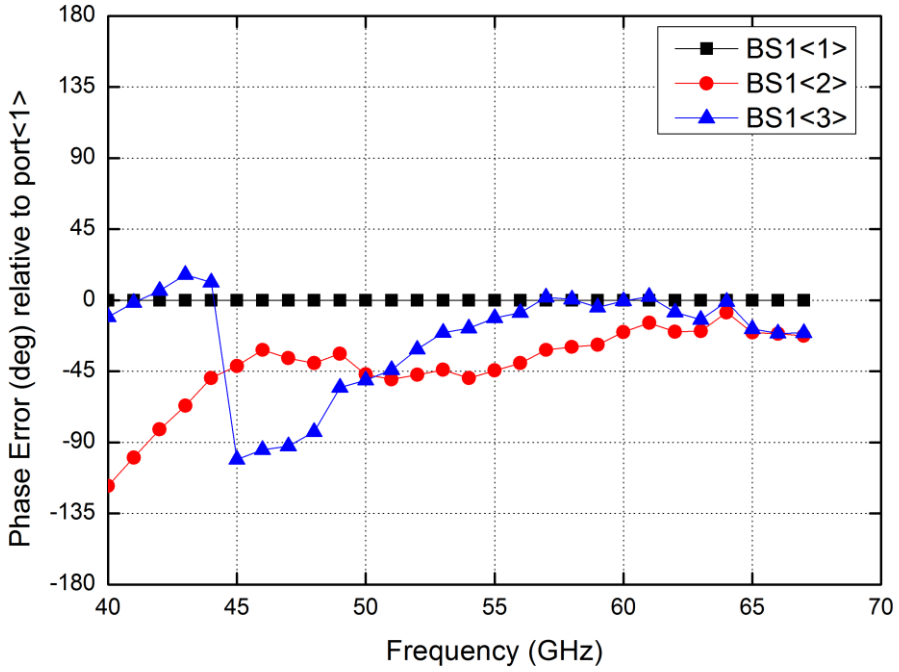

Fig. 4.158. Measured phase error of BS1 array at beam state3 in Tx mode.

doi:10.6342/NTU201603106

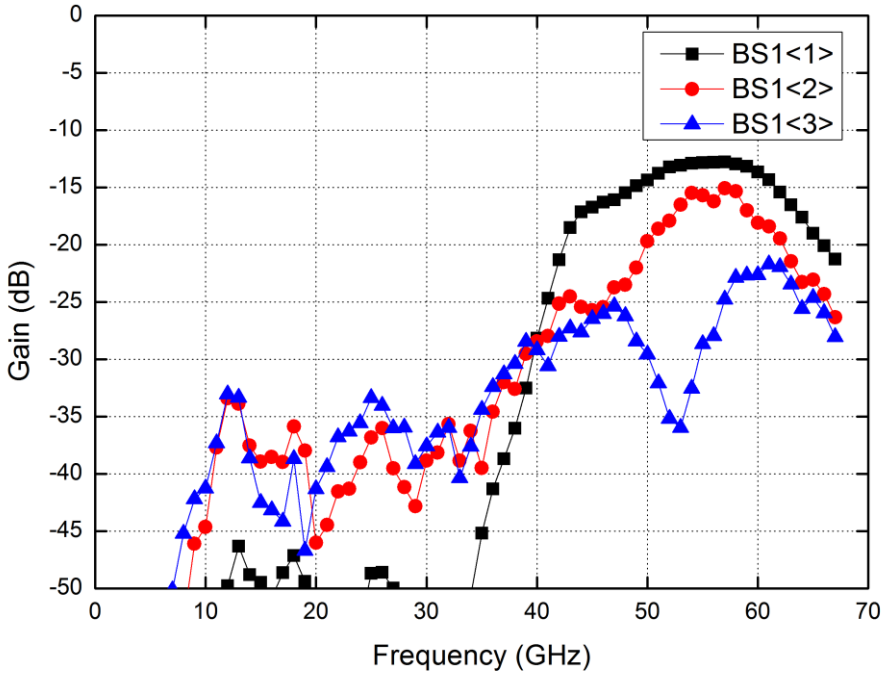

Fig. 4.159. Measured gain of BS1 array at beam state4 in Tx mode.

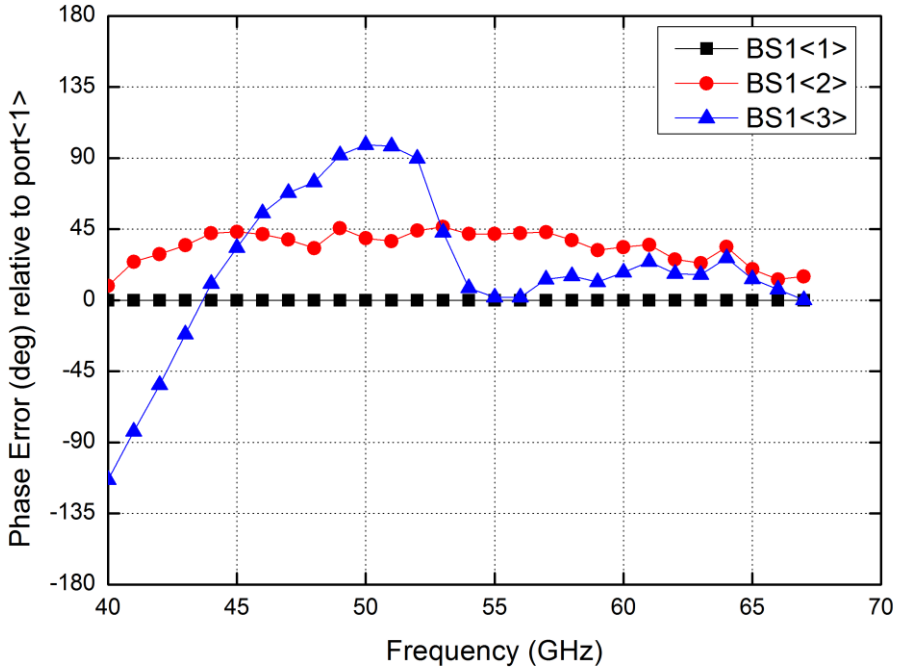

Fig. 4.160. Measured phase error of BS1 array at beam state4 in Tx mode.

doi:10.6342/NTU201603106

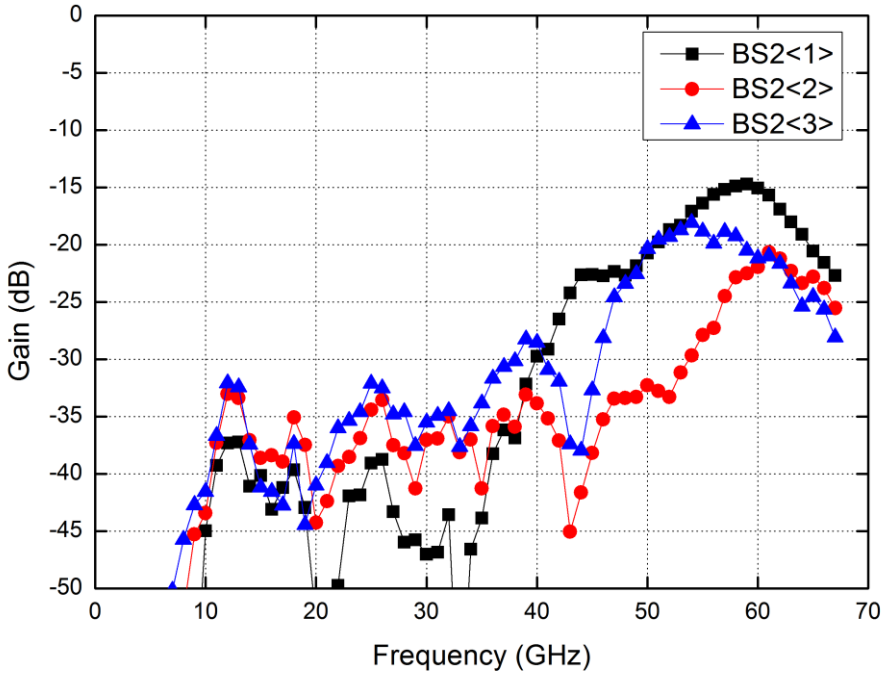

Fig. 4.161. Measured gain of BS2 array at beam state1 in Tx mode.

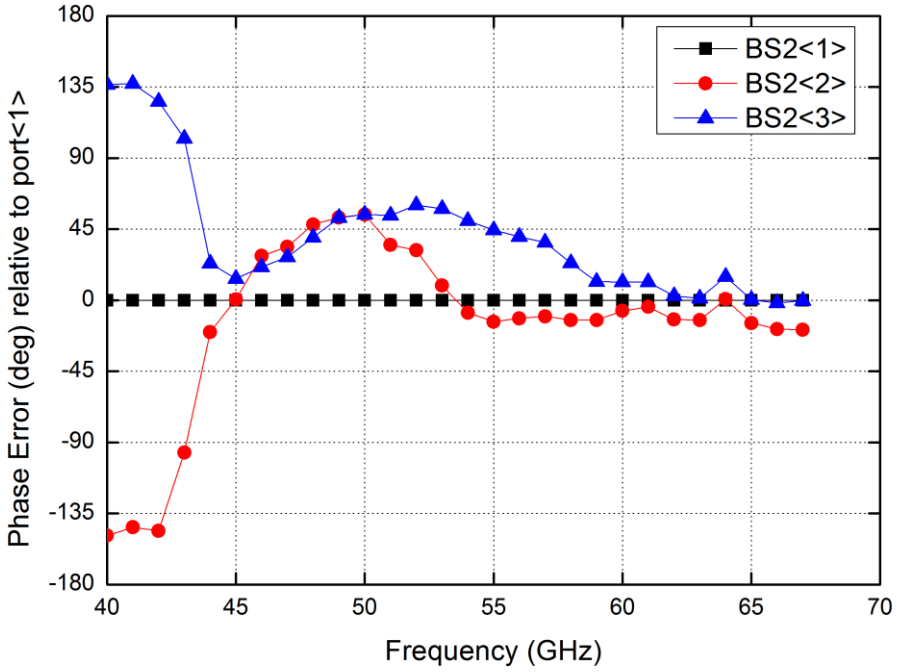

Fig. 4.162. Measured phase error of BS2 array at beam state1 in Tx mode.

doi:10.6342/NTU201603106

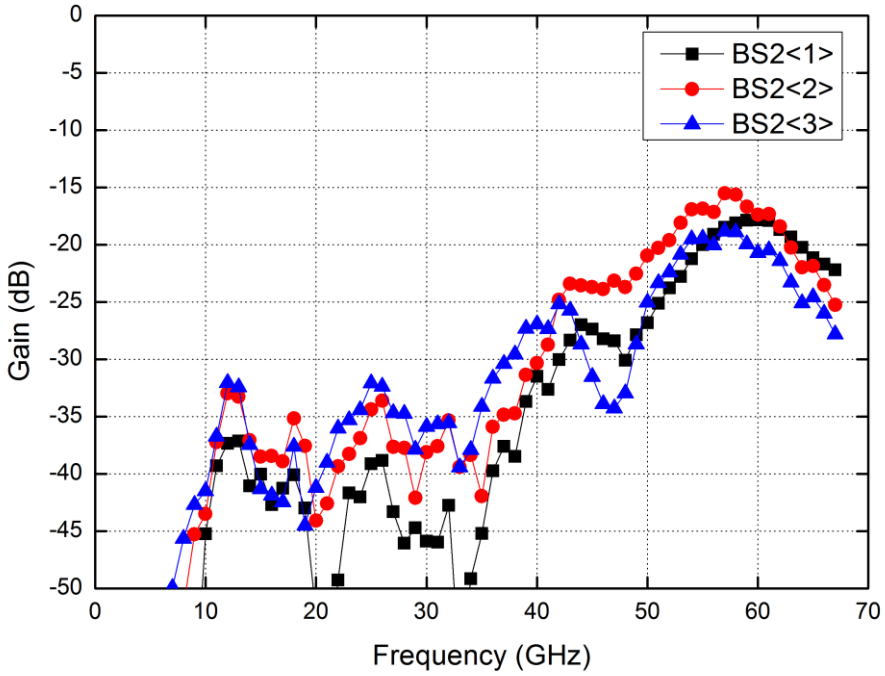

Fig. 4.163. Measured gain of BS2 array at beam state2 in Tx mode.

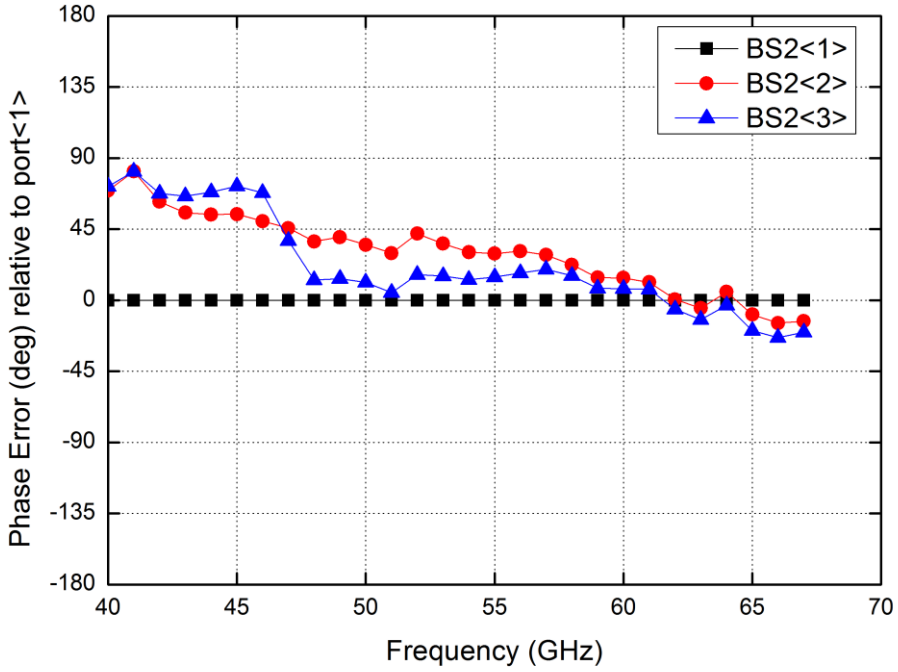

Fig. 4.164. Measured phase error of BS2 array at beam state2 in Tx mode.

doi:10.6342/NTU201603106

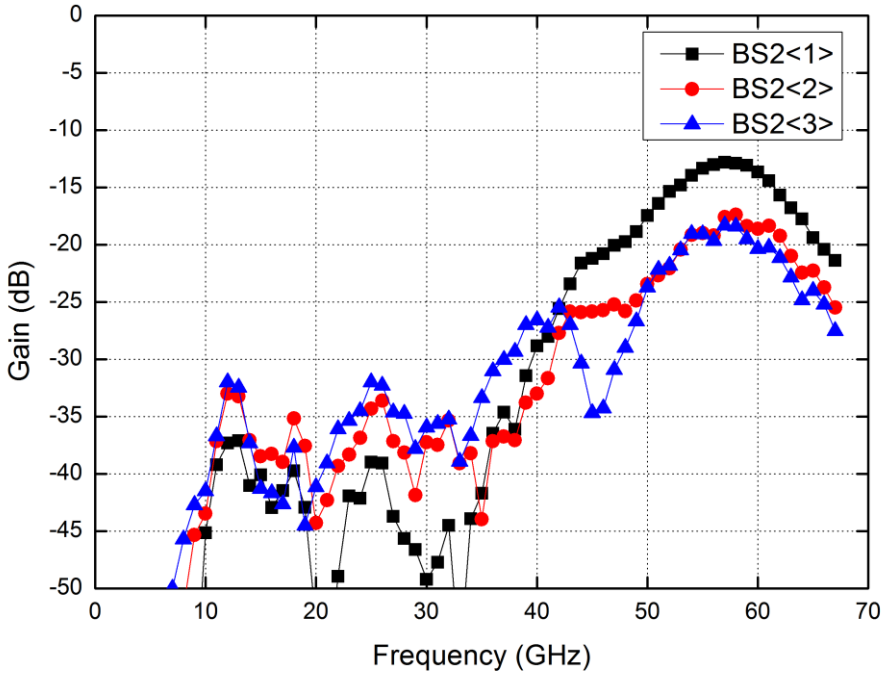

Fig. 4.165. Measured gain of BS2 array at beam state3 in Tx mode.

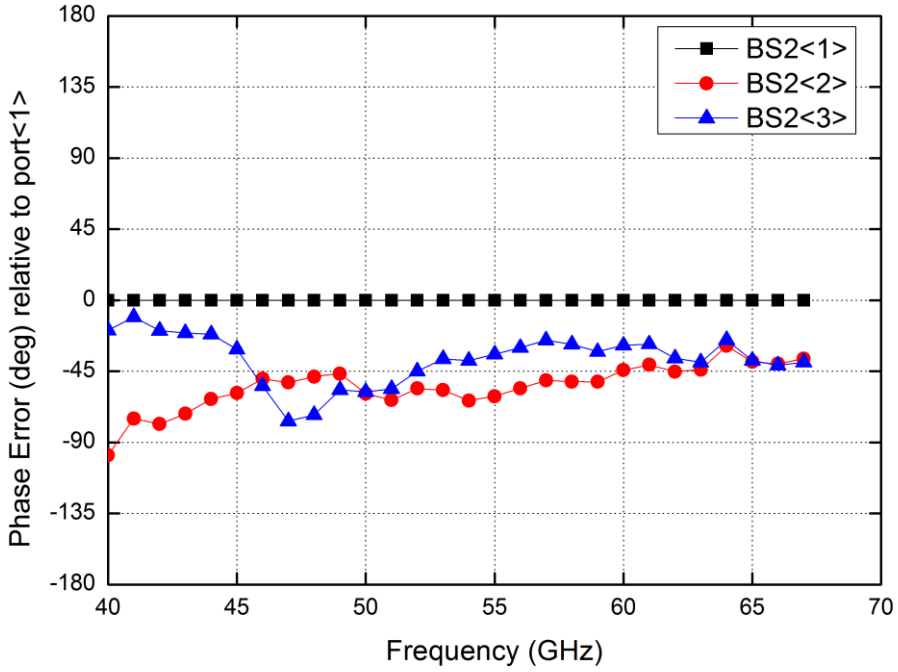

Fig. 4.166. Measured phase error of BS2 array at beam state3 in Tx mode.

doi:10.6342/NTU201603106

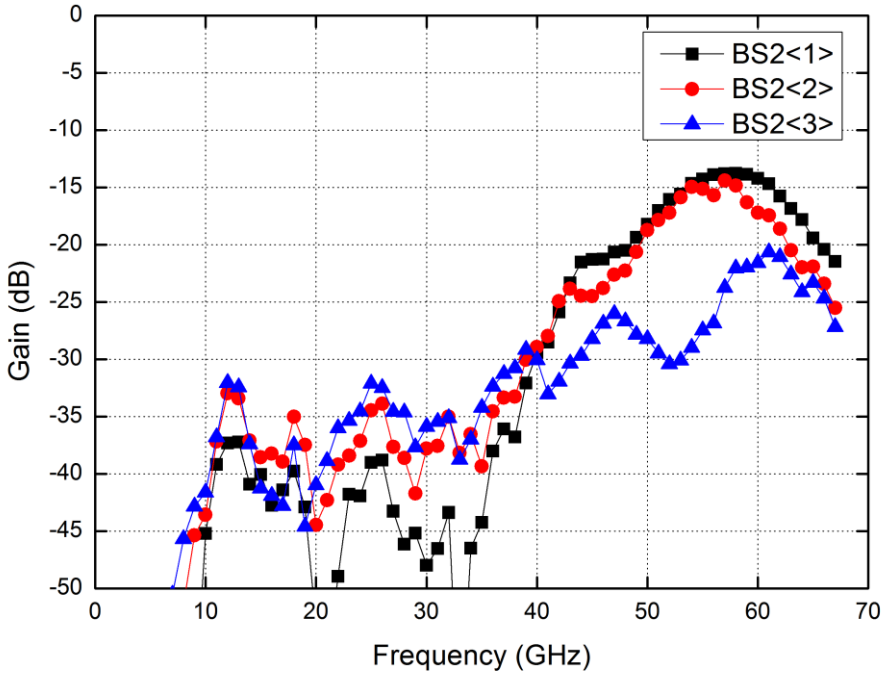

Fig. 4.167. Measured gain of BS2 array at beam state4 in Tx mode.

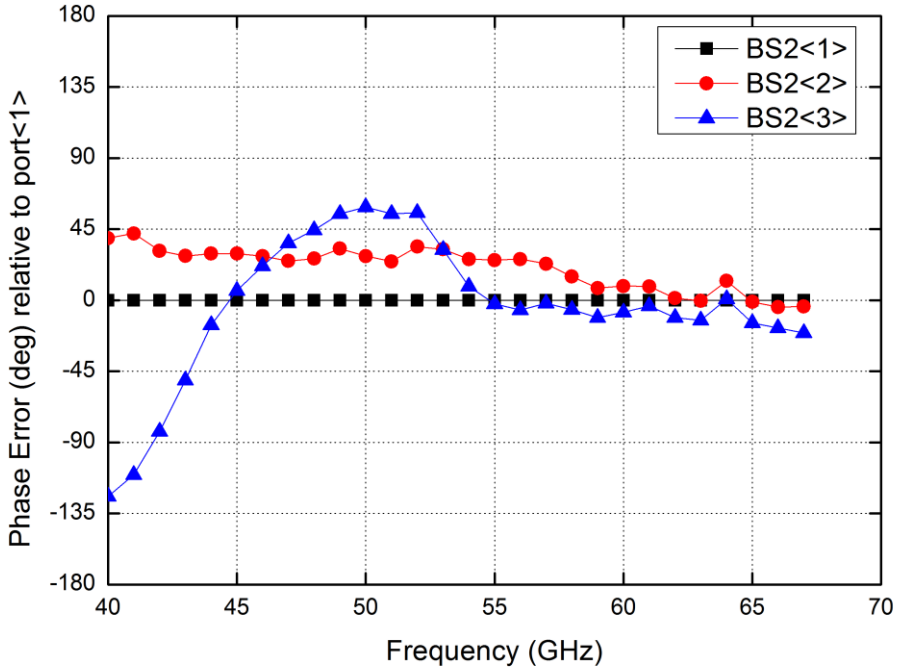

Fig. 4.168. Measured phase error of BS2 array at beam state4 in Tx mode.

doi:10.6342/NTU201603106

4.6 Revised system design

In this section, the revised system is designed, the modifications are based on the measured results of system and test circuits. The following sections present each modification from reason to result.

4.6.1 Revised I/O pads

The system chip is designed for flip-chip assembly, and the pads were in 126-μm pitch in the first version of system. However, the low reliability of assembly is reported by the assembly factory. In order to solve this problem, the I/O pads have modified to enhance the reliability. The new version of I/O pads are designed in 144-μm pitch, with use the 72×72 μm^2 bumping pads. The pad size and pitch are decided by the design rule of bumping pad, suggestion of assembly factory, and the compatibility of RF probes in 150-μm pitch. Fig. 4.169 shows the new version of I/O pads.

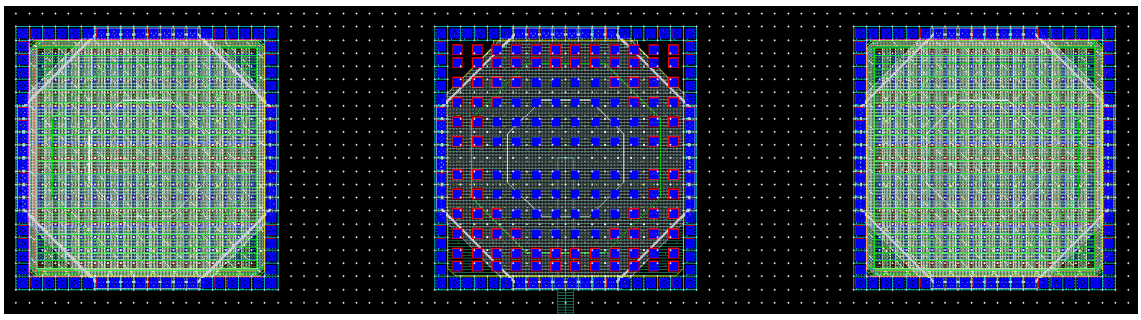

Fig. 4.169. GSG pump pad with 144-μm pitch for antenna ports.

doi:10.6342/NTU201603106

4.6.2 Voltage level-up shifter

In the digital control testing, we found that the function of gain control fails because the digital circuit offers the 1.1 V voltage is not adequate to turn off the PMOS switches (2.5 V is required) in the global bias circuit. The level shifters are designed to offer the voltage level shifting from 1.1 V to 2.5 V. The schematic and layout of the level shifter are shown in Figs. 4.170 and 4.171, respectively.

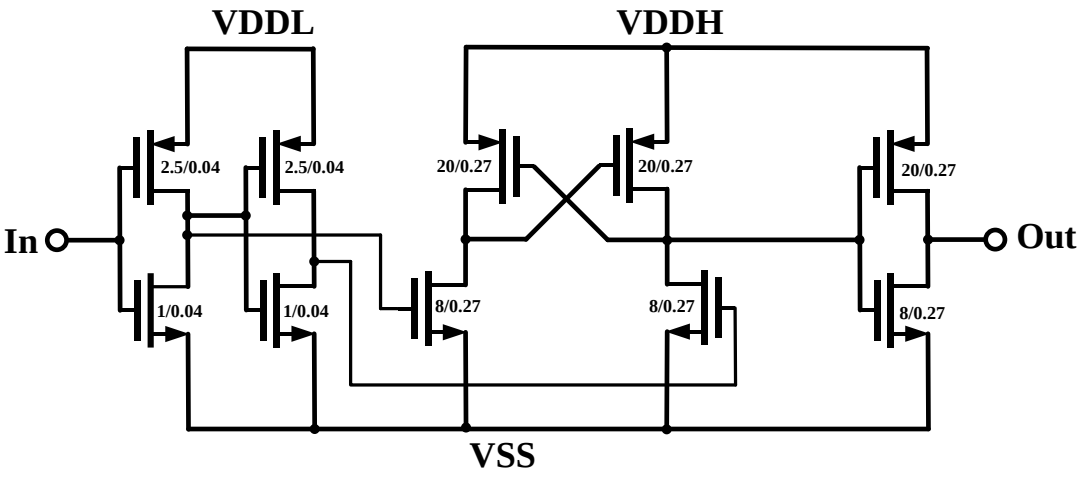

Fig. 4.170. Schematic of the voltage level-up shifter.

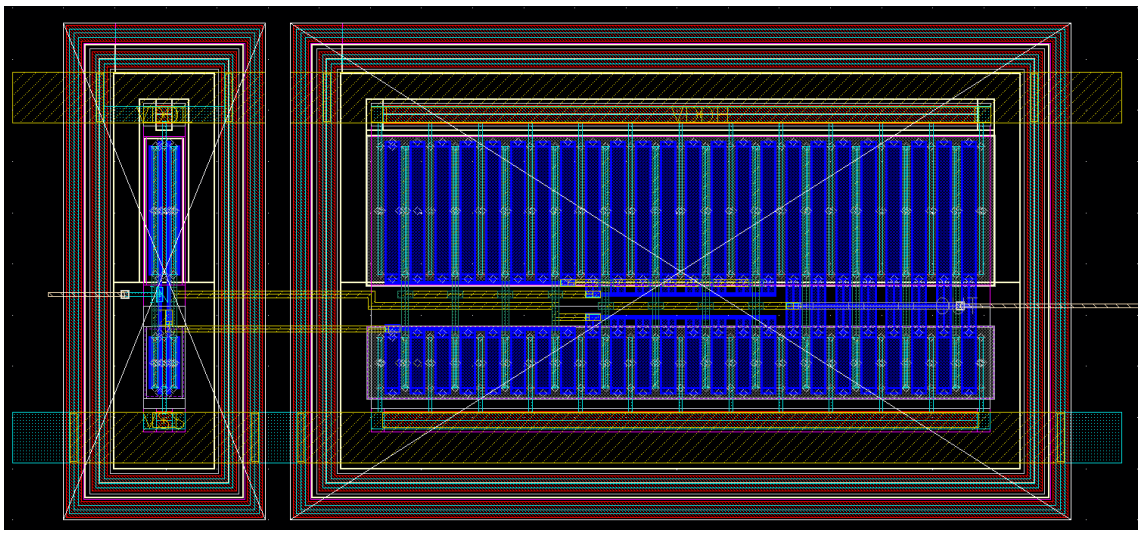

Fig. 4.171. Layout of the voltage level-up shifter.

doi:10.6342/NTU201603106

4.6.3 ESD protection for digital circuit

Due to the lack of ESD protection between I/O pads and digital circuit, the digital circuit is very weak because we found the testing samples have the high probability to fail. In this revised system, the ESD protection circuit have added to the I/O pads for the input of digital circuit. The schematic and layout of the ESD protection circuit for digital I/O pad as shown in Figs. 4.172 and 4.173, respectively.

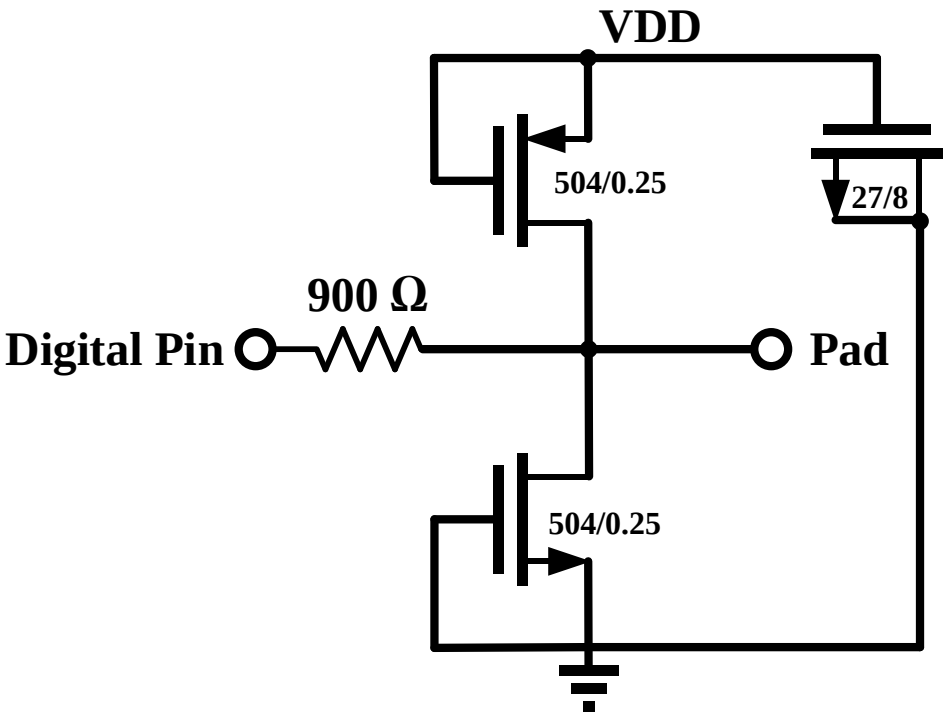

Fig. 4.172. Schematic of the ESD protection I/O pad.

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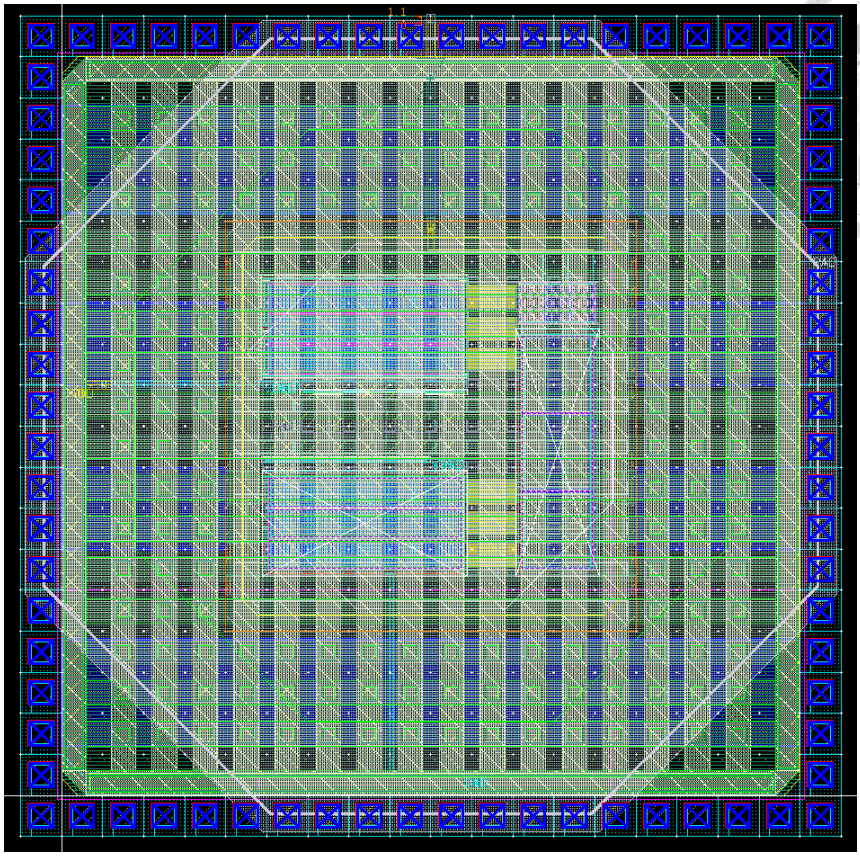

Fig. 4.173. Layout of the I/O pad with ESD protection.

4.6.4 Revised BDA

From section 3.7.1, we found the BDA have inconsistent results between the measurement and the simulation using the PDK model. Thus the revised model based on the measurement of the test devices have proposed. By using the revised model, the consistent comparison results are reached.

Based on the revised model, the revised version of BDA have designed. In order to avoid the high non-predicted behavior of the LVT devices, only the SVT devices are used in this version. The design procedure is the same as the first version. To compensate the gain drop to achieve the preliminary link budget of the system, the gate bias is designed

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to a higher voltage to reach a higher gain. That results in a higher current consumption but a more robust performance.

Fig. 4.174 shows the schematic of the revised BDA, the layout of circuit core and test circuit are shown in Figs. 4.175 and 4.176, respectively. The circuit core size is 0.12 mm^2, which is as compact as the first version of BDA. The simulated results of S-parameters and noise figure at Rx mode as shown in Figs. 4.177 and 4.178, respectively. It exhibits over 14.5-dB gain and lower than 6.9-dB noise figure from 57 to 66 GHz.

The simulated results of S-parameters at Tx mode as shown in Fig. 4.179. It shows over 17.7-dB gain from 57 to 66 GHz. The simulated large-signal performance 60 GHz is shown in Fig. 4.180. The dc power consumption is 96.9 mW at Tx mode and 38.7 mW at Rx mode, both biased at 200 μA reference current. In the gain/power control mode, the dc power consumption will be changed, and it will be presented in the next section.

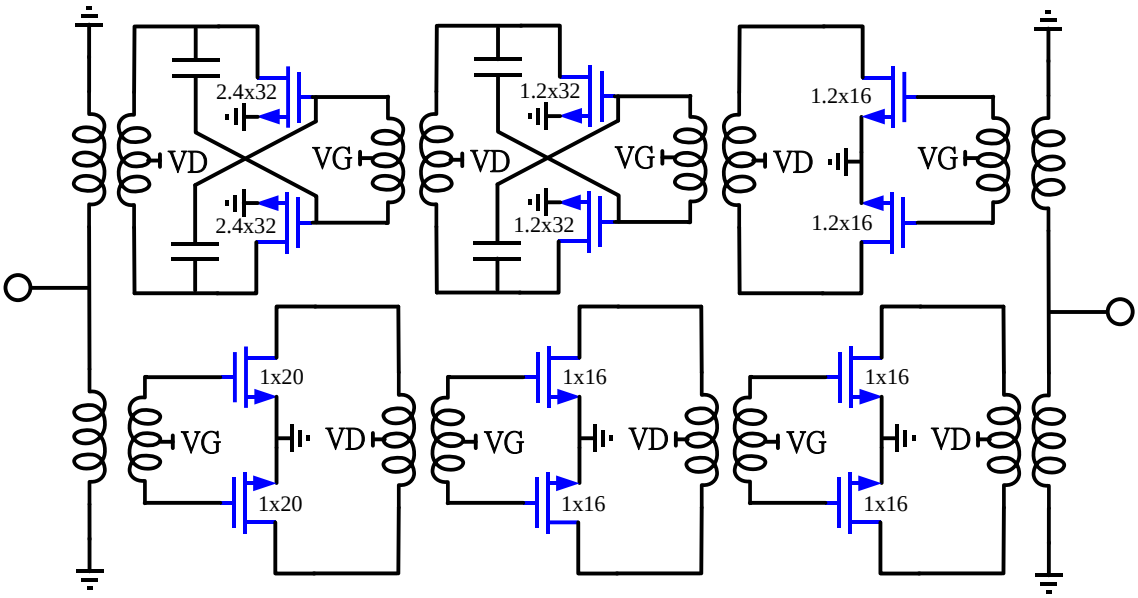

Fig. 4.174. Schematic of the revised BDA.

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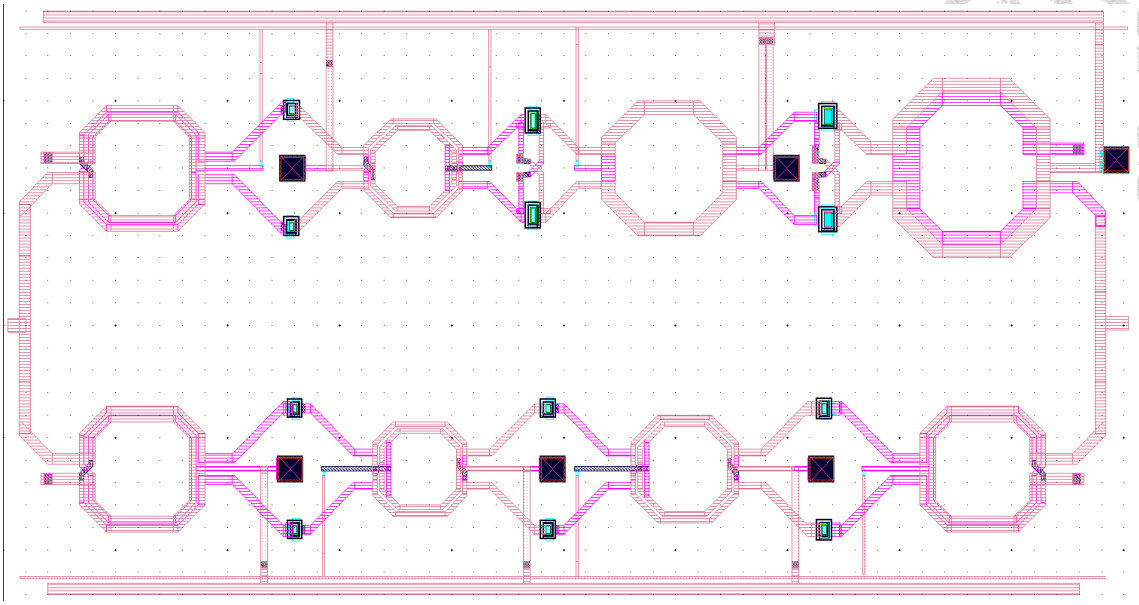

Fig. 4.175. Layout of the revised BDA (core).

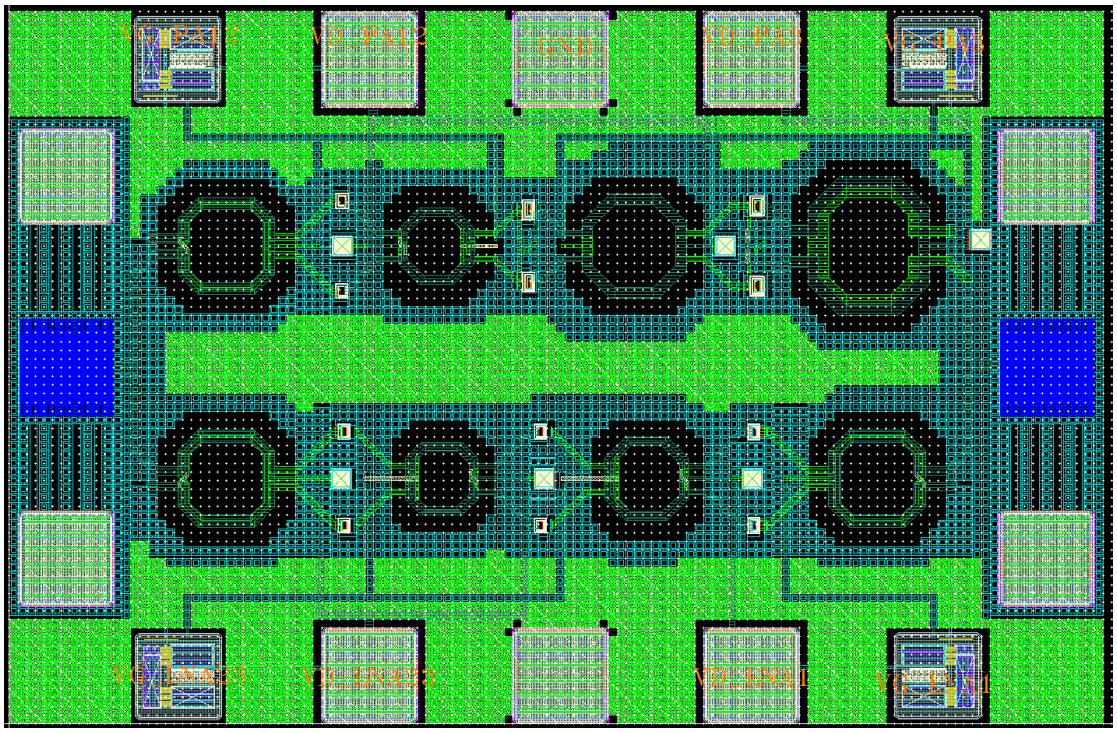

Fig. 4.176. Layout of the revised BDA (test circuit).

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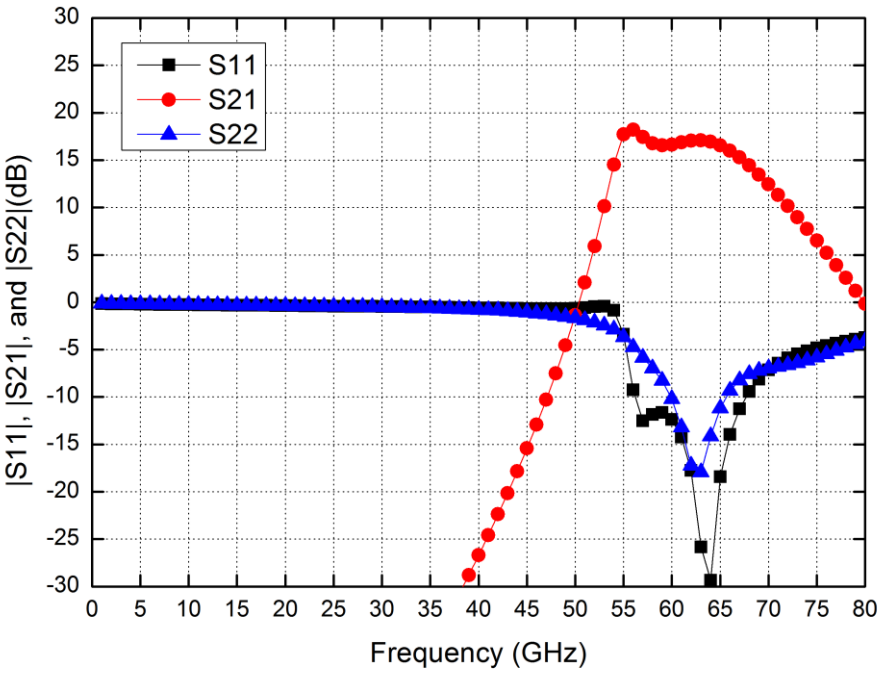

Fig. 4.177. Simulated S-parameters of revised BDA in Rx mode.

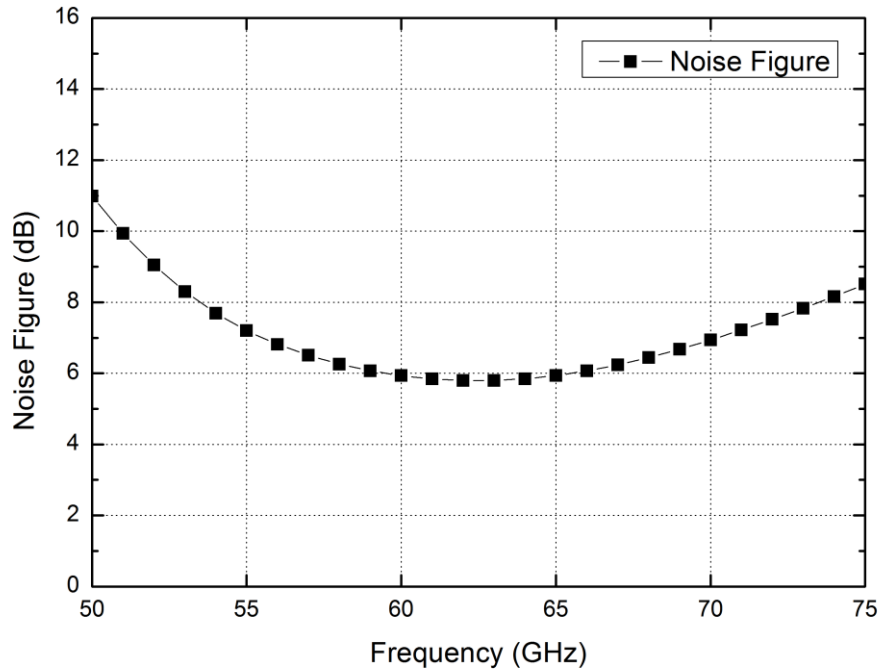

Fig. 4.178. Simulated noise figure of revised BDA in Rx mode.

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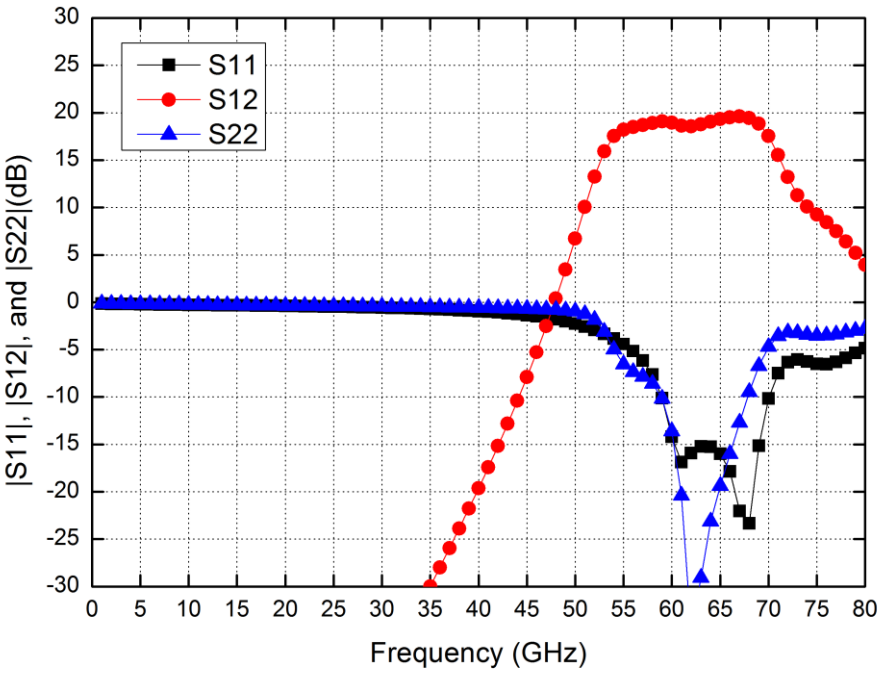

Fig. 4.179. Simulated S-parameters of revised BDA in Tx mode.

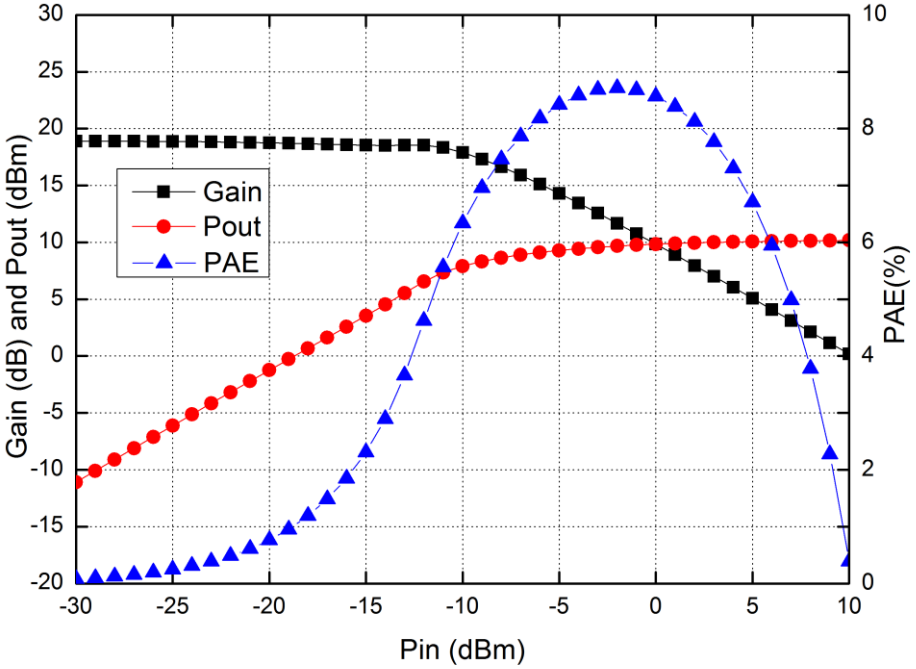

Fig. 4.180. Simulated large-signal performance of revised BDA at 60 GHz.

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4.6.5 New bias plan

By cooperating with the new version of BDA, the local bias circuit is modified. Fig. 4.181 shows the new version of local bias circuit. The current mirrors for Rx and Tx are identical, and the V-I mapping devices are designed to have the 40-nm channel length, which is the same as the devices used in the BDA. This can help to reduce the effect of channel length modulation. Besides, in order to offer higher gate voltage for BDA, the reference current of global bias circuit have pinched two to one, which offers the reference current from 150 μA to 300 μA in 50 μA steps. Table 4.10 shows the bias information among the gain/power control states.

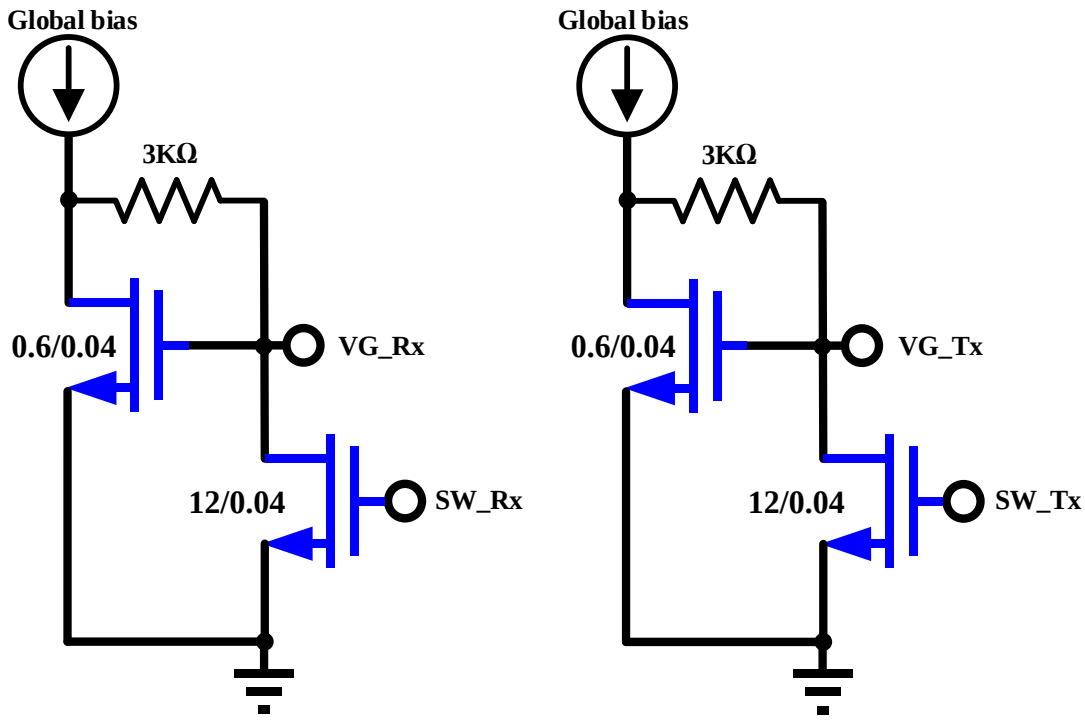

Fig. 4.181. New local bias circuit for the revised BDA and system.

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Table 4.10. The system dc consumption among the gain/power control mode.

PAR[3:0]	[XX00]	[XX10]	[XX01]	[XX11]
Iref (mA)	300	250	200	150
Idc (mA) at Rx Mode	208	175	141	107
Mapping voltage for Rx (V)	1.08	1	0.93	0.85
Idc (mA) at Tx Mode	519	436	352.4	268
Mapping voltage for Tx (V)	1.08	1	0.93	0.85

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4.6.6 Layout and pin definition

Fig. 4.182 shows the layout of the revised system, the chip size is 2.11 × 1.84 mm^2. The pin definition is shown in Fig. 4.183. Comparing with the first version of system, the total size have enlarged due to the modified I/O pads. Besides, two additional pads are added in the revised version of system. The digital VDD is designed to separate from the RF VDD. Another is a ground pad placed between the Tx and Rx port for probing with the RF GSG probes.

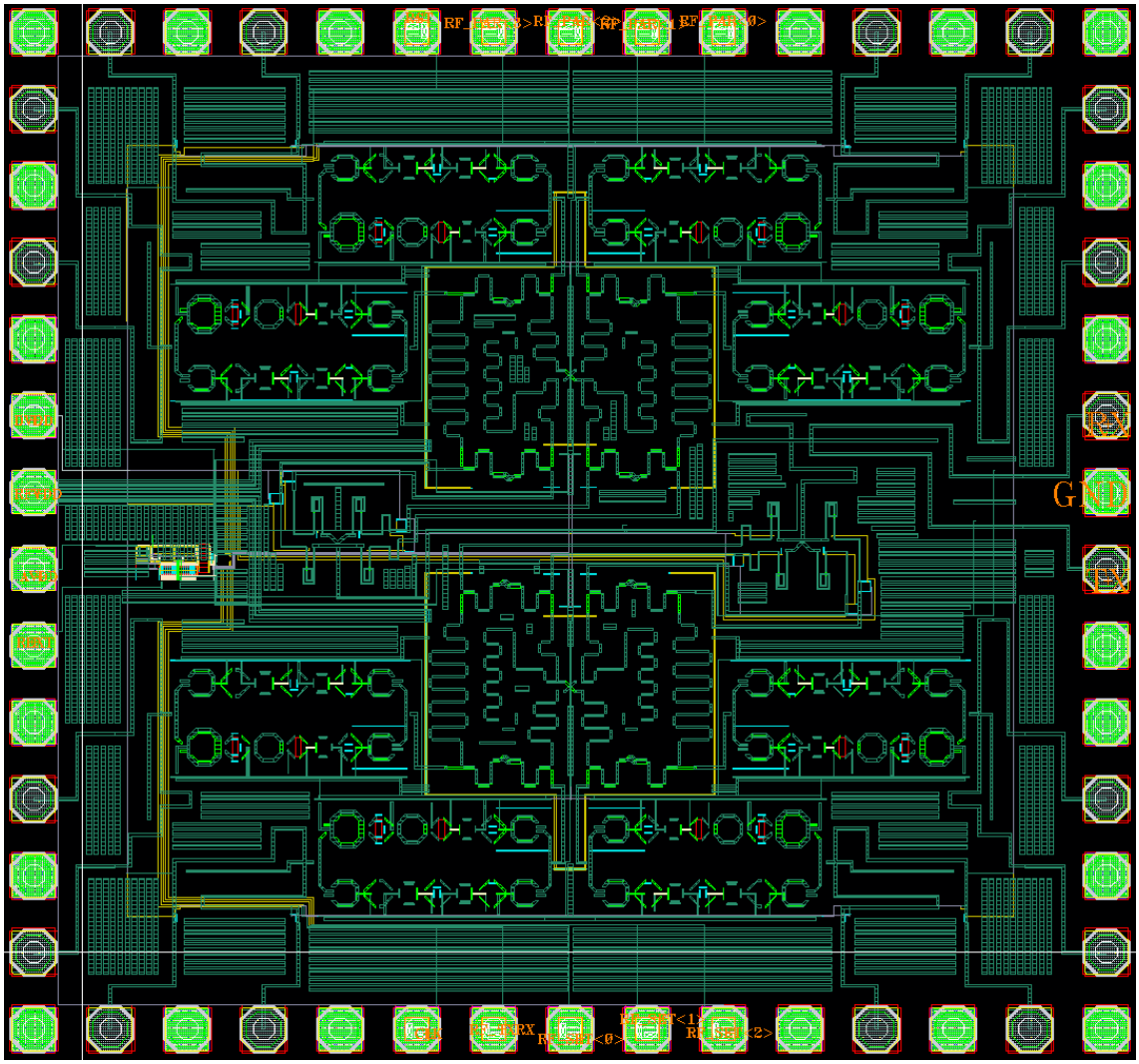

Fig. 4.182. Layout of the revised beamformer.

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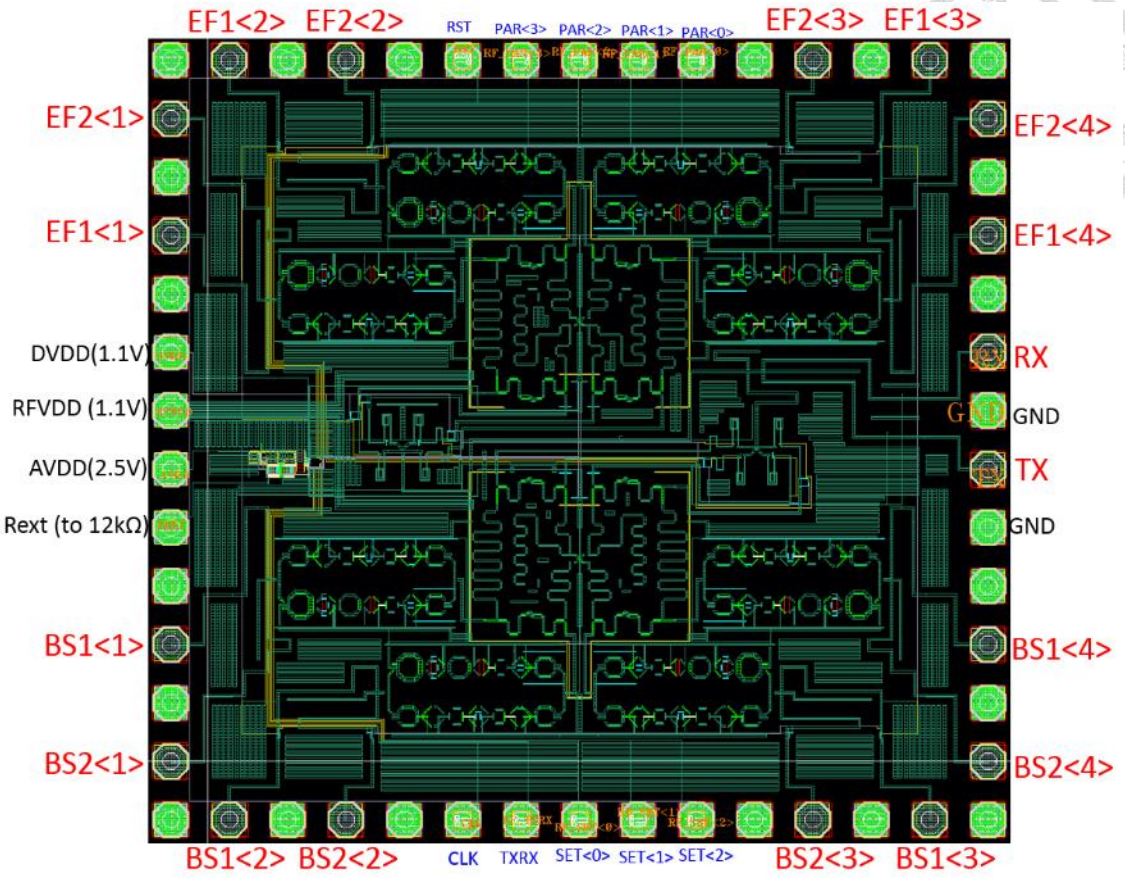

Fig. 4.183. Pin definition of the revised beamformer.

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4.7 Summary

In this chapter, a 60-GHz bidirectional beamformer based on the switchless BDAs is presented. By sharing the antenna of the Tx and Rx, the RF I/O is reduced to around half. Besides, by using the compact size of the BDAs, the system chip area can be minimized. The chip size of the first and the revised version is only 2.9 mm^2 and 3.88 mm^2, respectively. In the first version of system. Although the closer pitch of the I/O pads introduced the reliability problem of assembly, we have verified the control function by using bondwire and signal probing. Besides, we fixed some problems found in the first version of system. The revised version of system is under manufacturing in foundry now.

The system chip is compatible with commercial 60-GHz transceivers, and offers the signal distribution to 4-antenna array, total 16 antenna ports are supported. The 16-state beam steering can be achieved by selecting one of the four array and one of four beam state in the array. By cooperating with the two opposite broadside antenna array, the property of wide beam-width is possible to cover most of the solid angle of the space, and other two endfire arrays help to cover the direction which is not covered by the two broadside arrays. By using this beamformer in the phased array module, it is no need the separated Tx and Rx, the beamformer functions Tx or Rx by T/R mode switching. The antennas are sharing at Tx and Rx modes, and the reduced I/O ports minimized the effort of assembly. The omnidirectional beam steering is the most valuable application of this beamformer by cooperating with the four antenna arrays. Moreover, the two identical modules are expected to achieve the bidirectional data transmission regardless the direction of the two modules. In other words, bidirectional transmission and omnidirectional radiation can be simultaneously realized by this beamformer.

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Chapter 5 Conclusions

The research of switchless bidirectional amplifiers and bidirectional beamforming system are presented in this thesis. First, the advantages of bidirectional system and application in the phased array have demonstrated. The BDA is the most critical component in this system. The previous researches, classification, and merit of different topology have illustrated. The principle of operation, and the trade-off of design have been discussed.

Next, two 60-GHz BDAs using 90-nm and 40-nm CMOS process are proposed, the design principle and procedure have demonstrated. The 90-nm BDA performs the bidirectional function and the competitive performance by comparing with the individual amplifiers. In the 40-nm BDA, although the measured results are not as expected, we use the measured result of testing circuits on the same wafer to revise the foundry-offer model, and obtain a consistent results between re-simulation and measurement.

Finally, a bidirectional beamformer is proposed. By taking the advantages of bidirectional system, the I/O ports and chip size are minimized. The beamformer produces specific phase at the selected ports for antenna array. Thus the beam-steering function can be reached by using the beamformer in the phased-array module. Although it suffers the model and ESD problems that found in the measurement, the revised version of system have fixed all these problems and it is expected to work finely. Besides, a new version of BDA is designed with the revised model and integrated in the revised system.

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